

Specification:

1. Front-End Cluster

- **3-wide fetch** from instruction memory with PC redirection from branch predictor or next-PC logic.
- **Pre-decoder** detects control instructions (branch/call/return) and trains branch predictor for speculative fetch.
- **Branch Prediction Unit (BPU)**: Gshare predictor (10-bit GHR, 1024-entry 2-bit counters).
- **BTB**: 256-entry, 4-way set associative with pseudo-LRU replacement.
- **RAS**: 16-entry return address stack for accurate return prediction.
- **BPQ**: 16-entry queue for tracking speculative predictions and aiding recovery.
- **Prediction priority**: RAS > BTB (calls) > Gshare+BTB (conditional branches).
- **Instruction Queue**: 16-entry, 3-wide FIFO decouples fetch from backend.
- **Decoder**: 3-wide parallel decoding.

2. Reorder Cluster (Tomasulo-based OOO)

- **Dispatch Buffer**: Checks intra- and inter-bundle dependencies using RAT/ARF, does register renaming.
- **Allocation**: All-or-nothing dispatch to reservation stations (RS) or load/store buffer (LSB); ROB entry assigned to each instruction for in-order retirement.
- **Resources**: 6 ALU RS, 8 MUL/DIV RS, 16-entry LSB, 48-entry ROB.

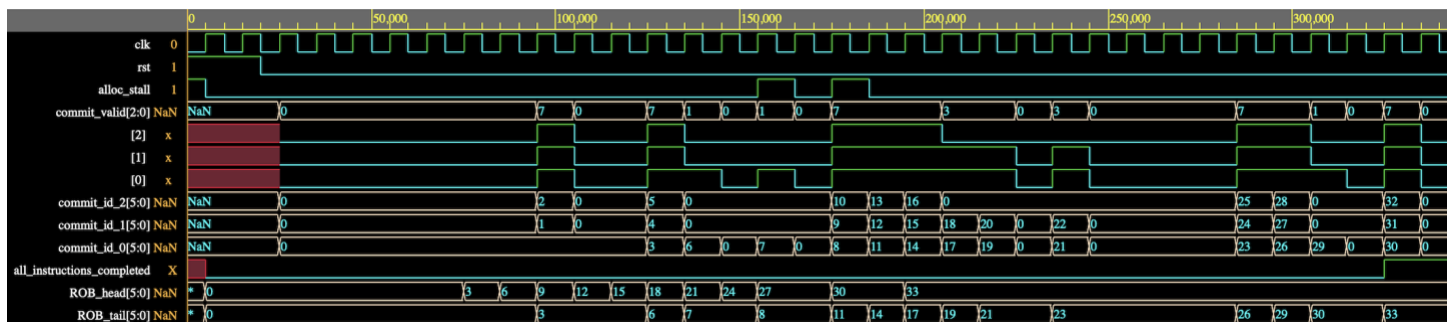
3. Execution Cluster

- **Functional Units**: 3 ALUs (1-cycle), 2 pipelined MUL/DIV units.
 - **Multiplier**: Radix-4 Booth, 3-cycle latency, 1/cycle throughput.
 - **Divider**: Radix-8, 11-cycle latency, fully pipelined.
- **Scheduler**: Oldest-ready-first issue from RS to FU.
- **Completion Buffer**: For result forwarding to CDB.

4. Memory Cluster

- **Address Generation Unit (AGU)** issues to load/store queues (8 entries each).
- **Data Memory**: 1 KB, 2 load pipes + 1 store pipe.
- **Memory Disambiguation**: Load-to-store forwarding, store coalescing.

Results Waveform:



The waveform shows commit lane: **commit_valid[0]**, **commit_valid[1]**, and **commit_valid[2]** retiring instructions strictly in **program order**, beginning with **ROB_ID = 0** and concluding with **ROB_ID = 32**. Instructions are also **issued in program order** to the execution units, but may complete out of order depending on operand availability and functional unit latency. The **Reorder Buffer (ROB)** then enforces in-order retirement to maintain precise architectural state. This approach allows out-of-order execution to hide latencies by overlapping independent instruction execution, thereby sustaining high instruction throughput.

I used a dependency heavy workload with long – latency mul /div Operations. We have 33 instructions completing in 24 cycles. Therefore **IPC = 1.3750**, (Note: For pure alu independent workload, the IPC will be close to 3.0)

Instructions used for testing:

Data Hazards occur when instructions exhibit dependencies on each other's data, potentially causing incorrect results or stalls in a pipeline. The three primary types are:

1. **Read-After-Write (RAW):** Also called a *true dependency*, occurs when an instruction needs to read a register that a prior instruction is still writing to. This enforces the correct program order to get the right data.
2. **Write-After-Write (WAW):** Also called an *output dependency*, arises when two instructions write to the same register in sequence. The processor must ensure the final write is preserved in program order.
3. **Write-After-Read (WAR):** Also called an *anti-dependency*, happens when an instruction writes to a register that a prior instruction reads. Without proper handling, this can cause the write to overwrite a value before the read completes

The following mix of instructions ensures the processor's **register renaming logic** handles all three dependency types correctly, while the **scheduling and forwarding paths** are stressed with interleaved arithmetic, memory, and multiply/divide instructions of varying latencies.

Instruction data-dependency and hazard table

Instr #	Instruction (assembly)	Dest	Src1	Src2	Description	Dependency Type(s)
0	addi x1, x0, 1	x1	x0	-	x1 = 1	-
1	addi x2, x0, 2	x2	x0	-	x2 = 2	-
2	addi x3, x0, 3	x3	x0	-	x3 = 3	-
3	sw x1, 4(x0)	-	x1	x0	Store x1 to memory[4]	RAW
4	sw x2, 8(x0)	-	x2	x0	Store x2 to memory[8]	RAW
5	sw x3, 12(x0)	-	x3	x0	Store x3 to memory[12]	RAW
6	sw x3, 16(x0)	-	x3	x0	Store x3 to memory[16]	RAW
7	mul x3, x1, x2	x3	x1	x2	x3 = x1 * x2	RAW, WAW
8	add x4, x2, x3	x4	x2	x3	x4 = x2 + x3	RAW
9	add x7, x3, x1	x7	x3	x1	x7 = x3 + x1	RAW
10	add x8, x8, x9	x8	x8	x9	x8 = x8 + x9	RAW
11	lb x1, 4(x0)	x1	x0	-	Load byte into x1 from mem[4]	WAW
12	lbu x9, 8(x0)	x9	x0	-	Load byte unsigned into x9 mem[8]	RAW
13	lw x9, 12(x0)	x9	x0	-	Load word into x9 from mem[12]	WAW, RAW
14	xor x15, x9, x10	x15	x9	x10	x15 = x9 ^ x10	RAW

15	add x10, x10, x11	x10	x10	x11	$x10 = x10 + x11$	RAW
16	add x11, x10, x9	x11	x10	x9	$x11 = x10 + x9$	RAW
17	sll x12, x9, x1	x12	x9	x1	$x12 = x9 \ll x1$	RAW
18	srl x13, x9, x1	x13	x9	x1	$x13 = x9 \gg x1$ (logical)	RAW
19	sub x10, x12, x11	x10	x12	x11	$x10 = x12 - x11$	RAW
20	and x13, x18, x19	x13	x18	x19	$x13 = x18 \& x19$	RAW
21	slt x14, x10, x12	x14	x10	x12	$x14 = (x10 < x12) ? 1 : 0$	RAW
22	add x11, x9, x10	x11	x9	x10	$x11 = x9 + x10$	RAW
23	div x6, x2, x1	x6	x2	x1	$x6 = x2 / x1$	RAW, WAW
24	lb x18, 16(x0)	x18	x0	-	Load byte into x18 from mem[16]	-
25	lb x19, 20(x0)	x19	x0	-	Load byte into x19 from mem[20]	-
26	sw x25, 20(x19)	-	x25	x19	Store x25 to memory[x19 + 20]	RAW
27	add x1, x9, x10	x1	x9	x10	$x1 = x9 + x10$	RAW
28	add x2, x9, x11	x2	x9	x11	$x2 = x9 + x11$	RAW
29	add x3, x1, x2	x3	x1	x2	$x3 = x1 + x2$	RAW
30	mul x8, x1, x3	x8	x1	x3	$x8 = x1 * x3$	RAW, WAW
31	or x7, x1, x2	x7	x1	x2	$x7 = x1$	x2
32	add x29, x7, x1	x29	x7	x1	$x29 = x7 + x1$	RAW

CPU Top-Level

The design.sv file implements the **complete top-level integration** of a RISC-V Tomasulo out-of-order processor. It serves as the main system-on-chip (SoC) wrapper that connects all major processor components into a unified, parameterized architecture.

1. Frontend with Branch Prediction

Module: frontend_with_branch_predictor

Key Features:

- Instruction Fetch: 3-wide instruction fetch with branch prediction
- Branch Predictor: GShare predictor with BTB (64 sets, 4 ways)
- Instruction Queue: 16-entry queue for fetch-decode buffering

- RAS Support: 16-entry Return Address Stack for call/return prediction
- BPQ Integration: Branch Prediction Queue for misprediction recovery

2. Instruction Decoder

Module: tomasulo_decoder

Key Features:

- 3-wide Decoding: Decodes up to 3 instructions per cycle
- RISC-V RV32I Support: Full instruction set decoding
- Error Detection: Comprehensive decoder error reporting
- Stall Handling: Integrates with allocation backpressure

3. Tomasulo Core (Backend)

Module: alloc_reorder_retire

Key Features:

- Register Renaming: 32-entry RAT with ROB-based renaming
- Resource Allocation: 48-entry ROB, 12 ALU RS, 4 Mul/Div RS, 8 Branch RS
- Out-of-Order Execution: Full Tomasulo algorithm implementation
- Checkpoint Management: 16 checkpoints for branch misprediction recovery
- In-Order Retirement: Ensures program order commitment

4. Functional Units

Module: func_unit

Key Features:

- 3 ALU Units: Arithmetic, logical, and comparison operations
- 2 Mul/Div Units: Multiplication and division with pipelined execution
- Priority Dispatch: ROB-based priority for oldest instruction first
- Result Generation: ALU_Result_t format for CDB integration

5. Branch Execution Unit

Module: branch_exec_unit

Key Features:

- Branch Resolution: All conditional and unconditional branches
- Misprediction Detection: Compares actual vs predicted outcomes
- BPQ Coordination: Verifies predictions against BPQ entries
- Recovery Signaling: Provides correct PC for misprediction recovery

6. Completion Buffer

Module: completion_buffer

Key Features:

- Result Collection: Aggregates results from all functional units
- CDB Distribution: 3-wide result broadcasting to reservation stations
- Bypass Mode: Zero-latency forwarding when buffer empty
- FIFO Ordering: Ensures proper result sequencing

7. Memory Subsystem

Module: top_memory_subsystem

Key Features:

- Load/Store Buffer: 16-entry LSB for memory operation management
- Memory Disambiguation: Store-to-load forwarding and violation detection
- Multi-Port Memory: 2 load ports, 1 store port
- Speculative Execution: Load speculation with recovery support

Pipeline Architecture

Pipeline Stages:

Fetch → Decode → Dispatch → Execute → Memory → Commit

Key Pipeline Features:

- 3-wide Superscalar: Processes up to 3 instructions per cycle
- Out-of-Order Execution: Tomasulo algorithm for maximum parallelism
- Speculative Execution: Branch prediction with recovery mechanisms
- In-Order Retirement: Maintains program correctness

Top Level Parameters

```
// Core Architecture
parameter int ISSUE_WIDTH = 3,           // Instructions per cycle
parameter int CDB_WIDTH = 3,            // Results per cycle
parameter int no_ROB = 48,              // Reorder buffer entries
parameter int no_RS_addsublog = 12,      // ALU reservation stations
parameter int no_RS_muldiv = 4,         // Mul/Div reservation stations
parameter int no_RS_branch = 8,         // Branch reservation stations
parameter int no_LoadStoreBuffer = 16,   // Load/Store buffer entries

// Frontend Configuration
parameter int IQ_DEPTH = 16,             // Instruction queue depth
parameter int BTB_SETS = 64,            // BTB sets
parameter int BTB_WAYS = 4,             // BTB ways
parameter int GSHARE_TABLE_BITS = 10,   // GShare predictor bits
parameter int RAS_DEPTH = 16,           // RAS depth
parameter int BPQ_DEPTH = 16,           // BPQ depth

// Memory Configuration
parameter int NUM_LD_PORTS = 2,          // Load ports
parameter int NUM_ST_PORTS = 1,         // Store ports
parameter int MEM_DEPTH = 1024,         // Data memory depth
parameter int LQ_DEPTH = 8,             // Load queue depth
parameter int SQ_DEPTH = 8,             // Store queue depth
```

Fetch Stage Overview

1. Frontend with Branch Predictor Integration (fetch.sv)

- Top-level module orchestrating the entire front-end.
 - **3-wide fetch capability** — processes up to 3 instructions simultaneously.
 - Integrated branch prediction using **BTB**, **Gshare**, and **RAS**.
 - **PC selection logic** with priority-based resolution:
 1. **Misprediction recovery** (highest priority)
 2. **Branch prediction** (if valid)
 3. **Sequential PC** (fallback)
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2. Fetch Unit (fetch_unit.sv)

- Instruction memory interface with **64-entry capacity**.
 - **Instruction Queue** — 16-entry FIFO for buffering fetched instructions.
 - Multi-ported design supporting **parallel enqueue/dequeue operations**.
 - **Stall handling** when instruction queue is full.
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3. Branch Predictor Unit (branch_predictor.sv)

- **3-tier prediction system:**
 - **BTB (Branch Target Buffer):** 64-set, 4-way associative cache for branch targets.
 - **Gshare Predictor:** 1024-entry Pattern History Table with 10-bit global history.
 - **RAS (Return Address Stack):** 16-entry stack for function call/return prediction.
 - **Branch Prediction Queue (BPQ):** 16-entry queue tracking in-flight predictions.
 - Parallel prediction for **all 3 fetch slots** simultaneously.
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4. Instruction Memory (fetch_unit.sv)

- **Byte-addressed** memory with 64-entry capacity.
 - Contains hardcoded **RISC-V test program** (arithmetic, memory, and control flow instructions).
 - Debug capabilities with **PC** and **cycle count tracking**.
 - **Initialization pulse** for system startup.
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Pipeline Flow Control

- Stall propagation through all stages.
 - Flush handling for branch mispredictions.
 - Queue management with **full/empty detection**.
 - Back-pressure support from downstream stages.
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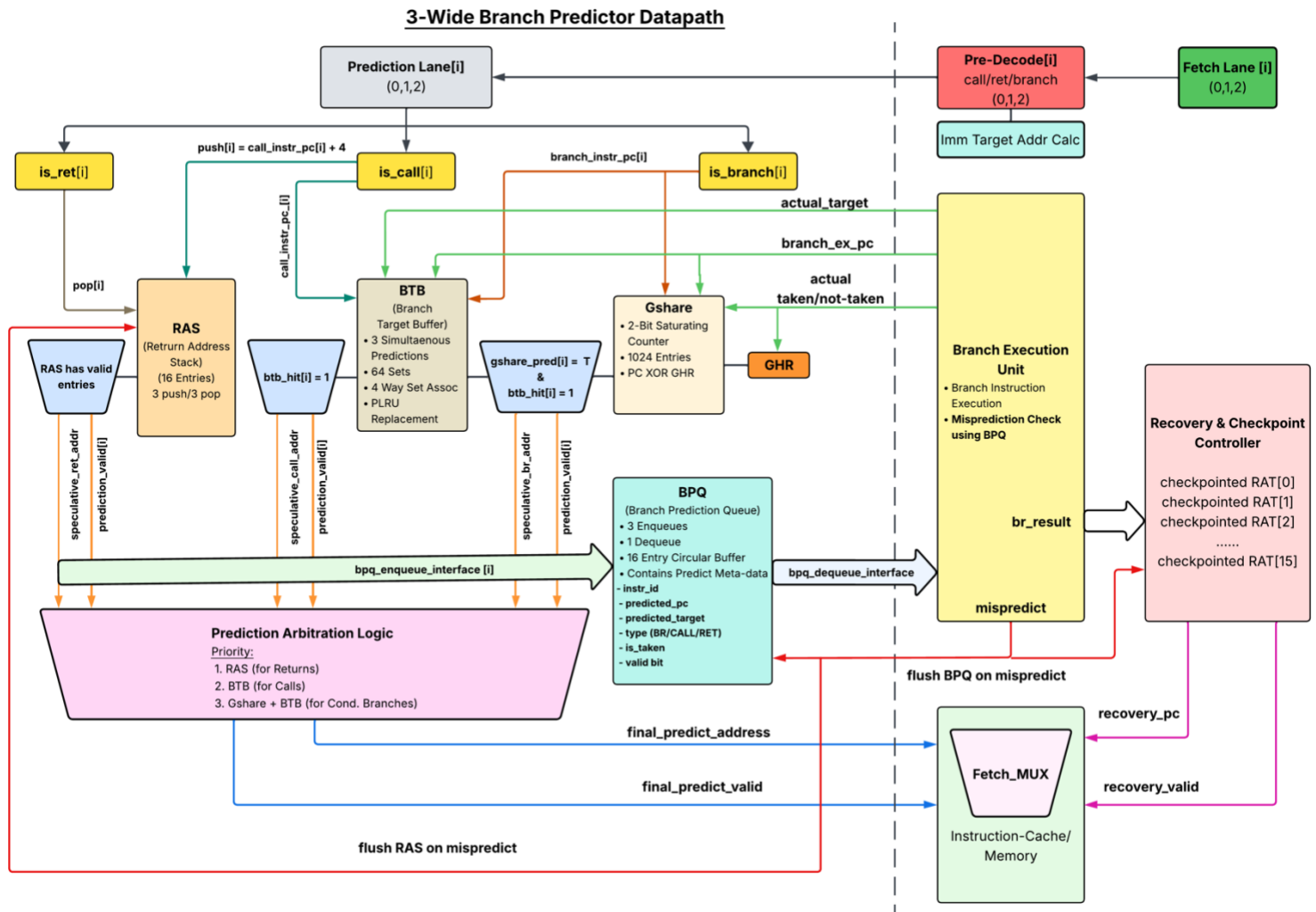
Instruction Types Supported

- **R-type:** Register-register operations.
- **I-type:** Immediate and load operations.
- **S-type:** Store operations.
- **B-type:** Conditional branches.
- **J-type:** Unconditional jumps (**JAL/JALR**).
- **Function calls/returns:** Predicted via **RAS**.

Detailed Functionality & Working Algorithm of the Branch Predictor

Branch Predictor Overview (3-Stage Hybrid)

- **BTB (Branch Target Buffer):** 4-way set associative, 64 sets (256 entries total), stores branch target addresses.
- **Gshare Predictor:** 1024-entry, 2-bit saturating counters with a 10-bit global history register for branch direction.
- **RAS (Return Address Stack):** 16-entry LIFO stack for CALL/RET predictions.
- **BPQ (Branch Prediction Queue):** Tracks in-flight predictions for later verification.



Prediction Process Priority:

1. **RET** → use RAS target (highest priority).
2. **CALL** with BTB hit → use BTB target.
3. **Branch** with BTB hit → use Gshare direction + BTB target.
4. Else → use sequential PC (PC + 4).

BTB Operation:

4-Way Set-Associative BTB

- **Configuration:** 64 sets \times 4 ways = 256 entries
- **Indexing:** set_index = PC[SET_IDX+1 : 2]
- **Tag:** tag = PC[XLEN-1 : SET_IDX+2]

Lookup (3 parallel fetch PCs)

1. Compute set_index and tag
2. Search all 4 ways in the indexed set
 - If valid & tag match → **BTB hit** → return target
 - Else → **BTB miss** → fetch sequential PC

Update on Branch Resolution

1. Recompute set_index and tag
2. Select empty way or PLRU victim
3. Write entry: valid=1, tag=computed_tag, target=actual_target
4. Update PLRU state

Gshare Operation:

Structure

- 1024-entry 2-bit saturating counter table
- 10-bit Global History Register (GHR)

Prediction

1. index = PC[11:2] XOR GHR[9:0]
2. Read counter from table
3. Predict: MSB = 0 → not taken, MSB = 1 → taken

Update

1. Recompute index
2. Increment counter if taken (max 11), decrement if not taken (min 00)
3. Update GHR: GHR = {GHR[8:0], actual_taken}

RAS Operation:

- **CALL:** Push (PC + 4).
- **RET:** Pop top address.
- Handles overflow (drop) & underflow (sequential PC).

BPQ Operation:

- Enqueue predictions at fetch.
- Dequeue at retirement; verify prediction.
- On misprediction → flush pipeline, update predictor tables, restart fetch from correct target.

Misprediction Recovery:

- Flush RAS/BPQ on mis-predict, correct predictor state (Update BTB with correct target address, and Gshare with actual T/NT), resume from actual target.

Decoder (decoder.sv)

Throughput & Role: 3-wide parallel decode, sits between fetch and allocation. Maintains pipeline flow with stall/ready signals.

Instruction Processing: Extracts opcode, funct3/funct7, source/dest regs, immediates. Classifies as ALU, Memory, Mul/Div, or Control. Generates unique 17-bit operation IDs.

Register Handling: Identifies src1/src2, determines dest reg, auto-zeroes dest for store/branch.

Flow Control: Handles backpressure (alloc_rdy, dec_rdy), stalls preserve decode state.

Error Handling: Detects invalid/unsupported ops, raises single-cycle error pulses, propagates to higher levels.

Data Packaging: Uses decode_entry_t struct with raw & decoded fields, immediates, op ID, type, valid flag.

Supported Ops: ALU (reg & imm), load/store, branches/jumps, M-extension (mul/div).

Function: Supplies clean, structured instruction info for register renaming, dependency resolution, and scheduling in the OoO backend.

Allocation/ Reorder/ Retire (alloc_reorder_retire.sv)

Core backend unit for allocation, register renaming, reordering, and retirement in a RISC-V Tomasulo triple-issue out-of-order CPU. Maintains correctness via **in-order retirement** while enabling **out-of-order execution**.

Architecture Overview

- **Register Renaming**
 - **RAT:** Maps architectural → physical registers (ROB entries).
 - **Temp RAT:** Handles intra-bundle dependencies during dispatch.
 - Multi-writer support for superscalar rename.
- **Reservation Stations**
 - ALU: 12 entries
 - Mul/Div: 4 entries
 - Load/Store Buffer: 16 entries
 - Branch: 8 entries
- **Reorder Buffer (ROB)**
 - 48-entry circular buffer, tracks completion & results.
 - Maintains program order for commit.
- **Checkpoints**
 - 16 snapshots for branch misprediction recovery.

Key Pipeline Stages

1. **Resource Availability Check**
 - Monitors free ROB slots, RS entries, checkpoints.
 - Issues stall signals if resources full.
2. **Dispatch**
 - Allocates ROB entries.
 - Resolves operands via RAT lookups & forwarding.
 - Handles intra-bundle hazards.
3. **Reservation Station Allocation**
 - Assigns instructions to matching functional units.
 - Tracks ready/busy states.
 - Wakeup logic on operand availability.

4. Writeback & Commit

- Receives results via CDB.
- Commits up to 3 instructions per cycle in-order.
- Updates ARF at retirement.

Advanced Features

- **Zero-Cycle Wakeup**
 - Immediate result forwarding from CDB.
 - Retirement bypass for completing instructions.
- **Branch Recovery**
 - Checkpoint-based state restore.
 - Selective speculative flush.
- **Triple-Issue**
 - Vectorized handling of 3 instructions/cycle.

Interfaces

- **Inputs:** Decoded instructions, FU completion, CDB results, branch resolution, memory store acks.
- **Outputs:** RS dispatch, commit signals, stall/flush control, recovery signals.

Performance Optimizations

- Parallel processing of instruction bundles.
- Resource tracking to avoid stalls.
- Multiple bypass networks for reduced hazards.
- Efficient selective checkpoint creation.

Forwarding Logic

The processor implements a multi-level forwarding system to achieve zero-cycle operand wakeup, eliminate data hazards, and maximize instruction throughput.

1. Dispatch-Stage Forwarding (Zero-Cycle Wakeup)

Intra-bundle forwarding: Later instructions in the same dispatch bundle can forward operands from earlier instructions.

```
// Search prior instructions in bundle for src1 dependency
for (prev = dispatch_idx - 1; prev >= 0; prev--) begin
    if (decode_reg[prev].valid && decode_reg[prev].dst != 0 &&
        decode_reg[prev].dst == decode_reg[dispatch_idx].src1 && !found_src1) begin
        dispatch_reg_next[dispatch_idx].src1_tag = (ROB_head + prev) % no_ROB;
        dispatch_reg_next[dispatch_idx].src1_ready = 1'b0;
        found_src1 = 1;
    end
end
end
```

CDB bypass at dispatch: Results currently on the Common Data Bus (CDB) are forwarded immediately.

```
for (int cdb_idx = 0; cdb_idx < CDB_WIDTH; cdb_idx++) begin
    if (cdb_results_in[cdb_idx].result_ready &&
        cdb_results_in[cdb_idx].ROB_index == dispatch_reg_next[dispatch_idx].src1_tag) begin
        dispatch_reg_next[dispatch_idx].src1_value = cdb_results_in[cdb_idx].result;
        dispatch_reg_next[dispatch_idx].src1_ready = 1'b1;
    end
    // Also check previous cycle's CDB results (cdb_results_reg_1)
end
```

Retirement bypass: Results retiring in the same cycle are forwarded to dispatch stage.

```
for (int retire_idx = 0; retire_idx < ISSUE_WIDTH; retire_idx++) begin
    if (retire_info_current[retire_idx].result_ready &&
        retire_info_current[retire_idx].ROB_index == dispatch_reg_next[dispatch_idx].src1_tag) begin
        dispatch_reg_next[dispatch_idx].src1_value = retire_info_current[retire_idx].result;
        dispatch_reg_next[dispatch_idx].src1_ready = 1'b1;
    end
end
```

2. Reservation Station Allocation Forwarding

Additional forwarding occurs during RS allocation for operands not ready at dispatch.

```
if (!dispatch_reg[dispatch_idx].src1_ready) begin
    for (int retire_idx = 0; retire_idx < ISSUE_WIDTH; retire_idx++) begin
        if (retire_info_reg_1[retire_idx].result_ready &&
            retire_info_reg_1[retire_idx].ROB_index == dispatch_reg[dispatch_idx].src1_tag) begin
            AS_RS[dispatch_reg[dispatch_idx].rs_index].src1_value <= retire_info_reg_1[retire_idx].result;
            AS_RS[dispatch_reg[dispatch_idx].rs_index].src1_valid <= 1'b1;
        end
    end
end
```

3. CDB Broadcast Wakeup Logic (4-Level Priority)

When broadcasting on the CDB, the processor applies strict priority forwarding for all RS and buffers:

- **Level 1:** Current CDB results
- **Level 2:** 1-cycle delayed CDB results
- **Level 3:** Current retirement results
- **Level 4:** 1-cycle delayed retirement results

Example for src1 in ALU RS:

```
// Level 1: Current CDB
for (int cdb_idx = 0; cdb_idx < CDB_WIDTH && !found_src1; cdb_idx++) begin
    if (cdb_results_in[cdb_idx].result_ready &&
        cdb_results_in[cdb_idx].ROB_index == AS_RS[as_idx].src1_tag) begin
        AS_RS[as_idx].src1_value <= cdb_results_in[cdb_idx].result;
        AS_RS[as_idx].src1_valid <= 1'b1;
        found_src1 = 1;
    end
end
```

```
// Level 2: Delayed CDB
// Level 3: Current Retirement Results
// Level 4: Delayed Retirement Results
```

4. Forwarding Targets

- **ALU Reservation Stations:** src1 and src2 operands
- **Mul/Div Reservation Stations:** src1 and src2 operands
- **Load/Store Buffer:** Address operand (src_valid) and store data operand (store_data_valid)

All receive comprehensive forwarding via the 4-level priority.

5. Ready Signal Update

Operands ready signals and overall RS ready signal updated when operands are valid:

```
for (as_idx = 0; as_idx < no_RS_addsublog; as_idx++) begin
    if (AS_RS[as_idx].busy && !AS_RS[as_idx].ready) begin
        AS_RS[as_idx].ready <= AS_RS[as_idx].src1_valid && AS_RS[as_idx].src2_valid;
    end
end
```

For stores:

```
if (is_store(LS_buffer[ls_idx].op)) begin
    LS_buffer[ls_idx].ready <= LS_buffer[ls_idx].src_valid && LS_buffer[ls_idx].store_data_valid;
end else begin
    LS_buffer[ls_idx].ready <= LS_buffer[ls_idx].src_valid;
end
```

Completion Buffer (completion_buffer.sv)

The completion buffer acts as a centralized hub for collecting and distributing execution results within the RISC-V Tomasulo processor. It interfaces between multiple functional units and the Common Data Bus (CDB), ensuring proper ordering and efficient delivery of results to waiting instructions.

Key Features:

- **Multi-Input Handling:** Supports up to 10 functional unit inputs (ALU, Mul/Div, Branch, Memory) and dispatches up to 3 results per cycle on a 48-entry circular FIFO buffer.
- **Dual-Mode Operation:**
 - *Normal Mode:* Buffers results in FIFO order to maintain correct sequencing.
 - *Bypass Mode:* Enables zero-latency forwarding by directly routing results to the CDB when the buffer is empty, the number of ready inputs fits the CDB width, and CDB outputs are ready.
- **FIFO Management:** Employs modulo wraparound pointers (head_ptr, tail_ptr) and a counter for tracking valid entries.
- **Control Logic:** Ensures sequential enqueue/dequeue operations, and provides early warning signals (buffer_almost_full) to prevent stalls.
- **Status Monitoring:** Outputs buffer full/empty flags and current occupancy count for pipeline flow control.

Operation Flow:

- Functional units submit results flagged as ready, which are stored at the tail of the buffer; the buffer count increments accordingly.
- Up to three results are dispatched per cycle from the buffer head to the CDB, with the buffer count decrementing on successful dispatch.
- When conditions allow, the bypass mode enables direct, zero-latency forwarding of results from functional units to the CDB, bypassing the buffer entirely.

Performance Optimizations:

- Zero-latency bypass reduces average latency by forwarding results immediately when possible.
- FIFO ordering preserves program order and simplifies pointer management with efficient modulo arithmetic.
- Capacity management with early warnings prevents buffer overflows and pipeline stalls.

Integration with Tomasulo Algorithm:

- The 3-wide CDB interface supports concurrent broadcasting to multiple reservation stations, with ready handshaking for backpressure control.
- Aggregates results from all functional units, maintaining ROB indices to support precise wakeup logic.
- Implements stall prevention via buffer capacity signaling and bypass mode.

Design Benefits:

- Centralizes result management across diverse execution units.
- Efficiently distributes results while preserving ordering and minimizing latency.
- Scales easily with parameterizable buffer depths and CDB widths.
- Enhances pipeline throughput by preventing stalls and enabling fast wakeups.

Execution Units Overview:

1. ALU (Arithmetic Logic Unit) Execution Unit

Files:

- alu_top.sv – Dispatch and routing logic for ALU operations
- alu_unit.sv – Core functional unit implementation

Key Points:

- **Configuration:** 3 ALU units, dispatched from 12 reservation stations with ROB-based priority
 - **Operations:** ADD, SUB, ADDI, AND, OR, XOR, SLL, SRL, SRA, SLT, SLTU
 - **Execution:** Single-cycle
 - **Features:** Immediate operand support, priority-based dispatch
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2. Multiplication / Division Unit

Files:

- mul_div_top.sv – Dispatch and routing logic
- mul_div.sv – Functional unit for multiply/divide
- radix_4_multiplier.sv – 3-stage pipelined Booth-encoded multiplier
- radix_8_divisor.sv – Pipelined Radix-8 divider

Key Points:

- **Configuration:** 2 Mul/Div units, can issue multiply and divide simultaneously
 - **Multiplier:** Radix-4 Booth encoding + CSA tree, 3-stage pipeline
 - **Divider:** Radix-8 iterative algorithm, pipelined
 - **Features:** Multi-cycle execution, signed/unsigned support, tag-based result tracking
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3. Branch Execution Unit

Files:

- branch_execution_unit.sv – Branch execution and prediction verification

Key Points:

- **Operations:** JAL, JALR, BEQ, BNE, BLT, BGE, BLTU, BGEU
 - **Features:**
 - Branch prediction validation (BPQ interface)
 - Misprediction detection and recovery
 - Call/return handling
 - ROB-priority dispatch from 8 reservation stations
 - Error detection and reporting
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Memory Management Unit

Core Memory Management Files

1. top_memory_subsystem.sv - Top-Level Integration

Purpose: Top-level wrapper that instantiates and connects MMU and data memory

Key Features:

- Module integration: Connects memory_management_unit with data_mem
 - Interface abstraction: Exposes only necessary external ports
 - Parameter passing: Configures both MMU and data memory with consistent parameters
 - Signal routing: Handles all memory interface signals between components
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2. memory_management_unit.sv - Core Memory Logic

Purpose: Implements sophisticated memory disambiguation and load/store execution

Key Features:

- Load/Store Buffer (LSB) management: 16-entry buffer for in-flight memory operations
 - Memory disambiguation: Handles store-to-load forwarding and address conflicts
 - Load Queue (LQ): 8-entry queue for load operations with violation detection
 - Store Queue (SQ): 8-entry queue for store operations with coalescing
 - Multiple ports: 2 load ports, 1 store port for parallel memory access
-

3. data_mem.sv - Data Memory Interface

Purpose: Provides the actual memory storage and access interface

Key Features:

- Multi-port memory: Supports multiple simultaneous read/write operations
 - Configurable depth: Parameterized memory size (default 1024 entries)
 - Byte-level access: Supports byte, half-word, and word operations
 - Signed/unsigned support: Handles both signed and unsigned load operations
 - Memory timing: Provides realistic memory access timing
-

Memory Management Architecture

1. Load/Store Buffer (LSB) Interface

// From alloc_reorder_retire.sv

input LS_Buffer_Entry_t [LSB_SIZE-1:0] lsb_entries

- Source: alloc_reorder_retire.sv - Receives memory operations from dispatch
 - Purpose: Holds in-flight load/store instructions waiting for execution
 - Size: 16 entries (configurable via LSB_SIZE parameter)
-

2. Memory Execution Pipeline

// Memory ports configuration

parameter NUM_LD_PORTS = 2, // 2 load ports

parameter NUM_ST_PORTS = 1, // 1 store port

parameter LQ_DEPTH = 8, // Load queue depth

parameter SQ_DEPTH = 8 // Store queue depth

3. Result Interface

// To completion_buffer.sv and alloc_reorder_retire.sv
output ALU_Result_t [NUM_LD_PORTS-1:0] load_cdb_result

- Destination: completion_buffer.sv - Load results sent to CDB
- Purpose: Provides load results for wakeup logic and retirement

Key Memory Management Features

1. Store-to-Load Forwarding

Implementation: memory_management_unit.sv

- Address comparison: Compares load addresses with pending store addresses
- Data forwarding: Forwards store data to dependent loads when addresses match
- Performance benefit: Eliminates memory access latency for forwarded loads

2. Memory Disambiguation

Implementation: memory_management_unit.sv

- Address conflict detection: Identifies potential store-load conflicts
- Speculative execution: Allows loads to execute speculatively
- Violation detection: Detects when speculative loads violate program order
- Recovery mechanism: Handles violations through ROB-based recovery

3. Load/Store Coalescing

Implementation: memory_management_unit.sv

- Store coalescing: Combines adjacent store operations to same address
- Load optimization: Optimizes load operations for better performance
- Memory bandwidth: Reduces memory traffic through coalescing

Integration with Other Components

1. Allocation Interface

File: alloc_reorder_retire.sv

- LSB allocation: Allocates Load/Store Buffer entries during dispatch
- Dependency resolution: Resolves memory operand dependencies
- Resource tracking: Monitors LSB availability for stall prevention

2. Completion Interface

File: completion_buffer.sv

- Load result delivery: Provides load results to completion buffer
- CDB integration: Integrates with Common Data Bus for result broadcasting
- Wakeup support: Enables operand wakeup for dependent instructions

3. ROB Interface

File: alloc_reorder_retire.sv

```
// ROB head information for in-order commit
input logic [$clog2(ROB_SIZE)-1:0] rob_head [ISSUE_WIDTH-1:0]
```

- In-order commit: Ensures stores commit in program order only when the store instruction reaches the head of ROB
 - Store commit signals: Provides store completion status to ROB
 - Violation reporting: Reports memory violations for ROB handling
-

Instrumentation & Checker System

This system enhances the observability and correctness verification of a Tomasulo-style processor by integrating two complementary components:

- **Instrumentation System (instrumentation.sv):** Provides detailed real-time monitoring and debugging support.
 - **Checker System (checker.sv):** Ensures program correctness by verifying executed instructions against expected results.
-

1. Instrumentation System (instrumentation.sv)

Purpose

Enables comprehensive visibility into the processor pipeline, allowing detailed performance analysis and debugging of complex out-of-order execution dynamics.

Key Features

A. IPC Monitoring

- Tracks Instructions Per Cycle (IPC) from the first instruction commit until the last.
- Records cycle counts and committed instruction counts.
- Computes IPC as the ratio of instructions committed over total cycles.

B. Pipeline Stage Monitoring

- **Decode / Dispatch Stage:**
Displays instruction details including program counter (PC), instruction encoding, type, destination/source registers, opcode, function codes, and immediates.
- **Reorder Buffer (ROB):**
Shows validity, readiness, destination register, computed value, instruction ID, and PC of all ROB entries.
- **Reservation Stations (RS):**
Monitors:
 - ALU reservation stations (add/sub/logic ops)
 - Mul/Div reservation stations
 - Load/Store buffers for memory operations

C. Forwarding Monitoring

- **Common Data Bus (CDB) Forwarding:**
Tracks current and delayed cycle forwarding events from functional units to waiting instructions.
- **Retirement Bypass:**
Observes forwarding directly from retirement stage bypassing the CDB.

- **Intra-Bundle Forwarding:**
Detects forwarding between instructions within the same dispatch bundle.
-

2. Checker System (checker.sv)

Purpose

Validates program correctness by real-time comparison of actual versus expected register values during instruction commit.

Key Features

A. Expected Value Tracking

Utilizes a structured data type to store, per instruction:

- Commit PC
- Destination register
- Expected and actual values
- Pass/fail status
- Instruction string
- ROB ID

B. Instruction Coverage

Supports correctness verification for all 33 instructions in the test program, including:

- **Immediate Instructions:** (e.g., addi)
- **Arithmetic Instructions:** (add, sub, mul, div, and, or, xor, sll, srl, slt)
- **Memory Instructions:** (load byte, load byte unsigned, load word)
- **Store Instructions:** (e.g., sw), with special handling since they have no destination register but affect memory correctness.

C. Real-Time Verification

- Monitors each instruction upon commit.
- Compares actual register values to expected values immediately.
- Prints pass/fail messages with timestamps for rapid debugging feedback.

D. Comprehensive Summary

At program completion, outputs a detailed table summarizing all instruction checks, including expected and actual values and pass/fail status.

Checker Output

```
=== Starting Testbench ===
[Time 0] Initializing with reset=1
[Time 20000] Releasing reset
[Time 35000] Starting main test loop
[Time 35000] Test completed successfully
[105000] ARF Checker: PASS - ROB[0] addi x1, x0, 1 -> x1 = 1
[105000] ARF Checker: PASS - ROB[1] addi x2, x0, 2 -> x2 = 2
[105000] ARF Checker: PASS - ROB[2] addi x3, x0, 3 -> x3 = 3
[135000] ARF Checker: PASS - ROB[3] sw x1, 4(x0) -> x0 = 0
[135000] ARF Checker: PASS - ROB[4] sw x2, 8(x0) -> x0 = 0
[135000] ARF Checker: PASS - ROB[5] sw x3, 12(x0) -> x0 = 0
[145000] ARF Checker: PASS - ROB[6] sw x3, 16(x0) -> x0 = 0
[165000] ARF Checker: PASS - ROB[7] mul x3, x1, x2 -> x3 = 2
[185000] ARF Checker: PASS - ROB[8] add x4, x2, x3 -> x4 = 4
[185000] ARF Checker: PASS - ROB[9] add x7, x3, x1 -> x7 = 3
[185000] ARF Checker: PASS - ROB[10] add x8, x8, x9 -> x8 = 0
[195000] ARF Checker: PASS - ROB[11] lb x1, 4(x0) -> x1 = 1
[195000] ARF Checker: PASS - ROB[12] lbu x9, 8(x0) -> x9 = 2
[195000] ARF Checker: PASS - ROB[13] lw x9, 12(x0) -> x9 = 3
[205000] ARF Checker: PASS - ROB[14] xor x15, x9, x10 -> x15 = 3
[205000] ARF Checker: PASS - ROB[15] add x10, x10, x11 -> x10 = 0
[205000] ARF Checker: PASS - ROB[16] add x11, x10, x9 -> x11 = 3
[215000] ARF Checker: PASS - ROB[17] sll x12, x9, x1 -> x12 = 6
[215000] ARF Checker: PASS - ROB[18] srl x13, x9, x1 -> x13 = 1
[225000] ARF Checker: PASS - ROB[19] sub x10, x12, x11 -> x10 = 3
[225000] ARF Checker: PASS - ROB[20] and x13, x18, x19 -> x13 = 0
[245000] ARF Checker: PASS - ROB[21] slt x14, x10, x12 -> x14 = 1
[245000] ARF Checker: PASS - ROB[22] add x11, x9, x10 -> x11 = 6
[295000] ARF Checker: PASS - ROB[23] div x6, x1, x2 -> x6 = 2
[295000] ARF Checker: PASS - ROB[24] lb x18, 16(x0) -> x18 = 3
[295000] ARF Checker: PASS - ROB[25] lb x19, 20(x0) -> x19 = 5
[305000] ARF Checker: PASS - ROB[26] sw x25, 20(x19) -> x0 = 0
[305000] ARF Checker: PASS - ROB[27] add x1, x9, x10 -> x1 = 6
[305000] ARF Checker: PASS - ROB[28] add x2, x9, x11 -> x2 = 9
[315000] ARF Checker: PASS - ROB[29] add x3, x1, x2 -> x3 = 15
[335000] ARF Checker: PASS - ROB[30] mul x8, x1, x3 -> x8 = 90
[335000] ARF Checker: PASS - ROB[31] or x7, x1, x2 -> x7 = 15
[335000] ARF Checker: PASS - ROB[32] add x29, x7, x1 -> x29 = 21
```

Performance Monitoring

```
[345000] ===== PERFORMANCE METRICS =====
[345000] Cycle Count: 32
[345000] Total Instructions Committed: 33
[345000] All Instructions Completed: 1
```

```
[345000] ===== IPC ANALYSIS =====
[345000] IPC Measurement Period: Cycles 8 to 31
[345000] Total Cycles Measured: 24
[345000] Instructions Committed: 33
[345000] FINAL IPC: 1.3750
[345000] =====
```

```
$finish called from file "testbench.sv", line 169.
```

```
$finish at simulation time 355000
```

```
V C S S i m u l a t i o n R e p o r t
```

=== CHECKER COMPREHENSIVE SUMMARY ===

Total checks performed: 33

Passed: 33, Failed: 0

=== ALL CHECKS PASSED ===

Detailed Results:

ROB_ID	PC	Instruction	Dest	Actual	Expected	Status
0	0	addi x1, x0, 1	x 1	1	1	PASS
1	4	addi x2, x0, 2	x 2	2	2	PASS
2	8	addi x3, x0, 3	x 3	3	3	PASS
3	12	sw x1, 4(x0)	--	--	--	PASS
4	16	sw x2, 8(x0)	--	--	--	PASS
5	20	sw x3, 12(x0)	--	--	--	PASS
6	24	sw x3, 16(x0)	--	--	--	PASS
7	28	mul x3, x1, x2	x 3	2	2	PASS
8	32	add x4, x2, x3	x 4	4	4	PASS
9	36	add x7, x3, x1	x 7	3	3	PASS
10	40	add x8, x8, x9	x 8	0	0	PASS
11	44	lb x1, 4(x0)	x 1	1	1	PASS
12	48	lbu x9, 8(x0)	x 9	2	2	PASS
13	52	lw x9, 12(x0)	x 9	3	3	PASS
14	56	xor x15, x9, x10	x15	3	3	PASS
15	60	add x10, x10, x11	x10	0	0	PASS
16	64	add x11, x10, x9	x11	3	3	PASS
17	68	sll x12, x9, x1	x12	6	6	PASS
18	72	srl x13, x9, x1	x13	1	1	PASS
19	76	sub x10, x12, x11	x10	3	3	PASS
20	80	and x13, x18, x19	x13	0	0	PASS
21	84	slt x14, x10, x12	x14	1	1	PASS
22	88	add x11, x9, x10	x11	6	6	PASS
23	92	div x6, x1, x2	x 6	2	2	PASS
24	96	lb x18, 16(x0)	x18	3	3	PASS
25	100	lb x19, 20(x0)	x19	5	5	PASS
26	104	sw x25, 20(x19)	--	--	--	PASS
27	108	add x1, x9, x10	x 1	6	6	PASS
28	112	add x2, x9, x11	x 2	9	9	PASS
29	116	add x3, x1, x2	x 3	15	15	PASS
30	120	mul x8, x1, x3	x 8	90	90	PASS
31	124	or x7, x1, x2	x 7	15	15	PASS
32	128	add x29, x7, x1	x29	21	21	PASS

Full Instrumentation Debug Output Log

=== Starting Testbench ===

[Time 0] Initializing with reset=1

[Time 20000] Releasing reset

[Time 35000] Starting main test loop

[Time 35000] Test completed successfully

[75000] ===== DECODE/DISPATCH STAGE =====

[75000] DECODE[0]: PC=0x00000000 Instr=0x00100093 Type=0 Dst=1 Src1=0 Src2=0 Opcode=0x13 Func3=0x0 Func7=0x00 Operation=0x00013 Imm=0x00000001

[75000] DECODE[1]: PC=0x00000004 Instr=0x00200113 Type=0 Dst=2 Src1=0 Src2=0 Opcode=0x13 Func3=0x0 Func7=0x00 Operation=0x00013 Imm=0x00000002

[75000] DECODE[2]: PC=0x00000008 Instr=0x00300193 Type=0 Dst=3 Src1=0 Src2=0 Opcode=0x13 Func3=0x0 Func7=0x00 Operation=0x00013 Imm=0x00000003

```

[85000] ===== DECODE/DISPATCH STAGE =====
[85000] DECODE[0]: PC=0x0000000c Instr=0x00102223 Type=1 Dst=0 Src1=0 Src2=1 Opcode=0x23 Func3=0x2 Func7=0x00 Operation=0x00123
Imm=0x00000004
[85000] DECODE[1]: PC=0x00000010 Instr=0x00202423 Type=1 Dst=0 Src1=0 Src2=2 Opcode=0x23 Func3=0x2 Func7=0x00 Operation=0x00123
Imm=0x00000008
[85000] DECODE[2]: PC=0x00000014 Instr=0x00302623 Type=1 Dst=0 Src1=0 Src2=3 Opcode=0x23 Func3=0x2 Func7=0x00 Operation=0x00123
Imm=0x0000000c
[85000] DISPATCH[0]: ROB_ID=0 RS_ID=0 RS_Alloc=1 Src1_Ready=1 Src2_Ready=1 Dst=1 Src1=0 Src2=0 Src1_Tag=0 Src2_Tag=0
Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00013 Type=0 PC=0x00000000 Instr=0x00100093
[85000] DISPATCH[1]: ROB_ID=1 RS_ID=1 RS_Alloc=1 Src1_Ready=1 Src2_Ready=1 Dst=2 Src1=0 Src2=0 Src1_Tag=0 Src2_Tag=0
Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00013 Type=0 PC=0x00000004 Instr=0x00200113
[85000] DISPATCH[2]: ROB_ID=2 RS_ID=2 RS_Alloc=1 Src1_Ready=1 Src2_Ready=1 Dst=3 Src1=0 Src2=0 Src1_Tag=0 Src2_Tag=0
Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00013 Type=0 PC=0x00000008 Instr=0x00300193

[85000] ===== CURRENT RAT AND VALID =====
[85000] RAT[1]: Tag=0 Valid=1
[85000] RAT[2]: Tag=1 Valid=1
[85000] RAT[3]: Tag=2 Valid=1

[95000] ===== DECODE/DISPATCH STAGE =====
[95000] DECODE[0]: PC=0x00000018 Instr=0x00302823 Type=1 Dst=0 Src1=0 Src2=3 Opcode=0x23 Func3=0x2 Func7=0x00 Operation=0x00123
Imm=0x00000010
[95000] DECODE[1]: PC=0x0000001c Instr=0x022081b3 Type=2 Dst=3 Src1=1 Src2=2 Opcode=0x33 Func3=0x0 Func7=0x01 Operation=0x00433
Imm=0x00000000
[95000] DECODE[2]: PC=0x00000020 Instr=0x00310233 Type=0 Dst=4 Src1=2 Src2=3 Opcode=0x33 Func3=0x0 Func7=0x00 Operation=0x00033
Imm=0x00000000
[95000] DISPATCH[0]: ROB_ID=3 RS_ID=0 RS_Alloc=1 Src1_Ready=1 Src2_Ready=0 Dst=0 Src1=0 Src2=1 Src1_Tag=0 Src2_Tag=0
Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00123 Type=1 PC=0x0000000c Instr=0x00102223
[95000] DISPATCH[1]: ROB_ID=4 RS_ID=1 RS_Alloc=1 Src1_Ready=1 Src2_Ready=0 Dst=0 Src1=0 Src2=2 Src1_Tag=0 Src2_Tag=1
Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00123 Type=1 PC=0x00000010 Instr=0x00202423
[95000] DISPATCH[2]: ROB_ID=5 RS_ID=2 RS_Alloc=1 Src1_Ready=1 Src2_Ready=0 Dst=0 Src1=0 Src2=3 Src1_Tag=0 Src2_Tag=2
Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00123 Type=1 PC=0x00000014 Instr=0x00302623

[95000] ===== REORDER BUFFER (ROB) =====
[95000] ROB Head: 6, ROB Tail: 0
[95000] ROB[0]: Valid=1 Ready=0 Dest=1 Value=0x00000000 Instr_ID=0 PC=0x00000000
[95000] ROB[1]: Valid=1 Ready=0 Dest=2 Value=0x00000000 Instr_ID=1 PC=0x00000004
[95000] ROB[2]: Valid=1 Ready=0 Dest=3 Value=0x00000000 Instr_ID=2 PC=0x00000008

[95000] ===== RESERVATION STATIONS =====
[95000] --- ALU Reservation Stations ---
[95000] ALU_RS[0]: Busy=1 Ready=1 ROB_ID=0 Op=0x00013 Src1_Valid=1 Src1_Tag=0 Src1_Value=0x00000000 Src2_Valid=1 Src2_Tag=0
Src2_Value=0x00000000
[95000] ALU_RS[1]: Busy=1 Ready=1 ROB_ID=1 Op=0x00013 Src1_Valid=1 Src1_Tag=0 Src1_Value=0x00000000 Src2_Valid=1 Src2_Tag=0
Src2_Value=0x00000000
[95000] ALU_RS[2]: Busy=1 Ready=1 ROB_ID=2 Op=0x00013 Src1_Valid=1 Src1_Tag=0 Src1_Value=0x00000000 Src2_Valid=1 Src2_Tag=0
Src2_Value=0x00000000

[95000] ===== EXECUTION STAGE (CDB INPUT) =====
[95000] CDB[0]: ROB_ID=0 Result=0x00000001 Ready=1
[95000] CDB[1]: ROB_ID=1 Result=0x00000002 Ready=1
[95000] CDB[2]: ROB_ID=2 Result=0x00000003 Ready=1

[95000] ===== CURRENT RAT AND VALID =====
[95000] RAT[1]: Tag=0 Valid=1
[95000] RAT[2]: Tag=1 Valid=1
[95000] RAT[3]: Tag=2 Valid=1
[105000] IPC MONITOR: Starting IPC tracking at cycle 8 (first commit)

[105000] ===== DECODE/DISPATCH STAGE =====
[105000] DECODE[0]: PC=0x00000024 Instr=0x001183b3 Type=0 Dst=7 Src1=3 Src2=1 Opcode=0x33 Func3=0x0 Func7=0x00 Operation=0x00033
Imm=0x00000000
[105000] DECODE[1]: PC=0x00000028 Instr=0x00940433 Type=0 Dst=8 Src1=8 Src2=9 Opcode=0x33 Func3=0x0 Func7=0x00 Operation=0x00033
Imm=0x00000000

```

[105000] DECODE[2]: PC=0x0000002c Instr=0x00400083 Type=1 Dst=1 Src1=0 Src2=4 Opcode=0x03 Func3=0x0 Func7=0x00 Operation=0x00003 Imm=0x00000004

[105000] DISPATCH[0]: ROB_ID=6 RS_ID=3 RS_Alloc=1 Src1_Ready=1 Src2_Ready=1 Dst=0 Src1=0 Src2=3 Src1_Tag=0 Src2_Tag=0 Src1_Value=0x00000000 Src2_Value=0x00000003 Operation=0x00123 Type=1 PC=0x00000018 Instr=0x00302823

[105000] DISPATCH[1]: ROB_ID=7 RS_ID=0 RS_Alloc=1 Src1_Ready=1 Src2_Ready=1 Dst=3 Src1=1 Src2=2 Src1_Tag=0 Src2_Tag=1 Src1_Value=0x00000001 Src2_Value=0x00000002 Operation=0x00433 Type=2 PC=0x0000001c Instr=0x022081b3

[105000] DISPATCH[2]: ROB_ID=8 RS_ID=3 RS_Alloc=1 Src1_Ready=1 Src2_Ready=0 Dst=4 Src1=2 Src2=3 Src1_Tag=0 Src2_Tag=7 Src1_Value=0x00000002 Src2_Value=0x00000000 Operation=0x00033 Type=0 PC=0x00000020 Instr=0x00310233

[105000] ===== REORDER BUFFER (ROB) =====

[105000] ROB Head: 9, ROB Tail: 3

[105000] ROB[3]: Valid=1 Ready=0 Dest=0 Value=0x00000000 Instr_ID=3 PC=0x0000000c

[105000] ROB[4]: Valid=1 Ready=0 Dest=0 Value=0x00000000 Instr_ID=4 PC=0x00000010

[105000] ROB[5]: Valid=1 Ready=0 Dest=0 Value=0x00000000 Instr_ID=5 PC=0x00000014

[105000] ===== RESERVATION STATIONS =====

[105000] --- Load/Store Buffer ---

[105000] LSB[0]: Busy=1 Ready=0 ROB_ID=3 Op=0x00123 Src_Valid=1 Src_Tag=0 Src_Value=0x00000000 Store_Data_Valid=0 Store_Data_Tag=0 Store_Data=0x00000000

[105000] LSB[1]: Busy=1 Ready=0 ROB_ID=4 Op=0x00123 Src_Valid=1 Src_Tag=0 Src_Value=0x00000000 Store_Data_Valid=0 Store_Data_Tag=1 Store_Data=0x00000000

[105000] LSB[2]: Busy=1 Ready=0 ROB_ID=5 Op=0x00123 Src_Valid=1 Src_Tag=0 Src_Value=0x00000000 Store_Data_Valid=0 Store_Data_Tag=2 Store_Data=0x00000000

[105000] ===== FORWARDING MESSAGES =====

[105000] FORWARD[CDB_DELAYED->LSB_STORE]: CDB_DELAYED[0] ROB_ID=0 -> LSB[0] ROB_ID=3 Store_Data=0x00000001

[105000] FORWARD[CDB_DELAYED->LSB_STORE]: CDB_DELAYED[1] ROB_ID=1 -> LSB[1] ROB_ID=4 Store_Data=0x00000002

[105000] FORWARD[CDB_DELAYED->LSB_STORE]: CDB_DELAYED[2] ROB_ID=2 -> LSB[2] ROB_ID=5 Store_Data=0x00000003

[105000] FORWARD[INTRA_SRC2]: DISPATCH[1] ROB_ID=7 -> DISPATCH[2] ROB_ID=8 Reg=3

[105000] ===== INSTRUCTIONS COMMITTED THIS CYCLE =====

[105000] COMMITTED[0]: ROB_ID=0

[105000] COMMITTED[1]: ROB_ID=1

[105000] COMMITTED[2]: ROB_ID=2

[105000] Total Instructions Committed This Cycle: 3

[105000] ===== CURRENT RAT AND VALID =====

[105000] RAT[3]: Tag=7 Valid=1

[105000] RAT[4]: Tag=8 Valid=1

[105000] ===== ARCHITECTURAL REGISTER FILE (ARF) =====

[105000] ARF[1]: Value=0x00000001

[105000] ARF[2]: Value=0x00000002

[105000] ARF[3]: Value=0x00000003

[105000] ARF Checker: PASS - ROB[0] addi x1, x0, 1 -> x1 = 1

[105000] ARF Checker: PASS - ROB[1] addi x2, x0, 2 -> x2 = 2

[105000] ARF Checker: PASS - ROB[2] addi x3, x0, 3 -> x3 = 3

[115000] ===== DECODE/DISPATCH STAGE =====

[115000] DECODE[0]: PC=0x00000030 Instr=0x00804483 Type=1 Dst=9 Src1=0 Src2=8 Opcode=0x03 Func3=0x4 Func7=0x00 Operation=0x00203 Imm=0x00000008

[115000] DECODE[1]: PC=0x00000034 Instr=0x00c02483 Type=1 Dst=9 Src1=0 Src2=12 Opcode=0x03 Func3=0x2 Func7=0x00 Operation=0x00103 Imm=0x0000000c

[115000] DECODE[2]: PC=0x00000038 Instr=0x00a4c7b3 Type=0 Dst=15 Src1=9 Src2=10 Opcode=0x33 Func3=0x4 Func7=0x00 Operation=0x00233 Imm=0x00000000

[115000] DISPATCH[0]: ROB_ID=9 RS_ID=0 RS_Alloc=1 Src1_Ready=0 Src2_Ready=1 Dst=7 Src1=3 Src2=1 Src1_Tag=7 Src2_Tag=0 Src1_Value=0x00000000 Src2_Value=0x00000001 Operation=0x00033 Type=0 PC=0x00000024 Instr=0x001183b3

[115000] DISPATCH[1]: ROB_ID=10 RS_ID=1 RS_Alloc=1 Src1_Ready=1 Src2_Ready=1 Dst=8 Src1=8 Src2=9 Src1_Tag=0 Src2_Tag=1 Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00033 Type=0 PC=0x00000028 Instr=0x00940433

[115000] DISPATCH[2]: ROB_ID=11 RS_ID=4 RS_Alloc=1 Src1_Ready=1 Src2_Ready=0 Dst=1 Src1=0 Src2=4 Src1_Tag=0 Src2_Tag=8 Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00003 Type=1 PC=0x0000002c Instr=0x00400083

[115000] ===== REORDER BUFFER (ROB) =====

[115000] ROB Head: 12, ROB Tail: 3

[115000] ROB[3]: Valid=1 Ready=0 Dest=0 Value=0x00000000 Instr_ID=3 PC=0x0000000c

[115000] ROB[4]: Valid=1 Ready=0 Dest=0 Value=0x00000000 Instr_ID=4 PC=0x00000010
[115000] ROB[5]: Valid=1 Ready=0 Dest=0 Value=0x00000000 Instr_ID=5 PC=0x00000014
[115000] ROB[6]: Valid=1 Ready=0 Dest=0 Value=0x00000000 Instr_ID=6 PC=0x00000018
[115000] ROB[7]: Valid=1 Ready=0 Dest=3 Value=0x00000000 Instr_ID=7 PC=0x0000001c
[115000] ROB[8]: Valid=1 Ready=0 Dest=4 Value=0x00000000 Instr_ID=8 PC=0x00000020

[115000] ===== RESERVATION STATIONS =====

[115000] --- ALU Reservation Stations ---

[115000] ALU_RS[3]: Busy=1 Ready=0 ROB_ID=8 Op=0x00033 Src1_Valid=1 Src1_Tag=0 Src1_Value=0x00000002 Src2_Valid=0 Src2_Tag=7
Src2_Value=0x00000000

[115000] --- Mul/Div Reservation Stations ---

[115000] MD_RS[0]: Busy=1 Ready=1 ROB_ID=7 Op=0x00433 Src1_Valid=1 Src1_Tag=0 Src1_Value=0x00000001 Src2_Valid=1 Src2_Tag=1
Src2_Value=0x00000002

[115000] --- Load/Store Buffer ---

[115000] LSB[0]: Busy=1 Ready=0 ROB_ID=3 Op=0x00123 Src_Valid=1 Src_Tag=0 Src_Value=0x00000000 Store_Data_Valid=1 Store_Data_Tag=0
Store_Data=0x00000001

[115000] LSB[1]: Busy=1 Ready=0 ROB_ID=4 Op=0x00123 Src_Valid=1 Src_Tag=0 Src_Value=0x00000000 Store_Data_Valid=1 Store_Data_Tag=1
Store_Data=0x00000002

[115000] LSB[2]: Busy=1 Ready=0 ROB_ID=5 Op=0x00123 Src_Valid=1 Src_Tag=0 Src_Value=0x00000000 Store_Data_Valid=1 Store_Data_Tag=2
Store_Data=0x00000003

[115000] LSB[3]: Busy=1 Ready=1 ROB_ID=6 Op=0x00123 Src_Valid=1 Src_Tag=0 Src_Value=0x00000000 Store_Data_Valid=1 Store_Data_Tag=0
Store_Data=0x00000003

[115000] ===== CURRENT RAT AND VALID =====

[115000] RAT[1]: Tag=11 Valid=1

[115000] RAT[3]: Tag=7 Valid=1

[115000] RAT[4]: Tag=8 Valid=1

[115000] RAT[7]: Tag=9 Valid=1

[115000] RAT[8]: Tag=10 Valid=1

[115000] ===== ARCHITECTURAL REGISTER FILE (ARF) =====

[115000] ARF[1]: Value=0x00000001

[115000] ARF[2]: Value=0x00000002

[115000] ARF[3]: Value=0x00000003

[115000] [MMU] STORE ISSUED: SQ[0] ROB_ID=3 Addr=0x00000004 Data=0x00000001 Size=2

[125000] [MMU] LOAD ENQUEUED: LSB[4] ROB_ID=11 Op=0x00003 Addr=0x00000004 Size=0

[125000] ===== DECODE/DISPATCH STAGE =====

[125000] DECODE[0]: PC=0x0000003c Instr=0x00b50533 Type=0 Dst=10 Src1=10 Src2=11 Opcode=0x33 Func3=0x0 Func7=0x00 Operation=0x00033
Imm=0x00000000

[125000] DECODE[1]: PC=0x00000040 Instr=0x009545b3 Type=0 Dst=11 Src1=10 Src2=9 Opcode=0x33 Func3=0x4 Func7=0x00 Operation=0x00233
Imm=0x00000000

[125000] DECODE[2]: PC=0x00000044 Instr=0x00149633 Type=0 Dst=12 Src1=9 Src2=1 Opcode=0x33 Func3=0x1 Func7=0x00 Operation=0x000b3
Imm=0x00000000

[125000] DISPATCH[0]: ROB_ID=12 RS_ID=5 RS_Alloc=1 Src1_Ready=1 Src2_Ready=0 Dst=9 Src1=0 Src2=8 Src1_Tag=0 Src2_Tag=10
Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00203 Type=1 PC=0x00000030 Instr=0x00804483

[125000] DISPATCH[1]: ROB_ID=13 RS_ID=6 RS_Alloc=1 Src1_Ready=1 Src2_Ready=1 Dst=9 Src1=0 Src2=12 Src1_Tag=0 Src2_Tag=1
Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00103 Type=1 PC=0x00000034 Instr=0x00c02483

[125000] DISPATCH[2]: ROB_ID=14 RS_ID=2 RS_Alloc=1 Src1_Ready=0 Src2_Ready=1 Dst=15 Src1=9 Src2=10 Src1_Tag=13 Src2_Tag=8
Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00233 Type=0 PC=0x00000038 Instr=0x00a4c7b3

[125000] ===== REORDER BUFFER (ROB) =====

[125000] ROB Head: 15, ROB Tail: 3

[125000] ROB[3]: Valid=1 Ready=1 Dest=0 Value=0x00000000 Instr_ID=3 PC=0x0000000c

[125000] ROB[4]: Valid=1 Ready=1 Dest=0 Value=0x00000000 Instr_ID=4 PC=0x00000010

[125000] ROB[5]: Valid=1 Ready=1 Dest=0 Value=0x00000000 Instr_ID=5 PC=0x00000014

[125000] ROB[6]: Valid=1 Ready=0 Dest=0 Value=0x00000000 Instr_ID=6 PC=0x00000018

[125000] ROB[7]: Valid=1 Ready=0 Dest=3 Value=0x00000000 Instr_ID=7 PC=0x0000001c

[125000] ROB[8]: Valid=1 Ready=0 Dest=4 Value=0x00000000 Instr_ID=8 PC=0x00000020

[125000] ROB[9]: Valid=1 Ready=0 Dest=7 Value=0x00000000 Instr_ID=9 PC=0x00000024

[125000] ROB[10]: Valid=1 Ready=0 Dest=8 Value=0x00000000 Instr_ID=10 PC=0x00000028

[125000] ROB[11]: Valid=1 Ready=0 Dest=1 Value=0x00000000 Instr_ID=11 PC=0x0000002c

[125000] ===== RESERVATION STATIONS =====

[125000] --- ALU Reservation Stations ---


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[125000] ALU_RS[0]: Busy=1 Ready=0 ROB_ID=9 Op=0x00033 Src1_Valid=0 Src1_Tag=7 Src1_Value=0x00000000 Src2_Valid=1 Src2_Tag=0
Src2_Value=0x00000001
[125000] ALU_RS[1]: Busy=1 Ready=1 ROB_ID=10 Op=0x00033 Src1_Valid=1 Src1_Tag=0 Src1_Value=0x00000000 Src2_Valid=1 Src2_Tag=1
Src2_Value=0x00000000
[125000] ALU_RS[3]: Busy=1 Ready=0 ROB_ID=8 Op=0x00033 Src1_Valid=1 Src1_Tag=0 Src1_Value=0x00000002 Src2_Valid=0 Src2_Tag=7
Src2_Value=0x00000000
[125000] --- Load/Store Buffer ---
[125000] LSB[3]: Busy=1 Ready=1 ROB_ID=6 Op=0x00123 Src_Valid=1 Src_Tag=0 Src_Value=0x00000000 Store_Data_Valid=1 Store_Data_Tag=0
Store_Data=0x00000003
[125000] LSB[4]: Busy=1 Ready=1 ROB_ID=11 Op=0x00003 Src_Valid=1 Src_Tag=0 Src_Value=0x00000000 Store_Data_Valid=0 Store_Data_Tag=0
Store_Data=0x00000000

[125000] ===== EXECUTION STAGE (CDB INPUT) =====
[125000] CDB[0]: ROB_ID=10 Result=0x00000000 Ready=1

[125000] ===== FORWARDING MESSAGES =====
[125000] FORWARD[INTRA_SRC1]: DISPATCH[0] ROB_ID=12 -> DISPATCH[2] ROB_ID=14 Reg=9
[125000] FORWARD[INTRA_SRC1]: DISPATCH[1] ROB_ID=13 -> DISPATCH[2] ROB_ID=14 Reg=9

[125000] ===== CURRENT RAT AND VALID =====
[125000] RAT[1]: Tag=11 Valid=1
[125000] RAT[3]: Tag=7 Valid=1
[125000] RAT[4]: Tag=8 Valid=1
[125000] RAT[7]: Tag=9 Valid=1
[125000] RAT[8]: Tag=10 Valid=1
[125000] RAT[9]: Tag=13 Valid=1
[125000] RAT[15]: Tag=14 Valid=1

[125000] ===== ARCHITECTURAL REGISTER FILE (ARF) =====
[125000] ARF[1]: Value=0x00000001
[125000] ARF[2]: Value=0x00000002
[125000] ARF[3]: Value=0x00000003
[125000] [MMU] LOAD ISSUED: LQ[0] ROB_ID=11 Addr=0x00000004 Size=0
[125000] [MMU] STORE ISSUED: SQ[1] ROB_ID=4 Addr=0x00000008 Data=0x00000002 Size=2
[125000] [MMU] LOAD ISSUED: LQ[0] ROB_ID=11 Addr=0x00000004 Size=0
[125000] [MMU] STORE ISSUED: SQ[1] ROB_ID=4 Addr=0x00000008 Data=0x00000002 Size=2
[135000] [MMU] LOAD ENQUEUED: LSB[5] ROB_ID=12 Op=0x00203 Addr=0x00000008 Size=2
[135000] [MMU] LOAD ENQUEUED: LSB[6] ROB_ID=13 Op=0x00103 Addr=0x0000000c Size=2

[135000] ===== DECODE/DISPATCH STAGE =====
[135000] DECODE[0]: PC=0x00000048 Instr=0x0014d6b3 Type=0 Dst=13 Src1=9 Src2=1 Opcode=0x33 Func3=0x5 Func7=0x00 Operation=0x002b3
Imm=0x00000000
[135000] DECODE[1]: PC=0x0000004c Instr=0x40b60533 Type=0 Dst=10 Src1=12 Src2=11 Opcode=0x33 Func3=0x0 Func7=0x20 Operation=0x08033
Imm=0x00000000
[135000] DECODE[2]: PC=0x00000050 Instr=0x013976b3 Type=0 Dst=13 Src1=18 Src2=19 Opcode=0x33 Func3=0x7 Func7=0x00
Operation=0x003b3 Imm=0x00000000
[135000] DISPATCH[0]: ROB_ID=15 RS_ID=4 RS_Alloc=1 Src1_Ready=1 Src2_Ready=1 Dst=10 Src1=10 Src2=11 Src1_Tag=0 Src2_Tag=10
Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00033 Type=0 PC=0x0000003c Instr=0x00b50533
[135000] DISPATCH[1]: ROB_ID=16 RS_ID=5 RS_Alloc=1 Src1_Ready=0 Src2_Ready=0 Dst=11 Src1=10 Src2=9 Src1_Tag=15 Src2_Tag=13
Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00233 Type=0 PC=0x00000040 Instr=0x009545b3
[135000] DISPATCH[2]: ROB_ID=17 RS_ID=6 RS_Alloc=1 Src1_Ready=0 Src2_Ready=0 Dst=12 Src1=9 Src2=1 Src1_Tag=13 Src2_Tag=11
Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x000b3 Type=0 PC=0x00000044 Instr=0x00149633

[135000] ===== REORDER BUFFER (ROB) =====
[135000] ROB Head: 18, ROB Tail: 6
[135000] ROB[6]: Valid=1 Ready=1 Dest=0 Value=0x00000000 Instr_ID=6 PC=0x00000018
[135000] ROB[7]: Valid=1 Ready=0 Dest=3 Value=0x00000000 Instr_ID=7 PC=0x0000001c
[135000] ROB[8]: Valid=1 Ready=0 Dest=4 Value=0x00000000 Instr_ID=8 PC=0x00000020
[135000] ROB[9]: Valid=1 Ready=0 Dest=7 Value=0x00000000 Instr_ID=9 PC=0x00000024
[135000] ROB[10]: Valid=1 Ready=1 Dest=8 Value=0x00000000 Instr_ID=10 PC=0x00000028
[135000] ROB[11]: Valid=1 Ready=0 Dest=1 Value=0x00000000 Instr_ID=11 PC=0x0000002c
[135000] ROB[12]: Valid=1 Ready=0 Dest=9 Value=0x00000000 Instr_ID=12 PC=0x00000030
[135000] ROB[13]: Valid=1 Ready=0 Dest=9 Value=0x00000000 Instr_ID=13 PC=0x00000034
[135000] ROB[14]: Valid=1 Ready=0 Dest=15 Value=0x00000000 Instr_ID=14 PC=0x00000038

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[135000] ===== RESERVATION STATIONS =====
[135000] --- ALU Reservation Stations ---
[135000] ALU_RS[0]: Busy=1 Ready=0 ROB_ID=9 Op=0x00033 Src1_Valid=0 Src1_Tag=7 Src1_Value=0x00000000 Src2_Valid=1 Src2_Tag=0
Src2_Value=0x00000001
[135000] ALU_RS[2]: Busy=1 Ready=0 ROB_ID=14 Op=0x00233 Src1_Valid=0 Src1_Tag=13 Src1_Value=0x00000000 Src2_Valid=1 Src2_Tag=8
Src2_Value=0x00000000
[135000] ALU_RS[3]: Busy=1 Ready=0 ROB_ID=8 Op=0x00033 Src1_Valid=1 Src1_Tag=0 Src1_Value=0x00000002 Src2_Valid=0 Src2_Tag=7
Src2_Value=0x00000000
[135000] --- Load/Store Buffer ---
[135000] LSB[5]: Busy=1 Ready=1 ROB_ID=12 Op=0x00203 Src_Valid=1 Src_Tag=0 Src_Value=0x00000000 Store_Data_Valid=0 Store_Data_Tag=0
Store_Data=0x00000000
[135000] LSB[6]: Busy=1 Ready=1 ROB_ID=13 Op=0x00103 Src_Valid=1 Src_Tag=0 Src_Value=0x00000000 Store_Data_Valid=0 Store_Data_Tag=0
Store_Data=0x00000000

[135000] ===== EXECUTION STAGE (CDB INPUT) =====
[135000] CDB[0]: ROB_ID=11 Result=0x00000001 Ready=1

[135000] ===== FORWARDING MESSAGES =====
[135000] FORWARD[INTRA_SRC1]: DISPATCH[0] ROB_ID=15 -> DISPATCH[1] ROB_ID=16 Reg=10

[135000] ===== INSTRUCTIONS COMMITTED THIS CYCLE =====
[135000] COMMITTED[0]: ROB_ID=3
[135000] COMMITTED[1]: ROB_ID=4
[135000] COMMITTED[2]: ROB_ID=5
[135000] Total Instructions Committed This Cycle: 3

[135000] ===== CURRENT RAT AND VALID =====
[135000] RAT[1]: Tag=11 Valid=1
[135000] RAT[3]: Tag=7 Valid=1
[135000] RAT[4]: Tag=8 Valid=1
[135000] RAT[7]: Tag=9 Valid=1
[135000] RAT[8]: Tag=10 Valid=1
[135000] RAT[9]: Tag=13 Valid=1
[135000] RAT[10]: Tag=15 Valid=1
[135000] RAT[11]: Tag=16 Valid=1
[135000] RAT[12]: Tag=17 Valid=1
[135000] RAT[15]: Tag=14 Valid=1

[135000] ===== ARCHITECTURAL REGISTER FILE (ARF) =====
[135000] ARF[1]: Value=0x00000001
[135000] ARF[2]: Value=0x00000002
[135000] ARF[3]: Value=0x00000003
[135000] ARF Checker: PASS - ROB[3] sw x1, 4(x0) -> x0 = 0
[135000] ARF Checker: PASS - ROB[4] sw x2, 8(x0) -> x0 = 0
[135000] ARF Checker: PASS - ROB[5] sw x3, 12(x0) -> x0 = 0
[135000] [MMU] LOAD FORWARDED: LQ[1] ROB_ID=12 Addr=0x00000008 Size=2 Data=0x00000002 from Store ROB_ID=4
[135000] [MMU] LOAD FORWARDED: LQ[2] ROB_ID=13 Addr=0x0000000c Size=2 Data=0x00000003 from Store ROB_ID=5
[135000] [MMU] STORE ISSUED: SQ[2] ROB_ID=5 Addr=0x0000000c Data=0x00000003 Size=2
[135000] [MMU] LOAD FORWARDED: LQ[1] ROB_ID=12 Addr=0x00000008 Size=2 Data=0x00000002 from Store ROB_ID=4
[135000] [MMU] LOAD FORWARDED: LQ[2] ROB_ID=13 Addr=0x0000000c Size=2 Data=0x00000003 from Store ROB_ID=5
[135000] [MMU] STORE ISSUED: SQ[2] ROB_ID=5 Addr=0x0000000c Data=0x00000003 Size=2

[145000] ===== DECODE/DISPATCH STAGE =====
[145000] DECODE[0]: PC=0x00000054 Instr=0x00c52733 Type=0 Dst=14 Src1=10 Src2=12 Opcode=0x33 Func3=0x2 Func7=0x00 Operation=0x00133
Imm=0x00000000
[145000] DECODE[1]: PC=0x00000058 Instr=0x00a485b3 Type=0 Dst=11 Src1=9 Src2=10 Opcode=0x33 Func3=0x0 Func7=0x00 Operation=0x00033
Imm=0x00000000
[145000] DECODE[2]: PC=0x0000005c Instr=0x02114333 Type=2 Dst=6 Src1=2 Src2=1 Opcode=0x33 Func3=0x4 Func7=0x01 Operation=0x00633
Imm=0x00000000
[145000] DISPATCH[0]: ROB_ID=18 RS_ID=1 RS_Alloc=1 Src1_Ready=0 Src2_Ready=1 Dst=13 Src1=9 Src2=1 Src1_Tag=13 Src2_Tag=11
Src1_Value=0x00000000 Src2_Value=0x00000001 Operation=0x002b3 Type=0 PC=0x00000048 Instr=0x0014d6b3
[145000] DISPATCH[1]: ROB_ID=19 RS_ID=7 RS_Alloc=1 Src1_Ready=0 Src2_Ready=0 Dst=10 Src1=12 Src2=11 Src1_Tag=17 Src2_Tag=16
Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x08033 Type=0 PC=0x0000004c Instr=0x40b60533
[145000] DISPATCH[2]: ROB_ID=20 RS_ID=8 RS_Alloc=1 Src1_Ready=1 Src2_Ready=1 Dst=13 Src1=18 Src2=19 Src1_Tag=13 Src2_Tag=11
Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x003b3 Type=0 PC=0x00000050 Instr=0x013976b3

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[145000] ===== REORDER BUFFER (ROB) =====

[145000] ROB Head: 21, ROB Tail: 7

[145000] ROB[7]: Valid=1 Ready=0 Dest=3 Value=0x00000000 Instr_ID=7 PC=0x0000001c

[145000] ROB[8]: Valid=1 Ready=0 Dest=4 Value=0x00000000 Instr_ID=8 PC=0x00000020

[145000] ROB[9]: Valid=1 Ready=0 Dest=7 Value=0x00000000 Instr_ID=9 PC=0x00000024

[145000] ROB[10]: Valid=1 Ready=1 Dest=8 Value=0x00000000 Instr_ID=10 PC=0x00000028

[145000] ROB[11]: Valid=1 Ready=1 Dest=1 Value=0x00000001 Instr_ID=11 PC=0x0000002c

[145000] ROB[12]: Valid=1 Ready=0 Dest=9 Value=0x00000000 Instr_ID=12 PC=0x00000030

[145000] ROB[13]: Valid=1 Ready=0 Dest=9 Value=0x00000000 Instr_ID=13 PC=0x00000034

[145000] ROB[14]: Valid=1 Ready=0 Dest=15 Value=0x00000000 Instr_ID=14 PC=0x00000038

[145000] ROB[15]: Valid=1 Ready=0 Dest=10 Value=0x00000000 Instr_ID=15 PC=0x0000003c

[145000] ROB[16]: Valid=1 Ready=0 Dest=11 Value=0x00000000 Instr_ID=16 PC=0x00000040

[145000] ROB[17]: Valid=1 Ready=0 Dest=12 Value=0x00000000 Instr_ID=17 PC=0x00000044

[145000] ===== RESERVATION STATIONS =====

[145000] --- ALU Reservation Stations ---

[145000] ALU_RS[0]: Busy=1 Ready=0 ROB_ID=9 Op=0x00033 Src1_Valid=0 Src1_Tag=7 Src1_Value=0x00000000 Src2_Valid=1 Src2_Tag=0 Src2_Value=0x00000001

[145000] ALU_RS[2]: Busy=1 Ready=0 ROB_ID=14 Op=0x00233 Src1_Valid=0 Src1_Tag=13 Src1_Value=0x00000000 Src2_Valid=1 Src2_Tag=8 Src2_Value=0x00000000

[145000] ALU_RS[3]: Busy=1 Ready=0 ROB_ID=8 Op=0x00033 Src1_Valid=1 Src1_Tag=0 Src1_Value=0x00000002 Src2_Valid=0 Src2_Tag=7 Src2_Value=0x00000000

[145000] ALU_RS[4]: Busy=1 Ready=1 ROB_ID=15 Op=0x00033 Src1_Valid=1 Src1_Tag=0 Src1_Value=0x00000000 Src2_Valid=1 Src2_Tag=10 Src2_Value=0x00000000

[145000] ALU_RS[5]: Busy=1 Ready=0 ROB_ID=16 Op=0x00233 Src1_Valid=0 Src1_Tag=15 Src1_Value=0x00000000 Src2_Valid=0 Src2_Tag=13 Src2_Value=0x00000000

[145000] ALU_RS[6]: Busy=1 Ready=0 ROB_ID=17 Op=0x000b3 Src1_Valid=0 Src1_Tag=13 Src1_Value=0x00000000 Src2_Valid=0 Src2_Tag=11 Src2_Value=0x00000000

[145000] ===== FORWARDING MESSAGES =====

[145000] FORWARD[CDB_DELAYED->ALU_SRC2]: CDB_DELAYED[0] ROB_ID=11 -> ALU_RS[6] ROB_ID=17 Value=0x00000001

[145000] ===== INSTRUCTIONS COMMITTED THIS CYCLE =====

[145000] COMMITTED[0]: ROB_ID=6

[145000] Total Instructions Committed This Cycle: 1

[145000] ===== CURRENT RAT AND VALID =====

[145000] RAT[1]: Tag=11 Valid=1

[145000] RAT[3]: Tag=7 Valid=1

[145000] RAT[4]: Tag=8 Valid=1

[145000] RAT[7]: Tag=9 Valid=1

[145000] RAT[8]: Tag=10 Valid=1

[145000] RAT[9]: Tag=13 Valid=1

[145000] RAT[10]: Tag=19 Valid=1

[145000] RAT[11]: Tag=16 Valid=1

[145000] RAT[12]: Tag=17 Valid=1

[145000] RAT[13]: Tag=20 Valid=1

[145000] RAT[15]: Tag=14 Valid=1

[145000] ===== ARCHITECTURAL REGISTER FILE (ARF) =====

[145000] ARF[1]: Value=0x00000001

[145000] ARF[2]: Value=0x00000002

[145000] ARF[3]: Value=0x00000003

[145000] ARF Checker: PASS - ROB[6] sw x3, 16(x0) -> x0 = 0

[145000] [MMU] STORE ISSUED: SQ[3] ROB_ID=6 Addr=0x00000010 Data=0x00000003 Size=2

[155000] ===== DECODE/DISPATCH STAGE =====

[155000] DECODE[0]: PC=0x00000060 Instr=0x01000903 Type=1 Dst=18 Src1=0 Src2=16 Opcode=0x03 Func3=0x0 Func7=0x00 Operation=0x00003 Imm=0x00000010

[155000] DECODE[1]: PC=0x00000064 Instr=0x01400983 Type=1 Dst=19 Src1=0 Src2=20 Opcode=0x03 Func3=0x0 Func7=0x00 Operation=0x00003 Imm=0x00000014

[155000] DECODE[2]: PC=0x00000068 Instr=0x0199aa23 Type=1 Dst=0 Src1=19 Src2=25 Opcode=0x23 Func3=0x2 Func7=0x00 Operation=0x00123 Imm=0x00000014

[155000] DISPATCH[0]: ROB_ID=21 RS_ID=9 RS_Alloc=1 Src1_Ready=0 Src2_Ready=0 Dst=14 Src1=10 Src2=12 Src1_Tag=19 Src2_Tag=17 Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00133 Type=0 PC=0x00000054 Instr=0x00c52733
[155000] DISPATCH[1]: ROB_ID=22 RS_ID=10 RS_Alloc=1 Src1_Ready=0 Src2_Ready=0 Dst=11 Src1=9 Src2=10 Src1_Tag=13 Src2_Tag=19 Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00033 Type=0 PC=0x00000058 Instr=0x00a485b3
[155000] DISPATCH[2]: ROB_ID=23 RS_ID=0 RS_Alloc=1 Src1_Ready=1 Src2_Ready=1 Dst=6 Src1=2 Src2=1 Src1_Tag=13 Src2_Tag=11 Src1_Value=0x00000002 Src2_Value=0x00000001 Operation=0x00633 Type=2 PC=0x0000005c Instr=0x02114333

[155000] ===== REORDER BUFFER (ROB) =====

[155000] ROB Head: 24, ROB Tail: 7
[155000] ROB[7]: Valid=1 Ready=0 Dest=3 Value=0x00000000 Instr_ID=7 PC=0x0000001c
[155000] ROB[8]: Valid=1 Ready=0 Dest=4 Value=0x00000000 Instr_ID=8 PC=0x00000020
[155000] ROB[9]: Valid=1 Ready=0 Dest=7 Value=0x00000000 Instr_ID=9 PC=0x00000024
[155000] ROB[10]: Valid=1 Ready=1 Dest=8 Value=0x00000000 Instr_ID=10 PC=0x00000028
[155000] ROB[11]: Valid=1 Ready=1 Dest=1 Value=0x00000001 Instr_ID=11 PC=0x0000002c
[155000] ROB[12]: Valid=1 Ready=0 Dest=9 Value=0x00000000 Instr_ID=12 PC=0x00000030
[155000] ROB[13]: Valid=1 Ready=0 Dest=9 Value=0x00000000 Instr_ID=13 PC=0x00000034
[155000] ROB[14]: Valid=1 Ready=0 Dest=15 Value=0x00000000 Instr_ID=14 PC=0x00000038
[155000] ROB[15]: Valid=1 Ready=0 Dest=10 Value=0x00000000 Instr_ID=15 PC=0x0000003c
[155000] ROB[16]: Valid=1 Ready=0 Dest=11 Value=0x00000000 Instr_ID=16 PC=0x00000040
[155000] ROB[17]: Valid=1 Ready=0 Dest=12 Value=0x00000000 Instr_ID=17 PC=0x00000044
[155000] ROB[18]: Valid=1 Ready=0 Dest=13 Value=0x00000000 Instr_ID=18 PC=0x00000048
[155000] ROB[19]: Valid=1 Ready=0 Dest=10 Value=0x00000000 Instr_ID=19 PC=0x0000004c
[155000] ROB[20]: Valid=1 Ready=0 Dest=13 Value=0x00000000 Instr_ID=20 PC=0x00000050

[155000] ===== RESERVATION STATIONS =====

[155000] --- ALU Reservation Stations ---
[155000] ALU_RS[0]: Busy=1 Ready=0 ROB_ID=9 Op=0x00033 Src1_Valid=0 Src1_Tag=7 Src1_Value=0x00000000 Src2_Valid=1 Src2_Tag=0 Src2_Value=0x00000001
[155000] ALU_RS[1]: Busy=1 Ready=0 ROB_ID=18 Op=0x002b3 Src1_Valid=0 Src1_Tag=13 Src1_Value=0x00000000 Src2_Valid=1 Src2_Tag=11 Src2_Value=0x00000001
[155000] ALU_RS[2]: Busy=1 Ready=0 ROB_ID=14 Op=0x00233 Src1_Valid=0 Src1_Tag=13 Src1_Value=0x00000000 Src2_Valid=1 Src2_Tag=8 Src2_Value=0x00000000
[155000] ALU_RS[3]: Busy=1 Ready=0 ROB_ID=8 Op=0x00033 Src1_Valid=1 Src1_Tag=0 Src1_Value=0x00000002 Src2_Valid=0 Src2_Tag=7 Src2_Value=0x00000000
[155000] ALU_RS[5]: Busy=1 Ready=0 ROB_ID=16 Op=0x00233 Src1_Valid=0 Src1_Tag=15 Src1_Value=0x00000000 Src2_Valid=0 Src2_Tag=13 Src2_Value=0x00000000
[155000] ALU_RS[6]: Busy=1 Ready=0 ROB_ID=17 Op=0x000b3 Src1_Valid=0 Src1_Tag=13 Src1_Value=0x00000000 Src2_Valid=1 Src2_Tag=11 Src2_Value=0x00000001
[155000] ALU_RS[7]: Busy=1 Ready=0 ROB_ID=19 Op=0x08033 Src1_Valid=0 Src1_Tag=17 Src1_Value=0x00000000 Src2_Valid=0 Src2_Tag=16 Src2_Value=0x00000000
[155000] ALU_RS[8]: Busy=1 Ready=1 ROB_ID=20 Op=0x003b3 Src1_Valid=1 Src1_Tag=13 Src1_Value=0x00000000 Src2_Valid=1 Src2_Tag=11 Src2_Value=0x00000000

[155000] ===== EXECUTION STAGE (CDB INPUT) =====

[155000] CDB[0]: ROB_ID=15 Result=0x00000000 Ready=1
[155000] CDB[1]: ROB_ID=7 Result=0x00000002 Ready=1
[155000] CDB[2]: ROB_ID=12 Result=0x00000002 Ready=1

[155000] ===== FORWARDING MESSAGES =====

[155000] FORWARD[CDB_CURR->ALU_SRC1]: CDB[0] ROB_ID=15 -> ALU_RS[5] ROB_ID=16 Value=0x00000000
[155000] FORWARD[CDB_CURR->ALU_SRC1]: CDB[1] ROB_ID=7 -> ALU_RS[0] ROB_ID=9 Value=0x00000002
[155000] FORWARD[CDB_CURR->ALU_SRC2]: CDB[1] ROB_ID=7 -> ALU_RS[3] ROB_ID=8 Value=0x00000002
[155000] FORWARD[RETIRE_CURR->ALU_SRC1]: RETIRE_CURR[0] ROB_ID=7 -> ALU_RS[0] ROB_ID=9 Value=0x00000002
[155000] FORWARD[RETIRE_CURR->ALU_SRC2]: RETIRE_CURR[0] ROB_ID=7 -> ALU_RS[3] ROB_ID=8 Value=0x00000002

[155000] ===== CURRENT RAT AND VALID =====

[155000] RAT[1]: Tag=11 Valid=1
[155000] RAT[3]: Tag=7 Valid=1
[155000] RAT[4]: Tag=8 Valid=1
[155000] RAT[6]: Tag=23 Valid=1
[155000] RAT[7]: Tag=9 Valid=1
[155000] RAT[8]: Tag=10 Valid=1
[155000] RAT[9]: Tag=13 Valid=1
[155000] RAT[10]: Tag=19 Valid=1
[155000] RAT[11]: Tag=22 Valid=1

[155000] RAT[12]: Tag=17 Valid=1
[155000] RAT[13]: Tag=20 Valid=1
[155000] RAT[14]: Tag=21 Valid=1
[155000] RAT[15]: Tag=14 Valid=1

[155000] ===== ARCHITECTURAL REGISTER FILE (ARF) =====

[155000] ARF[1]: Value=0x00000001
[155000] ARF[2]: Value=0x00000002
[155000] ARF[3]: Value=0x00000003

[165000] ===== DECODE/DISPATCH STAGE =====

[165000] DECODE[0]: PC=0x0000006c Instr=0x00a480b3 Type=0 Dst=1 Src1=9 Src2=10 Opcode=0x33 Func3=0x0 Func7=0x00 Operation=0x00033 Imm=0x00000000
[165000] DECODE[1]: PC=0x00000070 Instr=0x00b48133 Type=0 Dst=2 Src1=9 Src2=11 Opcode=0x33 Func3=0x0 Func7=0x00 Operation=0x00033 Imm=0x00000000
[165000] DECODE[2]: PC=0x00000074 Instr=0x002081b3 Type=0 Dst=3 Src1=1 Src2=2 Opcode=0x33 Func3=0x0 Func7=0x00 Operation=0x00033 Imm=0x00000000
[165000] DISPATCH[0]: ROB_ID=24 RS_ID=0 RS_Alloc=1 Src1_Ready=1 Src2_Ready=1 Dst=18 Src1=0 Src2=16 Src1_Tag=0 Src2_Tag=17 Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00003 Type=1 PC=0x00000060 Instr=0x01000903
[165000] DISPATCH[1]: ROB_ID=25 RS_ID=1 RS_Alloc=1 Src1_Ready=1 Src2_Ready=1 Dst=19 Src1=0 Src2=20 Src1_Tag=0 Src2_Tag=19 Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00003 Type=1 PC=0x00000064 Instr=0x01400983
[165000] DISPATCH[2]: ROB_ID=26 RS_ID=2 RS_Alloc=1 Src1_Ready=0 Src2_Ready=1 Dst=0 Src1=19 Src2=25 Src1_Tag=25 Src2_Tag=11 Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00123 Type=1 PC=0x00000068 Instr=0x0199aa23

[165000] ===== REORDER BUFFER (ROB) =====

[165000] ROB Head: 27, ROB Tail: 8
[165000] ROB[8]: Valid=1 Ready=0 Dest=4 Value=0x00000000 Instr_ID=8 PC=0x00000020
[165000] ROB[9]: Valid=1 Ready=0 Dest=7 Value=0x00000000 Instr_ID=9 PC=0x00000024
[165000] ROB[10]: Valid=1 Ready=1 Dest=8 Value=0x00000000 Instr_ID=10 PC=0x00000028
[165000] ROB[11]: Valid=1 Ready=1 Dest=1 Value=0x00000001 Instr_ID=11 PC=0x0000002c
[165000] ROB[12]: Valid=1 Ready=1 Dest=9 Value=0x00000002 Instr_ID=12 PC=0x00000030
[165000] ROB[13]: Valid=1 Ready=0 Dest=9 Value=0x00000000 Instr_ID=13 PC=0x00000034
[165000] ROB[14]: Valid=1 Ready=0 Dest=15 Value=0x00000000 Instr_ID=14 PC=0x00000038
[165000] ROB[15]: Valid=1 Ready=1 Dest=10 Value=0x00000000 Instr_ID=15 PC=0x0000003c
[165000] ROB[16]: Valid=1 Ready=0 Dest=11 Value=0x00000000 Instr_ID=16 PC=0x00000040
[165000] ROB[17]: Valid=1 Ready=0 Dest=12 Value=0x00000000 Instr_ID=17 PC=0x00000044
[165000] ROB[18]: Valid=1 Ready=0 Dest=13 Value=0x00000000 Instr_ID=18 PC=0x00000048
[165000] ROB[19]: Valid=1 Ready=0 Dest=10 Value=0x00000000 Instr_ID=19 PC=0x0000004c
[165000] ROB[20]: Valid=1 Ready=0 Dest=13 Value=0x00000000 Instr_ID=20 PC=0x00000050
[165000] ROB[21]: Valid=1 Ready=0 Dest=14 Value=0x00000000 Instr_ID=21 PC=0x00000054
[165000] ROB[22]: Valid=1 Ready=0 Dest=11 Value=0x00000000 Instr_ID=22 PC=0x00000058
[165000] ROB[23]: Valid=1 Ready=0 Dest=6 Value=0x00000000 Instr_ID=23 PC=0x0000005c

[165000] ===== RESERVATION STATIONS =====

[165000] --- ALU Reservation Stations ---
[165000] ALU_RS[0]: Busy=1 Ready=0 ROB_ID=9 Op=0x00033 Src1_Valid=1 Src1_Tag=7 Src1_Value=0x00000002 Src2_Valid=1 Src2_Tag=0 Src2_Value=0x00000001
[165000] ALU_RS[1]: Busy=1 Ready=0 ROB_ID=18 Op=0x002b3 Src1_Valid=0 Src1_Tag=13 Src1_Value=0x00000000 Src2_Valid=1 Src2_Tag=11 Src2_Value=0x00000001
[165000] ALU_RS[2]: Busy=1 Ready=0 ROB_ID=14 Op=0x00233 Src1_Valid=0 Src1_Tag=13 Src1_Value=0x00000000 Src2_Valid=1 Src2_Tag=8 Src2_Value=0x00000000
[165000] ALU_RS[3]: Busy=1 Ready=0 ROB_ID=8 Op=0x00033 Src1_Valid=1 Src1_Tag=0 Src1_Value=0x00000002 Src2_Valid=1 Src2_Tag=7 Src2_Value=0x00000002
[165000] ALU_RS[5]: Busy=1 Ready=0 ROB_ID=16 Op=0x00233 Src1_Valid=1 Src1_Tag=15 Src1_Value=0x00000000 Src2_Valid=0 Src2_Tag=13 Src2_Value=0x00000000
[165000] ALU_RS[6]: Busy=1 Ready=0 ROB_ID=17 Op=0x000b3 Src1_Valid=0 Src1_Tag=13 Src1_Value=0x00000000 Src2_Valid=1 Src2_Tag=11 Src2_Value=0x00000001
[165000] ALU_RS[7]: Busy=1 Ready=0 ROB_ID=19 Op=0x08033 Src1_Valid=0 Src1_Tag=17 Src1_Value=0x00000000 Src2_Valid=0 Src2_Tag=16 Src2_Value=0x00000000
[165000] ALU_RS[9]: Busy=1 Ready=0 ROB_ID=21 Op=0x00133 Src1_Valid=0 Src1_Tag=19 Src1_Value=0x00000000 Src2_Valid=0 Src2_Tag=17 Src2_Value=0x00000000
[165000] ALU_RS[10]: Busy=1 Ready=0 ROB_ID=22 Op=0x00033 Src1_Valid=0 Src1_Tag=13 Src1_Value=0x00000000 Src2_Valid=0 Src2_Tag=19 Src2_Value=0x00000000
[165000] --- Mul/Div Reservation Stations ---

[165000] MD_RS[0]: Busy=1 Ready=1 ROB_ID=23 Op=0x00633 Src1_Valid=1 Src1_Tag=13 Src1_Value=0x00000002 Src2_Valid=1 Src2_Tag=11 Src2_Value=0x00000001

[165000] ===== EXECUTION STAGE (CDB INPUT) =====

[165000] CDB[0]: ROB_ID=13 Result=0x00000003 Ready=1

[165000] CDB[1]: ROB_ID=20 Result=0x00000000 Ready=1

[165000] ===== FORWARDING MESSAGES =====

[165000] FORWARD[CDB_CURR->ALU_SRC1]: CDB[0] ROB_ID=13 -> ALU_RS[1] ROB_ID=18 Value=0x00000003

[165000] FORWARD[CDB_CURR->ALU_SRC1]: CDB[0] ROB_ID=13 -> ALU_RS[2] ROB_ID=14 Value=0x00000003

[165000] FORWARD[CDB_CURR->ALU_SRC2]: CDB[0] ROB_ID=13 -> ALU_RS[5] ROB_ID=16 Value=0x00000003

[165000] FORWARD[CDB_CURR->ALU_SRC1]: CDB[0] ROB_ID=13 -> ALU_RS[6] ROB_ID=17 Value=0x00000003

[165000] FORWARD[CDB_CURR->ALU_SRC1]: CDB[0] ROB_ID=13 -> ALU_RS[10] ROB_ID=22 Value=0x00000003

[165000] FORWARD[INTRA_SRC1]: DISPATCH[1] ROB_ID=25 -> DISPATCH[2] ROB_ID=26 Reg=19

[165000] ===== INSTRUCTIONS COMMITTED THIS CYCLE =====

[165000] COMMITTED[0]: ROB_ID=7

[165000] Total Instructions Committed This Cycle: 1

[165000] ===== CURRENT RAT AND VALID =====

[165000] RAT[1]: Tag=11 Valid=1

[165000] RAT[4]: Tag=8 Valid=1

[165000] RAT[6]: Tag=23 Valid=1

[165000] RAT[7]: Tag=9 Valid=1

[165000] RAT[8]: Tag=10 Valid=1

[165000] RAT[9]: Tag=13 Valid=1

[165000] RAT[10]: Tag=19 Valid=1

[165000] RAT[11]: Tag=22 Valid=1

[165000] RAT[12]: Tag=17 Valid=1

[165000] RAT[13]: Tag=20 Valid=1

[165000] RAT[14]: Tag=21 Valid=1

[165000] RAT[15]: Tag=14 Valid=1

[165000] RAT[18]: Tag=24 Valid=1

[165000] RAT[19]: Tag=25 Valid=1

[165000] ===== ARCHITECTURAL REGISTER FILE (ARF) =====

[165000] ARF[1]: Value=0x00000001

[165000] ARF[2]: Value=0x00000002

[165000] ARF[3]: Value=0x00000002

[165000] ARF Checker: PASS - ROB[7] mul x3, x1, x2 -> x3 = 2

[175000] [MMU] LOAD ENQUEUED: LSB[0] ROB_ID=24 Op=0x00003 Addr=0x00000010 Size=0

[175000] [MMU] LOAD ENQUEUED: LSB[1] ROB_ID=25 Op=0x00003 Addr=0x00000014 Size=0

[175000] ===== DECODE/DISPATCH STAGE =====

[175000] DECODE[0]: PC=0x0000006c Instr=0x00a480b3 Type=0 Dst=1 Src1=9 Src2=10 Opcode=0x33 Func3=0x0 Func7=0x00 Operation=0x00033 Imm=0x00000000

[175000] DECODE[1]: PC=0x00000070 Instr=0x00b48133 Type=0 Dst=2 Src1=9 Src2=11 Opcode=0x33 Func3=0x0 Func7=0x00 Operation=0x00033 Imm=0x00000000

[175000] DECODE[2]: PC=0x00000074 Instr=0x002081b3 Type=0 Dst=3 Src1=1 Src2=2 Opcode=0x33 Func3=0x0 Func7=0x00 Operation=0x00033 Imm=0x00000000

[175000] DISPATCH[0]: ROB_ID=24 RS_ID=0 RS_Alloc=1 Src1_Ready=1 Src2_Ready=1 Dst=18 Src1=0 Src2=16 Src1_Tag=0 Src2_Tag=17 Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00003 Type=1 PC=0x00000060 Instr=0x01000903

[175000] DISPATCH[1]: ROB_ID=25 RS_ID=1 RS_Alloc=1 Src1_Ready=1 Src2_Ready=1 Dst=19 Src1=0 Src2=20 Src1_Tag=0 Src2_Tag=19 Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00003 Type=1 PC=0x00000064 Instr=0x01400983

[175000] DISPATCH[2]: ROB_ID=26 RS_ID=2 RS_Alloc=1 Src1_Ready=0 Src2_Ready=1 Dst=0 Src1=19 Src2=25 Src1_Tag=25 Src2_Tag=11 Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00123 Type=1 PC=0x00000068 Instr=0x0199aa23

[175000] ===== REORDER BUFFER (ROB) =====

[175000] ROB Head: 27, ROB Tail: 8

[175000] ROB[8]: Valid=1 Ready=0 Dest=4 Value=0x00000000 Instr_ID=8 PC=0x00000020

[175000] ROB[9]: Valid=1 Ready=0 Dest=7 Value=0x00000000 Instr_ID=9 PC=0x00000024

[175000] ROB[10]: Valid=1 Ready=1 Dest=8 Value=0x00000000 Instr_ID=10 PC=0x00000028

[175000] ROB[11]: Valid=1 Ready=1 Dest=1 Value=0x00000001 Instr_ID=11 PC=0x0000002c

[175000] ROB[12]: Valid=1 Ready=1 Dest=9 Value=0x00000002 Instr_ID=12 PC=0x00000030

[175000] ROB[13]: Valid=1 Ready=1 Dest=9 Value=0x00000003 Instr_ID=13 PC=0x00000034

[175000] ROB[14]: Valid=1 Ready=0 Dest=15 Value=0x00000000 Instr_ID=14 PC=0x00000038
[175000] ROB[15]: Valid=1 Ready=1 Dest=10 Value=0x00000000 Instr_ID=15 PC=0x0000003c
[175000] ROB[16]: Valid=1 Ready=0 Dest=11 Value=0x00000000 Instr_ID=16 PC=0x00000040
[175000] ROB[17]: Valid=1 Ready=0 Dest=12 Value=0x00000000 Instr_ID=17 PC=0x00000044
[175000] ROB[18]: Valid=1 Ready=0 Dest=13 Value=0x00000000 Instr_ID=18 PC=0x00000048
[175000] ROB[19]: Valid=1 Ready=0 Dest=10 Value=0x00000000 Instr_ID=19 PC=0x0000004c
[175000] ROB[20]: Valid=1 Ready=1 Dest=13 Value=0x00000000 Instr_ID=20 PC=0x00000050
[175000] ROB[21]: Valid=1 Ready=0 Dest=14 Value=0x00000000 Instr_ID=21 PC=0x00000054
[175000] ROB[22]: Valid=1 Ready=0 Dest=11 Value=0x00000000 Instr_ID=22 PC=0x00000058
[175000] ROB[23]: Valid=1 Ready=0 Dest=6 Value=0x00000000 Instr_ID=23 PC=0x0000005c
[175000] ROB[24]: Valid=1 Ready=0 Dest=18 Value=0x00000000 Instr_ID=24 PC=0x00000060
[175000] ROB[25]: Valid=1 Ready=0 Dest=19 Value=0x00000000 Instr_ID=25 PC=0x00000064
[175000] ROB[26]: Valid=1 Ready=0 Dest=0 Value=0x00000000 Instr_ID=26 PC=0x00000068

[175000] ===== RESERVATION STATIONS =====

[175000] --- ALU Reservation Stations ---

[175000] ALU_RS[0]: Busy=1 Ready=1 ROB_ID=9 Op=0x00033 Src1_Valid=1 Src1_Tag=7 Src1_Value=0x00000002 Src2_Valid=1 Src2_Tag=0
Src2_Value=0x00000001
[175000] ALU_RS[1]: Busy=1 Ready=0 ROB_ID=18 Op=0x002b3 Src1_Valid=1 Src1_Tag=13 Src1_Value=0x00000003 Src2_Valid=1 Src2_Tag=11
Src2_Value=0x00000001
[175000] ALU_RS[2]: Busy=1 Ready=0 ROB_ID=14 Op=0x00233 Src1_Valid=1 Src1_Tag=13 Src1_Value=0x00000003 Src2_Valid=1 Src2_Tag=8
Src2_Value=0x00000000
[175000] ALU_RS[3]: Busy=1 Ready=1 ROB_ID=8 Op=0x00033 Src1_Valid=1 Src1_Tag=0 Src1_Value=0x00000002 Src2_Valid=1 Src2_Tag=7
Src2_Value=0x00000002
[175000] ALU_RS[5]: Busy=1 Ready=0 ROB_ID=16 Op=0x00233 Src1_Valid=1 Src1_Tag=15 Src1_Value=0x00000000 Src2_Valid=1 Src2_Tag=13
Src2_Value=0x00000003
[175000] ALU_RS[6]: Busy=1 Ready=0 ROB_ID=17 Op=0x000b3 Src1_Valid=1 Src1_Tag=13 Src1_Value=0x00000003 Src2_Valid=1 Src2_Tag=11
Src2_Value=0x00000001
[175000] ALU_RS[7]: Busy=1 Ready=0 ROB_ID=19 Op=0x08033 Src1_Valid=0 Src1_Tag=17 Src1_Value=0x00000000 Src2_Valid=0 Src2_Tag=16
Src2_Value=0x00000000
[175000] ALU_RS[9]: Busy=1 Ready=0 ROB_ID=21 Op=0x00133 Src1_Valid=0 Src1_Tag=19 Src1_Value=0x00000000 Src2_Valid=0 Src2_Tag=17
Src2_Value=0x00000000
[175000] ALU_RS[10]: Busy=1 Ready=0 ROB_ID=22 Op=0x00033 Src1_Valid=1 Src1_Tag=13 Src1_Value=0x00000003 Src2_Valid=0 Src2_Tag=19
Src2_Value=0x00000000
[175000] --- Load/Store Buffer ---
[175000] LSB[0]: Busy=1 Ready=1 ROB_ID=24 Op=0x00003 Src_Valid=1 Src_Tag=0 Src_Value=0x00000000 Store_Data_Valid=0 Store_Data_Tag=0
Store_Data=0x00000000
[175000] LSB[1]: Busy=1 Ready=1 ROB_ID=25 Op=0x00003 Src_Valid=1 Src_Tag=0 Src_Value=0x00000000 Store_Data_Valid=0 Store_Data_Tag=0
Store_Data=0x00000000
[175000] LSB[2]: Busy=1 Ready=0 ROB_ID=26 Op=0x00123 Src_Valid=0 Src_Tag=25 Src_Value=0x00000000 Store_Data_Valid=1 Store_Data_Tag=11
Store_Data=0x00000000

[175000] ===== EXECUTION STAGE (CDB INPUT) =====

[175000] CDB[0]: ROB_ID=8 Result=0x00000004 Ready=1

[175000] CDB[1]: ROB_ID=9 Result=0x00000003 Ready=1

[175000] ===== FORWARDING MESSAGES =====

[175000] FORWARD[INTRA_SRC1]: DISPATCH[1] ROB_ID=25 -> DISPATCH[2] ROB_ID=26 Reg=19

[175000] ===== CURRENT RAT AND VALID =====

[175000] RAT[1]: Tag=11 Valid=1
[175000] RAT[4]: Tag=8 Valid=1
[175000] RAT[6]: Tag=23 Valid=1
[175000] RAT[7]: Tag=9 Valid=1
[175000] RAT[8]: Tag=10 Valid=1
[175000] RAT[9]: Tag=13 Valid=1
[175000] RAT[10]: Tag=19 Valid=1
[175000] RAT[11]: Tag=22 Valid=1
[175000] RAT[12]: Tag=17 Valid=1
[175000] RAT[13]: Tag=20 Valid=1
[175000] RAT[14]: Tag=21 Valid=1
[175000] RAT[15]: Tag=14 Valid=1
[175000] RAT[18]: Tag=24 Valid=1
[175000] RAT[19]: Tag=25 Valid=1


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[175000] ===== ARCHITECTURAL REGISTER FILE (ARF) =====
[175000] ARF[1]: Value=0x00000001
[175000] ARF[2]: Value=0x00000002
[175000] ARF[3]: Value=0x00000002
[175000] [MMU] LOAD ISSUED: LQ[3] ROB_ID=24 Addr=0x00000010 Size=0
[175000] [MMU] LOAD ISSUED: LQ[4] ROB_ID=25 Addr=0x00000014 Size=0
[175000] [MMU] LOAD ISSUED: LQ[3] ROB_ID=24 Addr=0x00000010 Size=0
[175000] [MMU] LOAD ISSUED: LQ[4] ROB_ID=25 Addr=0x00000014 Size=0

[185000] ===== DECODE/DISPATCH STAGE =====
[185000] DECODE[0]: PC=0x00000078 Instr=0x02308433 Type=2 Dst=8 Src1=1 Src2=3 Opcode=0x33 Func3=0x0 Func7=0x01 Operation=0x00433
Imm=0x00000000
[185000] DECODE[1]: PC=0x0000007c Instr=0x0020e3b3 Type=0 Dst=7 Src1=1 Src2=2 Opcode=0x33 Func3=0x6 Func7=0x00 Operation=0x00333
Imm=0x00000000
[185000] DECODE[2]: PC=0x00000080 Instr=0x00138eb3 Type=0 Dst=29 Src1=7 Src2=1 Opcode=0x33 Func3=0x0 Func7=0x00 Operation=0x00033
Imm=0x00000000
[185000] DISPATCH[0]: ROB_ID=27 RS_ID=4 RS_Alloc=1 Src1_Ready=1 Src2_Ready=0 Dst=1 Src1=9 Src2=10 Src1_Tag=13 Src2_Tag=19
Src1_Value=0x00000003 Src2_Value=0x00000000 Operation=0x00033 Type=0 PC=0x0000006c Instr=0x00a480b3
[185000] DISPATCH[1]: ROB_ID=28 RS_ID=8 RS_Alloc=1 Src1_Ready=1 Src2_Ready=0 Dst=2 Src1=9 Src2=11 Src1_Tag=13 Src2_Tag=22
Src1_Value=0x00000003 Src2_Value=0x00000000 Operation=0x00033 Type=0 PC=0x00000070 Instr=0x00b48133
[185000] DISPATCH[2]: ROB_ID=29 RS_ID=11 RS_Alloc=1 Src1_Ready=0 Src2_Ready=0 Dst=3 Src1=1 Src2=2 Src1_Tag=27 Src2_Tag=28
Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00033 Type=0 PC=0x00000074 Instr=0x002081b3

[185000] ===== REORDER BUFFER (ROB) =====
[185000] ROB Head: 30, ROB Tail: 11
[185000] ROB[11]: Valid=1 Ready=1 Dest=1 Value=0x00000001 Instr_ID=11 PC=0x0000002c
[185000] ROB[12]: Valid=1 Ready=1 Dest=9 Value=0x00000002 Instr_ID=12 PC=0x00000030
[185000] ROB[13]: Valid=1 Ready=1 Dest=9 Value=0x00000003 Instr_ID=13 PC=0x00000034
[185000] ROB[14]: Valid=1 Ready=0 Dest=15 Value=0x00000000 Instr_ID=14 PC=0x00000038
[185000] ROB[15]: Valid=1 Ready=1 Dest=10 Value=0x00000000 Instr_ID=15 PC=0x0000003c
[185000] ROB[16]: Valid=1 Ready=0 Dest=11 Value=0x00000000 Instr_ID=16 PC=0x00000040
[185000] ROB[17]: Valid=1 Ready=0 Dest=12 Value=0x00000000 Instr_ID=17 PC=0x00000044
[185000] ROB[18]: Valid=1 Ready=0 Dest=13 Value=0x00000000 Instr_ID=18 PC=0x00000048
[185000] ROB[19]: Valid=1 Ready=0 Dest=10 Value=0x00000000 Instr_ID=19 PC=0x0000004c
[185000] ROB[20]: Valid=1 Ready=1 Dest=13 Value=0x00000000 Instr_ID=20 PC=0x00000050
[185000] ROB[21]: Valid=1 Ready=0 Dest=14 Value=0x00000000 Instr_ID=21 PC=0x00000054
[185000] ROB[22]: Valid=1 Ready=0 Dest=11 Value=0x00000000 Instr_ID=22 PC=0x00000058
[185000] ROB[23]: Valid=1 Ready=0 Dest=6 Value=0x00000000 Instr_ID=23 PC=0x0000005c
[185000] ROB[24]: Valid=1 Ready=0 Dest=18 Value=0x00000000 Instr_ID=24 PC=0x00000060
[185000] ROB[25]: Valid=1 Ready=0 Dest=19 Value=0x00000000 Instr_ID=25 PC=0x00000064
[185000] ROB[26]: Valid=1 Ready=0 Dest=0 Value=0x00000000 Instr_ID=26 PC=0x00000068

[185000] ===== RESERVATION STATIONS =====
[185000] --- ALU Reservation Stations ---
[185000] ALU_RS[1]: Busy=1 Ready=1 ROB_ID=18 Op=0x002b3 Src1_Valid=1 Src1_Tag=13 Src1_Value=0x00000003 Src2_Valid=1 Src2_Tag=11
Src2_Value=0x00000001
[185000] ALU_RS[2]: Busy=1 Ready=1 ROB_ID=14 Op=0x00233 Src1_Valid=1 Src1_Tag=13 Src1_Value=0x00000003 Src2_Valid=1 Src2_Tag=8
Src2_Value=0x00000000
[185000] ALU_RS[5]: Busy=1 Ready=1 ROB_ID=16 Op=0x00233 Src1_Valid=1 Src1_Tag=15 Src1_Value=0x00000000 Src2_Valid=1 Src2_Tag=13
Src2_Value=0x00000003
[185000] ALU_RS[6]: Busy=1 Ready=1 ROB_ID=17 Op=0x000b3 Src1_Valid=1 Src1_Tag=13 Src1_Value=0x00000003 Src2_Valid=1 Src2_Tag=11
Src2_Value=0x00000001
[185000] ALU_RS[7]: Busy=1 Ready=0 ROB_ID=19 Op=0x08033 Src1_Valid=0 Src1_Tag=17 Src1_Value=0x00000000 Src2_Valid=0 Src2_Tag=16
Src2_Value=0x00000000
[185000] ALU_RS[9]: Busy=1 Ready=0 ROB_ID=21 Op=0x00133 Src1_Valid=0 Src1_Tag=19 Src1_Value=0x00000000 Src2_Valid=0 Src2_Tag=17
Src2_Value=0x00000000
[185000] ALU_RS[10]: Busy=1 Ready=0 ROB_ID=22 Op=0x00033 Src1_Valid=1 Src1_Tag=13 Src1_Value=0x00000003 Src2_Valid=0 Src2_Tag=19
Src2_Value=0x00000000
[185000] --- Load/Store Buffer ---
[185000] LSB[2]: Busy=1 Ready=0 ROB_ID=26 Op=0x00123 Src_Valid=0 Src_Tag=25 Src_Value=0x00000000 Store_Data_Valid=1 Store_Data_Tag=11
Store_Data=0x00000000

[185000] ===== FORWARDING MESSAGES =====
[185000] FORWARD[INTRA_SRC1]: DISPATCH[0] ROB_ID=27 -> DISPATCH[2] ROB_ID=29 Reg=1
[185000] FORWARD[INTRA_SRC2]: DISPATCH[1] ROB_ID=28 -> DISPATCH[2] ROB_ID=29 Reg=2

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[185000] ===== INSTRUCTIONS COMMITTED THIS CYCLE =====

[185000] COMMITTED[0]: ROB_ID=8

[185000] COMMITTED[1]: ROB_ID=9

[185000] COMMITTED[2]: ROB_ID=10

[185000] Total Instructions Committed This Cycle: 3

[185000] ===== CURRENT RAT AND VALID =====

[185000] RAT[1]: Tag=27 Valid=1

[185000] RAT[2]: Tag=28 Valid=1

[185000] RAT[3]: Tag=29 Valid=1

[185000] RAT[6]: Tag=23 Valid=1

[185000] RAT[9]: Tag=13 Valid=1

[185000] RAT[10]: Tag=19 Valid=1

[185000] RAT[11]: Tag=22 Valid=1

[185000] RAT[12]: Tag=17 Valid=1

[185000] RAT[13]: Tag=20 Valid=1

[185000] RAT[14]: Tag=21 Valid=1

[185000] RAT[15]: Tag=14 Valid=1

[185000] RAT[18]: Tag=24 Valid=1

[185000] RAT[19]: Tag=25 Valid=1

[185000] ===== ARCHITECTURAL REGISTER FILE (ARF) =====

[185000] ARF[1]: Value=0x00000001

[185000] ARF[2]: Value=0x00000002

[185000] ARF[3]: Value=0x00000002

[185000] ARF[4]: Value=0x00000004

[185000] ARF[7]: Value=0x00000003

[185000] ARF Checker: PASS - ROB[8] add x4, x2, x3 -> x4 = 4

[185000] ARF Checker: PASS - ROB[9] add x7, x3, x1 -> x7 = 3

[185000] ARF Checker: PASS - ROB[10] add x8, x8, x9 -> x8 = 0

[195000] ===== DECODE/DISPATCH STAGE =====

[195000] DECODE[0]: PC=0x00000078 Instr=0x02308433 Type=2 Dst=8 Src1=1 Src2=3 Opcode=0x33 Func3=0x0 Func7=0x01 Operation=0x00433 Imm=0x00000000

[195000] DECODE[1]: PC=0x0000007c Instr=0x0020e3b3 Type=0 Dst=7 Src1=1 Src2=2 Opcode=0x33 Func3=0x6 Func7=0x00 Operation=0x00333 Imm=0x00000000

[195000] DECODE[2]: PC=0x00000080 Instr=0x00138eb3 Type=0 Dst=29 Src1=7 Src2=1 Opcode=0x33 Func3=0x0 Func7=0x00 Operation=0x00033 Imm=0x00000000

[195000] DISPATCH[0]: ROB_ID=27 RS_ID=4 RS_Alloc=1 Src1_Ready=1 Src2_Ready=0 Dst=1 Src1=9 Src2=10 Src1_Tag=13 Src2_Tag=19 Src1_Value=0x00000003 Src2_Value=0x00000000 Operation=0x00033 Type=0 PC=0x0000006c Instr=0x00a480b3

[195000] DISPATCH[1]: ROB_ID=28 RS_ID=8 RS_Alloc=1 Src1_Ready=1 Src2_Ready=0 Dst=2 Src1=9 Src2=11 Src1_Tag=13 Src2_Tag=22 Src1_Value=0x00000003 Src2_Value=0x00000000 Operation=0x00033 Type=0 PC=0x00000070 Instr=0x00b48133

[195000] DISPATCH[2]: ROB_ID=29 RS_ID=11 RS_Alloc=1 Src1_Ready=0 Src2_Ready=0 Dst=3 Src1=1 Src2=2 Src1_Tag=27 Src2_Tag=28 Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00033 Type=0 PC=0x00000074 Instr=0x002081b3

[195000] ===== REORDER BUFFER (ROB) =====

[195000] ROB Head: 30, ROB Tail: 14

[195000] ROB[14]: Valid=1 Ready=0 Dest=15 Value=0x00000000 Instr_ID=14 PC=0x00000038

[195000] ROB[15]: Valid=1 Ready=1 Dest=10 Value=0x00000000 Instr_ID=15 PC=0x0000003c

[195000] ROB[16]: Valid=1 Ready=0 Dest=11 Value=0x00000000 Instr_ID=16 PC=0x00000040

[195000] ROB[17]: Valid=1 Ready=0 Dest=12 Value=0x00000000 Instr_ID=17 PC=0x00000044

[195000] ROB[18]: Valid=1 Ready=0 Dest=13 Value=0x00000000 Instr_ID=18 PC=0x00000048

[195000] ROB[19]: Valid=1 Ready=0 Dest=10 Value=0x00000000 Instr_ID=19 PC=0x0000004c

[195000] ROB[20]: Valid=1 Ready=1 Dest=13 Value=0x00000000 Instr_ID=20 PC=0x00000050

[195000] ROB[21]: Valid=1 Ready=0 Dest=14 Value=0x00000000 Instr_ID=21 PC=0x00000054

[195000] ROB[22]: Valid=1 Ready=0 Dest=11 Value=0x00000000 Instr_ID=22 PC=0x00000058

[195000] ROB[23]: Valid=1 Ready=0 Dest=6 Value=0x00000000 Instr_ID=23 PC=0x0000005c

[195000] ROB[24]: Valid=1 Ready=0 Dest=18 Value=0x00000000 Instr_ID=24 PC=0x00000060

[195000] ROB[25]: Valid=1 Ready=0 Dest=19 Value=0x00000000 Instr_ID=25 PC=0x00000064

[195000] ROB[26]: Valid=1 Ready=0 Dest=0 Value=0x00000000 Instr_ID=26 PC=0x00000068

[195000] ROB[27]: Valid=1 Ready=0 Dest=1 Value=0x00000000 Instr_ID=27 PC=0x0000006c

[195000] ROB[28]: Valid=1 Ready=0 Dest=2 Value=0x00000000 Instr_ID=28 PC=0x00000070

[195000] ROB[29]: Valid=1 Ready=0 Dest=3 Value=0x00000000 Instr_ID=29 PC=0x00000074

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[195000] ===== RESERVATION STATIONS =====
[195000] --- ALU Reservation Stations ---
[195000] ALU_RS[1]: Busy=1 Ready=1 ROB_ID=18 Op=0x002b3 Src1_Valid=1 Src1_Tag=13 Src1_Value=0x00000003 Src2_Valid=1 Src2_Tag=11
Src2_Value=0x00000001
[195000] ALU_RS[4]: Busy=1 Ready=0 ROB_ID=27 Op=0x00033 Src1_Valid=1 Src1_Tag=13 Src1_Value=0x00000003 Src2_Valid=0 Src2_Tag=19
Src2_Value=0x00000000
[195000] ALU_RS[7]: Busy=1 Ready=0 ROB_ID=19 Op=0x08033 Src1_Valid=0 Src1_Tag=17 Src1_Value=0x00000000 Src2_Valid=0 Src2_Tag=16
Src2_Value=0x00000000
[195000] ALU_RS[8]: Busy=1 Ready=0 ROB_ID=28 Op=0x00033 Src1_Valid=1 Src1_Tag=13 Src1_Value=0x00000003 Src2_Valid=0 Src2_Tag=22
Src2_Value=0x00000000
[195000] ALU_RS[9]: Busy=1 Ready=0 ROB_ID=21 Op=0x00133 Src1_Valid=0 Src1_Tag=19 Src1_Value=0x00000000 Src2_Valid=0 Src2_Tag=17
Src2_Value=0x00000000
[195000] ALU_RS[10]: Busy=1 Ready=0 ROB_ID=22 Op=0x00033 Src1_Valid=1 Src1_Tag=13 Src1_Value=0x00000003 Src2_Valid=0 Src2_Tag=19
Src2_Value=0x00000000
[195000] ALU_RS[11]: Busy=1 Ready=0 ROB_ID=29 Op=0x00033 Src1_Valid=0 Src1_Tag=27 Src1_Value=0x00000000 Src2_Valid=0 Src2_Tag=28
Src2_Value=0x00000000
[195000] --- Load/Store Buffer ---
[195000] LSB[2]: Busy=1 Ready=0 ROB_ID=26 Op=0x00123 Src_Valid=0 Src_Tag=25 Src_Value=0x00000000 Store_Data_Valid=1 Store_Data_Tag=11
Store_Data=0x00000000

[195000] ===== EXECUTION STAGE (CDB INPUT) =====
[195000] CDB[0]: ROB_ID=14 Result=0x00000003 Ready=1
[195000] CDB[1]: ROB_ID=16 Result=0x00000003 Ready=1
[195000] CDB[2]: ROB_ID=17 Result=0x00000006 Ready=1

[195000] ===== FORWARDING MESSAGES =====
[195000] FORWARD[CDB_CURR->ALU_SRC2]: CDB[1] ROB_ID=16 -> ALU_RS[7] ROB_ID=19 Value=0x00000003
[195000] FORWARD[CDB_CURR->ALU_SRC1]: CDB[2] ROB_ID=17 -> ALU_RS[7] ROB_ID=19 Value=0x00000006
[195000] FORWARD[CDB_CURR->ALU_SRC2]: CDB[2] ROB_ID=17 -> ALU_RS[9] ROB_ID=21 Value=0x00000006
[195000] FORWARD[RETIRE_CURR->ALU_SRC2]: RETIRE_CURR[2] ROB_ID=16 -> ALU_RS[7] ROB_ID=19 Value=0x00000003
[195000] FORWARD[INTRA_SRC1]: DISPATCH[0] ROB_ID=27 -> DISPATCH[2] ROB_ID=29 Reg=1
[195000] FORWARD[INTRA_SRC2]: DISPATCH[1] ROB_ID=28 -> DISPATCH[2] ROB_ID=29 Reg=2

[195000] ===== INSTRUCTIONS COMMITTED THIS CYCLE =====
[195000] COMMITTED[0]: ROB_ID=11
[195000] COMMITTED[1]: ROB_ID=12
[195000] COMMITTED[2]: ROB_ID=13
[195000] Total Instructions Committed This Cycle: 3

[195000] ===== CURRENT RAT AND VALID =====
[195000] RAT[1]: Tag=27 Valid=1
[195000] RAT[2]: Tag=28 Valid=1
[195000] RAT[3]: Tag=29 Valid=1
[195000] RAT[6]: Tag=23 Valid=1
[195000] RAT[10]: Tag=19 Valid=1
[195000] RAT[11]: Tag=22 Valid=1
[195000] RAT[12]: Tag=17 Valid=1
[195000] RAT[13]: Tag=20 Valid=1
[195000] RAT[14]: Tag=21 Valid=1
[195000] RAT[15]: Tag=14 Valid=1
[195000] RAT[18]: Tag=24 Valid=1
[195000] RAT[19]: Tag=25 Valid=1

[195000] ===== ARCHITECTURAL REGISTER FILE (ARF) =====
[195000] ARF[1]: Value=0x00000001
[195000] ARF[2]: Value=0x00000002
[195000] ARF[3]: Value=0x00000002
[195000] ARF[4]: Value=0x00000004
[195000] ARF[7]: Value=0x00000003
[195000] ARF[9]: Value=0x00000003
[195000] ARF Checker: PASS - ROB[11] lb x1, 4(x0) -> x1 = 1
[195000] ARF Checker: PASS - ROB[12] lbu x9, 8(x0) -> x9 = 2
[195000] ARF Checker: PASS - ROB[13] lw x9, 12(x0) -> x9 = 3

[205000] ===== DECODE/DISPATCH STAGE =====

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[205000] DECODE[0]: PC=0x00000078 Instr=0x02308433 Type=2 Dst=8 Src1=1 Src2=3 Opcode=0x33 Func3=0x0 Func7=0x01 Operation=0x00433
Imm=0x00000000
[205000] DECODE[1]: PC=0x0000007c Instr=0x0020e3b3 Type=0 Dst=7 Src1=1 Src2=2 Opcode=0x33 Func3=0x6 Func7=0x00 Operation=0x00333
Imm=0x00000000
[205000] DECODE[2]: PC=0x00000080 Instr=0x00138eb3 Type=0 Dst=29 Src1=7 Src2=1 Opcode=0x33 Func3=0x0 Func7=0x00 Operation=0x00033
Imm=0x00000000
[205000] DISPATCH[0]: ROB_ID=30 RS_ID=0 RS_Alloc=1 Src1_Ready=0 Src2_Ready=0 Dst=8 Src1=1 Src2=3 Src1_Tag=27 Src2_Tag=29
Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00433 Type=2 PC=0x00000078 Instr=0x02308433
[205000] DISPATCH[1]: ROB_ID=31 RS_ID=0 RS_Alloc=1 Src1_Ready=0 Src2_Ready=0 Dst=7 Src1=1 Src2=2 Src1_Tag=27 Src2_Tag=28
Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00333 Type=0 PC=0x0000007c Instr=0x0020e3b3
[205000] DISPATCH[2]: ROB_ID=32 RS_ID=2 RS_Alloc=1 Src1_Ready=0 Src2_Ready=0 Dst=29 Src1=7 Src2=1 Src1_Tag=31 Src2_Tag=27
Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00033 Type=0 PC=0x00000080 Instr=0x00138eb3

[205000] ===== REORDER BUFFER (ROB) =====
[205000] ROB Head: 33, ROB Tail: 17
[205000] ROB[17]: Valid=1 Ready=1 Dest=12 Value=0x00000006 Instr_ID=17 PC=0x00000044
[205000] ROB[18]: Valid=1 Ready=0 Dest=13 Value=0x00000000 Instr_ID=18 PC=0x00000048
[205000] ROB[19]: Valid=1 Ready=0 Dest=10 Value=0x00000000 Instr_ID=19 PC=0x0000004c
[205000] ROB[20]: Valid=1 Ready=1 Dest=13 Value=0x00000000 Instr_ID=20 PC=0x00000050
[205000] ROB[21]: Valid=1 Ready=0 Dest=14 Value=0x00000000 Instr_ID=21 PC=0x00000054
[205000] ROB[22]: Valid=1 Ready=0 Dest=11 Value=0x00000000 Instr_ID=22 PC=0x00000058
[205000] ROB[23]: Valid=1 Ready=0 Dest=6 Value=0x00000000 Instr_ID=23 PC=0x0000005c
[205000] ROB[24]: Valid=1 Ready=0 Dest=18 Value=0x00000000 Instr_ID=24 PC=0x00000060
[205000] ROB[25]: Valid=1 Ready=0 Dest=19 Value=0x00000000 Instr_ID=25 PC=0x00000064
[205000] ROB[26]: Valid=1 Ready=0 Dest=0 Value=0x00000000 Instr_ID=26 PC=0x00000068
[205000] ROB[27]: Valid=1 Ready=0 Dest=1 Value=0x00000000 Instr_ID=27 PC=0x0000006c
[205000] ROB[28]: Valid=1 Ready=0 Dest=2 Value=0x00000000 Instr_ID=28 PC=0x00000070
[205000] ROB[29]: Valid=1 Ready=0 Dest=3 Value=0x00000000 Instr_ID=29 PC=0x00000074

[205000] ===== RESERVATION STATIONS =====
[205000] --- ALU Reservation Stations ---
[205000] ALU_RS[4]: Busy=1 Ready=0 ROB_ID=27 Op=0x00033 Src1_Valid=1 Src1_Tag=13 Src1_Value=0x00000003 Src2_Valid=0 Src2_Tag=19
Src2_Value=0x00000000
[205000] ALU_RS[7]: Busy=1 Ready=0 ROB_ID=19 Op=0x08033 Src1_Valid=1 Src1_Tag=17 Src1_Value=0x00000006 Src2_Valid=1 Src2_Tag=16
Src2_Value=0x00000003
[205000] ALU_RS[8]: Busy=1 Ready=0 ROB_ID=28 Op=0x00033 Src1_Valid=1 Src1_Tag=13 Src1_Value=0x00000003 Src2_Valid=0 Src2_Tag=22
Src2_Value=0x00000000
[205000] ALU_RS[9]: Busy=1 Ready=0 ROB_ID=21 Op=0x00133 Src1_Valid=0 Src1_Tag=19 Src1_Value=0x00000000 Src2_Valid=1 Src2_Tag=17
Src2_Value=0x00000006
[205000] ALU_RS[10]: Busy=1 Ready=0 ROB_ID=22 Op=0x00033 Src1_Valid=1 Src1_Tag=13 Src1_Value=0x00000003 Src2_Valid=0 Src2_Tag=19
Src2_Value=0x00000000
[205000] ALU_RS[11]: Busy=1 Ready=0 ROB_ID=29 Op=0x00033 Src1_Valid=0 Src1_Tag=27 Src1_Value=0x00000000 Src2_Valid=0 Src2_Tag=28
Src2_Value=0x00000000
[205000] --- Load/Store Buffer ---
[205000] LSB[2]: Busy=1 Ready=0 ROB_ID=26 Op=0x00123 Src_Valid=0 Src_Tag=25 Src_Value=0x00000000 Store_Data_Valid=1 Store_Data_Tag=11
Store_Data=0x00000000

[205000] ===== EXECUTION STAGE (CDB INPUT) =====
[205000] CDB[0]: ROB_ID=24 Result=0x00000003 Ready=1
[205000] CDB[1]: ROB_ID=25 Result=0x00000005 Ready=1
[205000] CDB[2]: ROB_ID=18 Result=0x00000001 Ready=1

[205000] ===== FORWARDING MESSAGES =====
[205000] FORWARD[CDB_CURR->LSB_SRC]: CDB[1] ROB_ID=25 -> LSB[2] ROB_ID=26 Value=0x00000005
[205000] FORWARD[INTRA_SRC1]: DISPATCH[1] ROB_ID=31 -> DISPATCH[2] ROB_ID=32 Reg=7

[205000] ===== INSTRUCTIONS COMMITTED THIS CYCLE =====
[205000] COMMITTED[0]: ROB_ID=14
[205000] COMMITTED[1]: ROB_ID=15
[205000] COMMITTED[2]: ROB_ID=16
[205000] Total Instructions Committed This Cycle: 3

[205000] ===== CURRENT RAT AND VALID =====
[205000] RAT[1]: Tag=27 Valid=1
[205000] RAT[2]: Tag=28 Valid=1

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[205000] RAT[3]: Tag=29 Valid=1
[205000] RAT[6]: Tag=23 Valid=1
[205000] RAT[7]: Tag=31 Valid=1
[205000] RAT[8]: Tag=30 Valid=1
[205000] RAT[10]: Tag=19 Valid=1
[205000] RAT[11]: Tag=22 Valid=1
[205000] RAT[12]: Tag=17 Valid=1
[205000] RAT[13]: Tag=20 Valid=1
[205000] RAT[14]: Tag=21 Valid=1
[205000] RAT[18]: Tag=24 Valid=1
[205000] RAT[19]: Tag=25 Valid=1
[205000] RAT[29]: Tag=32 Valid=1

[205000] ===== ARCHITECTURAL REGISTER FILE (ARF) =====

[205000] ARF[1]: Value=0x00000001
[205000] ARF[2]: Value=0x00000002
[205000] ARF[3]: Value=0x00000002
[205000] ARF[4]: Value=0x00000004
[205000] ARF[7]: Value=0x00000003
[205000] ARF[9]: Value=0x00000003
[205000] ARF[11]: Value=0x00000003
[205000] ARF[15]: Value=0x00000003
[205000] ARF Checker: PASS - ROB[14] xor x15, x9, x10 -> x15 = 3
[205000] ARF Checker: PASS - ROB[15] add x10, x10, x11 -> x10 = 0
[205000] ARF Checker: PASS - ROB[16] add x11, x10, x9 -> x11 = 3

[215000] ===== DECODE/DISPATCH STAGE =====

[215000] DECODE[0]: PC=0x00000078 Instr=0x02308433 Type=2 Dst=8 Src1=1 Src2=3 Opcode=0x33 Func3=0x0 Func7=0x01 Operation=0x00433
Imm=0x00000000
[215000] DECODE[1]: PC=0x0000007c Instr=0x0020e3b3 Type=0 Dst=7 Src1=1 Src2=2 Opcode=0x33 Func3=0x6 Func7=0x00 Operation=0x00333
Imm=0x00000000
[215000] DECODE[2]: PC=0x00000080 Instr=0x00138eb3 Type=0 Dst=29 Src1=7 Src2=1 Opcode=0x33 Func3=0x0 Func7=0x00 Operation=0x00033
Imm=0x00000000
[215000] DISPATCH[0]: ROB_ID=30 RS_ID=0 RS_Alloc=1 Src1_Ready=0 Src2_Ready=0 Dst=8 Src1=1 Src2=3 Src1_Tag=27 Src2_Tag=29
Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00433 Type=2 PC=0x00000078 Instr=0x02308433
[215000] DISPATCH[1]: ROB_ID=31 RS_ID=0 RS_Alloc=1 Src1_Ready=0 Src2_Ready=0 Dst=7 Src1=1 Src2=2 Src1_Tag=27 Src2_Tag=28
Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00333 Type=0 PC=0x0000007c Instr=0x0020e3b3
[215000] DISPATCH[2]: ROB_ID=32 RS_ID=2 RS_Alloc=1 Src1_Ready=0 Src2_Ready=0 Dst=29 Src1=7 Src2=1 Src1_Tag=31 Src2_Tag=27
Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00033 Type=0 PC=0x00000080 Instr=0x00138eb3

[215000] ===== REORDER BUFFER (ROB) =====

[215000] ROB Head: 33, ROB Tail: 19
[215000] ROB[19]: Valid=1 Ready=0 Dest=10 Value=0x00000000 Instr_ID=19 PC=0x0000004c
[215000] ROB[20]: Valid=1 Ready=1 Dest=13 Value=0x00000000 Instr_ID=20 PC=0x00000050
[215000] ROB[21]: Valid=1 Ready=0 Dest=14 Value=0x00000000 Instr_ID=21 PC=0x00000054
[215000] ROB[22]: Valid=1 Ready=0 Dest=11 Value=0x00000000 Instr_ID=22 PC=0x00000058
[215000] ROB[23]: Valid=1 Ready=0 Dest=6 Value=0x00000000 Instr_ID=23 PC=0x0000005c
[215000] ROB[24]: Valid=1 Ready=1 Dest=18 Value=0x00000003 Instr_ID=24 PC=0x00000060
[215000] ROB[25]: Valid=1 Ready=1 Dest=19 Value=0x00000005 Instr_ID=25 PC=0x00000064
[215000] ROB[26]: Valid=1 Ready=0 Dest=0 Value=0x00000000 Instr_ID=26 PC=0x00000068
[215000] ROB[27]: Valid=1 Ready=0 Dest=1 Value=0x00000000 Instr_ID=27 PC=0x0000006c
[215000] ROB[28]: Valid=1 Ready=0 Dest=2 Value=0x00000000 Instr_ID=28 PC=0x00000070
[215000] ROB[29]: Valid=1 Ready=0 Dest=3 Value=0x00000000 Instr_ID=29 PC=0x00000074
[215000] ROB[30]: Valid=1 Ready=0 Dest=8 Value=0x00000000 Instr_ID=30 PC=0x00000078
[215000] ROB[31]: Valid=1 Ready=0 Dest=7 Value=0x00000000 Instr_ID=31 PC=0x0000007c
[215000] ROB[32]: Valid=1 Ready=0 Dest=29 Value=0x00000000 Instr_ID=0 PC=0x00000080

[215000] ===== RESERVATION STATIONS =====

[215000] --- ALU Reservation Stations ---
[215000] ALU_RS[0]: Busy=1 Ready=0 ROB_ID=31 Op=0x00333 Src1_Valid=0 Src1_Tag=27 Src1_Value=0x00000000 Src2_Valid=0 Src2_Tag=28
Src2_Value=0x00000000
[215000] ALU_RS[2]: Busy=1 Ready=0 ROB_ID=32 Op=0x00033 Src1_Valid=0 Src1_Tag=31 Src1_Value=0x00000000 Src2_Valid=0 Src2_Tag=27
Src2_Value=0x00000000
[215000] ALU_RS[4]: Busy=1 Ready=0 ROB_ID=27 Op=0x00033 Src1_Valid=1 Src1_Tag=13 Src1_Value=0x00000003 Src2_Valid=0 Src2_Tag=19
Src2_Value=0x00000000

[215000] ALU_RS[7]: Busy=1 Ready=1 ROB_ID=19 Op=0x08033 Src1_Valid=1 Src1_Tag=17 Src1_Value=0x00000006 Src2_Valid=1 Src2_Tag=16 Src2_Value=0x00000003
[215000] ALU_RS[8]: Busy=1 Ready=0 ROB_ID=28 Op=0x00033 Src1_Valid=1 Src1_Tag=13 Src1_Value=0x00000003 Src2_Valid=0 Src2_Tag=22 Src2_Value=0x00000000
[215000] ALU_RS[9]: Busy=1 Ready=0 ROB_ID=21 Op=0x00133 Src1_Valid=0 Src1_Tag=19 Src1_Value=0x00000000 Src2_Valid=1 Src2_Tag=17 Src2_Value=0x00000006
[215000] ALU_RS[10]: Busy=1 Ready=0 ROB_ID=22 Op=0x00033 Src1_Valid=1 Src1_Tag=13 Src1_Value=0x00000003 Src2_Valid=0 Src2_Tag=19 Src2_Value=0x00000000
[215000] ALU_RS[11]: Busy=1 Ready=0 ROB_ID=29 Op=0x00033 Src1_Valid=0 Src1_Tag=27 Src1_Value=0x00000000 Src2_Valid=0 Src2_Tag=28 Src2_Value=0x00000000
[215000] --- Mul/Div Reservation Stations ---
[215000] MD_RS[0]: Busy=1 Ready=0 ROB_ID=30 Op=0x00433 Src1_Valid=0 Src1_Tag=27 Src1_Value=0x00000000 Src2_Valid=0 Src2_Tag=29 Src2_Value=0x00000000
[215000] --- Load/Store Buffer ---
[215000] LSB[2]: Busy=1 Ready=0 ROB_ID=26 Op=0x00123 Src_Valid=1 Src_Tag=25 Src_Value=0x00000005 Store_Data_Valid=1 Store_Data_Tag=11 Store_Data=0x00000000

[215000] ===== EXECUTION STAGE (CDB INPUT) =====

[215000] CDB[0]: ROB_ID=19 Result=0x00000003 Ready=1

[215000] ===== FORWARDING MESSAGES =====

[215000] FORWARD[CDB_CURR->ALU_SRC2]: CDB[0] ROB_ID=19 -> ALU_RS[4] ROB_ID=27 Value=0x00000003
[215000] FORWARD[CDB_CURR->ALU_SRC1]: CDB[0] ROB_ID=19 -> ALU_RS[9] ROB_ID=21 Value=0x00000003
[215000] FORWARD[CDB_CURR->ALU_SRC2]: CDB[0] ROB_ID=19 -> ALU_RS[10] ROB_ID=22 Value=0x00000003
[215000] FORWARD[RETIRE_CURR->ALU_SRC2]: RETIRE_CURR[0] ROB_ID=19 -> ALU_RS[4] ROB_ID=27 Value=0x00000003
[215000] FORWARD[RETIRE_CURR->ALU_SRC1]: RETIRE_CURR[0] ROB_ID=19 -> ALU_RS[9] ROB_ID=21 Value=0x00000003
[215000] FORWARD[RETIRE_CURR->ALU_SRC2]: RETIRE_CURR[0] ROB_ID=19 -> ALU_RS[10] ROB_ID=22 Value=0x00000003
[215000] FORWARD[INTRA_SRC1]: DISPATCH[1] ROB_ID=31 -> DISPATCH[2] ROB_ID=32 Reg=7

[215000] ===== INSTRUCTIONS COMMITTED THIS CYCLE =====

[215000] COMMITTED[0]: ROB_ID=17

[215000] COMMITTED[1]: ROB_ID=18

[215000] Total Instructions Committed This Cycle: 2

[215000] ===== CURRENT RAT AND VALID =====

[215000] RAT[1]: Tag=27 Valid=1

[215000] RAT[2]: Tag=28 Valid=1

[215000] RAT[3]: Tag=29 Valid=1

[215000] RAT[6]: Tag=23 Valid=1

[215000] RAT[7]: Tag=31 Valid=1

[215000] RAT[8]: Tag=30 Valid=1

[215000] RAT[10]: Tag=19 Valid=1

[215000] RAT[11]: Tag=22 Valid=1

[215000] RAT[13]: Tag=20 Valid=1

[215000] RAT[14]: Tag=21 Valid=1

[215000] RAT[18]: Tag=24 Valid=1

[215000] RAT[19]: Tag=25 Valid=1

[215000] RAT[29]: Tag=32 Valid=1

[215000] ===== ARCHITECTURAL REGISTER FILE (ARF) =====

[215000] ARF[1]: Value=0x00000001

[215000] ARF[2]: Value=0x00000002

[215000] ARF[3]: Value=0x00000002

[215000] ARF[4]: Value=0x00000004

[215000] ARF[7]: Value=0x00000003

[215000] ARF[9]: Value=0x00000003

[215000] ARF[11]: Value=0x00000003

[215000] ARF[12]: Value=0x00000006

[215000] ARF[13]: Value=0x00000001

[215000] ARF[15]: Value=0x00000003

[215000] ARF Checker: PASS - ROB[17] sll x12, x9, x1 -> x12 = 6

[215000] ARF Checker: PASS - ROB[18] srl x13, x9, x1 -> x13 = 1

[225000] ===== DECODE/DISPATCH STAGE =====

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[225000] DECODE[0]: PC=0x00000078 Instr=0x02308433 Type=2 Dst=8 Src1=1 Src2=3 Opcode=0x33 Func3=0x0 Func7=0x01 Operation=0x00433
Imm=0x00000000
[225000] DECODE[1]: PC=0x0000007c Instr=0x0020e3b3 Type=0 Dst=7 Src1=1 Src2=2 Opcode=0x33 Func3=0x6 Func7=0x00 Operation=0x00333
Imm=0x00000000
[225000] DECODE[2]: PC=0x00000080 Instr=0x00138eb3 Type=0 Dst=29 Src1=7 Src2=1 Opcode=0x33 Func3=0x0 Func7=0x00 Operation=0x00033
Imm=0x00000000
[225000] DISPATCH[0]: ROB_ID=30 RS_ID=0 RS_Alloc=1 Src1_Ready=0 Src2_Ready=0 Dst=8 Src1=1 Src2=3 Src1_Tag=27 Src2_Tag=29
Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00433 Type=2 PC=0x00000078 Instr=0x02308433
[225000] DISPATCH[1]: ROB_ID=31 RS_ID=0 RS_Alloc=1 Src1_Ready=0 Src2_Ready=0 Dst=7 Src1=1 Src2=2 Src1_Tag=27 Src2_Tag=28
Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00333 Type=0 PC=0x0000007c Instr=0x0020e3b3
[225000] DISPATCH[2]: ROB_ID=32 RS_ID=2 RS_Alloc=1 Src1_Ready=0 Src2_Ready=0 Dst=29 Src1=7 Src2=1 Src1_Tag=31 Src2_Tag=27
Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00033 Type=0 PC=0x00000080 Instr=0x00138eb3

[225000] ===== REORDER BUFFER (ROB) =====
[225000] ROB Head: 33, ROB Tail: 21
[225000] ROB[21]: Valid=1 Ready=0 Dest=14 Value=0x00000000 Instr_ID=21 PC=0x00000054
[225000] ROB[22]: Valid=1 Ready=0 Dest=11 Value=0x00000000 Instr_ID=22 PC=0x00000058
[225000] ROB[23]: Valid=1 Ready=0 Dest=6 Value=0x00000000 Instr_ID=23 PC=0x0000005c
[225000] ROB[24]: Valid=1 Ready=1 Dest=18 Value=0x00000003 Instr_ID=24 PC=0x00000060
[225000] ROB[25]: Valid=1 Ready=1 Dest=19 Value=0x00000005 Instr_ID=25 PC=0x00000064
[225000] ROB[26]: Valid=1 Ready=1 Dest=0 Value=0x00000000 Instr_ID=26 PC=0x00000068
[225000] ROB[27]: Valid=1 Ready=0 Dest=1 Value=0x00000000 Instr_ID=27 PC=0x0000006c
[225000] ROB[28]: Valid=1 Ready=0 Dest=2 Value=0x00000000 Instr_ID=28 PC=0x00000070
[225000] ROB[29]: Valid=1 Ready=0 Dest=3 Value=0x00000000 Instr_ID=29 PC=0x00000074
[225000] ROB[30]: Valid=1 Ready=0 Dest=8 Value=0x00000000 Instr_ID=30 PC=0x00000078
[225000] ROB[31]: Valid=1 Ready=0 Dest=7 Value=0x00000000 Instr_ID=31 PC=0x0000007c
[225000] ROB[32]: Valid=1 Ready=0 Dest=29 Value=0x00000000 Instr_ID=0 PC=0x00000080

[225000] ===== RESERVATION STATIONS =====
[225000] --- ALU Reservation Stations ---
[225000] ALU_RS[0]: Busy=1 Ready=0 ROB_ID=31 Op=0x00333 Src1_Valid=0 Src1_Tag=27 Src1_Value=0x00000000 Src2_Valid=0 Src2_Tag=28
Src2_Value=0x00000000
[225000] ALU_RS[2]: Busy=1 Ready=0 ROB_ID=32 Op=0x00033 Src1_Valid=0 Src1_Tag=31 Src1_Value=0x00000000 Src2_Valid=0 Src2_Tag=27
Src2_Value=0x00000000
[225000] ALU_RS[4]: Busy=1 Ready=0 ROB_ID=27 Op=0x00033 Src1_Valid=1 Src1_Tag=13 Src1_Value=0x00000003 Src2_Valid=1 Src2_Tag=19
Src2_Value=0x00000003
[225000] ALU_RS[8]: Busy=1 Ready=0 ROB_ID=28 Op=0x00033 Src1_Valid=1 Src1_Tag=13 Src1_Value=0x00000003 Src2_Valid=0 Src2_Tag=22
Src2_Value=0x00000000
[225000] ALU_RS[9]: Busy=1 Ready=0 ROB_ID=21 Op=0x00133 Src1_Valid=1 Src1_Tag=19 Src1_Value=0x00000003 Src2_Valid=1 Src2_Tag=17
Src2_Value=0x00000006
[225000] ALU_RS[10]: Busy=1 Ready=0 ROB_ID=22 Op=0x00033 Src1_Valid=1 Src1_Tag=13 Src1_Value=0x00000003 Src2_Valid=1 Src2_Tag=19
Src2_Value=0x00000003
[225000] ALU_RS[11]: Busy=1 Ready=0 ROB_ID=29 Op=0x00033 Src1_Valid=0 Src1_Tag=27 Src1_Value=0x00000000 Src2_Valid=0 Src2_Tag=28
Src2_Value=0x00000000
[225000] --- Mul/Div Reservation Stations ---
[225000] MD_RS[0]: Busy=1 Ready=0 ROB_ID=30 Op=0x00433 Src1_Valid=0 Src1_Tag=27 Src1_Value=0x00000000 Src2_Valid=0 Src2_Tag=29
Src2_Value=0x00000000

[225000] ===== FORWARDING MESSAGES =====
[225000] FORWARD[INTRA_SRC1]: DISPATCH[1] ROB_ID=31 -> DISPATCH[2] ROB_ID=32 Reg=7

[225000] ===== INSTRUCTIONS COMMITTED THIS CYCLE =====
[225000] COMMITTED[0]: ROB_ID=19
[225000] COMMITTED[1]: ROB_ID=20
[225000] Total Instructions Committed This Cycle: 2

[225000] ===== CURRENT RAT AND VALID =====
[225000] RAT[1]: Tag=27 Valid=1
[225000] RAT[2]: Tag=28 Valid=1
[225000] RAT[3]: Tag=29 Valid=1
[225000] RAT[6]: Tag=23 Valid=1
[225000] RAT[7]: Tag=31 Valid=1
[225000] RAT[8]: Tag=30 Valid=1
[225000] RAT[11]: Tag=22 Valid=1
[225000] RAT[14]: Tag=21 Valid=1

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[225000] RAT[18]: Tag=24 Valid=1
[225000] RAT[19]: Tag=25 Valid=1
[225000] RAT[29]: Tag=32 Valid=1

[225000] ===== ARCHITECTURAL REGISTER FILE (ARF) =====

[225000] ARF[1]: Value=0x00000001
[225000] ARF[2]: Value=0x00000002
[225000] ARF[3]: Value=0x00000002
[225000] ARF[4]: Value=0x00000004
[225000] ARF[7]: Value=0x00000003
[225000] ARF[9]: Value=0x00000003
[225000] ARF[10]: Value=0x00000003
[225000] ARF[11]: Value=0x00000003
[225000] ARF[12]: Value=0x00000006
[225000] ARF[15]: Value=0x00000003
[225000] ARF Checker: PASS - ROB[19] sub x10, x12, x11 -> x10 = 3
[225000] ARF Checker: PASS - ROB[20] and x13, x18, x19 -> x13 = 0

[235000] ===== DECODE/DISPATCH STAGE =====

[235000] DECODE[0]: PC=0x00000078 Instr=0x02308433 Type=2 Dst=8 Src1=1 Src2=3 Opcode=0x33 Func3=0x0 Func7=0x01 Operation=0x00433
Imm=0x00000000
[235000] DECODE[1]: PC=0x0000007c Instr=0x0020e3b3 Type=0 Dst=7 Src1=1 Src2=2 Opcode=0x33 Func3=0x6 Func7=0x00 Operation=0x00333
Imm=0x00000000
[235000] DECODE[2]: PC=0x00000080 Instr=0x00138eb3 Type=0 Dst=29 Src1=7 Src2=1 Opcode=0x33 Func3=0x0 Func7=0x00 Operation=0x00033
Imm=0x00000000
[235000] DISPATCH[0]: ROB_ID=30 RS_ID=0 RS_Alloc=1 Src1_Ready=0 Src2_Ready=0 Dst=8 Src1=1 Src2=3 Src1_Tag=27 Src2_Tag=29
Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00433 Type=2 PC=0x00000078 Instr=0x02308433
[235000] DISPATCH[1]: ROB_ID=31 RS_ID=0 RS_Alloc=1 Src1_Ready=0 Src2_Ready=0 Dst=7 Src1=1 Src2=2 Src1_Tag=27 Src2_Tag=28
Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00333 Type=0 PC=0x0000007c Instr=0x0020e3b3
[235000] DISPATCH[2]: ROB_ID=32 RS_ID=2 RS_Alloc=1 Src1_Ready=0 Src2_Ready=0 Dst=29 Src1=7 Src2=1 Src1_Tag=31 Src2_Tag=27
Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00033 Type=0 PC=0x00000080 Instr=0x00138eb3

[235000] ===== REORDER BUFFER (ROB) =====

[235000] ROB Head: 33, ROB Tail: 21
[235000] ROB[21]: Valid=1 Ready=0 Dest=14 Value=0x00000000 Instr_ID=21 PC=0x00000054
[235000] ROB[22]: Valid=1 Ready=0 Dest=11 Value=0x00000000 Instr_ID=22 PC=0x00000058
[235000] ROB[23]: Valid=1 Ready=0 Dest=6 Value=0x00000000 Instr_ID=23 PC=0x0000005c
[235000] ROB[24]: Valid=1 Ready=1 Dest=18 Value=0x00000003 Instr_ID=24 PC=0x00000060
[235000] ROB[25]: Valid=1 Ready=1 Dest=19 Value=0x00000005 Instr_ID=25 PC=0x00000064
[235000] ROB[26]: Valid=1 Ready=1 Dest=0 Value=0x00000000 Instr_ID=26 PC=0x00000068
[235000] ROB[27]: Valid=1 Ready=0 Dest=1 Value=0x00000000 Instr_ID=27 PC=0x0000006c
[235000] ROB[28]: Valid=1 Ready=0 Dest=2 Value=0x00000000 Instr_ID=28 PC=0x00000070
[235000] ROB[29]: Valid=1 Ready=0 Dest=3 Value=0x00000000 Instr_ID=29 PC=0x00000074
[235000] ROB[30]: Valid=1 Ready=0 Dest=8 Value=0x00000000 Instr_ID=30 PC=0x00000078
[235000] ROB[31]: Valid=1 Ready=0 Dest=7 Value=0x00000000 Instr_ID=31 PC=0x0000007c
[235000] ROB[32]: Valid=1 Ready=0 Dest=29 Value=0x00000000 Instr_ID=0 PC=0x00000080

[235000] ===== RESERVATION STATIONS =====

[235000] --- ALU Reservation Stations ---
[235000] ALU_RS[0]: Busy=1 Ready=0 ROB_ID=31 Op=0x00333 Src1_Valid=0 Src1_Tag=27 Src1_Value=0x00000000 Src2_Valid=0 Src2_Tag=28
Src2_Value=0x00000000
[235000] ALU_RS[2]: Busy=1 Ready=0 ROB_ID=32 Op=0x00033 Src1_Valid=0 Src1_Tag=31 Src1_Value=0x00000000 Src2_Valid=0 Src2_Tag=27
Src2_Value=0x00000000
[235000] ALU_RS[4]: Busy=1 Ready=1 ROB_ID=27 Op=0x00033 Src1_Valid=1 Src1_Tag=13 Src1_Value=0x00000003 Src2_Valid=1 Src2_Tag=19
Src2_Value=0x00000003
[235000] ALU_RS[8]: Busy=1 Ready=0 ROB_ID=28 Op=0x00033 Src1_Valid=1 Src1_Tag=13 Src1_Value=0x00000003 Src2_Valid=0 Src2_Tag=22
Src2_Value=0x00000000
[235000] ALU_RS[9]: Busy=1 Ready=1 ROB_ID=21 Op=0x00133 Src1_Valid=1 Src1_Tag=19 Src1_Value=0x00000003 Src2_Valid=1 Src2_Tag=17
Src2_Value=0x00000006
[235000] ALU_RS[10]: Busy=1 Ready=1 ROB_ID=22 Op=0x00033 Src1_Valid=1 Src1_Tag=13 Src1_Value=0x00000003 Src2_Valid=1 Src2_Tag=19
Src2_Value=0x00000003
[235000] ALU_RS[11]: Busy=1 Ready=0 ROB_ID=29 Op=0x00033 Src1_Valid=0 Src1_Tag=27 Src1_Value=0x00000000 Src2_Valid=0 Src2_Tag=28
Src2_Value=0x00000000
[235000] --- Mul/Div Reservation Stations ---

[235000] MD_RS[0]: Busy=1 Ready=0 ROB_ID=30 Op=0x00433 Src1_Valid=0 Src1_Tag=27 Src1_Value=0x00000000 Src2_Valid=0 Src2_Tag=29 Src2_Value=0x00000000

[235000] ===== EXECUTION STAGE (CDB INPUT) =====

[235000] CDB[0]: ROB_ID=21 Result=0x00000001 Ready=1

[235000] CDB[1]: ROB_ID=22 Result=0x00000006 Ready=1

[235000] CDB[2]: ROB_ID=27 Result=0x00000006 Ready=1

[235000] ===== FORWARDING MESSAGES =====

[235000] FORWARD[CDB_CURR->ALU_SRC2]: CDB[1] ROB_ID=22 -> ALU_RS[8] ROB_ID=28 Value=0x00000006

[235000] FORWARD[CDB_CURR->ALU_SRC1]: CDB[2] ROB_ID=27 -> ALU_RS[0] ROB_ID=31 Value=0x00000006

[235000] FORWARD[CDB_CURR->ALU_SRC2]: CDB[2] ROB_ID=27 -> ALU_RS[2] ROB_ID=32 Value=0x00000006

[235000] FORWARD[CDB_CURR->ALU_SRC1]: CDB[2] ROB_ID=27 -> ALU_RS[11] ROB_ID=29 Value=0x00000006

[235000] FORWARD[CDB_CURR->MD_SRC1]: CDB[2] ROB_ID=27 -> MD_RS[0] ROB_ID=30 Value=0x00000006

[235000] FORWARD[RETIRE_CURR->ALU_SRC2]: RETIRE_CURR[1] ROB_ID=22 -> ALU_RS[8] ROB_ID=28 Value=0x00000006

[235000] FORWARD[INTRA_SRC1]: DISPATCH[1] ROB_ID=31 -> DISPATCH[2] ROB_ID=32 Reg=7

[235000] ===== CURRENT RAT AND VALID =====

[235000] RAT[1]: Tag=27 Valid=1

[235000] RAT[2]: Tag=28 Valid=1

[235000] RAT[3]: Tag=29 Valid=1

[235000] RAT[6]: Tag=23 Valid=1

[235000] RAT[7]: Tag=31 Valid=1

[235000] RAT[8]: Tag=30 Valid=1

[235000] RAT[11]: Tag=22 Valid=1

[235000] RAT[14]: Tag=21 Valid=1

[235000] RAT[18]: Tag=24 Valid=1

[235000] RAT[19]: Tag=25 Valid=1

[235000] RAT[29]: Tag=32 Valid=1

[235000] ===== ARCHITECTURAL REGISTER FILE (ARF) =====

[235000] ARF[1]: Value=0x00000001

[235000] ARF[2]: Value=0x00000002

[235000] ARF[3]: Value=0x00000002

[235000] ARF[4]: Value=0x00000004

[235000] ARF[7]: Value=0x00000003

[235000] ARF[9]: Value=0x00000003

[235000] ARF[10]: Value=0x00000003

[235000] ARF[11]: Value=0x00000003

[235000] ARF[12]: Value=0x00000006

[235000] ARF[15]: Value=0x00000003

[245000] ===== DECODE/DISPATCH STAGE =====

[245000] DECODE[0]: PC=0x00000078 Instr=0x02308433 Type=2 Dst=8 Src1=1 Src2=3 Opcode=0x33 Func3=0x0 Func7=0x01 Operation=0x00433 Imm=0x00000000

[245000] DECODE[1]: PC=0x0000007c Instr=0x0020e3b3 Type=0 Dst=7 Src1=1 Src2=2 Opcode=0x33 Func3=0x6 Func7=0x00 Operation=0x00333 Imm=0x00000000

[245000] DECODE[2]: PC=0x00000080 Instr=0x00138eb3 Type=0 Dst=29 Src1=7 Src2=1 Opcode=0x33 Func3=0x0 Func7=0x00 Operation=0x00033 Imm=0x00000000

[245000] DISPATCH[0]: ROB_ID=30 RS_ID=0 RS_Alloc=1 Src1_Ready=0 Src2_Ready=0 Dst=8 Src1=1 Src2=3 Src1_Tag=27 Src2_Tag=29 Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00433 Type=2 PC=0x00000078 Instr=0x02308433

[245000] DISPATCH[1]: ROB_ID=31 RS_ID=0 RS_Alloc=1 Src1_Ready=0 Src2_Ready=0 Dst=7 Src1=1 Src2=2 Src1_Tag=27 Src2_Tag=28 Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00333 Type=0 PC=0x0000007c Instr=0x0020e3b3

[245000] DISPATCH[2]: ROB_ID=32 RS_ID=2 RS_Alloc=1 Src1_Ready=0 Src2_Ready=0 Dst=29 Src1=7 Src2=1 Src1_Tag=31 Src2_Tag=27 Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00033 Type=0 PC=0x00000080 Instr=0x00138eb3

[245000] ===== REORDER BUFFER (ROB) =====

[245000] ROB Head: 33, ROB Tail: 23

[245000] ROB[23]: Valid=1 Ready=0 Dest=6 Value=0x00000000 Instr_ID=23 PC=0x0000005c

[245000] ROB[24]: Valid=1 Ready=1 Dest=18 Value=0x00000003 Instr_ID=24 PC=0x00000060

[245000] ROB[25]: Valid=1 Ready=1 Dest=19 Value=0x00000005 Instr_ID=25 PC=0x00000064

[245000] ROB[26]: Valid=1 Ready=1 Dest=0 Value=0x00000000 Instr_ID=26 PC=0x00000068

[245000] ROB[27]: Valid=1 Ready=1 Dest=1 Value=0x00000006 Instr_ID=27 PC=0x0000006c

[245000] ROB[28]: Valid=1 Ready=0 Dest=2 Value=0x00000000 Instr_ID=28 PC=0x00000070

[245000] ROB[29]: Valid=1 Ready=0 Dest=3 Value=0x00000000 Instr_ID=29 PC=0x00000074

[245000] ROB[30]: Valid=1 Ready=0 Dest=8 Value=0x00000000 Instr_ID=30 PC=0x00000078
[245000] ROB[31]: Valid=1 Ready=0 Dest=7 Value=0x00000000 Instr_ID=31 PC=0x0000007c
[245000] ROB[32]: Valid=1 Ready=0 Dest=29 Value=0x00000000 Instr_ID=0 PC=0x00000080

[245000] ===== RESERVATION STATIONS =====

[245000] --- ALU Reservation Stations ---

[245000] ALU_RS[0]: Busy=1 Ready=0 ROB_ID=31 Op=0x00333 Src1_Valid=1 Src1_Tag=27 Src1_Value=0x00000006 Src2_Valid=0 Src2_Tag=28 Src2_Value=0x00000000

[245000] ALU_RS[2]: Busy=1 Ready=0 ROB_ID=32 Op=0x00033 Src1_Valid=0 Src1_Tag=31 Src1_Value=0x00000000 Src2_Valid=1 Src2_Tag=27 Src2_Value=0x00000006

[245000] ALU_RS[8]: Busy=1 Ready=0 ROB_ID=28 Op=0x00033 Src1_Valid=1 Src1_Tag=13 Src1_Value=0x00000003 Src2_Valid=1 Src2_Tag=22 Src2_Value=0x00000006

[245000] ALU_RS[11]: Busy=1 Ready=0 ROB_ID=29 Op=0x00033 Src1_Valid=1 Src1_Tag=27 Src1_Value=0x00000006 Src2_Valid=0 Src2_Tag=28 Src2_Value=0x00000000

[245000] --- Mul/Div Reservation Stations ---

[245000] MD_RS[0]: Busy=1 Ready=0 ROB_ID=30 Op=0x00433 Src1_Valid=1 Src1_Tag=27 Src1_Value=0x00000006 Src2_Valid=0 Src2_Tag=29 Src2_Value=0x00000000

[245000] ===== FORWARDING MESSAGES =====

[245000] FORWARD[INTRA_SRC1]: DISPATCH[1] ROB_ID=31 -> DISPATCH[2] ROB_ID=32 Reg=7

[245000] ===== INSTRUCTIONS COMMITTED THIS CYCLE =====

[245000] COMMITTED[0]: ROB_ID=21

[245000] COMMITTED[1]: ROB_ID=22

[245000] Total Instructions Committed This Cycle: 2

[245000] ===== CURRENT RAT AND VALID =====

[245000] RAT[1]: Tag=27 Valid=1

[245000] RAT[2]: Tag=28 Valid=1

[245000] RAT[3]: Tag=29 Valid=1

[245000] RAT[6]: Tag=23 Valid=1

[245000] RAT[7]: Tag=31 Valid=1

[245000] RAT[8]: Tag=30 Valid=1

[245000] RAT[18]: Tag=24 Valid=1

[245000] RAT[19]: Tag=25 Valid=1

[245000] RAT[29]: Tag=32 Valid=1

[245000] ===== ARCHITECTURAL REGISTER FILE (ARF) =====

[245000] ARF[1]: Value=0x00000001

[245000] ARF[2]: Value=0x00000002

[245000] ARF[3]: Value=0x00000002

[245000] ARF[4]: Value=0x00000004

[245000] ARF[7]: Value=0x00000003

[245000] ARF[9]: Value=0x00000003

[245000] ARF[10]: Value=0x00000003

[245000] ARF[11]: Value=0x00000006

[245000] ARF[12]: Value=0x00000006

[245000] ARF[14]: Value=0x00000001

[245000] ARF[15]: Value=0x00000003

[245000] ARF Checker: PASS - ROB[21] slt x14, x10, x12 -> x14 = 1

[245000] ARF Checker: PASS - ROB[22] add x11, x9, x10 -> x11 = 6

[255000] ===== DECODE/DISPATCH STAGE =====

[255000] DECODE[0]: PC=0x00000078 Instr=0x02308433 Type=2 Dst=8 Src1=1 Src2=3 Opcode=0x33 Func3=0x0 Func7=0x01 Operation=0x00433 Imm=0x00000000

[255000] DECODE[1]: PC=0x0000007c Instr=0x0020e3b3 Type=0 Dst=7 Src1=1 Src2=2 Opcode=0x33 Func3=0x6 Func7=0x00 Operation=0x00333 Imm=0x00000000

[255000] DECODE[2]: PC=0x00000080 Instr=0x00138eb3 Type=0 Dst=29 Src1=7 Src2=1 Opcode=0x33 Func3=0x0 Func7=0x00 Operation=0x00033 Imm=0x00000000

[255000] DISPATCH[0]: ROB_ID=30 RS_ID=0 RS_Alloc=1 Src1_Ready=0 Src2_Ready=0 Dst=8 Src1=1 Src2=3 Src1_Tag=27 Src2_Tag=29 Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00433 Type=2 PC=0x00000078 Instr=0x02308433

[255000] DISPATCH[1]: ROB_ID=31 RS_ID=0 RS_Alloc=1 Src1_Ready=0 Src2_Ready=0 Dst=7 Src1=1 Src2=2 Src1_Tag=27 Src2_Tag=28 Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00333 Type=0 PC=0x0000007c Instr=0x0020e3b3

[255000] DISPATCH[2]: ROB_ID=32 RS_ID=2 RS_Alloc=1 Src1_Ready=0 Src2_Ready=0 Dst=29 Src1=7 Src2=1 Src1_Tag=31 Src2_Tag=27 Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00033 Type=0 PC=0x00000080 Instr=0x00138eb3

[255000] ===== REORDER BUFFER (ROB) =====

[255000] ROB Head: 33, ROB Tail: 23

[255000] ROB[23]: Valid=1 Ready=0 Dest=6 Value=0x00000000 Instr_ID=23 PC=0x0000005c
[255000] ROB[24]: Valid=1 Ready=1 Dest=18 Value=0x00000003 Instr_ID=24 PC=0x00000060
[255000] ROB[25]: Valid=1 Ready=1 Dest=19 Value=0x00000005 Instr_ID=25 PC=0x00000064
[255000] ROB[26]: Valid=1 Ready=1 Dest=0 Value=0x00000000 Instr_ID=26 PC=0x00000068
[255000] ROB[27]: Valid=1 Ready=1 Dest=1 Value=0x00000006 Instr_ID=27 PC=0x0000006c
[255000] ROB[28]: Valid=1 Ready=0 Dest=2 Value=0x00000000 Instr_ID=28 PC=0x00000070
[255000] ROB[29]: Valid=1 Ready=0 Dest=3 Value=0x00000000 Instr_ID=29 PC=0x00000074
[255000] ROB[30]: Valid=1 Ready=0 Dest=8 Value=0x00000000 Instr_ID=30 PC=0x00000078
[255000] ROB[31]: Valid=1 Ready=0 Dest=7 Value=0x00000000 Instr_ID=31 PC=0x0000007c
[255000] ROB[32]: Valid=1 Ready=0 Dest=29 Value=0x00000000 Instr_ID=0 PC=0x00000080

[255000] ===== RESERVATION STATIONS =====

[255000] --- ALU Reservation Stations ---

[255000] ALU_RS[0]: Busy=1 Ready=0 ROB_ID=31 Op=0x00333 Src1_Valid=1 Src1_Tag=27 Src1_Value=0x00000006 Src2_Valid=0 Src2_Tag=28 Src2_Value=0x00000000
[255000] ALU_RS[2]: Busy=1 Ready=0 ROB_ID=32 Op=0x00033 Src1_Valid=0 Src1_Tag=31 Src1_Value=0x00000000 Src2_Valid=1 Src2_Tag=27 Src2_Value=0x00000006
[255000] ALU_RS[8]: Busy=1 Ready=1 ROB_ID=28 Op=0x00033 Src1_Valid=1 Src1_Tag=13 Src1_Value=0x00000003 Src2_Valid=1 Src2_Tag=22 Src2_Value=0x00000006
[255000] ALU_RS[11]: Busy=1 Ready=0 ROB_ID=29 Op=0x00033 Src1_Valid=1 Src1_Tag=27 Src1_Value=0x00000006 Src2_Valid=0 Src2_Tag=28 Src2_Value=0x00000000
[255000] --- Mul/Div Reservation Stations ---
[255000] MD_RS[0]: Busy=1 Ready=0 ROB_ID=30 Op=0x00433 Src1_Valid=1 Src1_Tag=27 Src1_Value=0x00000006 Src2_Valid=0 Src2_Tag=29 Src2_Value=0x00000000

[255000] ===== EXECUTION STAGE (CDB INPUT) =====

[255000] CDB[0]: ROB_ID=28 Result=0x00000009 Ready=1

[255000] ===== FORWARDING MESSAGES =====

[255000] FORWARD[CDB_CURR->ALU_SRC2]: CDB[0] ROB_ID=28 -> ALU_RS[0] ROB_ID=31 Value=0x00000009
[255000] FORWARD[CDB_CURR->ALU_SRC2]: CDB[0] ROB_ID=28 -> ALU_RS[11] ROB_ID=29 Value=0x00000009
[255000] FORWARD[INTRA_SRC1]: DISPATCH[1] ROB_ID=31 -> DISPATCH[2] ROB_ID=32 Reg=7

[255000] ===== CURRENT RAT AND VALID =====

[255000] RAT[1]: Tag=27 Valid=1
[255000] RAT[2]: Tag=28 Valid=1
[255000] RAT[3]: Tag=29 Valid=1
[255000] RAT[6]: Tag=23 Valid=1
[255000] RAT[7]: Tag=31 Valid=1
[255000] RAT[8]: Tag=30 Valid=1
[255000] RAT[18]: Tag=24 Valid=1
[255000] RAT[19]: Tag=25 Valid=1
[255000] RAT[29]: Tag=32 Valid=1

[255000] ===== ARCHITECTURAL REGISTER FILE (ARF) =====

[255000] ARF[1]: Value=0x00000001
[255000] ARF[2]: Value=0x00000002
[255000] ARF[3]: Value=0x00000002
[255000] ARF[4]: Value=0x00000004
[255000] ARF[7]: Value=0x00000003
[255000] ARF[9]: Value=0x00000003
[255000] ARF[10]: Value=0x00000003
[255000] ARF[11]: Value=0x00000006
[255000] ARF[12]: Value=0x00000006
[255000] ARF[14]: Value=0x00000001
[255000] ARF[15]: Value=0x00000003

[265000] ===== DECODE/DISPATCH STAGE =====

[265000] DECODE[0]: PC=0x00000078 Instr=0x02308433 Type=2 Dst=8 Src1=1 Src2=3 Opcode=0x33 Func3=0x0 Func7=0x01 Operation=0x00433 Imm=0x00000000
[265000] DECODE[1]: PC=0x0000007c Instr=0x0020e3b3 Type=0 Dst=7 Src1=1 Src2=2 Opcode=0x33 Func3=0x6 Func7=0x00 Operation=0x00333 Imm=0x00000000

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[265000] DECODE[2]: PC=0x00000080 Instr=0x00138eb3 Type=0 Dst=29 Src1=7 Src2=1 Opcode=0x33 Func3=0x0 Func7=0x00 Operation=0x00033
Imm=0x00000000
[265000] DISPATCH[0]: ROB_ID=30 RS_ID=0 RS_Alloc=1 Src1_Ready=0 Src2_Ready=0 Dst=8 Src1=1 Src2=3 Src1_Tag=27 Src2_Tag=29
Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00433 Type=2 PC=0x00000078 Instr=0x02308433
[265000] DISPATCH[1]: ROB_ID=31 RS_ID=0 RS_Alloc=1 Src1_Ready=0 Src2_Ready=0 Dst=7 Src1=1 Src2=2 Src1_Tag=27 Src2_Tag=28
Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00333 Type=0 PC=0x0000007c Instr=0x0020e3b3
[265000] DISPATCH[2]: ROB_ID=32 RS_ID=2 RS_Alloc=1 Src1_Ready=0 Src2_Ready=0 Dst=29 Src1=7 Src2=1 Src1_Tag=31 Src2_Tag=27
Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00033 Type=0 PC=0x00000080 Instr=0x00138eb3

[265000] ===== REORDER BUFFER (ROB) =====
[265000] ROB Head: 33, ROB Tail: 23
[265000] ROB[23]: Valid=1 Ready=0 Dest=6 Value=0x00000000 Instr_ID=23 PC=0x0000005c
[265000] ROB[24]: Valid=1 Ready=1 Dest=18 Value=0x00000003 Instr_ID=24 PC=0x00000060
[265000] ROB[25]: Valid=1 Ready=1 Dest=19 Value=0x00000005 Instr_ID=25 PC=0x00000064
[265000] ROB[26]: Valid=1 Ready=1 Dest=0 Value=0x00000000 Instr_ID=26 PC=0x00000068
[265000] ROB[27]: Valid=1 Ready=1 Dest=1 Value=0x00000006 Instr_ID=27 PC=0x0000006c
[265000] ROB[28]: Valid=1 Ready=1 Dest=2 Value=0x00000009 Instr_ID=28 PC=0x00000070
[265000] ROB[29]: Valid=1 Ready=0 Dest=3 Value=0x00000000 Instr_ID=29 PC=0x00000074
[265000] ROB[30]: Valid=1 Ready=0 Dest=8 Value=0x00000000 Instr_ID=30 PC=0x00000078
[265000] ROB[31]: Valid=1 Ready=0 Dest=7 Value=0x00000000 Instr_ID=31 PC=0x0000007c
[265000] ROB[32]: Valid=1 Ready=0 Dest=29 Value=0x00000000 Instr_ID=0 PC=0x00000080

[265000] ===== RESERVATION STATIONS =====
[265000] --- ALU Reservation Stations ---
[265000] ALU_RS[0]: Busy=1 Ready=0 ROB_ID=31 Op=0x00333 Src1_Valid=1 Src1_Tag=27 Src1_Value=0x00000006 Src2_Valid=1 Src2_Tag=28
Src2_Value=0x00000009
[265000] ALU_RS[2]: Busy=1 Ready=0 ROB_ID=32 Op=0x00033 Src1_Valid=0 Src1_Tag=31 Src1_Value=0x00000000 Src2_Valid=1 Src2_Tag=27
Src2_Value=0x00000006
[265000] ALU_RS[11]: Busy=1 Ready=0 ROB_ID=29 Op=0x00033 Src1_Valid=1 Src1_Tag=27 Src1_Value=0x00000006 Src2_Valid=1 Src2_Tag=28
Src2_Value=0x00000009
[265000] --- Mul/Div Reservation Stations ---
[265000] MD_RS[0]: Busy=1 Ready=0 ROB_ID=30 Op=0x00433 Src1_Valid=1 Src1_Tag=27 Src1_Value=0x00000006 Src2_Valid=0 Src2_Tag=29
Src2_Value=0x00000000

[265000] ===== FORWARDING MESSAGES =====
[265000] FORWARD[INTRA_SRC1]: DISPATCH[1] ROB_ID=31 -> DISPATCH[2] ROB_ID=32 Reg=7

[265000] ===== CURRENT RAT AND VALID =====
[265000] RAT[1]: Tag=27 Valid=1
[265000] RAT[2]: Tag=28 Valid=1
[265000] RAT[3]: Tag=29 Valid=1
[265000] RAT[6]: Tag=23 Valid=1
[265000] RAT[7]: Tag=31 Valid=1
[265000] RAT[8]: Tag=30 Valid=1
[265000] RAT[18]: Tag=24 Valid=1
[265000] RAT[19]: Tag=25 Valid=1
[265000] RAT[29]: Tag=32 Valid=1

[265000] ===== ARCHITECTURAL REGISTER FILE (ARF) =====
[265000] ARF[1]: Value=0x00000001
[265000] ARF[2]: Value=0x00000002
[265000] ARF[3]: Value=0x00000002
[265000] ARF[4]: Value=0x00000004
[265000] ARF[7]: Value=0x00000003
[265000] ARF[9]: Value=0x00000003
[265000] ARF[10]: Value=0x00000003
[265000] ARF[11]: Value=0x00000006
[265000] ARF[12]: Value=0x00000006
[265000] ARF[14]: Value=0x00000001
[265000] ARF[15]: Value=0x00000003

[275000] ===== DECODE/DISPATCH STAGE =====
[275000] DECODE[0]: PC=0x00000078 Instr=0x02308433 Type=2 Dst=8 Src1=1 Src2=3 Opcode=0x33 Func3=0x0 Func7=0x01 Operation=0x00433
Imm=0x00000000

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[275000] DECODE[1]: PC=0x0000007c Instr=0x0020e3b3 Type=0 Dst=7 Src1=1 Src2=2 Opcode=0x33 Func3=0x6 Func7=0x00 Operation=0x00333
Imm=0x00000000
[275000] DECODE[2]: PC=0x00000080 Instr=0x00138eb3 Type=0 Dst=29 Src1=7 Src2=1 Opcode=0x33 Func3=0x0 Func7=0x00 Operation=0x00033
Imm=0x00000000
[275000] DISPATCH[0]: ROB_ID=30 RS_ID=0 RS_Alloc=1 Src1_Ready=0 Src2_Ready=0 Dst=8 Src1=1 Src2=3 Src1_Tag=27 Src2_Tag=29
Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00433 Type=2 PC=0x00000078 Instr=0x02308433
[275000] DISPATCH[1]: ROB_ID=31 RS_ID=0 RS_Alloc=1 Src1_Ready=0 Src2_Ready=0 Dst=7 Src1=1 Src2=2 Src1_Tag=27 Src2_Tag=28
Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00333 Type=0 PC=0x0000007c Instr=0x0020e3b3
[275000] DISPATCH[2]: ROB_ID=32 RS_ID=2 RS_Alloc=1 Src1_Ready=0 Src2_Ready=0 Dst=29 Src1=7 Src2=1 Src1_Tag=31 Src2_Tag=27
Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00033 Type=0 PC=0x00000080 Instr=0x00138eb3

[275000] ===== REORDER BUFFER (ROB) =====
[275000] ROB Head: 33, ROB Tail: 23
[275000] ROB[23]: Valid=1 Ready=0 Dest=6 Value=0x00000000 Instr_ID=23 PC=0x0000005c
[275000] ROB[24]: Valid=1 Ready=1 Dest=18 Value=0x00000003 Instr_ID=24 PC=0x00000060
[275000] ROB[25]: Valid=1 Ready=1 Dest=19 Value=0x00000005 Instr_ID=25 PC=0x00000064
[275000] ROB[26]: Valid=1 Ready=1 Dest=0 Value=0x00000000 Instr_ID=26 PC=0x00000068
[275000] ROB[27]: Valid=1 Ready=1 Dest=1 Value=0x00000006 Instr_ID=27 PC=0x0000006c
[275000] ROB[28]: Valid=1 Ready=1 Dest=2 Value=0x00000009 Instr_ID=28 PC=0x00000070
[275000] ROB[29]: Valid=1 Ready=0 Dest=3 Value=0x00000000 Instr_ID=29 PC=0x00000074
[275000] ROB[30]: Valid=1 Ready=0 Dest=8 Value=0x00000000 Instr_ID=30 PC=0x00000078
[275000] ROB[31]: Valid=1 Ready=0 Dest=7 Value=0x00000000 Instr_ID=31 PC=0x0000007c
[275000] ROB[32]: Valid=1 Ready=0 Dest=29 Value=0x00000000 Instr_ID=0 PC=0x00000080

[275000] ===== RESERVATION STATIONS =====
[275000] --- ALU Reservation Stations ---
[275000] ALU_RS[0]: Busy=1 Ready=1 ROB_ID=31 Op=0x00333 Src1_Valid=1 Src1_Tag=27 Src1_Value=0x00000006 Src2_Valid=1 Src2_Tag=28
Src2_Value=0x00000009
[275000] ALU_RS[2]: Busy=1 Ready=0 ROB_ID=32 Op=0x00033 Src1_Valid=0 Src1_Tag=31 Src1_Value=0x00000000 Src2_Valid=1 Src2_Tag=27
Src2_Value=0x00000006
[275000] ALU_RS[11]: Busy=1 Ready=1 ROB_ID=29 Op=0x00033 Src1_Valid=1 Src1_Tag=27 Src1_Value=0x00000006 Src2_Valid=1 Src2_Tag=28
Src2_Value=0x00000009
[275000] --- Mul/Div Reservation Stations ---
[275000] MD_RS[0]: Busy=1 Ready=0 ROB_ID=30 Op=0x00433 Src1_Valid=1 Src1_Tag=27 Src1_Value=0x00000006 Src2_Valid=0 Src2_Tag=29
Src2_Value=0x00000000

[275000] ===== EXECUTION STAGE (CDB INPUT) =====
[275000] CDB[0]: ROB_ID=29 Result=0x0000000f Ready=1
[275000] CDB[1]: ROB_ID=31 Result=0x0000000f Ready=1

[275000] ===== FORWARDING MESSAGES =====
[275000] FORWARD[CDB_CURR->MD_SRC2]: CDB[0] ROB_ID=29 -> MD_RS[0] ROB_ID=30 Value=0x0000000f
[275000] FORWARD[CDB_CURR->ALU_SRC1]: CDB[1] ROB_ID=31 -> ALU_RS[2] ROB_ID=32 Value=0x0000000f
[275000] FORWARD[INTRA_SRC1]: DISPATCH[1] ROB_ID=31 -> DISPATCH[2] ROB_ID=32 Reg=7

[275000] ===== CURRENT RAT AND VALID =====
[275000] RAT[1]: Tag=27 Valid=1
[275000] RAT[2]: Tag=28 Valid=1
[275000] RAT[3]: Tag=29 Valid=1
[275000] RAT[6]: Tag=23 Valid=1
[275000] RAT[7]: Tag=31 Valid=1
[275000] RAT[8]: Tag=30 Valid=1
[275000] RAT[18]: Tag=24 Valid=1
[275000] RAT[19]: Tag=25 Valid=1
[275000] RAT[29]: Tag=32 Valid=1

[275000] ===== ARCHITECTURAL REGISTER FILE (ARF) =====
[275000] ARF[1]: Value=0x00000001
[275000] ARF[2]: Value=0x00000002
[275000] ARF[3]: Value=0x00000002
[275000] ARF[4]: Value=0x00000004
[275000] ARF[7]: Value=0x00000003
[275000] ARF[9]: Value=0x00000003
[275000] ARF[10]: Value=0x00000003
[275000] ARF[11]: Value=0x00000006

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[275000] ARF[12]: Value=0x00000006
[275000] ARF[14]: Value=0x00000001
[275000] ARF[15]: Value=0x00000003

[285000] ===== DECODE/DISPATCH STAGE =====

[285000] DECODE[0]: PC=0x00000078 Instr=0x02308433 Type=2 Dst=8 Src1=1 Src2=3 Opcode=0x33 Func3=0x0 Func7=0x01 Operation=0x00433 Imm=0x00000000
[285000] DECODE[1]: PC=0x0000007c Instr=0x0020e3b3 Type=0 Dst=7 Src1=1 Src2=2 Opcode=0x33 Func3=0x6 Func7=0x00 Operation=0x00333 Imm=0x00000000
[285000] DECODE[2]: PC=0x00000080 Instr=0x00138eb3 Type=0 Dst=29 Src1=7 Src2=1 Opcode=0x33 Func3=0x0 Func7=0x00 Operation=0x00033 Imm=0x00000000
[285000] DISPATCH[0]: ROB_ID=30 RS_ID=0 RS_Alloc=1 Src1_Ready=0 Src2_Ready=0 Dst=8 Src1=1 Src2=3 Src1_Tag=27 Src2_Tag=29 Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00433 Type=2 PC=0x00000078 Instr=0x02308433
[285000] DISPATCH[1]: ROB_ID=31 RS_ID=0 RS_Alloc=1 Src1_Ready=0 Src2_Ready=0 Dst=7 Src1=1 Src2=2 Src1_Tag=27 Src2_Tag=28 Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00333 Type=0 PC=0x0000007c Instr=0x0020e3b3
[285000] DISPATCH[2]: ROB_ID=32 RS_ID=2 RS_Alloc=1 Src1_Ready=0 Src2_Ready=0 Dst=29 Src1=7 Src2=1 Src1_Tag=31 Src2_Tag=27 Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00033 Type=0 PC=0x00000080 Instr=0x00138eb3

[285000] ===== REORDER BUFFER (ROB) =====

[285000] ROB Head: 33, ROB Tail: 23
[285000] ROB[23]: Valid=1 Ready=0 Dest=6 Value=0x00000000 Instr_ID=23 PC=0x0000005c
[285000] ROB[24]: Valid=1 Ready=1 Dest=18 Value=0x00000003 Instr_ID=24 PC=0x00000060
[285000] ROB[25]: Valid=1 Ready=1 Dest=19 Value=0x00000005 Instr_ID=25 PC=0x00000064
[285000] ROB[26]: Valid=1 Ready=1 Dest=0 Value=0x00000000 Instr_ID=26 PC=0x00000068
[285000] ROB[27]: Valid=1 Ready=1 Dest=1 Value=0x00000006 Instr_ID=27 PC=0x0000006c
[285000] ROB[28]: Valid=1 Ready=1 Dest=2 Value=0x00000009 Instr_ID=28 PC=0x00000070
[285000] ROB[29]: Valid=1 Ready=1 Dest=3 Value=0x0000000f Instr_ID=29 PC=0x00000074
[285000] ROB[30]: Valid=1 Ready=0 Dest=8 Value=0x00000000 Instr_ID=30 PC=0x00000078
[285000] ROB[31]: Valid=1 Ready=1 Dest=7 Value=0x0000000f Instr_ID=31 PC=0x0000007c
[285000] ROB[32]: Valid=1 Ready=0 Dest=29 Value=0x00000000 Instr_ID=0 PC=0x00000080

[285000] ===== RESERVATION STATIONS =====

[285000] --- ALU Reservation Stations ---
[285000] ALU_RS[2]: Busy=1 Ready=0 ROB_ID=32 Op=0x00033 Src1_Valid=1 Src1_Tag=31 Src1_Value=0x0000000f Src2_Valid=1 Src2_Tag=27 Src2_Value=0x00000006
[285000] --- Mul/Div Reservation Stations ---
[285000] MD_RS[0]: Busy=1 Ready=0 ROB_ID=30 Op=0x00433 Src1_Valid=1 Src1_Tag=27 Src1_Value=0x00000006 Src2_Valid=1 Src2_Tag=29 Src2_Value=0x0000000f

[285000] ===== EXECUTION STAGE (CDB INPUT) =====

[285000] CDB[0]: ROB_ID=23 Result=0x00000002 Ready=1

[285000] ===== FORWARDING MESSAGES =====

[285000] FORWARD[INTRA_SRC1]: DISPATCH[1] ROB_ID=31 -> DISPATCH[2] ROB_ID=32 Reg=7

[285000] ===== CURRENT RAT AND VALID =====

[285000] RAT[1]: Tag=27 Valid=1
[285000] RAT[2]: Tag=28 Valid=1
[285000] RAT[3]: Tag=29 Valid=1
[285000] RAT[6]: Tag=23 Valid=1
[285000] RAT[7]: Tag=31 Valid=1
[285000] RAT[8]: Tag=30 Valid=1
[285000] RAT[18]: Tag=24 Valid=1
[285000] RAT[19]: Tag=25 Valid=1
[285000] RAT[29]: Tag=32 Valid=1

[285000] ===== ARCHITECTURAL REGISTER FILE (ARF) =====

[285000] ARF[1]: Value=0x00000001
[285000] ARF[2]: Value=0x00000002
[285000] ARF[3]: Value=0x00000002
[285000] ARF[4]: Value=0x00000004
[285000] ARF[7]: Value=0x00000003
[285000] ARF[9]: Value=0x00000003
[285000] ARF[10]: Value=0x00000003
[285000] ARF[11]: Value=0x00000006

[285000] ARF[12]: Value=0x00000006
[285000] ARF[14]: Value=0x00000001
[285000] ARF[15]: Value=0x00000003

[295000] ===== DECODE/DISPATCH STAGE =====

[295000] DECODE[0]: PC=0x00000078 Instr=0x02308433 Type=2 Dst=8 Src1=1 Src2=3 Opcode=0x33 Func3=0x0 Func7=0x01 Operation=0x00433
Imm=0x00000000
[295000] DECODE[1]: PC=0x0000007c Instr=0x0020e3b3 Type=0 Dst=7 Src1=1 Src2=2 Opcode=0x33 Func3=0x6 Func7=0x00 Operation=0x00333
Imm=0x00000000
[295000] DECODE[2]: PC=0x00000080 Instr=0x00138eb3 Type=0 Dst=29 Src1=7 Src2=1 Opcode=0x33 Func3=0x0 Func7=0x00 Operation=0x00033
Imm=0x00000000
[295000] DISPATCH[0]: ROB_ID=30 RS_ID=0 RS_Alloc=1 Src1_Ready=0 Src2_Ready=0 Dst=8 Src1=1 Src2=3 Src1_Tag=27 Src2_Tag=29
Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00433 Type=2 PC=0x00000078 Instr=0x02308433
[295000] DISPATCH[1]: ROB_ID=31 RS_ID=0 RS_Alloc=1 Src1_Ready=0 Src2_Ready=0 Dst=7 Src1=1 Src2=2 Src1_Tag=27 Src2_Tag=28
Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00333 Type=0 PC=0x0000007c Instr=0x0020e3b3
[295000] DISPATCH[2]: ROB_ID=32 RS_ID=2 RS_Alloc=1 Src1_Ready=0 Src2_Ready=0 Dst=29 Src1=7 Src2=1 Src1_Tag=31 Src2_Tag=27
Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00033 Type=0 PC=0x00000080 Instr=0x00138eb3

[295000] ===== REORDER BUFFER (ROB) =====

[295000] ROB Head: 33, ROB Tail: 26
[295000] ROB[26]: Valid=1 Ready=1 Dest=0 Value=0x00000000 Instr_ID=26 PC=0x00000068
[295000] ROB[27]: Valid=1 Ready=1 Dest=1 Value=0x00000006 Instr_ID=27 PC=0x0000006c
[295000] ROB[28]: Valid=1 Ready=1 Dest=2 Value=0x00000009 Instr_ID=28 PC=0x00000070
[295000] ROB[29]: Valid=1 Ready=1 Dest=3 Value=0x0000000f Instr_ID=29 PC=0x00000074
[295000] ROB[30]: Valid=1 Ready=0 Dest=8 Value=0x00000000 Instr_ID=30 PC=0x00000078
[295000] ROB[31]: Valid=1 Ready=1 Dest=7 Value=0x0000000f Instr_ID=31 PC=0x0000007c
[295000] ROB[32]: Valid=1 Ready=0 Dest=29 Value=0x00000000 Instr_ID=0 PC=0x00000080

[295000] ===== RESERVATION STATIONS =====

[295000] --- ALU Reservation Stations ---
[295000] ALU_RS[2]: Busy=1 Ready=1 ROB_ID=32 Op=0x00033 Src1_Valid=1 Src1_Tag=31 Src1_Value=0x0000000f Src2_Valid=1 Src2_Tag=27
Src2_Value=0x00000006
[295000] --- Mul/Div Reservation Stations ---
[295000] MD_RS[0]: Busy=1 Ready=1 ROB_ID=30 Op=0x00433 Src1_Valid=1 Src1_Tag=27 Src1_Value=0x00000006 Src2_Valid=1 Src2_Tag=29
Src2_Value=0x0000000f

[295000] ===== EXECUTION STAGE (CDB INPUT) =====

[295000] CDB[0]: ROB_ID=32 Result=0x00000015 Ready=1

[295000] ===== FORWARDING MESSAGES =====

[295000] FORWARD[INTRA_SRC1]: DISPATCH[1] ROB_ID=31 -> DISPATCH[2] ROB_ID=32 Reg=7

[295000] ===== INSTRUCTIONS COMMITTED THIS CYCLE =====

[295000] COMMITTED[0]: ROB_ID=23
[295000] COMMITTED[1]: ROB_ID=24
[295000] COMMITTED[2]: ROB_ID=25
[295000] Total Instructions Committed This Cycle: 3

[295000] ===== CURRENT RAT AND VALID =====

[295000] RAT[1]: Tag=27 Valid=1
[295000] RAT[2]: Tag=28 Valid=1
[295000] RAT[3]: Tag=29 Valid=1
[295000] RAT[7]: Tag=31 Valid=1
[295000] RAT[8]: Tag=30 Valid=1
[295000] RAT[29]: Tag=32 Valid=1

[295000] ===== ARCHITECTURAL REGISTER FILE (ARF) =====

[295000] ARF[1]: Value=0x00000001
[295000] ARF[2]: Value=0x00000002
[295000] ARF[3]: Value=0x00000002
[295000] ARF[4]: Value=0x00000004
[295000] ARF[6]: Value=0x00000002
[295000] ARF[7]: Value=0x00000003
[295000] ARF[9]: Value=0x00000003
[295000] ARF[10]: Value=0x00000003

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[295000] ARF[11]: Value=0x00000006
[295000] ARF[12]: Value=0x00000006
[295000] ARF[14]: Value=0x00000001
[295000] ARF[15]: Value=0x00000003
[295000] ARF[18]: Value=0x00000003
[295000] ARF[19]: Value=0x00000005
[295000] ARF Checker: PASS - ROB[23] div x6, x1, x2 -> x6 = 2
[295000] ARF Checker: PASS - ROB[24] lb x18, 16(x0) -> x18 = 3
[295000] ARF Checker: PASS - ROB[25] lb x19, 20(x0) -> x19 = 5
[295000] [MMU] STORE ISSUED: SQ[4] ROB_ID=26 Addr=0x00000019 Data=0x00000000 Size=2

[305000] ===== DECODE/DISPATCH STAGE =====
[305000] DECODE[0]: PC=0x00000078 Instr=0x02308433 Type=2 Dst=8 Src1=1 Src2=3 Opcode=0x33 Func3=0x0 Func7=0x01 Operation=0x00433
Imm=0x00000000
[305000] DECODE[1]: PC=0x0000007c Instr=0x0020e3b3 Type=0 Dst=7 Src1=1 Src2=2 Opcode=0x33 Func3=0x6 Func7=0x00 Operation=0x00333
Imm=0x00000000
[305000] DECODE[2]: PC=0x00000080 Instr=0x00138eb3 Type=0 Dst=29 Src1=7 Src2=1 Opcode=0x33 Func3=0x0 Func7=0x00 Operation=0x00033
Imm=0x00000000
[305000] DISPATCH[0]: ROB_ID=30 RS_ID=0 RS_Alloc=1 Src1_Ready=0 Src2_Ready=0 Dst=8 Src1=1 Src2=3 Src1_Tag=27 Src2_Tag=29
Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00433 Type=2 PC=0x00000078 Instr=0x02308433
[305000] DISPATCH[1]: ROB_ID=31 RS_ID=0 RS_Alloc=1 Src1_Ready=0 Src2_Ready=0 Dst=7 Src1=1 Src2=2 Src1_Tag=27 Src2_Tag=28
Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00333 Type=0 PC=0x0000007c Instr=0x0020e3b3
[305000] DISPATCH[2]: ROB_ID=32 RS_ID=2 RS_Alloc=1 Src1_Ready=0 Src2_Ready=0 Dst=29 Src1=7 Src2=1 Src1_Tag=31 Src2_Tag=27
Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00033 Type=0 PC=0x00000080 Instr=0x00138eb3

[305000] ===== REORDER BUFFER (ROB) =====
[305000] ROB Head: 33, ROB Tail: 29
[305000] ROB[29]: Valid=1 Ready=1 Dest=3 Value=0x0000000f Instr_ID=29 PC=0x00000074
[305000] ROB[30]: Valid=1 Ready=0 Dest=8 Value=0x00000000 Instr_ID=30 PC=0x00000078
[305000] ROB[31]: Valid=1 Ready=1 Dest=7 Value=0x0000000f Instr_ID=31 PC=0x0000007c
[305000] ROB[32]: Valid=1 Ready=1 Dest=29 Value=0x00000015 Instr_ID=0 PC=0x00000080

[305000] ===== FORWARDING MESSAGES =====
[305000] FORWARD[INTRA_SRC1]: DISPATCH[1] ROB_ID=31 -> DISPATCH[2] ROB_ID=32 Reg=7

[305000] ===== INSTRUCTIONS COMMITTED THIS CYCLE =====
[305000] COMMITTED[0]: ROB_ID=26
[305000] COMMITTED[1]: ROB_ID=27
[305000] COMMITTED[2]: ROB_ID=28
[305000] Total Instructions Committed This Cycle: 3

[305000] ===== CURRENT RAT AND VALID =====
[305000] RAT[3]: Tag=29 Valid=1
[305000] RAT[7]: Tag=31 Valid=1
[305000] RAT[8]: Tag=30 Valid=1
[305000] RAT[29]: Tag=32 Valid=1

[305000] ===== ARCHITECTURAL REGISTER FILE (ARF) =====
[305000] ARF[1]: Value=0x00000006
[305000] ARF[2]: Value=0x00000009
[305000] ARF[3]: Value=0x00000002
[305000] ARF[4]: Value=0x00000004
[305000] ARF[6]: Value=0x00000002
[305000] ARF[7]: Value=0x00000003
[305000] ARF[9]: Value=0x00000003
[305000] ARF[10]: Value=0x00000003
[305000] ARF[11]: Value=0x00000006
[305000] ARF[12]: Value=0x00000006
[305000] ARF[14]: Value=0x00000001
[305000] ARF[15]: Value=0x00000003
[305000] ARF[18]: Value=0x00000003
[305000] ARF[19]: Value=0x00000005
[305000] ARF Checker: PASS - ROB[26] sw x25, 20(x19) -> x0 = 0
[305000] ARF Checker: PASS - ROB[27] add x1, x9, x10 -> x1 = 6
[305000] ARF Checker: PASS - ROB[28] add x2, x9, x11 -> x2 = 9

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[315000] ===== DECODE/DISPATCH STAGE =====
[315000] DECODE[0]: PC=0x00000078 Instr=0x02308433 Type=2 Dst=8 Src1=1 Src2=3 Opcode=0x33 Func3=0x0 Func7=0x01 Operation=0x00433
Imm=0x00000000
[315000] DECODE[1]: PC=0x0000007c Instr=0x0020e3b3 Type=0 Dst=7 Src1=1 Src2=2 Opcode=0x33 Func3=0x6 Func7=0x00 Operation=0x00333
Imm=0x00000000
[315000] DECODE[2]: PC=0x00000080 Instr=0x00138eb3 Type=0 Dst=29 Src1=7 Src2=1 Opcode=0x33 Func3=0x0 Func7=0x00 Operation=0x00033
Imm=0x00000000
[315000] DISPATCH[0]: ROB_ID=30 RS_ID=0 RS_Alloc=1 Src1_Ready=0 Src2_Ready=0 Dst=8 Src1=1 Src2=3 Src1_Tag=27 Src2_Tag=29
Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00433 Type=2 PC=0x00000078 Instr=0x02308433
[315000] DISPATCH[1]: ROB_ID=31 RS_ID=0 RS_Alloc=1 Src1_Ready=0 Src2_Ready=0 Dst=7 Src1=1 Src2=2 Src1_Tag=27 Src2_Tag=28
Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00333 Type=0 PC=0x0000007c Instr=0x0020e3b3
[315000] DISPATCH[2]: ROB_ID=32 RS_ID=2 RS_Alloc=1 Src1_Ready=0 Src2_Ready=0 Dst=29 Src1=7 Src2=1 Src1_Tag=31 Src2_Tag=27
Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00033 Type=0 PC=0x00000080 Instr=0x00138eb3

[315000] ===== REORDER BUFFER (ROB) =====
[315000] ROB Head: 33, ROB Tail: 30
[315000] ROB[30]: Valid=1 Ready=0 Dest=8 Value=0x00000000 Instr_ID=30 PC=0x00000078
[315000] ROB[31]: Valid=1 Ready=1 Dest=7 Value=0x0000000f Instr_ID=31 PC=0x0000007c
[315000] ROB[32]: Valid=1 Ready=1 Dest=29 Value=0x00000015 Instr_ID=0 PC=0x00000080

[315000] ===== FORWARDING MESSAGES =====
[315000] FORWARD[INTRA_SRC1]: DISPATCH[1] ROB_ID=31 -> DISPATCH[2] ROB_ID=32 Reg=7

[315000] ===== INSTRUCTIONS COMMITTED THIS CYCLE =====
[315000] COMMITTED[0]: ROB_ID=29
[315000] Total Instructions Committed This Cycle: 1

[315000] ===== CURRENT RAT AND VALID =====
[315000] RAT[7]: Tag=31 Valid=1
[315000] RAT[8]: Tag=30 Valid=1
[315000] RAT[29]: Tag=32 Valid=1

[315000] ===== ARCHITECTURAL REGISTER FILE (ARF) =====
[315000] ARF[1]: Value=0x00000006
[315000] ARF[2]: Value=0x00000009
[315000] ARF[3]: Value=0x0000000f
[315000] ARF[4]: Value=0x00000004
[315000] ARF[6]: Value=0x00000002
[315000] ARF[7]: Value=0x00000003
[315000] ARF[9]: Value=0x00000003
[315000] ARF[10]: Value=0x00000003
[315000] ARF[11]: Value=0x00000006
[315000] ARF[12]: Value=0x00000006
[315000] ARF[14]: Value=0x00000001
[315000] ARF[15]: Value=0x00000003
[315000] ARF[18]: Value=0x00000003
[315000] ARF[19]: Value=0x00000005
[315000] ARF Checker: PASS - ROB[29] add x3, x1, x2 -> x3 = 15

[325000] ===== DECODE/DISPATCH STAGE =====
[325000] DECODE[0]: PC=0x00000078 Instr=0x02308433 Type=2 Dst=8 Src1=1 Src2=3 Opcode=0x33 Func3=0x0 Func7=0x01 Operation=0x00433
Imm=0x00000000
[325000] DECODE[1]: PC=0x0000007c Instr=0x0020e3b3 Type=0 Dst=7 Src1=1 Src2=2 Opcode=0x33 Func3=0x6 Func7=0x00 Operation=0x00333
Imm=0x00000000
[325000] DECODE[2]: PC=0x00000080 Instr=0x00138eb3 Type=0 Dst=29 Src1=7 Src2=1 Opcode=0x33 Func3=0x0 Func7=0x00 Operation=0x00033
Imm=0x00000000
[325000] DISPATCH[0]: ROB_ID=30 RS_ID=0 RS_Alloc=1 Src1_Ready=0 Src2_Ready=0 Dst=8 Src1=1 Src2=3 Src1_Tag=27 Src2_Tag=29
Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00433 Type=2 PC=0x00000078 Instr=0x02308433
[325000] DISPATCH[1]: ROB_ID=31 RS_ID=0 RS_Alloc=1 Src1_Ready=0 Src2_Ready=0 Dst=7 Src1=1 Src2=2 Src1_Tag=27 Src2_Tag=28
Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00333 Type=0 PC=0x0000007c Instr=0x0020e3b3
[325000] DISPATCH[2]: ROB_ID=32 RS_ID=2 RS_Alloc=1 Src1_Ready=0 Src2_Ready=0 Dst=29 Src1=7 Src2=1 Src1_Tag=31 Src2_Tag=27
Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00033 Type=0 PC=0x00000080 Instr=0x00138eb3

[325000] ===== REORDER BUFFER (ROB) =====

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[325000] ROB Head: 33, ROB Tail: 30
[325000] ROB[30]: Valid=1 Ready=0 Dest=8 Value=0x00000000 Instr_ID=30 PC=0x00000078
[325000] ROB[31]: Valid=1 Ready=1 Dest=7 Value=0x0000000f Instr_ID=31 PC=0x0000007c
[325000] ROB[32]: Valid=1 Ready=1 Dest=29 Value=0x00000015 Instr_ID=0 PC=0x00000080

[325000] ===== EXECUTION STAGE (CDB INPUT) =====
[325000] CDB[0]: ROB_ID=30 Result=0x0000005a Ready=1

[325000] ===== FORWARDING MESSAGES =====
[325000] FORWARD[INTRA_SRC1]: DISPATCH[1] ROB_ID=31 -> DISPATCH[2] ROB_ID=32 Reg=7

[325000] ===== CURRENT RAT AND VALID =====
[325000] RAT[7]: Tag=31 Valid=1
[325000] RAT[8]: Tag=30 Valid=1
[325000] RAT[29]: Tag=32 Valid=1

[325000] ===== ARCHITECTURAL REGISTER FILE (ARF) =====
[325000] ARF[1]: Value=0x00000006
[325000] ARF[2]: Value=0x00000009
[325000] ARF[3]: Value=0x0000000f
[325000] ARF[4]: Value=0x00000004
[325000] ARF[6]: Value=0x00000002
[325000] ARF[7]: Value=0x00000003
[325000] ARF[9]: Value=0x00000003
[325000] ARF[10]: Value=0x00000003
[325000] ARF[11]: Value=0x00000006
[325000] ARF[12]: Value=0x00000006
[325000] ARF[14]: Value=0x00000001
[325000] ARF[15]: Value=0x00000003
[325000] ARF[18]: Value=0x00000003
[325000] ARF[19]: Value=0x00000005

[335000] ===== DECODE/DISPATCH STAGE =====
[335000] DECODE[0]: PC=0x00000078 Instr=0x02308433 Type=2 Dst=8 Src1=1 Src2=3 Opcode=0x33 Func3=0x0 Func7=0x01 Operation=0x00433 Imm=0x00000000
[335000] DECODE[1]: PC=0x0000007c Instr=0x0020e3b3 Type=0 Dst=7 Src1=1 Src2=2 Opcode=0x33 Func3=0x6 Func7=0x00 Operation=0x00333 Imm=0x00000000
[335000] DECODE[2]: PC=0x00000080 Instr=0x00138eb3 Type=0 Dst=29 Src1=7 Src2=1 Opcode=0x33 Func3=0x0 Func7=0x00 Operation=0x00033 Imm=0x00000000
[335000] DISPATCH[0]: ROB_ID=30 RS_ID=0 RS_Alloc=1 Src1_Ready=0 Src2_Ready=0 Dst=8 Src1=1 Src2=3 Src1_Tag=27 Src2_Tag=29 Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00433 Type=2 PC=0x00000078 Instr=0x02308433
[335000] DISPATCH[1]: ROB_ID=31 RS_ID=0 RS_Alloc=1 Src1_Ready=0 Src2_Ready=0 Dst=7 Src1=1 Src2=2 Src1_Tag=27 Src2_Tag=28 Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00333 Type=0 PC=0x0000007c Instr=0x0020e3b3
[335000] DISPATCH[2]: ROB_ID=32 RS_ID=2 RS_Alloc=1 Src1_Ready=0 Src2_Ready=0 Dst=29 Src1=7 Src2=1 Src1_Tag=31 Src2_Tag=27 Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00033 Type=0 PC=0x00000080 Instr=0x00138eb3

[335000] ===== FORWARDING MESSAGES =====
[335000] FORWARD[INTRA_SRC1]: DISPATCH[1] ROB_ID=31 -> DISPATCH[2] ROB_ID=32 Reg=7

[335000] ===== INSTRUCTIONS COMMITTED THIS CYCLE =====
[335000] COMMITTED[0]: ROB_ID=30
[335000] COMMITTED[1]: ROB_ID=31
[335000] COMMITTED[2]: ROB_ID=32
[335000] Total Instructions Committed This Cycle: 3

[335000] ===== ARCHITECTURAL REGISTER FILE (ARF) =====
[335000] ARF[1]: Value=0x00000006
[335000] ARF[2]: Value=0x00000009
[335000] ARF[3]: Value=0x0000000f
[335000] ARF[4]: Value=0x00000004
[335000] ARF[6]: Value=0x00000002
[335000] ARF[7]: Value=0x0000000f
[335000] ARF[8]: Value=0x0000005a
[335000] ARF[9]: Value=0x00000003
[335000] ARF[10]: Value=0x00000003

[335000] ARF[11]: Value=0x00000006
[335000] ARF[12]: Value=0x00000006
[335000] ARF[14]: Value=0x00000001
[335000] ARF[15]: Value=0x00000003
[335000] ARF[18]: Value=0x00000003
[335000] ARF[19]: Value=0x00000005
[335000] ARF[29]: Value=0x00000015

[335000] ===== PERFORMANCE METRICS =====

[335000] Cycle Count: 31
[335000] Total Instructions Committed: 33
[335000] All Instructions Completed: 1

[335000] ===== IPC ANALYSIS =====

[335000] IPC Measurement Period: Cycles 8 to 31
[335000] Total Cycles Measured: 24
[335000] Instructions Committed: 33
[335000] FINAL IPC: 1.3750

[335000] =====

[335000] ARF Checker: PASS - ROB[30] mul x8, x1, x3 -> x8 = 90

[335000] ARF Checker: PASS - ROB[31] or x7, x1, x2 -> x7 = 15

[335000] ARF Checker: PASS - ROB[32] add x29, x7, x1 -> x29 = 21

=== CHECKER COMPREHENSIVE SUMMARY ===

Total checks performed: 33

Passed: 33, Failed: 0

=== ALL CHECKS PASSED ===

Detailed Results:

ROB_ID | PC | Instruction | Dest | Actual | Expected | Status

ROB_ID	PC	Instruction	Dest	Actual	Expected	Status
0	0	addi x1, x0, 1	x 1	1	1	PASS
1	4	addi x2, x0, 2	x 2	2	2	PASS
2	8	addi x3, x0, 3	x 3	3	3	PASS
3	12	sw x1, 4(x0)	--	--	--	PASS
4	16	sw x2, 8(x0)	--	--	--	PASS
5	20	sw x3, 12(x0)	--	--	--	PASS
6	24	sw x3, 16(x0)	--	--	--	PASS
7	28	mul x3, x1, x2	x 3	2	2	PASS
8	32	add x4, x2, x3	x 4	4	4	PASS
9	36	add x7, x3, x1	x 7	3	3	PASS
10	40	add x8, x8, x9	x 8	0	0	PASS
11	44	lb x1, 4(x0)	x 1	1	1	PASS
12	48	lbu x9, 8(x0)	x 9	2	2	PASS
13	52	lw x9, 12(x0)	x 9	3	3	PASS
14	56	xor x15, x9, x10	x15	3	3	PASS
15	60	add x10, x10, x11	x10	0	0	PASS
16	64	add x11, x10, x9	x11	3	3	PASS
17	68	sll x12, x9, x1	x12	6	6	PASS
18	72	srl x13, x9, x1	x13	1	1	PASS
19	76	sub x10, x12, x11	x10	3	3	PASS
20	80	and x13, x18, x19	x13	0	0	PASS
21	84	slt x14, x10, x12	x14	1	1	PASS
22	88	add x11, x9, x10	x11	6	6	PASS
23	92	div x6, x1, x2	x 6	2	2	PASS
24	96	lb x18, 16(x0)	x18	3	3	PASS
25	100	lb x19, 20(x0)	x19	5	5	PASS
26	104	sw x25, 20(x19)	--	--	--	PASS
27	108	add x1, x9, x10	x 1	6	6	PASS
28	112	add x2, x9, x11	x 2	9	9	PASS
29	116	add x3, x1, x2	x 3	15	15	PASS
30	120	mul x8, x1, x3	x 8	90	90	PASS
31	124	or x7, x1, x2	x 7	15	15	PASS
32	128	add x29, x7, x1	x29	21	21	PASS

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```
[345000] ===== DECODE/DISPATCH STAGE =====
[345000] DECODE[0]: PC=0x00000078 Instr=0x02308433 Type=2 Dst=8 Src1=1 Src2=3 Opcode=0x33 Func3=0x0 Func7=0x01 Operation=0x00433
Imm=0x00000000
[345000] DECODE[1]: PC=0x0000007c Instr=0x0020e3b3 Type=0 Dst=7 Src1=1 Src2=2 Opcode=0x33 Func3=0x6 Func7=0x00 Operation=0x00333
Imm=0x00000000
[345000] DECODE[2]: PC=0x00000080 Instr=0x00138eb3 Type=0 Dst=29 Src1=7 Src2=1 Opcode=0x33 Func3=0x0 Func7=0x00 Operation=0x00033
Imm=0x00000000
[345000] DISPATCH[0]: ROB_ID=30 RS_ID=0 RS_Alloc=1 Src1_Ready=0 Src2_Ready=0 Dst=8 Src1=1 Src2=3 Src1_Tag=27 Src2_Tag=29
Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00433 Type=2 PC=0x00000078 Instr=0x02308433
[345000] DISPATCH[1]: ROB_ID=31 RS_ID=0 RS_Alloc=1 Src1_Ready=0 Src2_Ready=0 Dst=7 Src1=1 Src2=2 Src1_Tag=27 Src2_Tag=28
Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00333 Type=0 PC=0x0000007c Instr=0x0020e3b3
[345000] DISPATCH[2]: ROB_ID=32 RS_ID=2 RS_Alloc=1 Src1_Ready=0 Src2_Ready=0 Dst=29 Src1=7 Src2=1 Src1_Tag=31 Src2_Tag=27
Src1_Value=0x00000000 Src2_Value=0x00000000 Operation=0x00033 Type=0 PC=0x00000080 Instr=0x00138eb3
```

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[345000] ===== FORWARDING MESSAGES =====
[345000] FORWARD[INTRA_SRC1]: DISPATCH[1] ROB_ID=31 -> DISPATCH[2] ROB_ID=32 Reg=7
```

```
[345000] ===== ARCHITECTURAL REGISTER FILE (ARF) =====
[345000] ARF[1]: Value=0x00000006
[345000] ARF[2]: Value=0x00000009
[345000] ARF[3]: Value=0x0000000f
[345000] ARF[4]: Value=0x00000004
[345000] ARF[6]: Value=0x00000002
[345000] ARF[7]: Value=0x0000000f
[345000] ARF[8]: Value=0x0000005a
[345000] ARF[9]: Value=0x00000003
[345000] ARF[10]: Value=0x00000003
[345000] ARF[11]: Value=0x00000006
[345000] ARF[12]: Value=0x00000006
[345000] ARF[14]: Value=0x00000001
[345000] ARF[15]: Value=0x00000003
[345000] ARF[18]: Value=0x00000003
[345000] ARF[19]: Value=0x00000005
[345000] ARF[29]: Value=0x00000015
```

```
[345000] ===== PERFORMANCE METRICS =====
[345000] Cycle Count: 32
[345000] Total Instructions Committed: 33
[345000] All Instructions Completed: 1
```

```
[345000] ===== IPC ANALYSIS =====
[345000] IPC Measurement Period: Cycles 8 to 31
[345000] Total Cycles Measured: 24
[345000] Instructions Committed: 33
[345000] FINAL IPC: 1.3750
```

```
[345000] =====
$finish called from file "testbench.sv", line 169.
$finish at simulation time      355000
VCS Simulation Report
Time: 355000 ps
```