

EXPERIMENT 2

Group's members:

Mohammad Taghizadeh 810198373

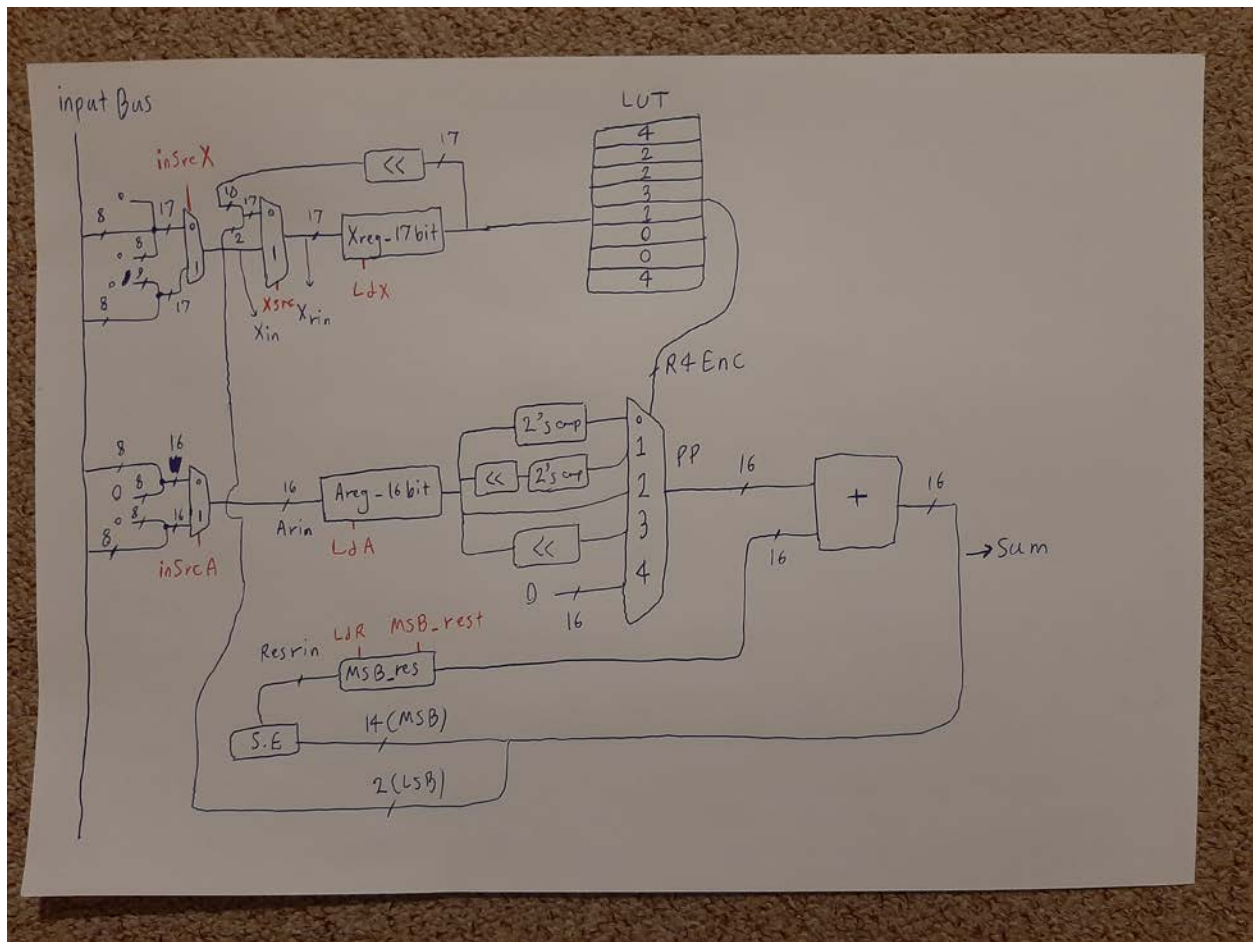
Arian Niakan 810198536

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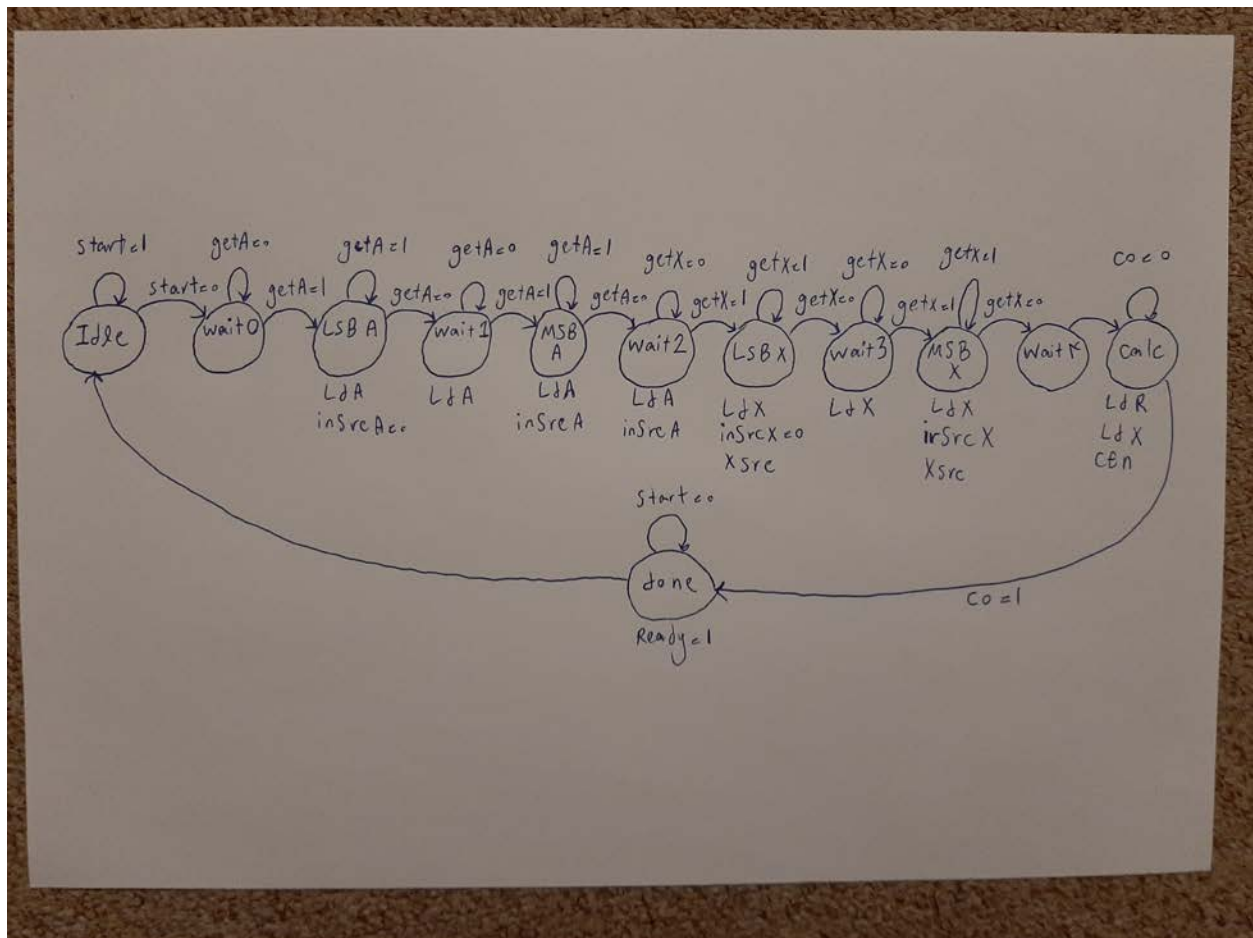
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RTL Design and Simulation

1. Data Path

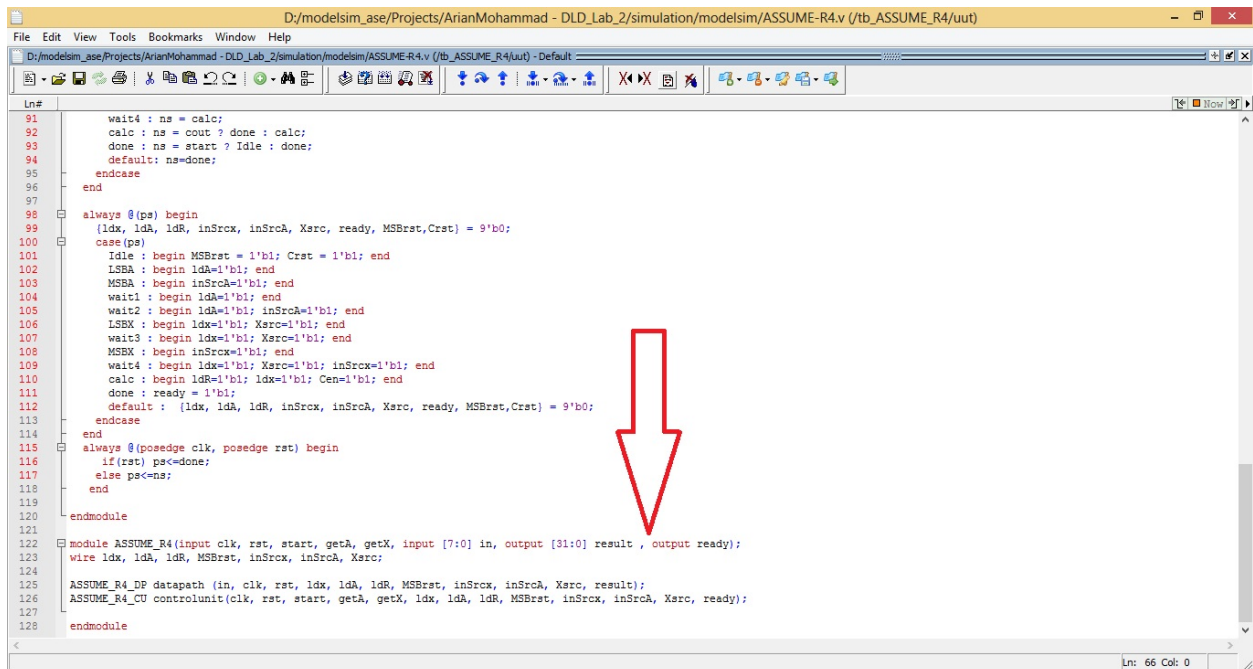


2. Controller state diagram



3. Verilog Code of Design

Top Level



```
Ln#
91      wait4 : ns = calc;
92      calc : ns = cout ? done : calc;
93      done : ns = start ? Idle : done;
94      default: ns=done;
95  endcase
96  end
97
98  always @(ps) begin
99      {ldx, ldA, ldR, inSrcx, inSrcA, Xsrc, ready, MSBrst,Crst} = 9'b0;
100     case (ps)
101         Idle : begin MSBrst = 1'b1; Crst = 1'b1; end
102         LSBA : begin ldA=1'b1; end
103         MSBA : begin inSrcA=1'b1; end
104         wait1 : begin ldA=1'b1; end
105         wait2 : begin ldA=1'b1; inSrcA=1'b1; end
106         LSBX : begin ldx=1'b1; Xsrc=1'b1; end
107         wait3 : begin ldx=1'b1; Xsrc=1'b1; end
108         MSBX : begin inSrcx=1'b1; end
109         wait4 : begin ldx=1'b1; Xsrc=1'b1; inSrcx=1'b1; end
110         calc : begin ldR=1'b1; ldx=1'b1; Cen=1'b1; end
111         done : ready = 1'b1;
112         default : {ldx, ldA, ldR, inSrcx, inSrcA, Xsrc, ready, MSBrst,Crst} = 9'b0;
113     endcase
114  end
115  always @(posedge clk, posedge rst) begin
116      if (rst) ps<=done;
117      else ps<=ns;
118  end
119  endmodule
120
121  module ASSUME_R4(input clk, rst, start, getA, getX, input [7:0] in, output [31:0] result , output ready);
122      wire ldx, ldA, ldR, MSBrst, inSrcx, inSrcA, Xsrc;
123
124      ASSUME_R4_DP datapath (in, clk, rst, ldx, ldA, ldR, MSBrst, inSrcx, inSrcA, Xsrc, result);
125      ASSUME_R4_CU controlunit(clk, rst, start, getA, getX, ldx, ldA, ldR, MSBrst, inSrcx, inSrcA, Xsrc, ready);
126  endmodule
127
128
```

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Data Path

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D:/modelsim_ase/Projects/ArianMohammad - DLD_Lab_2/simulation/modelsim/ASSUME-R4.v (/tb_ASSUME_R4/uut) - Default
Ln#
2 module ASSUME_R4_DP(input [7:0] in, input clk, rst, ldx, lda, ldr, MSBrst, inSrcx, inSrcA, Xsrc, output [31:0] result);
3 //defining our registers and their load and reset inputs
4 reg [16:0] Xreg;
5 reg [15:0] Areg, ResMSB;
6 wire [16:0] Xrin;
7 wire [15:0] Arin, Resrin;
8 always @(posedge clk, posedge MSBrst) begin
9     if (MSBrst) ResMSB<=16'b0;
10     else begin
11         if (rst) begin
12             Xreg <= 0;
13             Areg <= 0;
14             ResMSB <= 0;
15         end
16         if (ldx)
17             Xreg <= Xrin;
18         if (ldr)
19             ResMSB <= Resrin;
20         if (lda)
21             Areg <= Arin;
22     end
23 end
24 //defining the multiplexers that select our registers inputs
25 wire [16:0] Xin;
26 wire [15:0] sum, PP;
27 wire [2:0] R4ENC;
28 wire [14:0] SRX;
29 assign SRX = (Xreg >> 2);
30 assign Xin = inSrcx ? {in, Xreg[8:0]} : {8'b0, in, 1'b0};
31 assign Arin = inSrcA ? {in, Areg[7:0]} : {Areg[15:8], in};
32 assign Xrin = Xsrc? Xin : {sum[1:0], SRX};
33 assign PP = R4ENC == 3'b000 ? ~Areg
34             : R4ENC == 3'b001 ? ~(Areg << 1)
35             : R4ENC == 3'b010 ? Areg
36             : R4ENC == 3'b011 ? (Areg << 1)
37             : R4ENC == 3'b100 ? 16'b0
38             : 16'bx;
39 //defining the LUT as an array (which determines the select of our PP MIX
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```

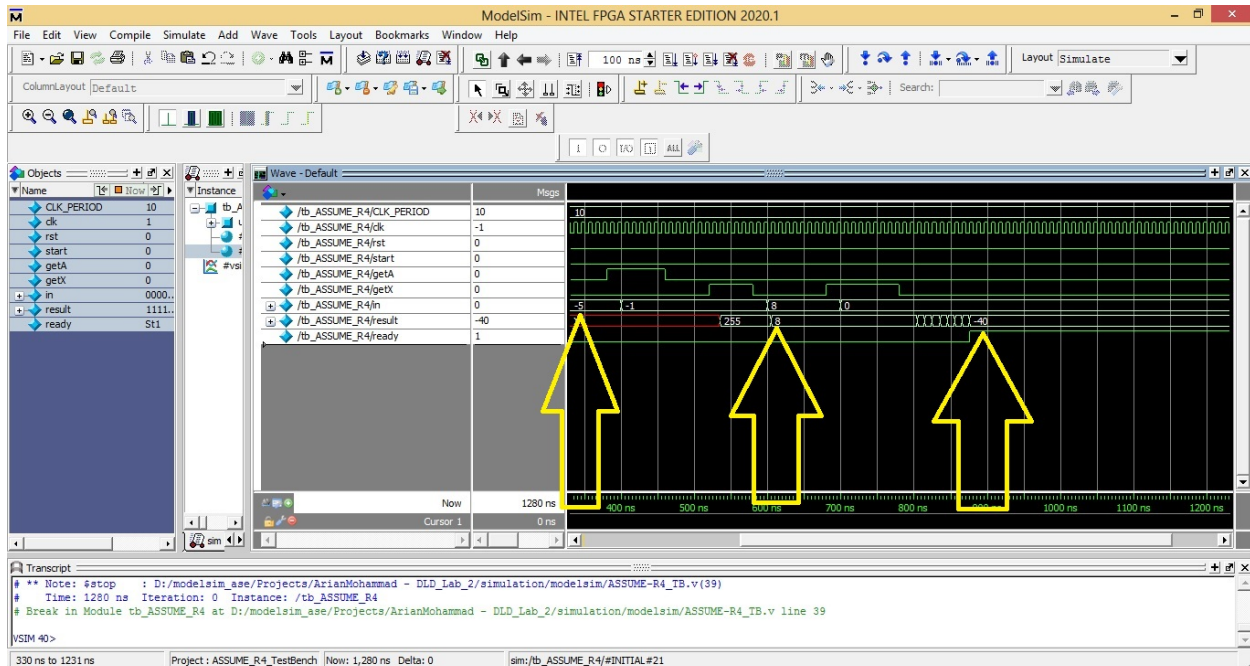
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D:/modelsim_ase/Projects/ArianMohammad - DLD_Lab_2/simulation/modelsim/ASSUME-R4.v (/tb_ASSUME_R4/uut) - Default
Ln#
31 assign Arin = inSrcA ? {in, Areg[7:0]} : {Areg[15:8], in};
32 assign Xrin = Xsrc? Xin : {sum[1:0], SRX};
33 assign PP = R4ENC == 3'b000 ? ~Areg
34             : R4ENC == 3'b001 ? ~(Areg << 1)
35             : R4ENC == 3'b010 ? Areg
36             : R4ENC == 3'b011 ? (Areg << 1)
37             : R4ENC == 3'b100 ? 16'b0
38             : 16'bx;
39 //defining the LUT as an array (which determines the select of our PP MIX
40
41 wire [2:0] LUT[0:7];
42 assign LUT [0] = 3'd4;
43 assign LUT [1] = 3'd2;
44 assign LUT [2] = 3'd2;
45 assign LUT [3] = 3'd3;
46 assign LUT [4] = 3'd1;
47 assign LUT [5] = 3'd0;
48 assign LUT [6] = 3'd0;
49 assign LUT [7] = 3'd4;
50 assign R4ENC = LUT[Xreg[2:0]];
51 // defining our adder result
52 assign sum=PP+ResMSB;
53 //sign extention
54 assign Resrin = {sum[15], sum[15], sum[15:2]};
55 assign result = {ResMSB,Xreg[16:1]};
56 endmodule
57
58 module counter8(input clk, Cen, Crst, output Cout);
59 reg [3:0] count;
60 always @(posedge clk, posedge Crst) begin
61     if (Crst) count=4'b0;
62     else begin
63         if (Cout) count = 0;
64         if (Cen) count = count+1;
65     end
66 end
67 assign Cout = count[2]&count[1]&count[0];
68 endmodule
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```

Controller

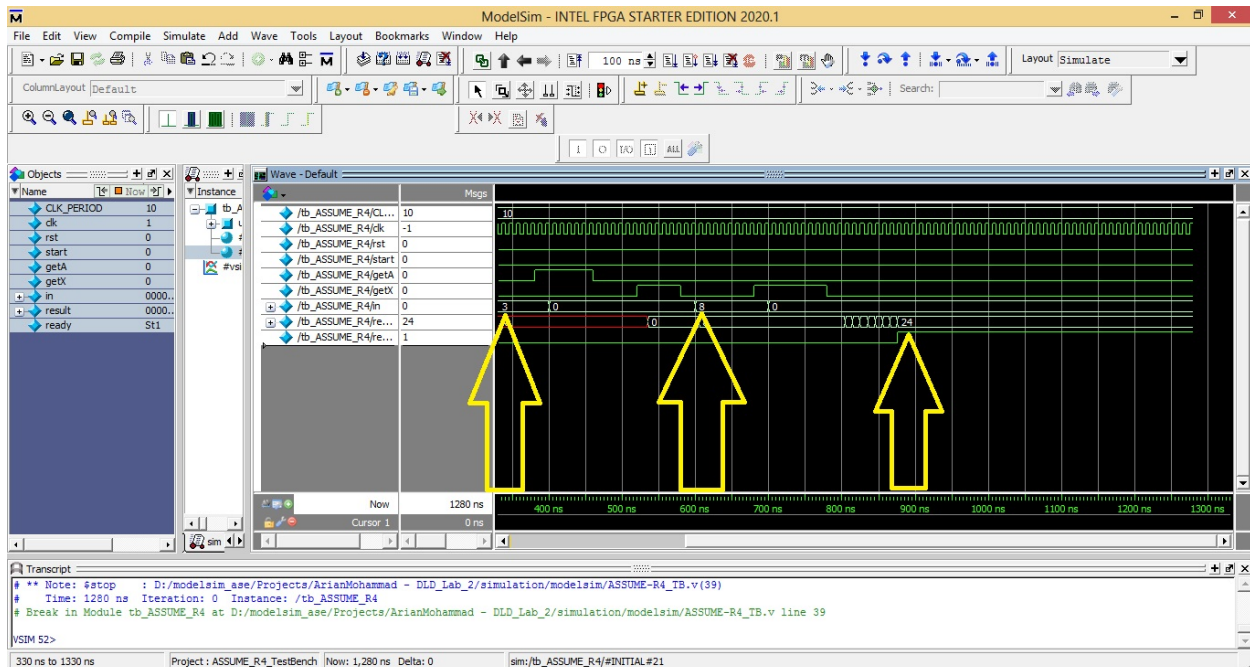
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D:/modelsim_ase/Projects/ArianMohammad - DLD_Lab_2/simulation/modelsim/ASSUME-R4.v (/tb_ASSUME_R4/uut) - Default
Ln#
70 module ASSUME_R4_CU(input clk, rst, start, getA, getX, output reg ldx, ldA, ldR, MSBrst, inSrcx, inSrcA, Xsrc, ready);
71 parameter [3:0] Idle = 4'd1, wait0 = 4'd2, LSBA = 4'd3, wait1 = 4'd4, MSBA = 4'd5, wait2 = 4'd6, LSBX = 4'd7,
72 wait3 = 4'd8, MSBX = 4'd9, wait4=4'd10, calc = 4'd11, done = 4'd0;
73
74
75 reg Cen, Crst;
76 wire cout;
77
78 counter8 counter (clk, Cen, Crst, cout);
79 reg [3:0] ps, ns;
80 always @(start, getA, getX, cout, ps) begin
81 case(ps)
82 Idle : ns = start ? Idle : wait0;
83 wait0 : ns = getA ? LSBA : wait0;
84 LSBA : ns = getA ? LSBA : wait1;
85 wait1 : ns = getA ? MSBA : wait1;
86 MSBA : ns = getA ? MSBA : wait2;
87 wait2 : ns = getX ? LSBX : wait2;
88 LSBX : ns = getX ? LSBX : wait3;
89 wait3 : ns = getX ? MSBX : wait3;
90 MSBX : ns = getX ? MSBX : wait4;
91 wait4 : ns = calc;
92 calc : ns = cout ? done : calc;
93 done : ns = start ? Idle : done;
94 default: ns=done;
95 endcase
96 end
97
98 always @(ps) begin
99 (ldx, ldA, ldR, inSrcx, inSrcA, Xsrc, ready, MSBrst,Crst) = 9'b0;
100 case(ps)
101 Idle : begin MSBrst = 1'b1; Crst = 1'b1; end
102 LSBA : begin ldA=1'b1; end
103 MSBA : begin inSrcA=1'b1; end
104 wait1 : begin ldA=1'b1; end
105 wait2 : begin ldA=1'b1; inSrcA=1'b1; end
106 LSBX : begin ldx=1'b1; Xsrc=1'b1; end
107 wait3 : begin ldx=1'b1; Xsrc=1'b1; end
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```


Simulation output of above Design

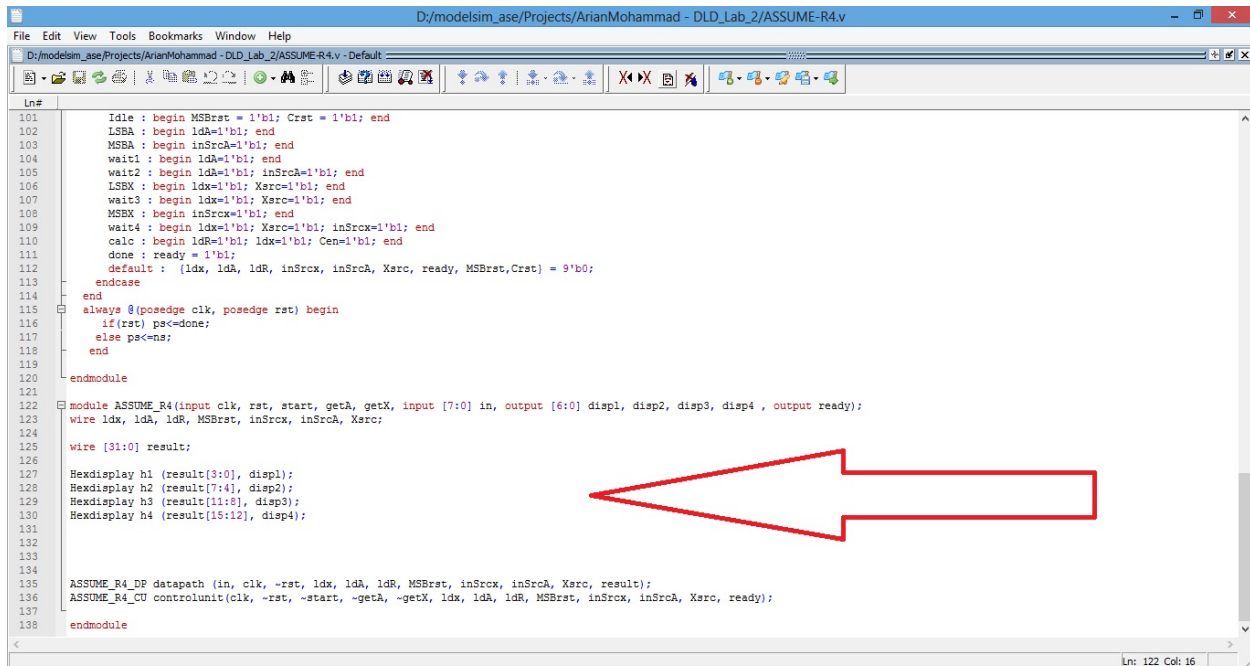
Signed number Multiplication



Unsigned number Multiplication

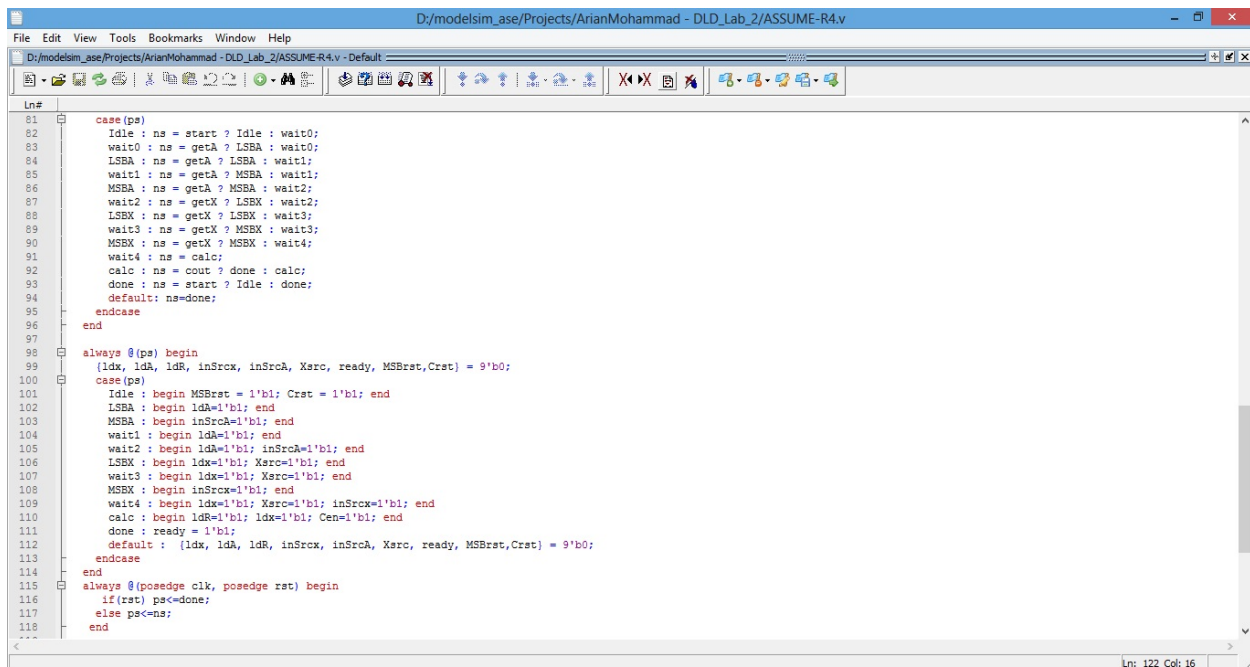


Modified Top Level of previous RTL Design



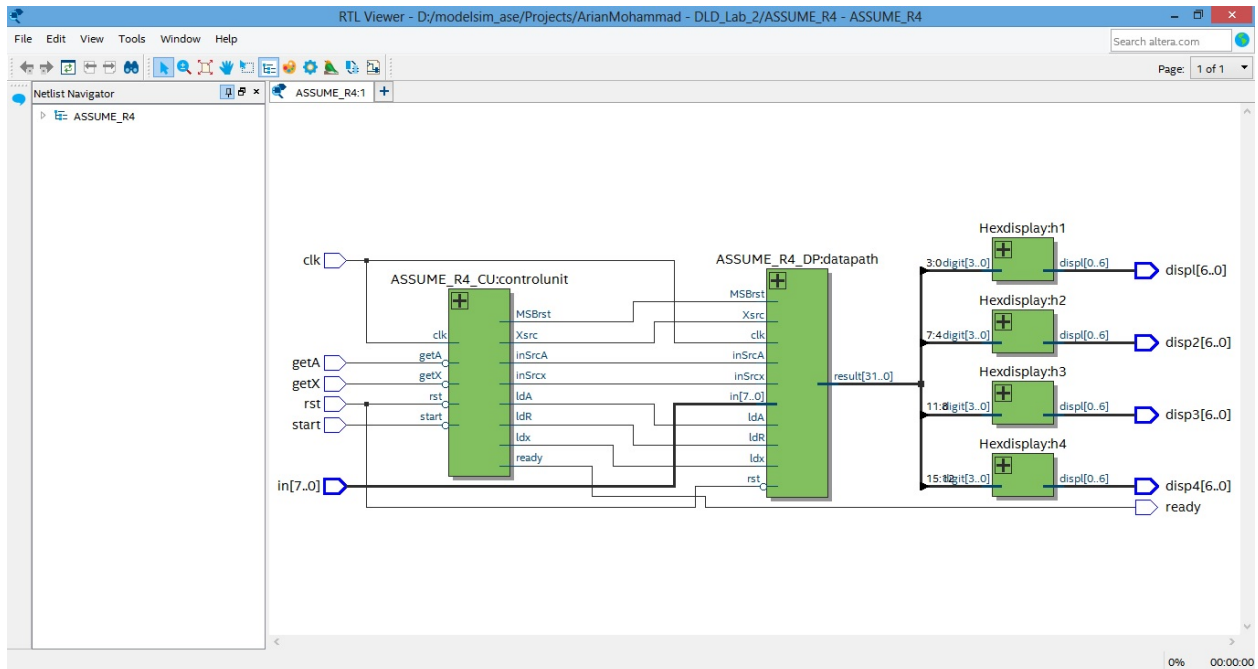
```
Ln#
101 Idle : begin MSBrst = 1'b1; Crst = 1'b1; end
102 LSBA : begin ldA=1'b1; end
103 MSBA : begin inSrcA=1'b1; end
104 wait1 : begin ldA=1'b1; end
105 wait2 : begin ldA=1'b1; inSrcA=1'b1; end
106 LSBX : begin ldX=1'b1; Xsrc=1'b1; end
107 wait3 : begin ldA=1'b1; Xsrc=1'b1; end
108 MSBX : begin inSrcX=1'b1; end
109 wait4 : begin ldX=1'b1; Xsrc=1'b1; inSrcX=1'b1; end
110 calc : begin ldR=1'b1; ldX=1'b1; Cen=1'b1; end
111 done : ready = 1'b1;
112 default : {ldX, ldA, ldR, inSrcX, inSrcA, Xsrc, ready, MSBrst,Crst} = 9'b0;
113 endcase
114 end
115 always @(posedge clk, posedge rst) begin
116 if(rst) ps<=done;
117 else ps<=ns;
118 end
119 endmodule
120
121
122 module ASSUME_R4(input clk, rst, start, getA, getX, input [7:0] in, output [6:0] displ, disp2, disp3, disp4 , output ready);
123 wire ldX, ldA, ldR, MSBrst, inSrcX, inSrcA, Xsrc;
124
125 wire [31:0] result;
126
127 Hexdisplay h1 (result[3:0], displ);
128 Hexdisplay h2 (result[7:4], disp2);
129 Hexdisplay h3 (result[11:8], disp3);
130 Hexdisplay h4 (result[15:12], disp4);
131
132
133
134 ASSUME_R4_DP datapath (in, clk, ~rst, ldX, ldA, ldR, MSBrst, inSrcX, inSrcA, Xsrc, result);
135 ASSUME_R4_CU controlunit(clk, ~rst, ~start, ~getA, ~getX, ldX, ldA, ldR, MSBrst, inSrcX, inSrcA, Xsrc, ready);
136
137 endmodule
138
```

Modified Controller of previous RTL Design



```
Ln#
81 case (ps)
82 Idle : ns = start ? Idle : wait0;
83 wait0 : ns = getA ? LSBA : wait0;
84 LSBA : ns = getA ? MSBA : wait1;
85 wait1 : ns = getA ? MSBA : wait1;
86 MSBA : ns = getA ? LSBX : wait2;
87 wait2 : ns = getX ? LSBX : wait2;
88 LSBX : ns = getX ? MSBX : wait3;
89 wait3 : ns = getX ? MSBX : wait3;
90 MSBX : ns = getX ? MSBX : wait4;
91 wait4 : ns = calc;
92 calc : ns = cout ? done : calc;
93 done : ns = start ? Idle : done;
94 default: ns=done;
95 endcase
96 end
97
98 always @(ps) begin
99 {ldX, ldA, ldR, inSrcX, inSrcA, Xsrc, ready, MSBrst,Crst} = 9'b0;
100 case (ps)
101 Idle : begin MSBrst = 1'b1; Crst = 1'b1; end
102 LSBA : begin ldA=1'b1; end
103 MSBA : begin inSrcA=1'b1; end
104 wait1 : begin ldA=1'b1; end
105 wait2 : begin ldA=1'b1; inSrcA=1'b1; end
106 LSBX : begin ldX=1'b1; Xsrc=1'b1; end
107 wait3 : begin ldA=1'b1; Xsrc=1'b1; end
108 MSBX : begin inSrcX=1'b1; end
109 wait4 : begin ldX=1'b1; Xsrc=1'b1; inSrcX=1'b1; end
110 calc : begin ldR=1'b1; ldX=1'b1; Cen=1'b1; end
111 done : ready = 1'b1;
112 default : {ldX, ldA, ldR, inSrcX, inSrcA, Xsrc, ready, MSBrst,Crst} = 9'b0;
113 endcase
114 end
115 always @(posedge clk, posedge rst) begin
116 if(rst) ps<=done;
117 else ps<=ns;
118 end
119 endmodule
120
```

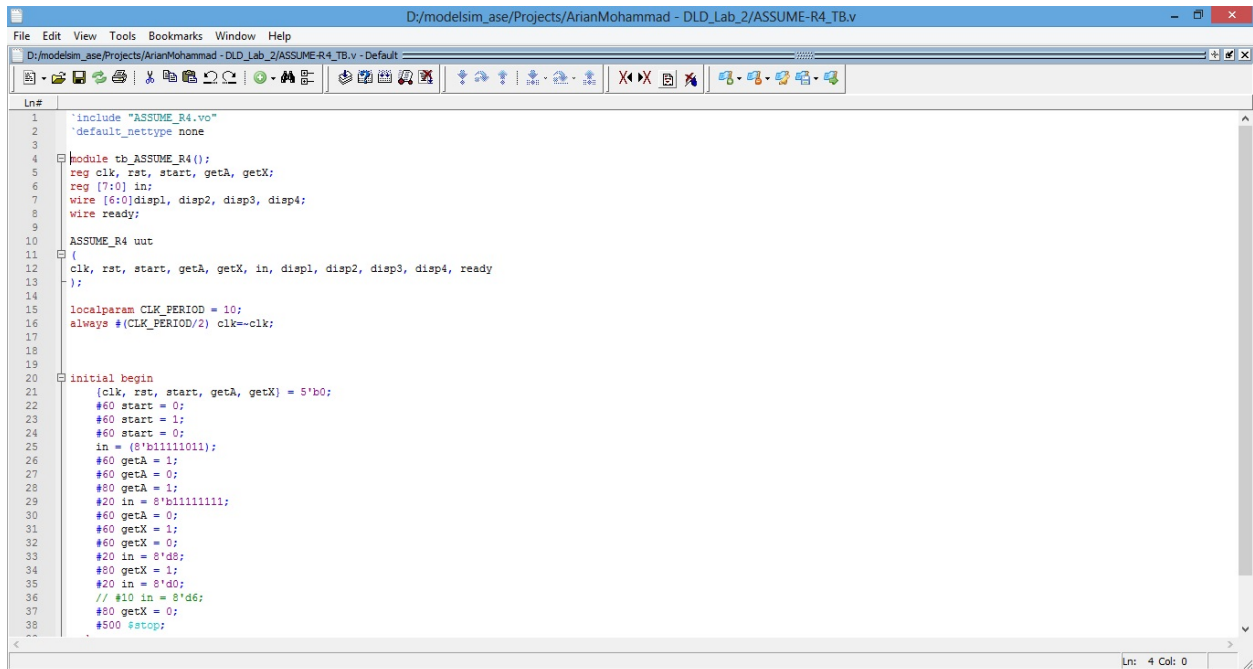

Quartus RTL viewer output



Quartus output Verilog code

```
D:/modelsim_ase/Projects/ArianMohammad - DLD_Lab_2/simulation/modelsim/ASSUME_R4.vo
File Edit View Tools Bookmarks Window Help
D:/modelsim_ase/Projects/ArianMohammad - DLD_Lab_2/simulation/modelsim/ASSUME_R4.vo - Default
Ln#
20 // DATE "05/18/2022 21:46:57"
21
22 //
23 // Device: Altera EP4CE6E22C6 Package TQFP144
24 //
25
26 //
27 // This Verilog file should be used for ModelSim-Altera (Verilog) only
28 //
29
30 `timescale 1 ps/ 1 ps
31
32 module ASSUME_R4 (
33     clk,
34     rst,
35     start,
36     getA,
37     getX,
38     in,
39     disp1,
40     disp2,
41     disp3,
42     disp4,
43     ready);
44     input clk;
45     input rst;
46     input start;
47     input getA;
48     input getX;
49     input [7:0] in;
50     output [6:0] disp1;
51     output [6:0] disp2;
52     output [6:0] disp3;
53     output [6:0] disp4;
54     output ready;
55
56 // Design Ports Information
57 // disp1[0] => Location: PIN_112, I/O Standard: 3.3-V LVTTL, Current Strength: 8mA
58 // disp2[0] => Location: PIN_112, I/O Standard: 3.3-V LVTTL, Current Strength: 8mA
59 // disp3[0] => Location: PIN_112, I/O Standard: 3.3-V LVTTL, Current Strength: 8mA
60 // disp4[0] => Location: PIN_112, I/O Standard: 3.3-V LVTTL, Current Strength: 8mA
61 // ready[0] => Location: PIN_112, I/O Standard: 3.3-V LVTTL, Current Strength: 8mA
62
63 endmodule
```

Quartus Verilog output Test Bench



The screenshot shows a Verilog testbench file named `ASSUME_R4_TB.v` in the Quartus IDE. The code is as follows:

```
1  `include "ASSUME_R4.vo"
2  `default_nettype none
3
4  module tb_ASSUME_R4();
5      reg clk, rst, start, getA, getX;
6      reg [7:0] in;
7      wire [6:0] displ, disp2, disp3, disp4;
8      wire ready;
9
10     ASSUME_R4 uut
11     (
12         clk, rst, start, getA, getX, in, displ, disp2, disp3, disp4, ready
13     );
14
15     localparam CLK_PERIOD = 10;
16     always # (CLK_PERIOD/2) clk=~clk;
17
18
19
20     initial begin
21         {clk, rst, start, getA, getX} = 5'b0;
22         #60 start = 0;
23         #60 start = 1;
24         #60 start = 0;
25         in = (8'b11111011);
26         #60 getA = 1;
27         #60 getA = 0;
28         #60 getA = 1;
29         #20 in = 8'b11111111;
30         #60 getA = 0;
31         #60 getX = 1;
32         #60 getX = 0;
33         #20 in = 8'd8;
34         #60 getX = 1;
35         #20 in = 8'd0;
36         // #10 in = 8'd6;
37         #80 getX = 0;
38         #500 $stop;
```

The IDE window title is `D:/modelsim_ase/Projects/ArianMohammad - DLD_Lab_2/ASSUME-R4_TB.v`. The status bar at the bottom right shows `Ln: 4 Col: 0`.

As you can see in above image, product of inputs (3 and 4) is shown on FPGA's seven segments