

EXPERIMENT 3

Group's Members:

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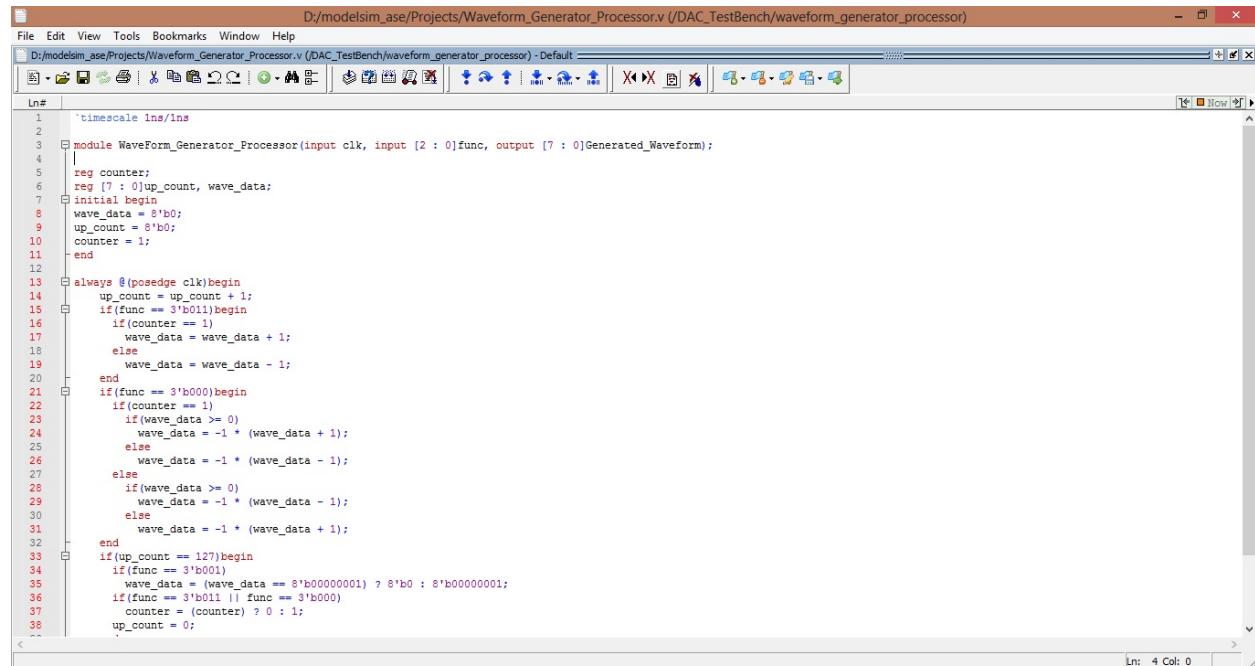
Arian Niakan 810198536

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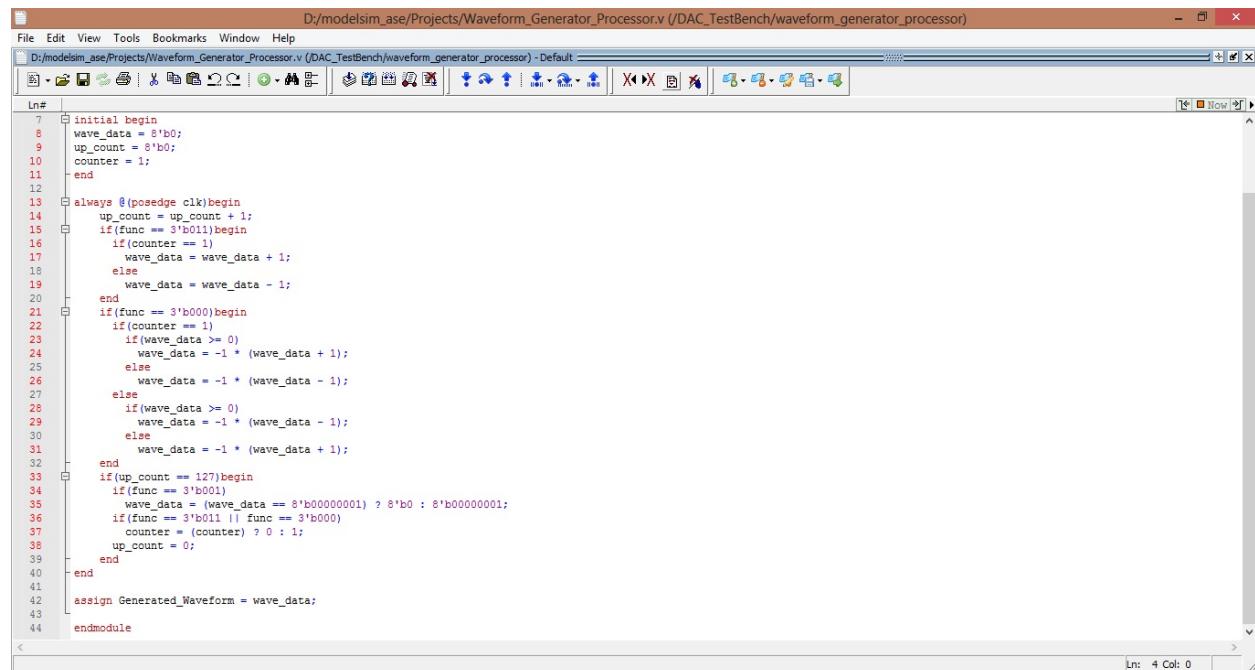
2 Waveform Generator

Waveform Generator Processor Verilog code



The screenshot shows the ModelSim IDE interface with the file `D:/modelsim_ase/Projects/Waveform_Generator_Processor.v` open. The code implements a waveform generator processor with the following structure:

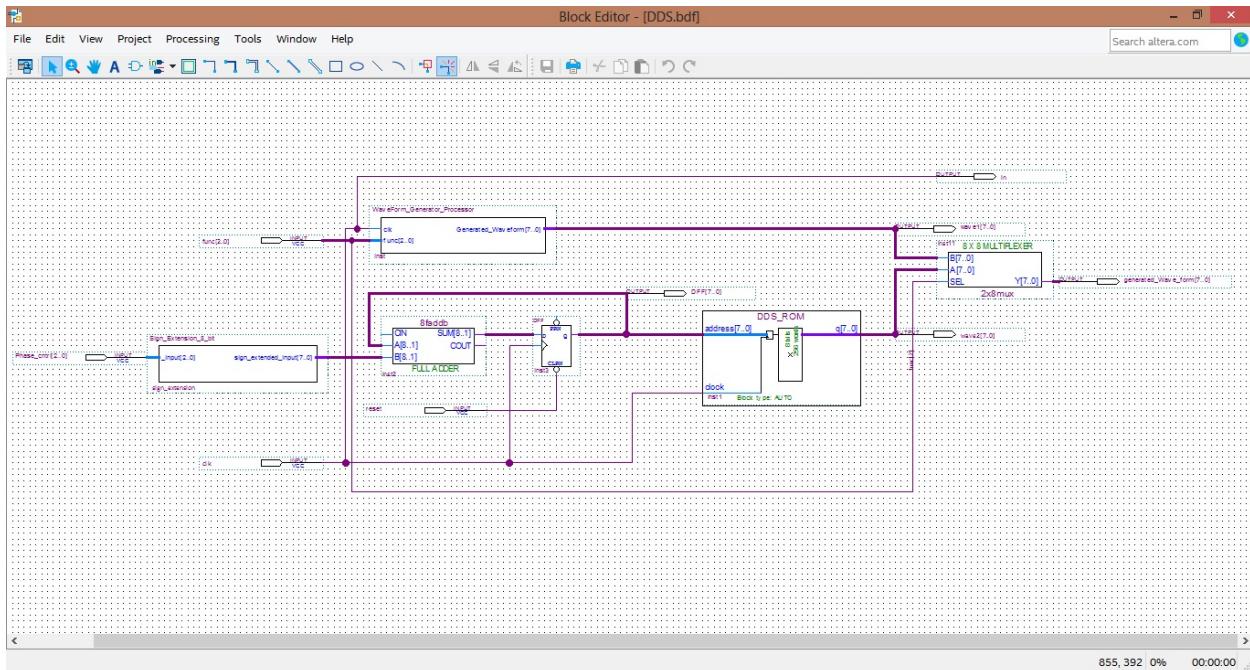
```
1 `timescale 1ns/1ns
2
3 module WaveForm_Generator_Processor(input clk, input [2 : 0]func, output [7 : 0]Generated_Waveform);
4
5   reg counter;
6   reg [7 : 0]up_count, wave_data;
7
8   initial begin
9     wave_data = 8'b0;
10    up_count = 8'b0;
11    counter = 1;
12  end
13
14  always @(posedge clk)begin
15    up_count = up_count + 1;
16    if(func == 3'b011)begin
17      if(counter == 1)
18        wave_data = wave_data + 1;
19      else
20        wave_data = wave_data - 1;
21    end
22    if(func == 3'b000)begin
23      if(counter == 1)
24        if(wave_data >= 0)
25          wave_data = -1 * (wave_data + 1);
26        else
27          wave_data = -1 * (wave_data - 1);
28      else
29        if(wave_data >= 0)
30          wave_data = -1 * (wave_data - 1);
31        else
32          wave_data = -1 * (wave_data + 1);
33    end
34    if(up_count == 127)begin
35      if(func == 3'b001)
36        wave_data = (wave_data == 8'b00000001) ? 8'b0 : 8'b00000001;
37      if(func == 3'b011 || func == 3'b000)
38        counter = (counter) ? 0 : 1;
39      up_count = 0;
40    end
41  end
42
43  assign Generated_Waveform = wave_data;
44
45 endmodule
```



This screenshot shows the same Verilog code as above, but with several lines highlighted in red, indicating errors or warnings. The highlighted lines are:

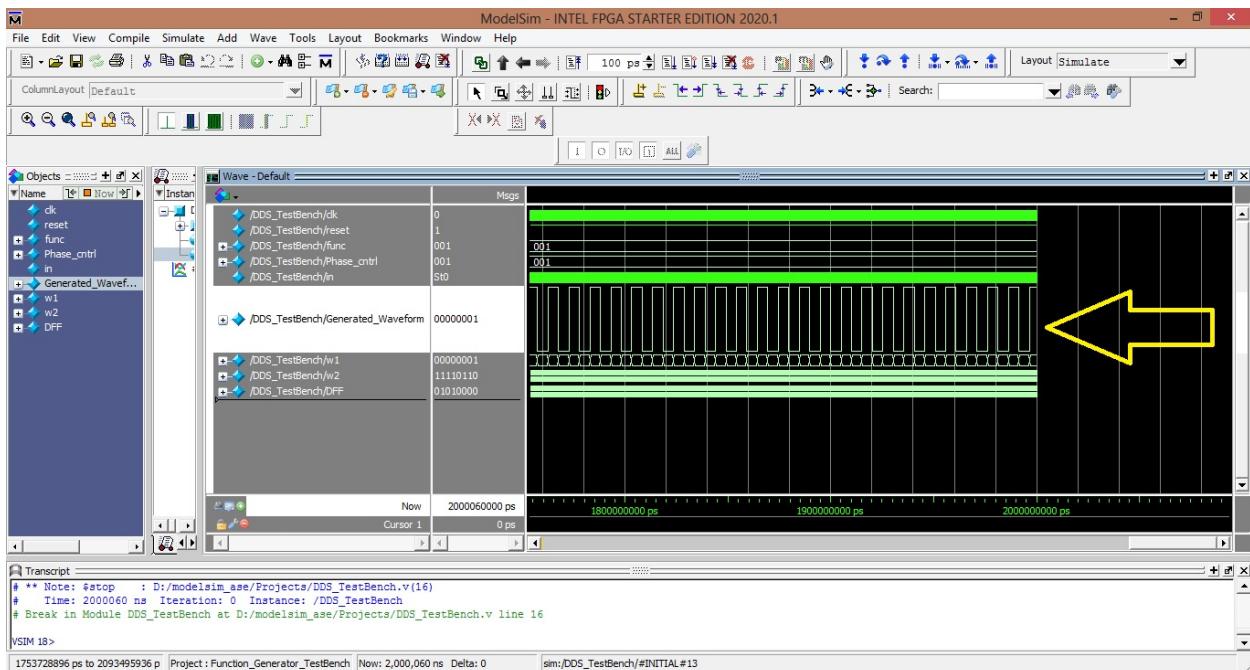
- Line 14: `always @(posedge clk)begin`
- Line 15: `up_count = up_count + 1;`
- Line 16: `if(func == 3'b011)begin`
- Line 17: `if(counter == 1)`
- Line 18: `wave_data = wave_data + 1;`
- Line 21: `end`
- Line 22: `if(func == 3'b000)begin`
- Line 23: `if(counter == 1)`
- Line 24: `if(wave_data >= 0)`
- Line 25: `wave_data = -1 * (wave_data + 1);`
- Line 26: `else`
- Line 27: `wave_data = -1 * (wave_data - 1);`
- Line 28: `else`
- Line 29: `if(wave_data >= 0)`
- Line 30: `wave_data = -1 * (wave_data - 1);`
- Line 31: `else`
- Line 32: `wave_data = -1 * (wave_data + 1);`
- Line 33: `end`
- Line 34: `if(up_count == 127)begin`
- Line 35: `if(func == 3'b001)`
- Line 36: `wave_data = (wave_data == 8'b00000001) ? 8'b0 : 8'b00000001;`
- Line 37: `if(func == 3'b011 || func == 3'b000)`
- Line 38: `counter = (counter) ? 0 : 1;`
- Line 39: `up_count = 0;`
- Line 40: `end`
- Line 41: `end`
- Line 42: `assign Generated_Waveform = wave_data;`
- Line 43: `endmodule`

DDS schematic diagram

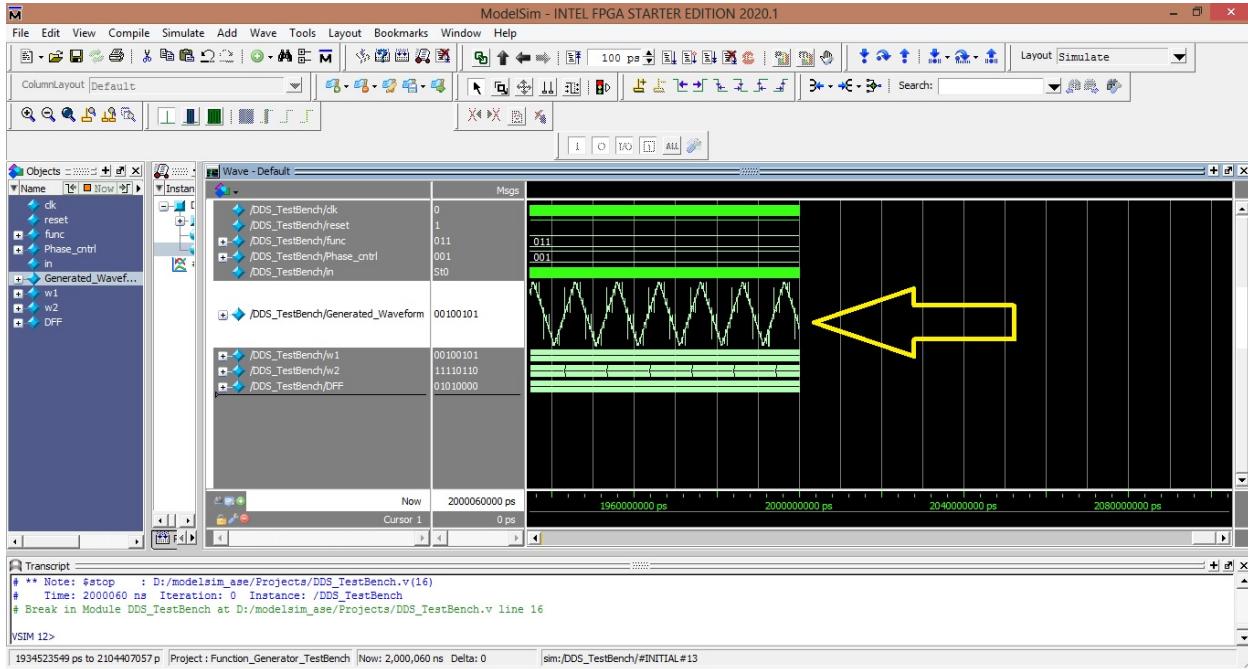


Simulation output of above DDS

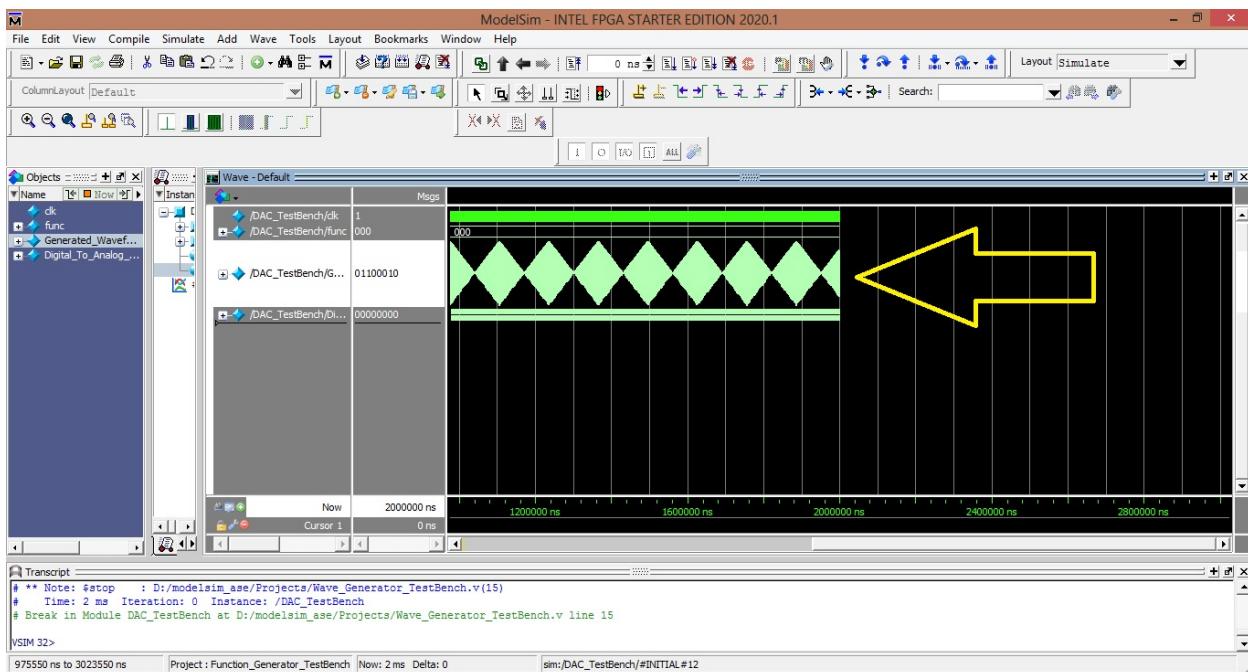
Square wave



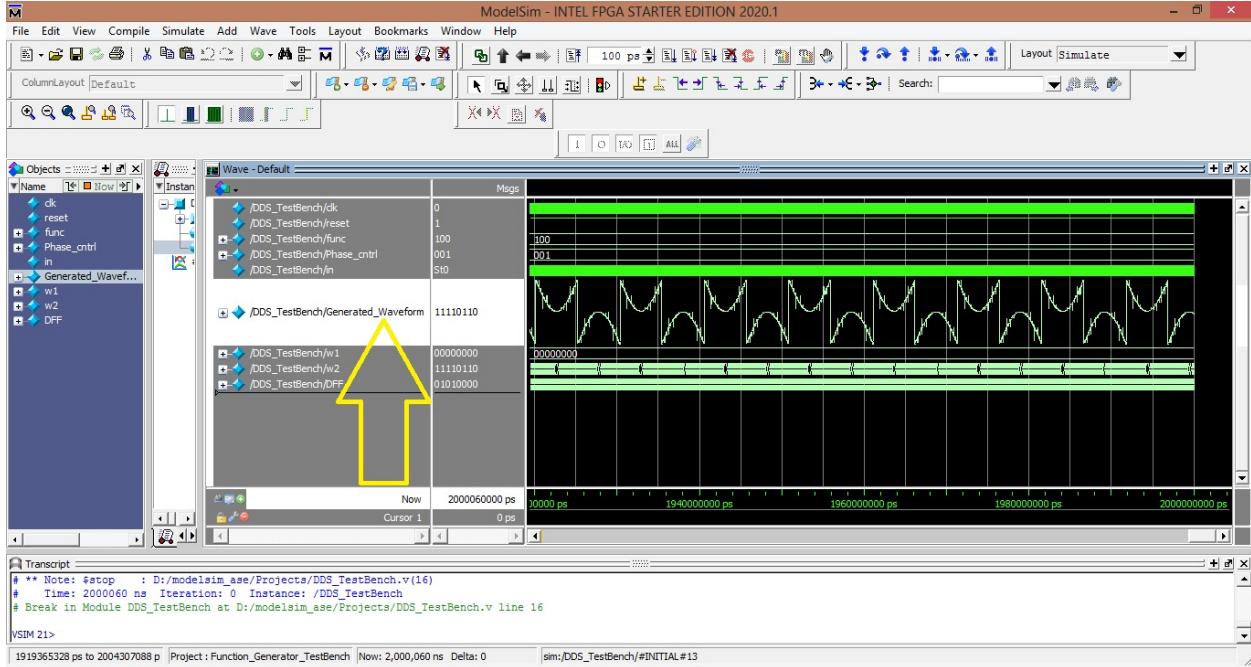
Triangle wave



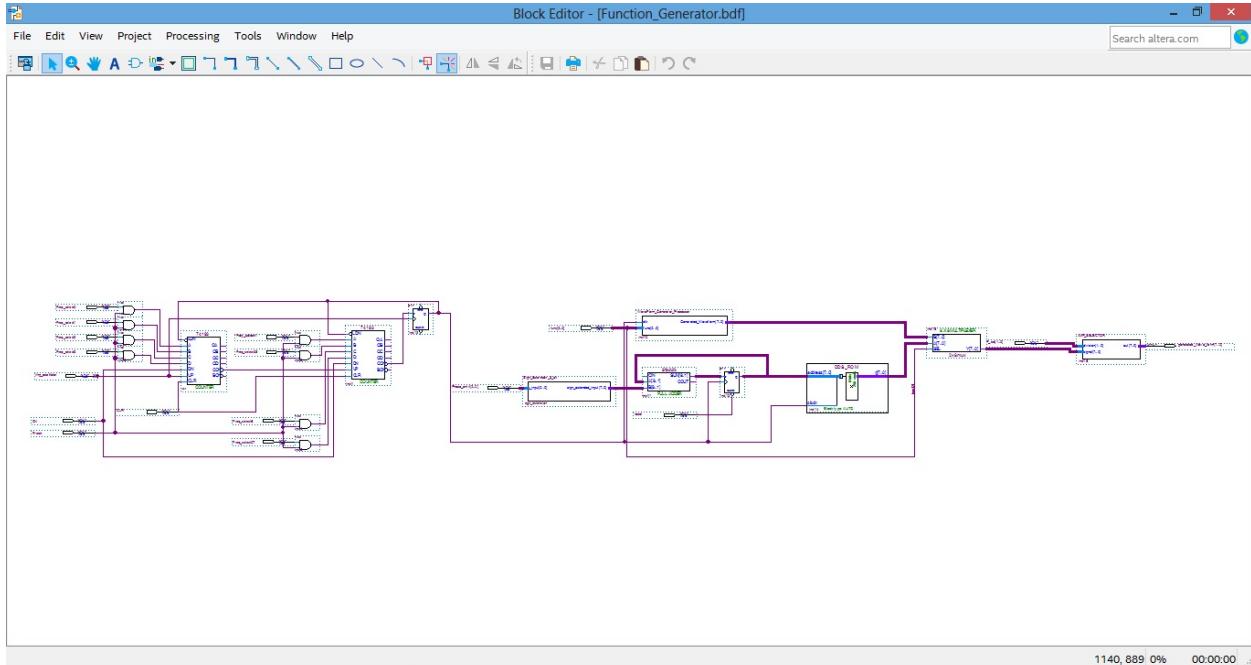
Rhomboid wave



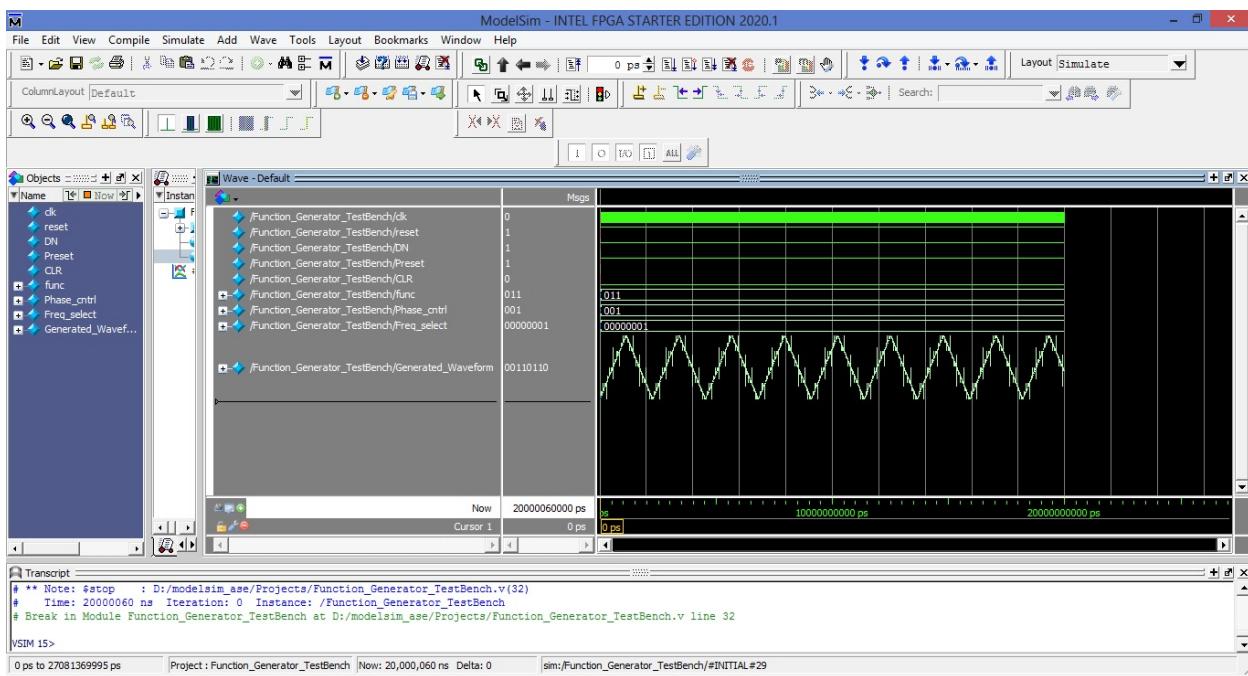
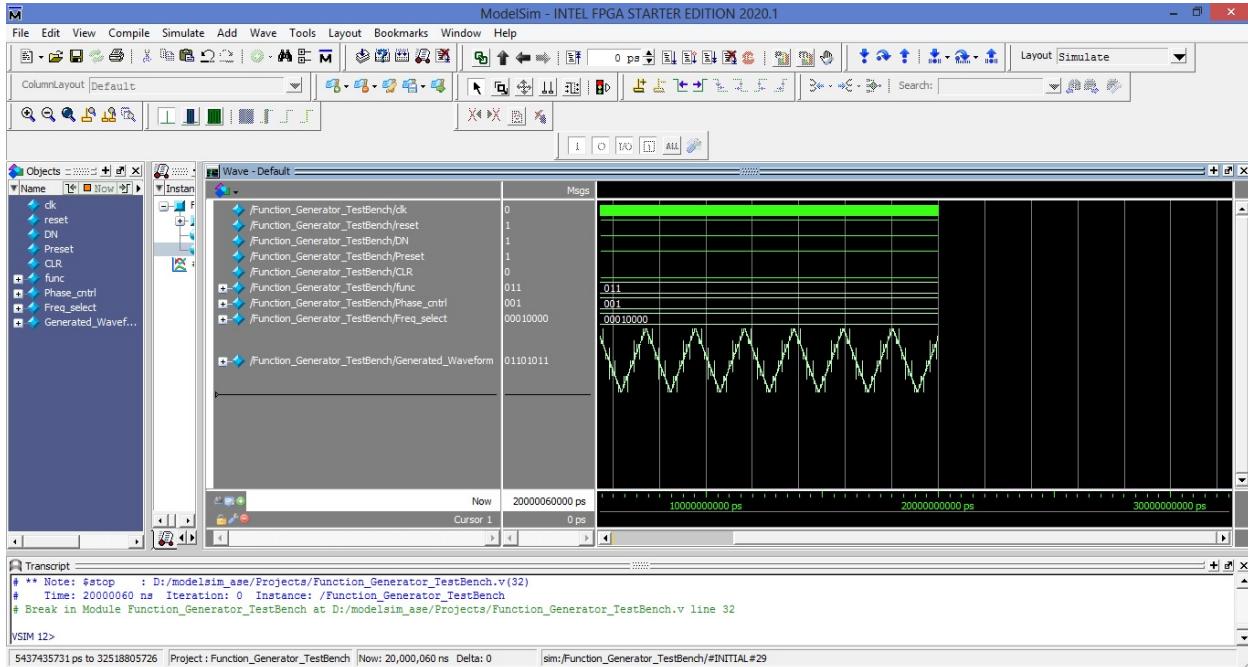
Sine wave



3 Frequency Selector

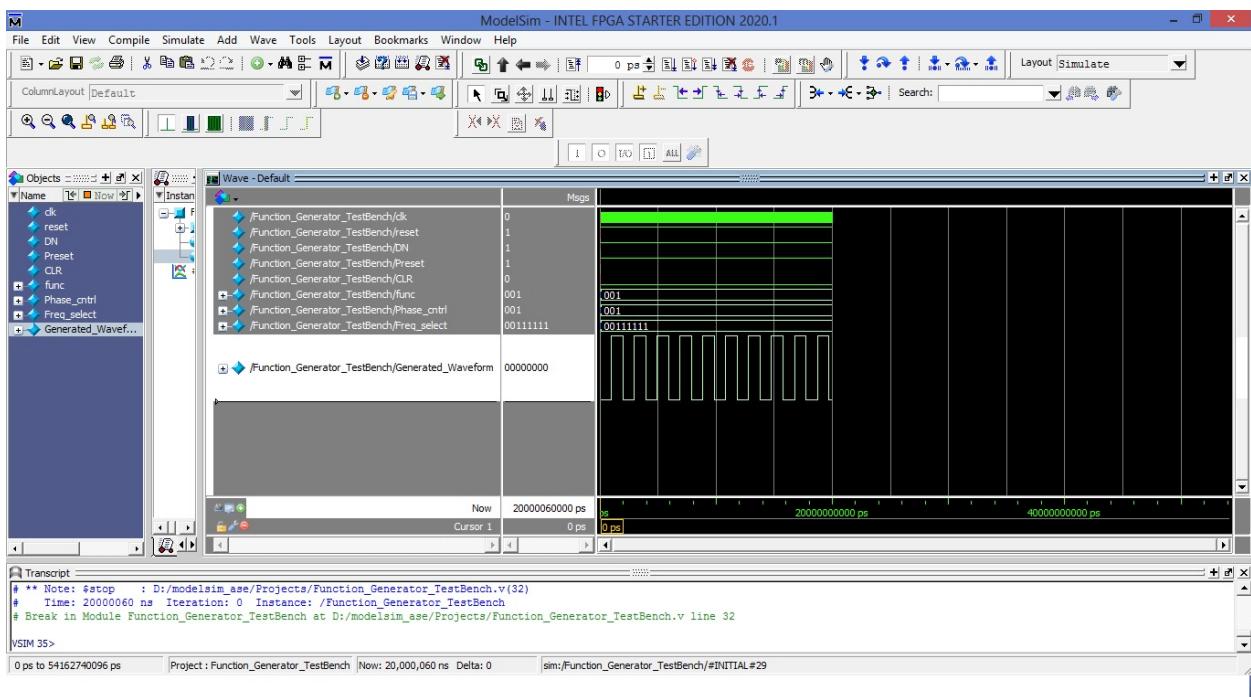
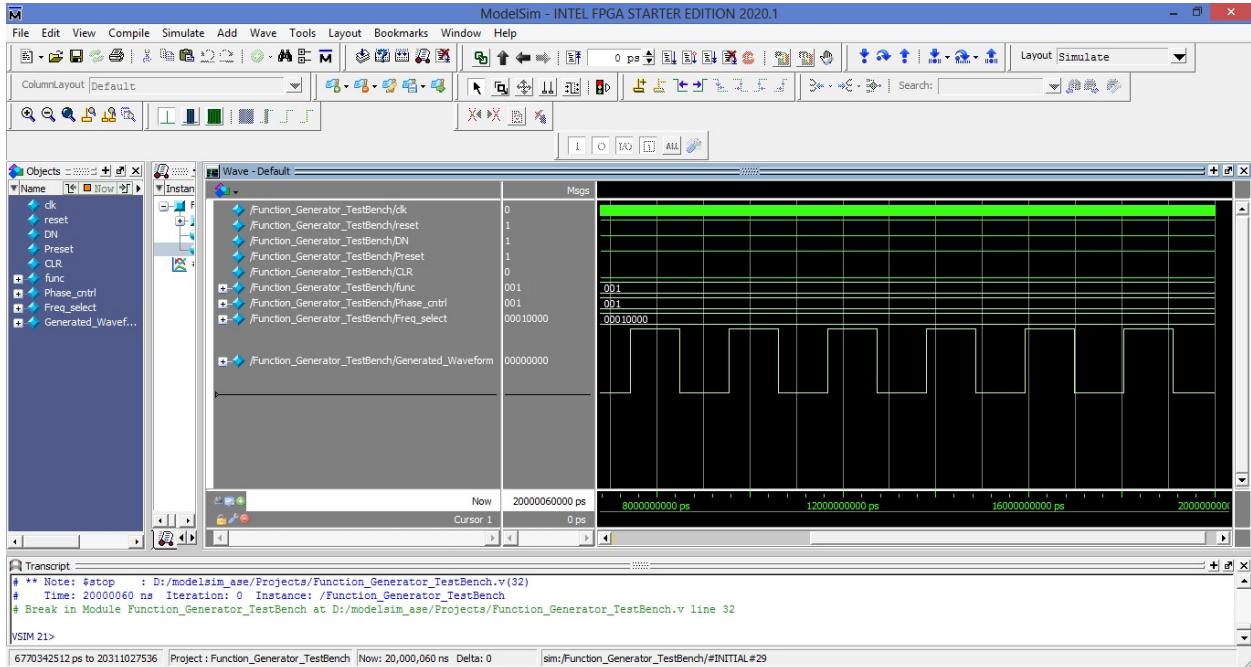


Triangle wave

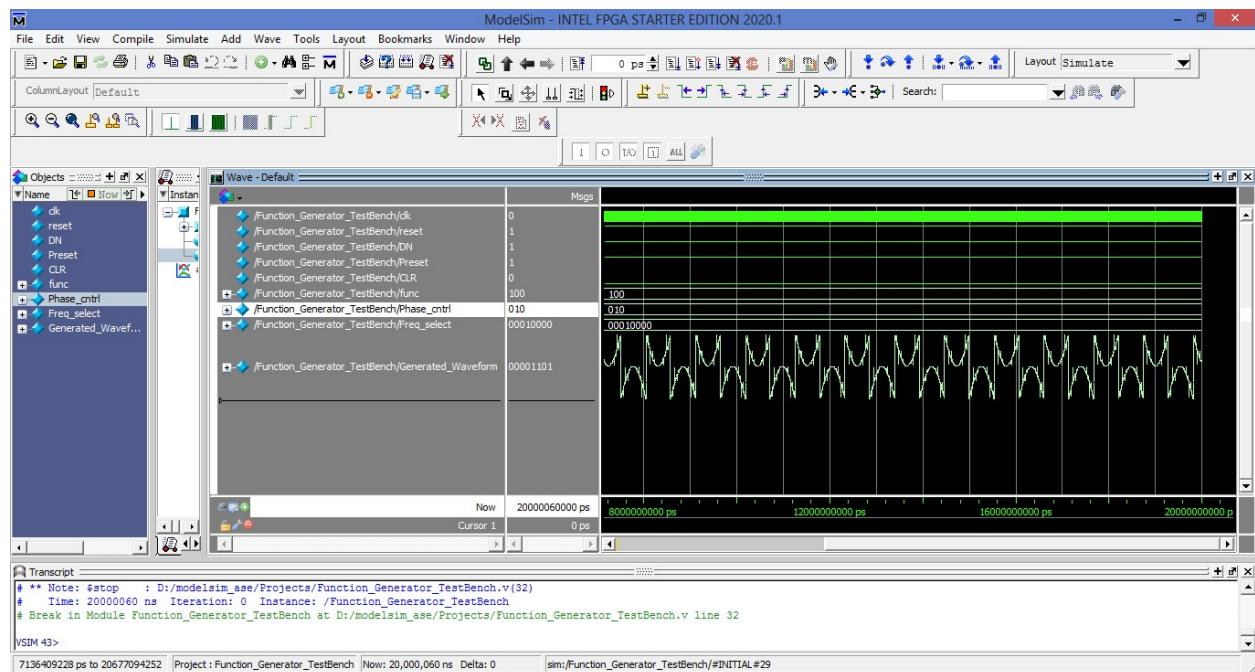
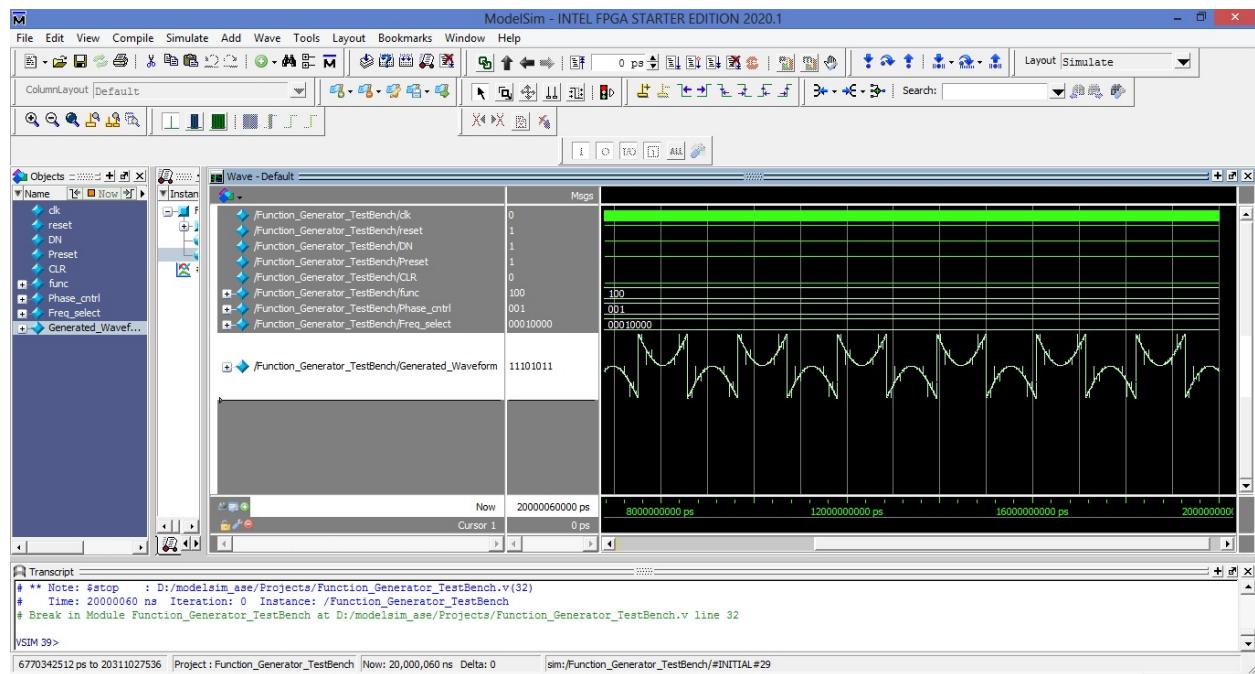


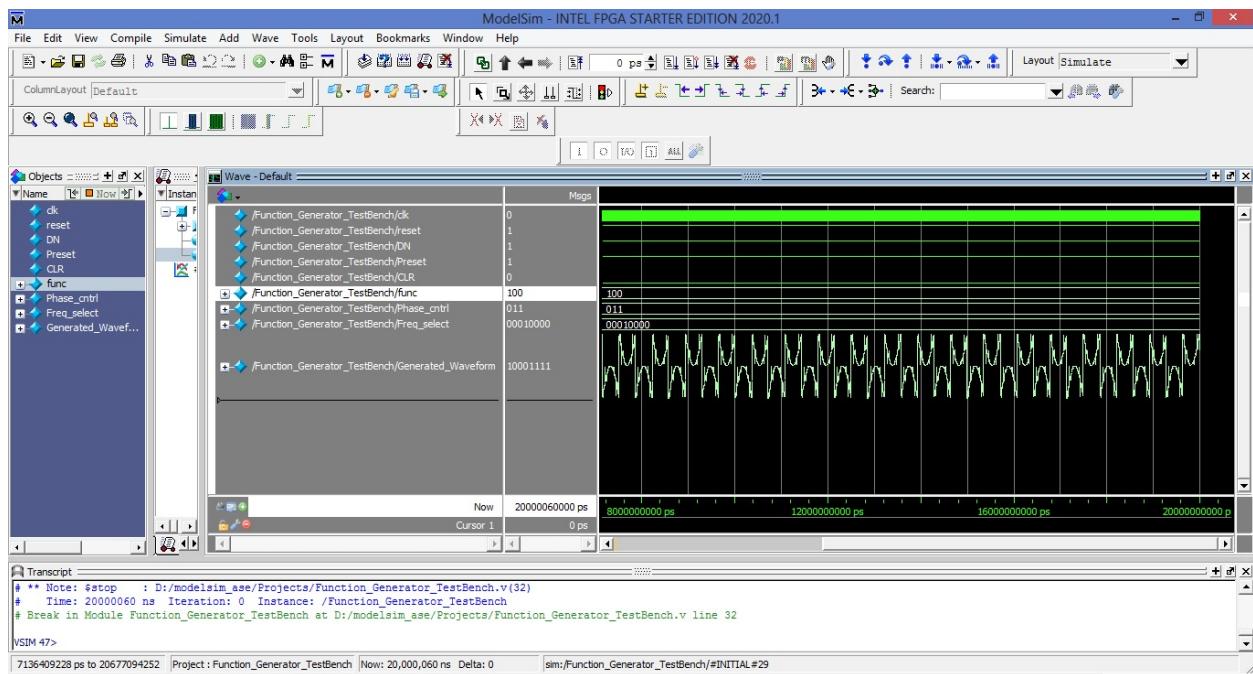
As you see, by increasing Freq_select input, frequency of signal has been increased thus number of periods has been increased

Square wave



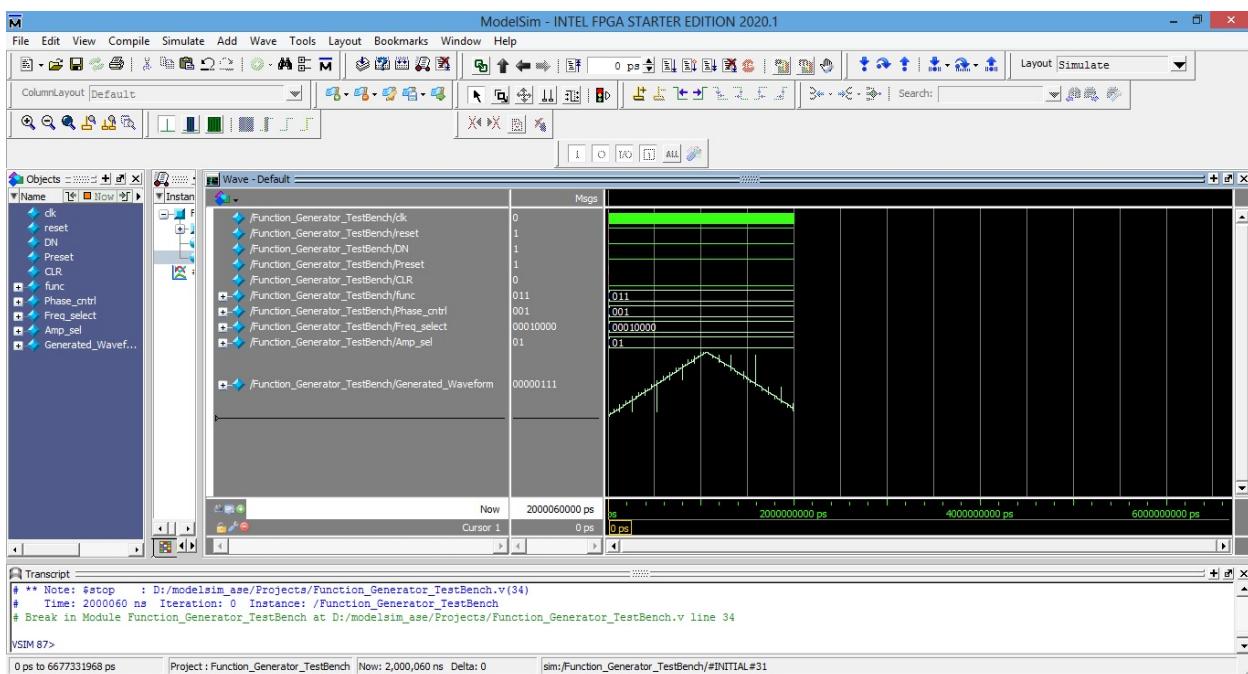
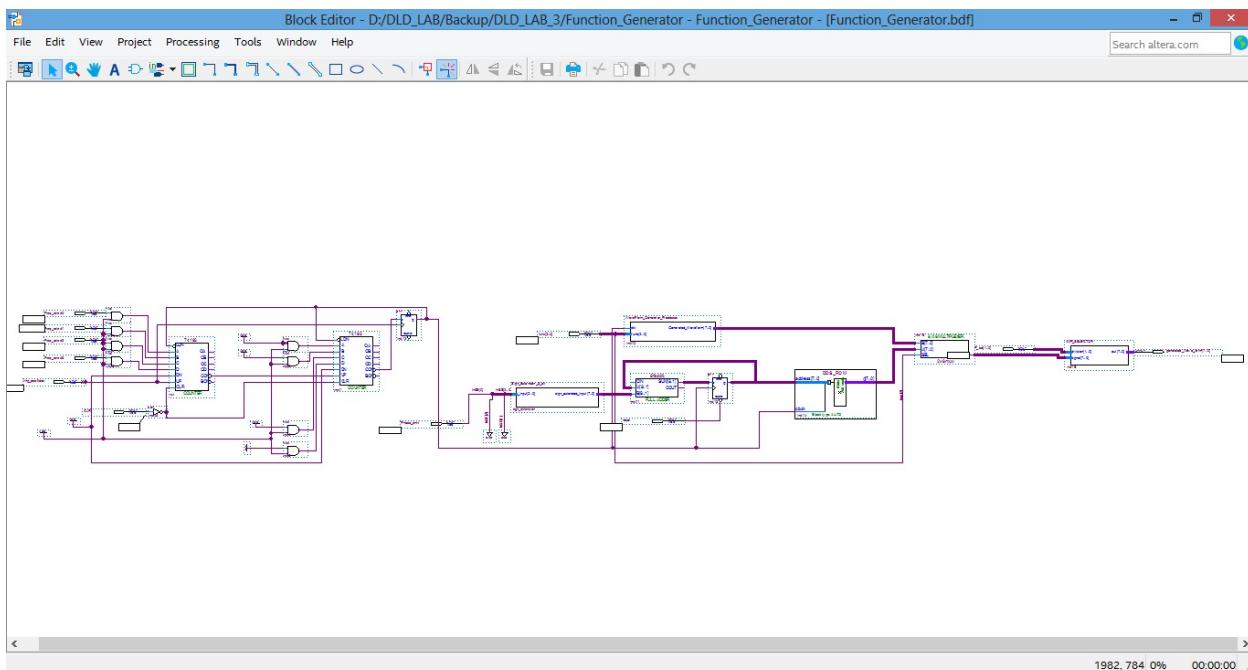
As you see, by increasing Freq_select input, frequency of signal has been increased thus number of periods has been increased

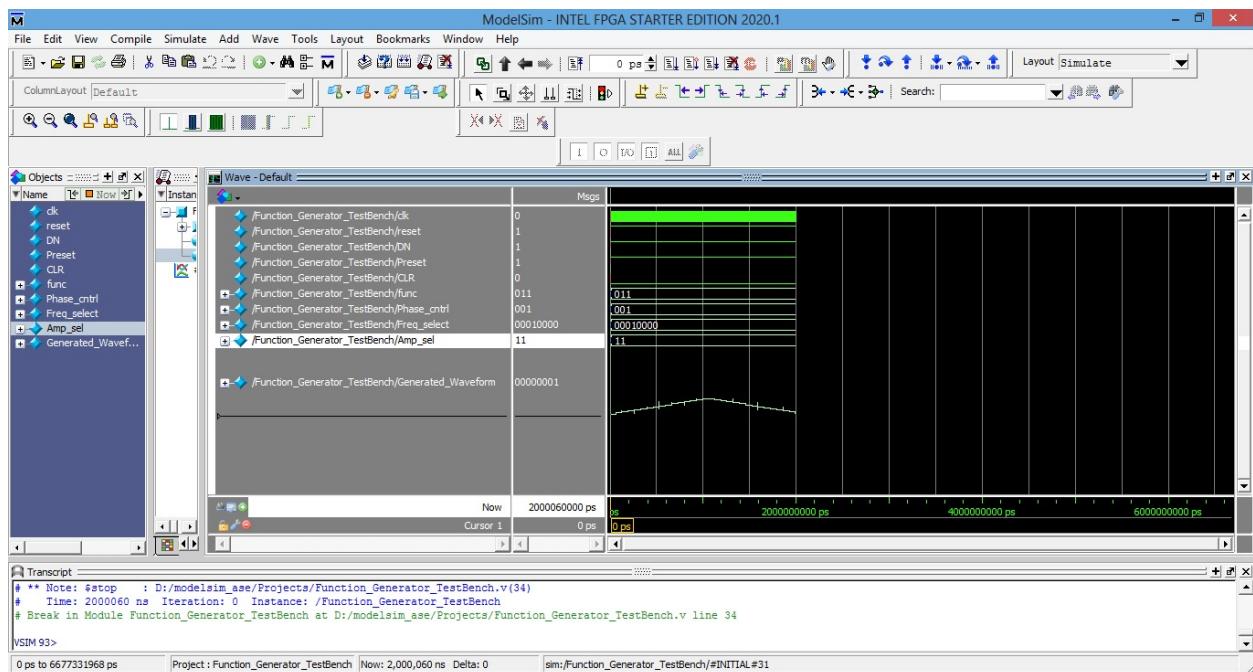
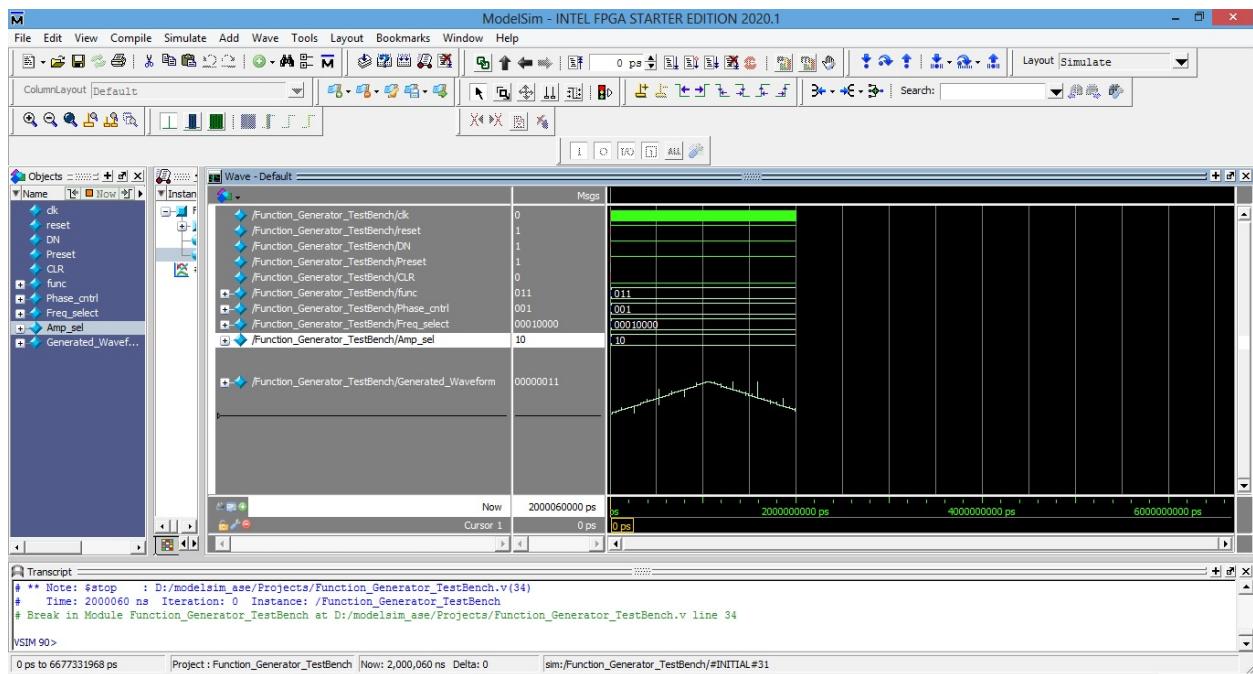




As you see, by increasing Phase_cntrl input, frequency of signal has been increased thus number of periods has been increased

4 Amplitude Selector





As you see, each time Amp_sel input increases, amplitude of signal is divided by 2.

