EXPERMINT 4

Group's members:

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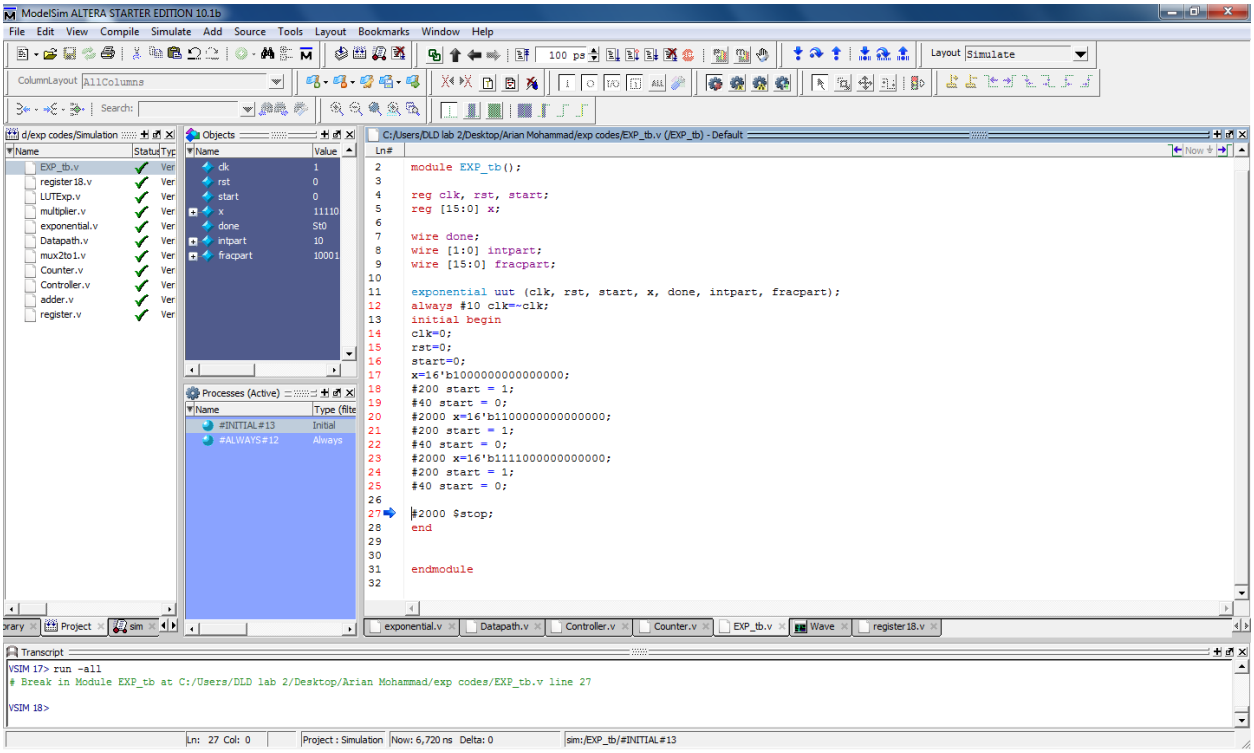
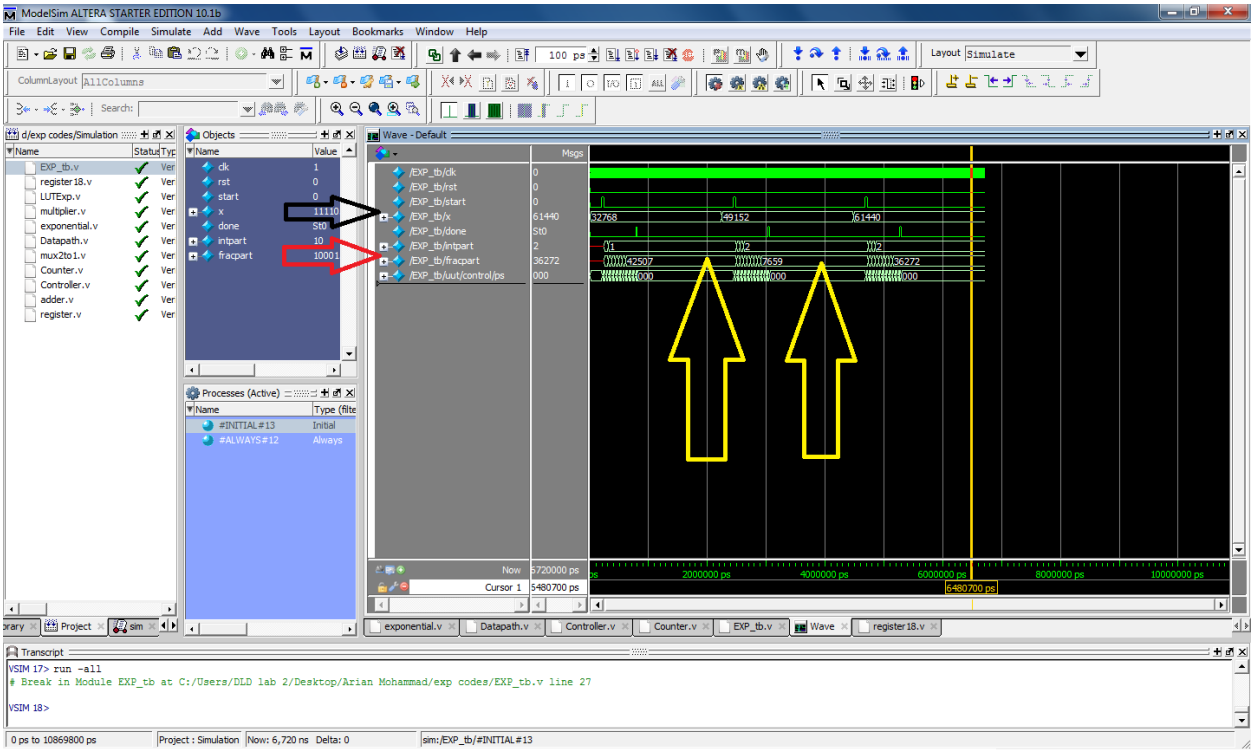
1. Exponential Engine

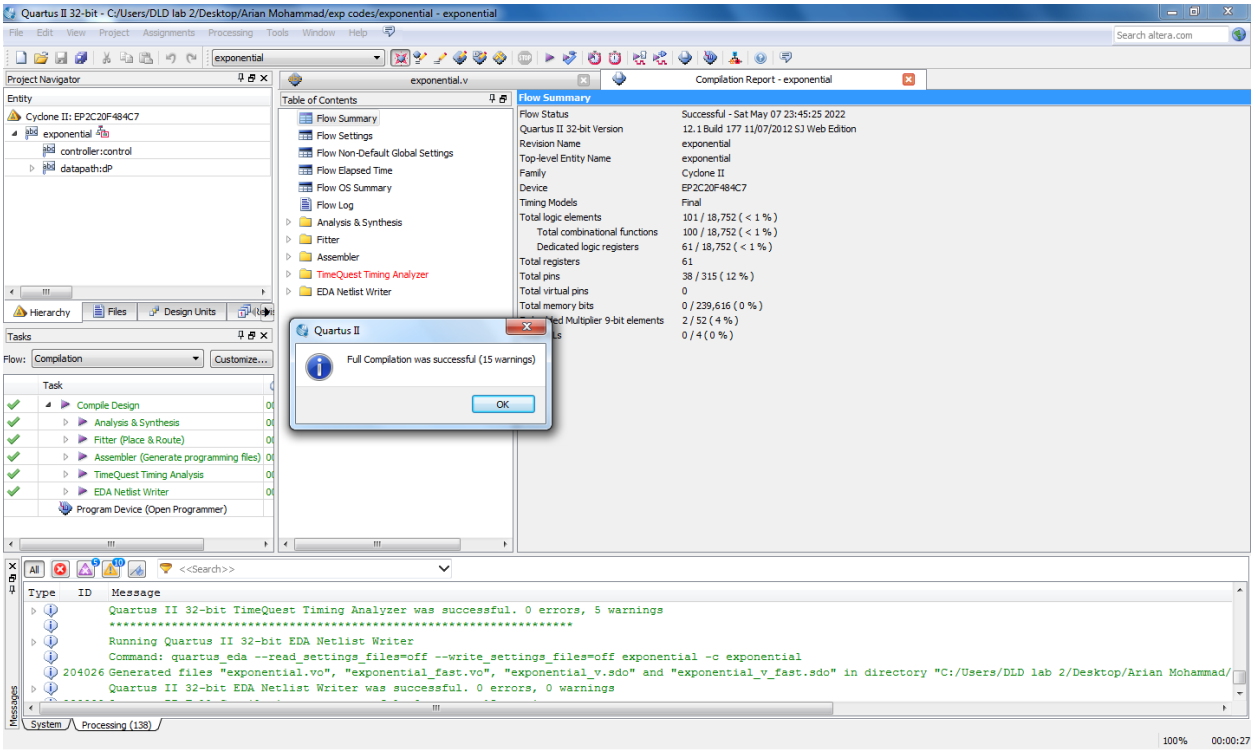
Exponential Engine Test Bench



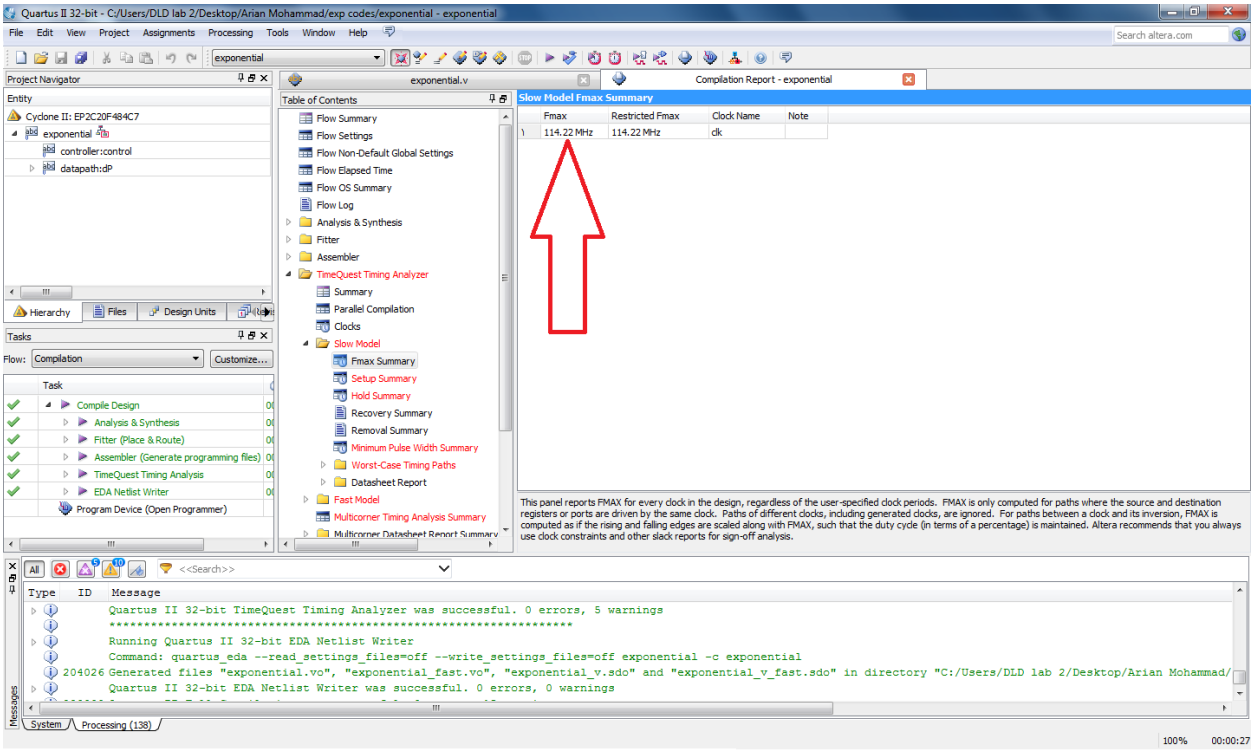
Simulation Output of above Exponential Engine Test Bench



Quartus Synthesis Report of Exponential Engine

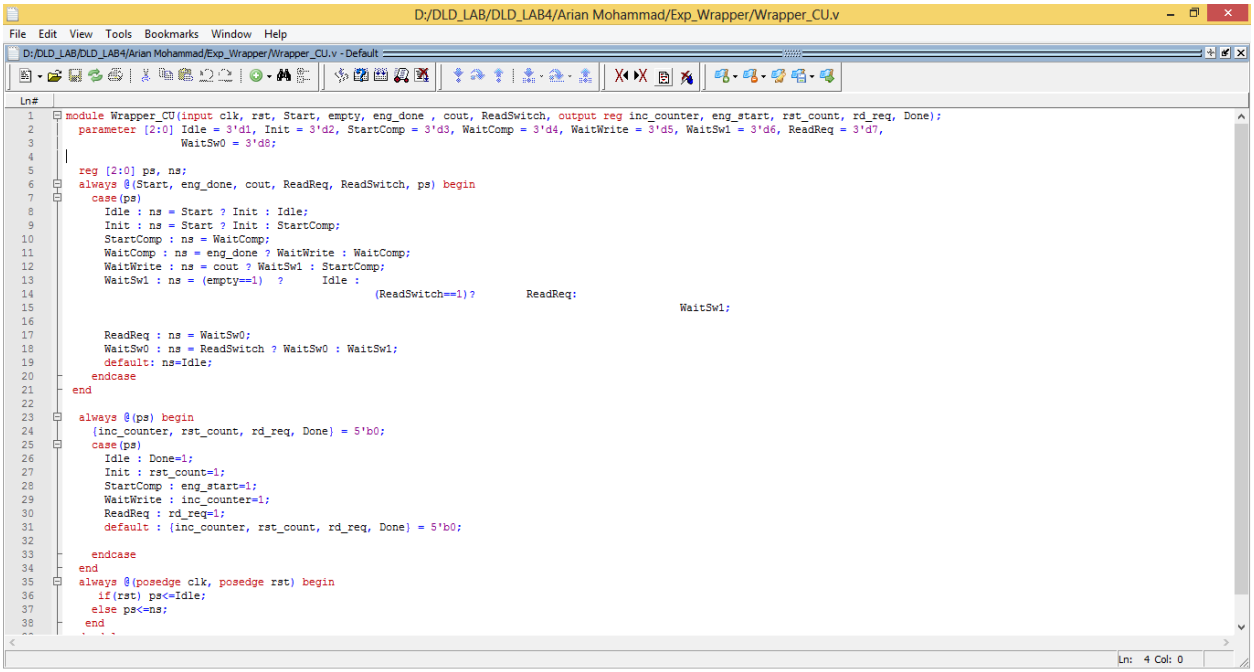


Maximum Frequency of Exponential Engine

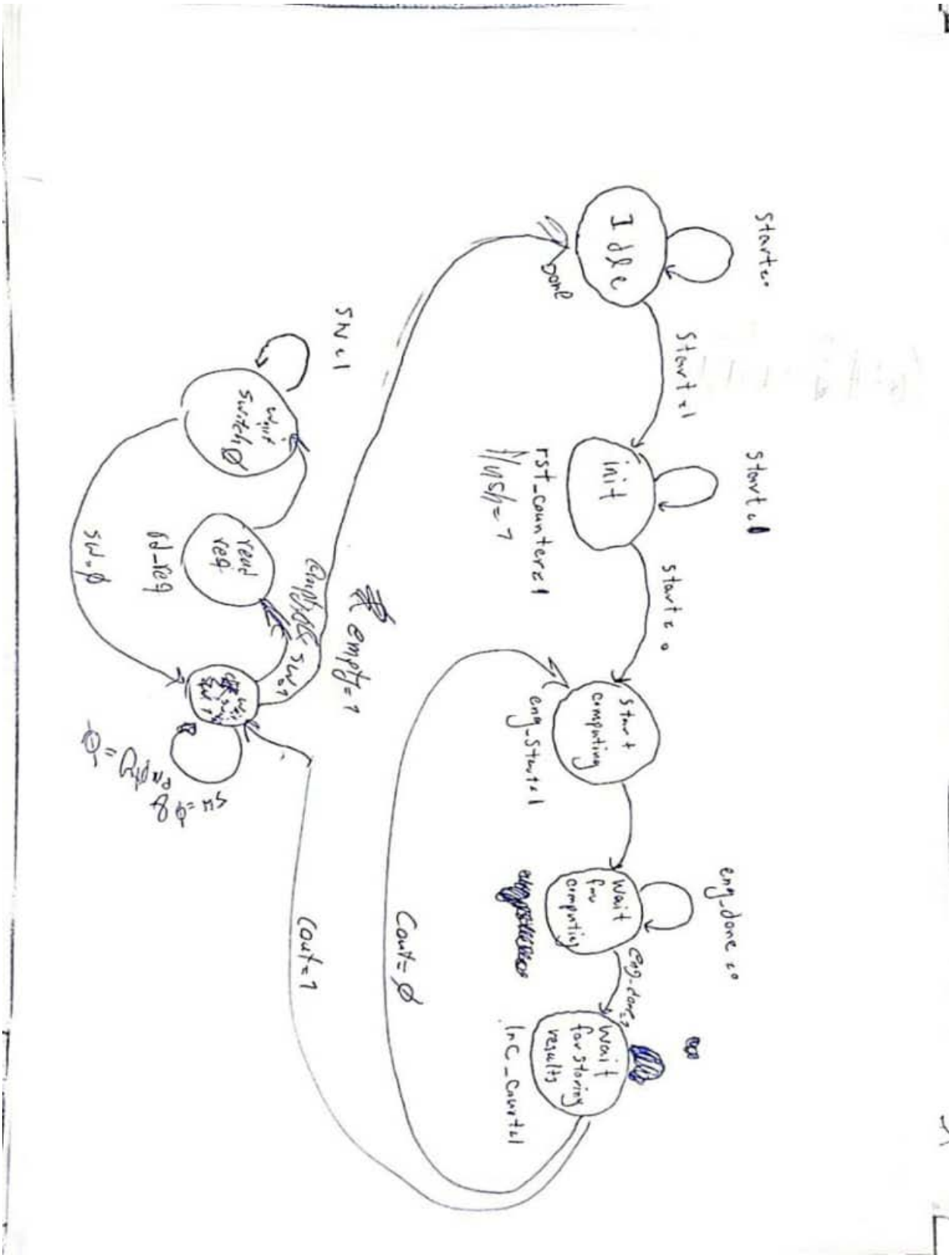


2.2 Wrapper Controller

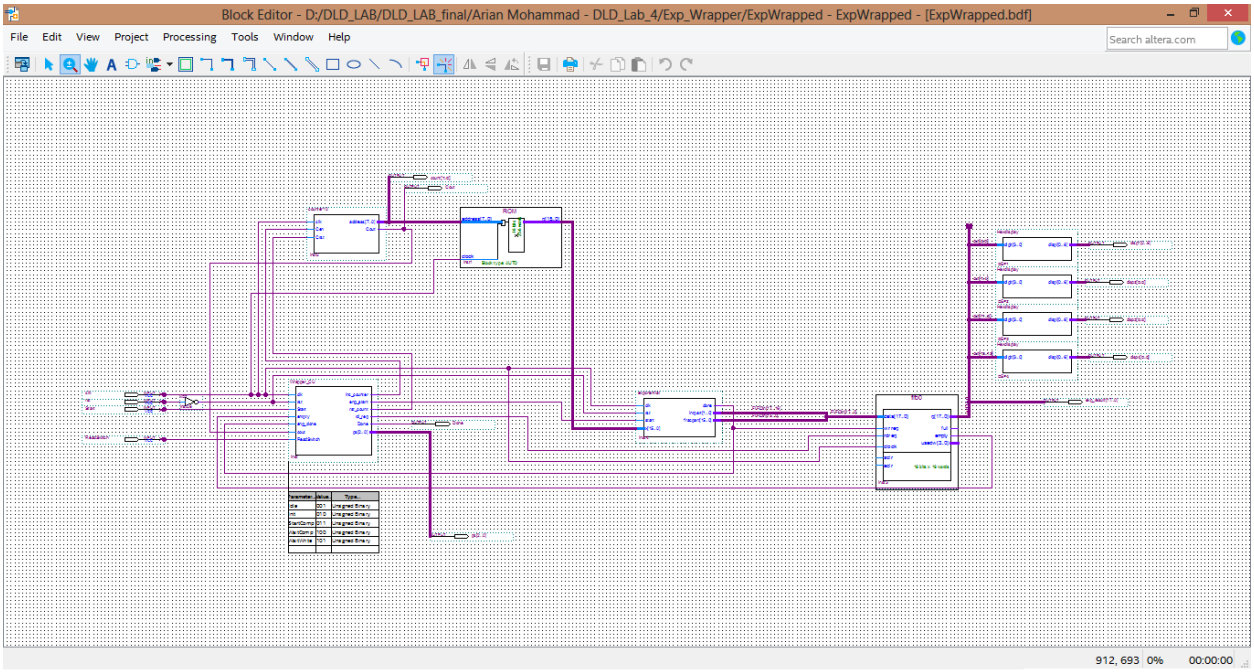
Wrapper Controller Verilog Code



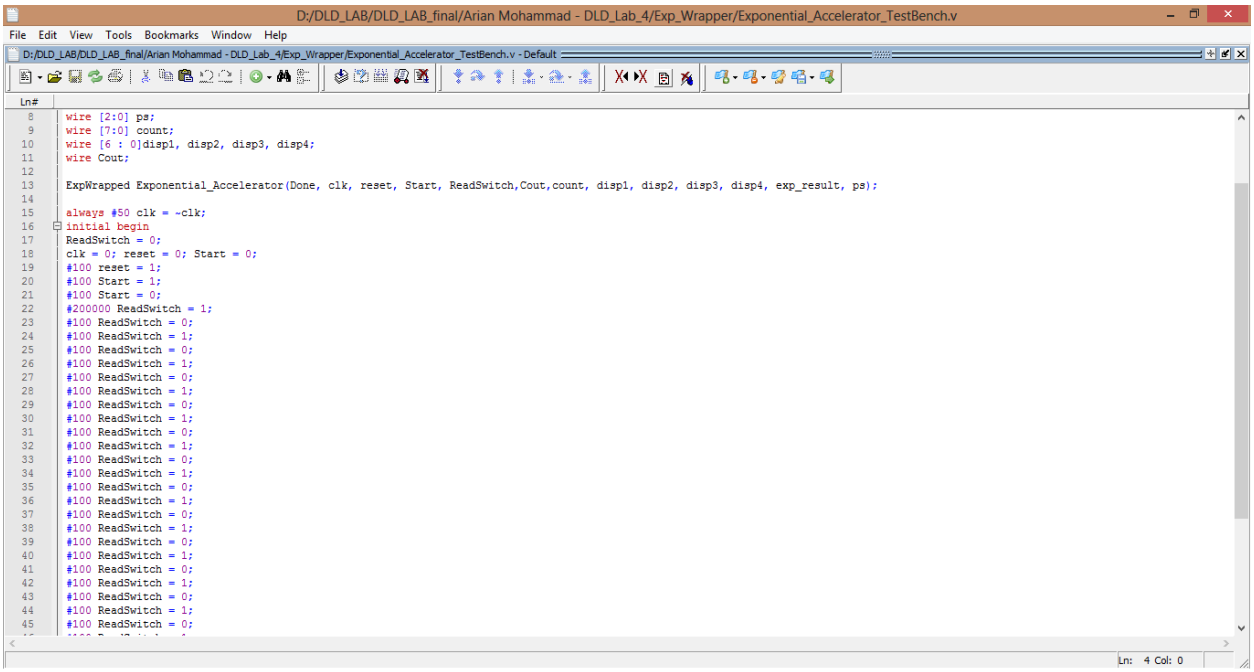
Wrapper Controller State Diagram`

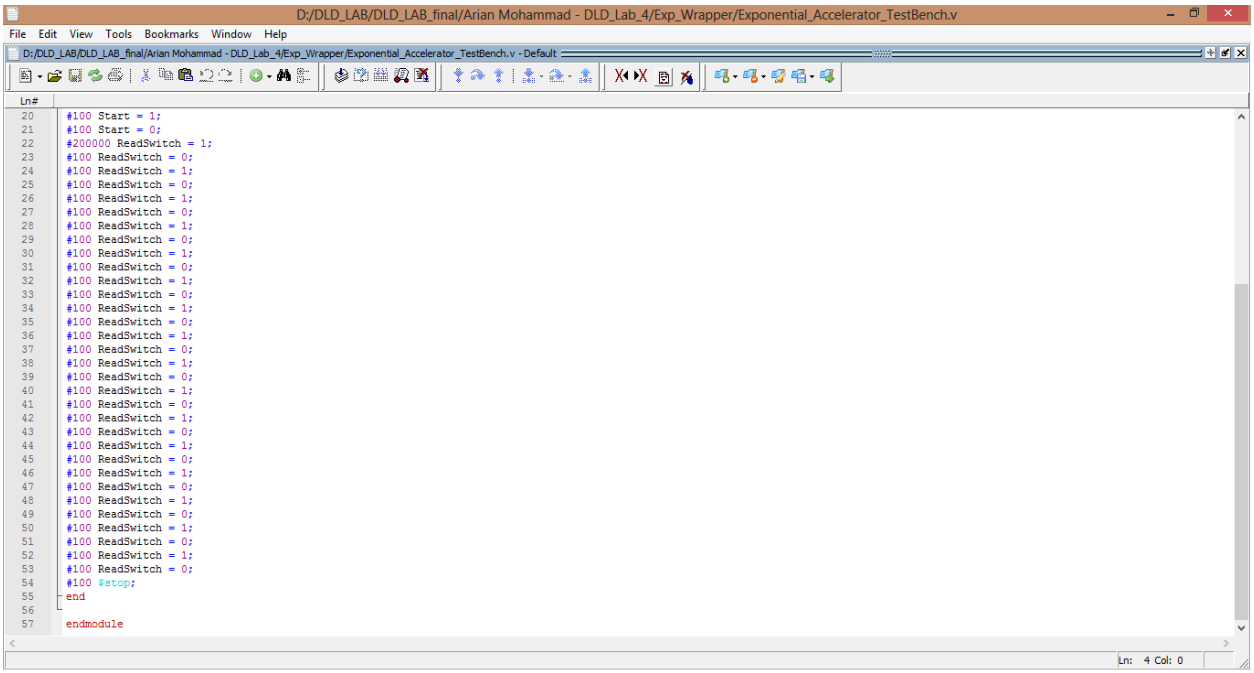


Exponential Accelerator Schematic Diagram

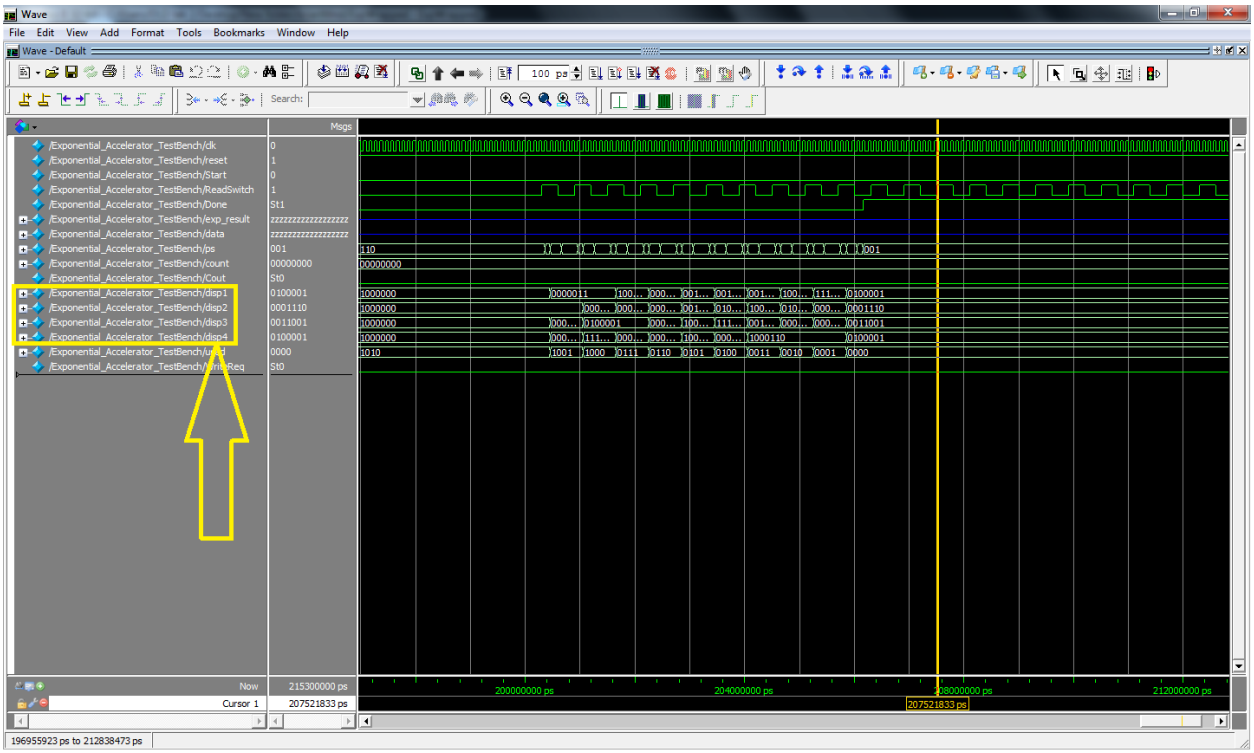


Exponential Accelerator Test Bench



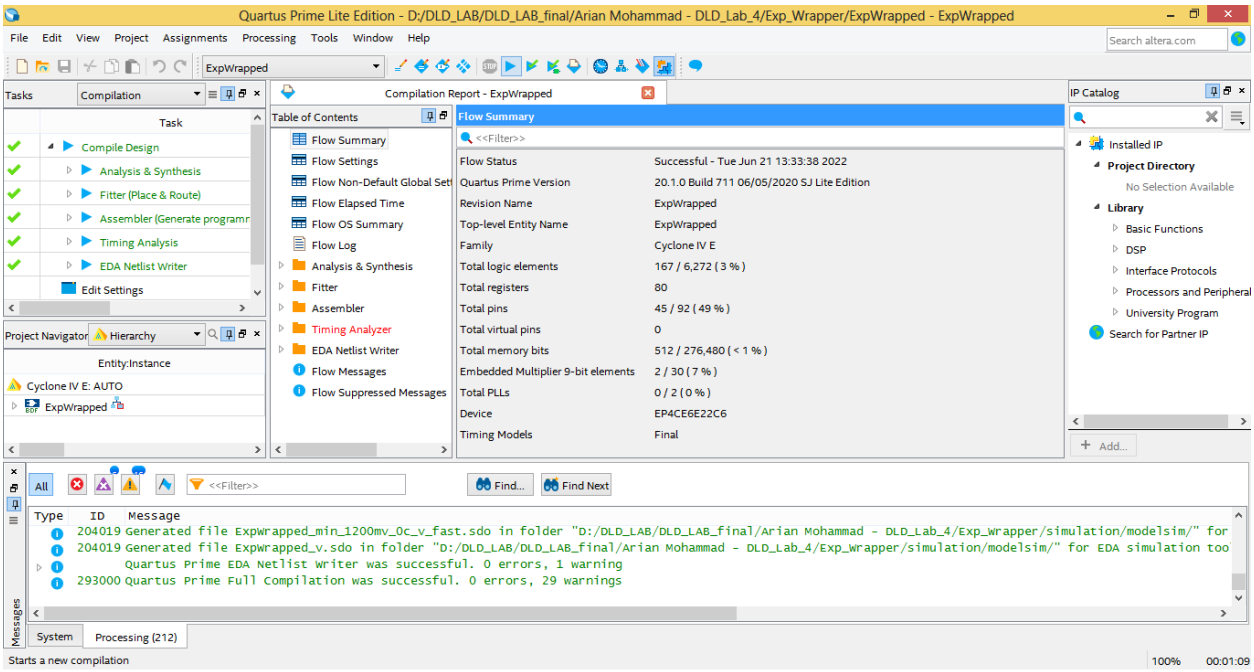


Simulation Output of above Exponential Accelerator Test Bench

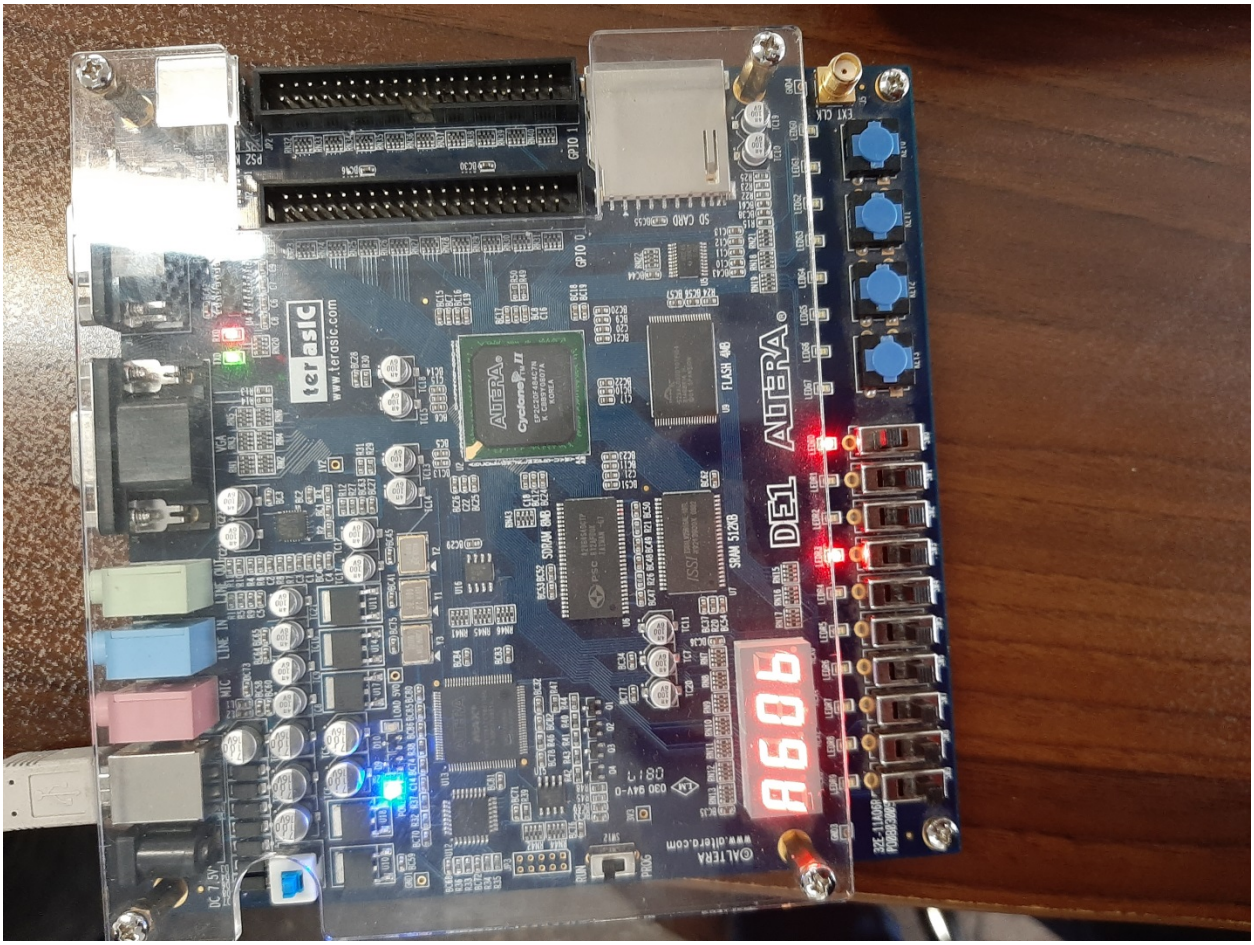


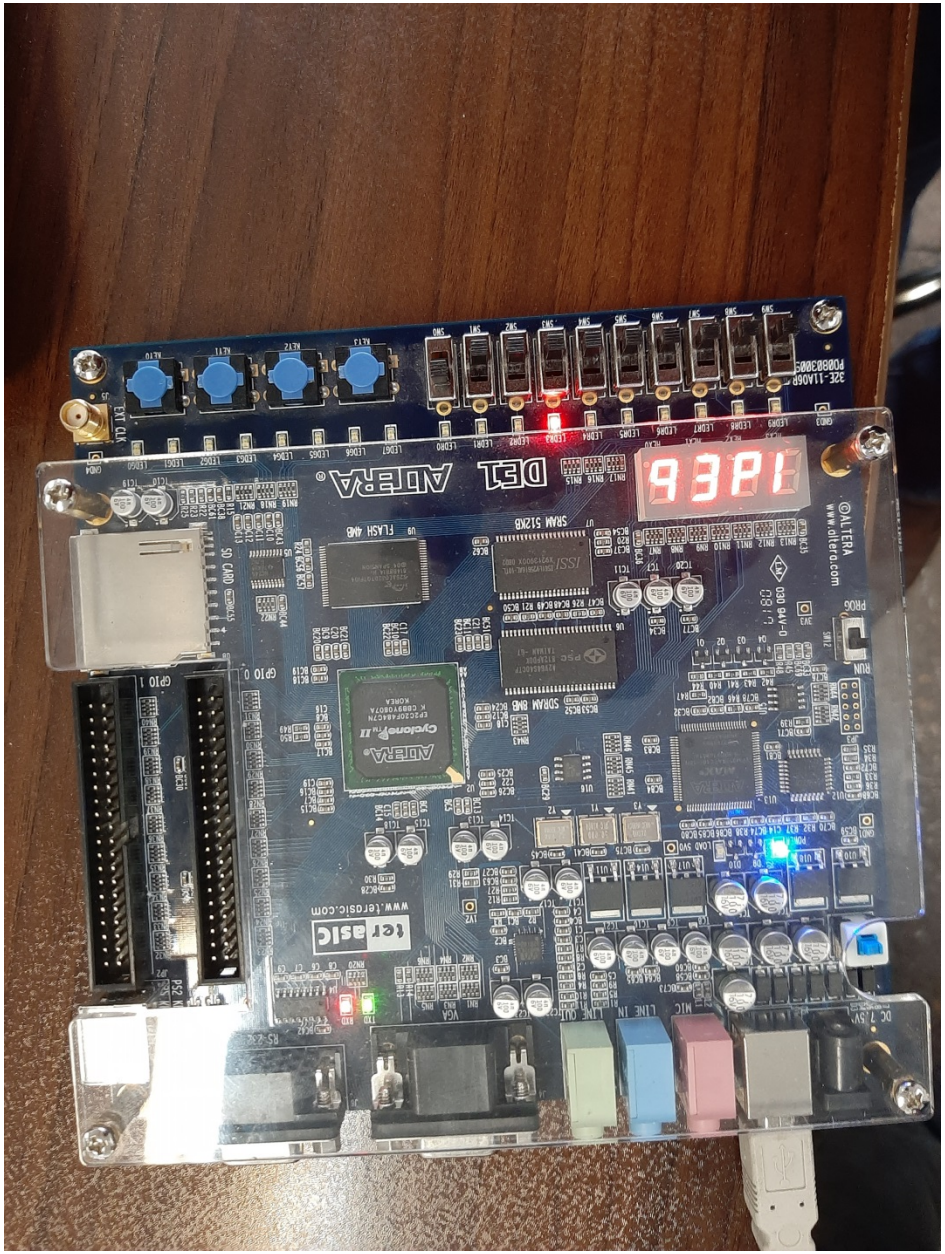
3 Implementing Accelerator on FPGA

Quartus Synthesis Report of Exponential Accelerator



Output Results of Exponential Accelerator on FPGA

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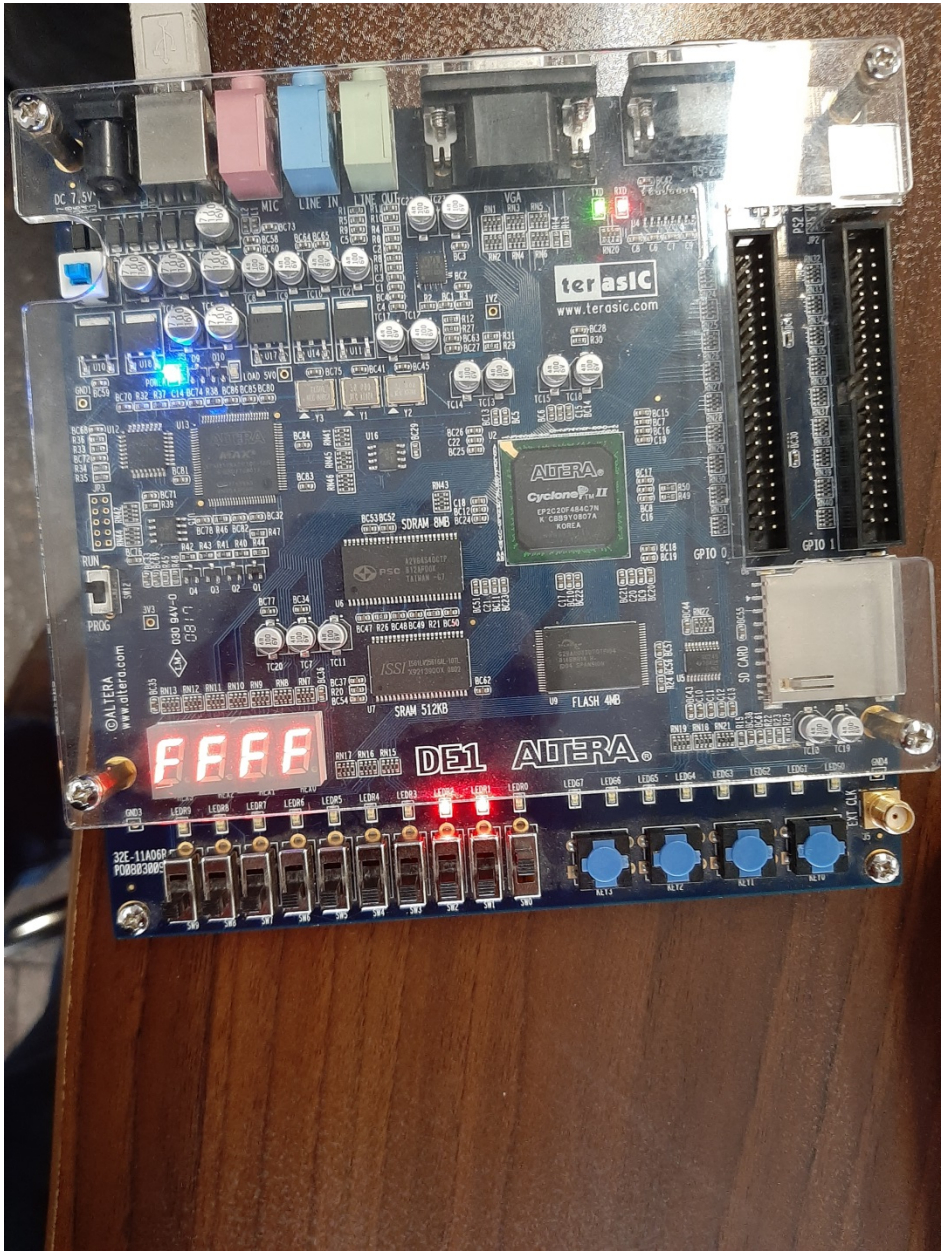
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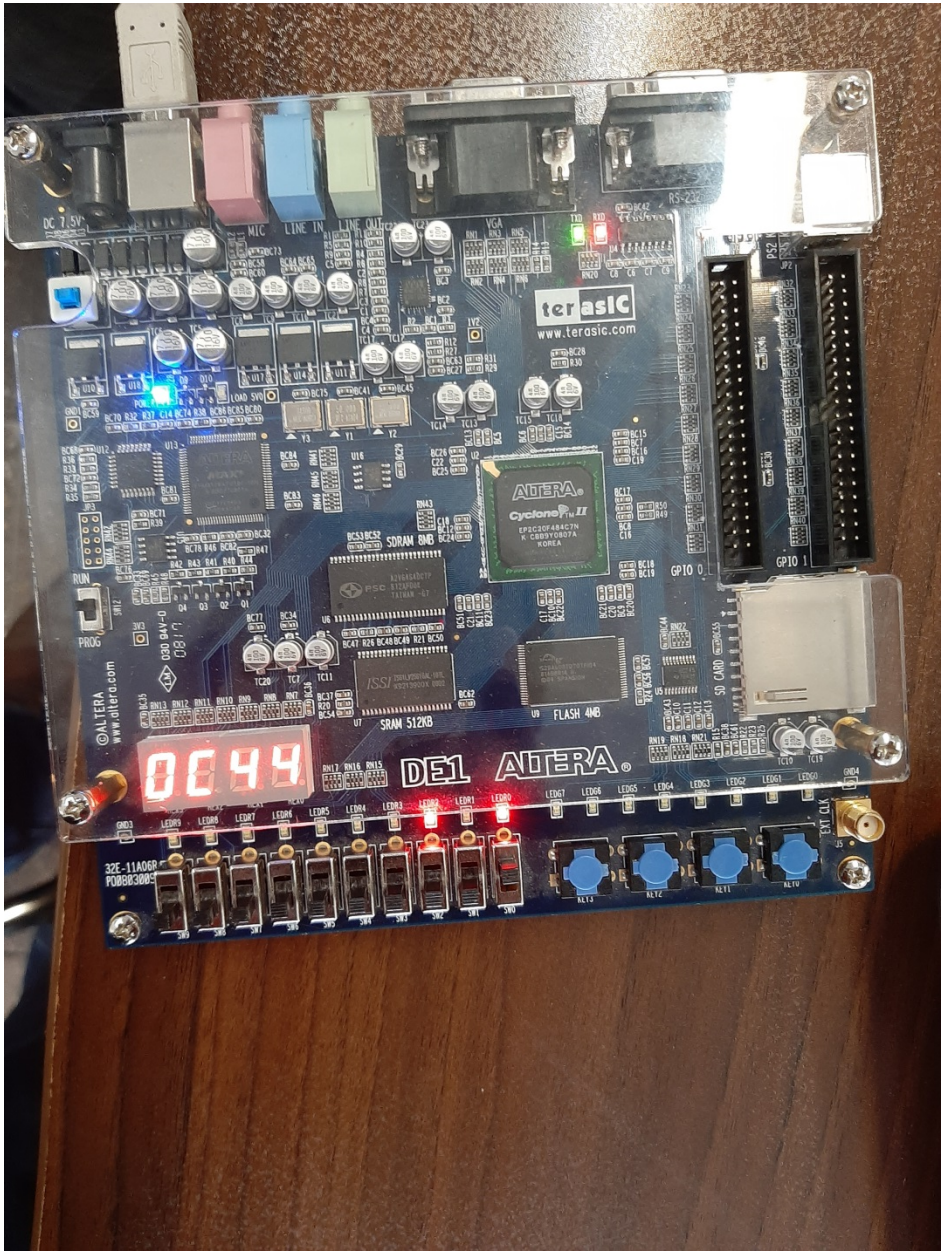
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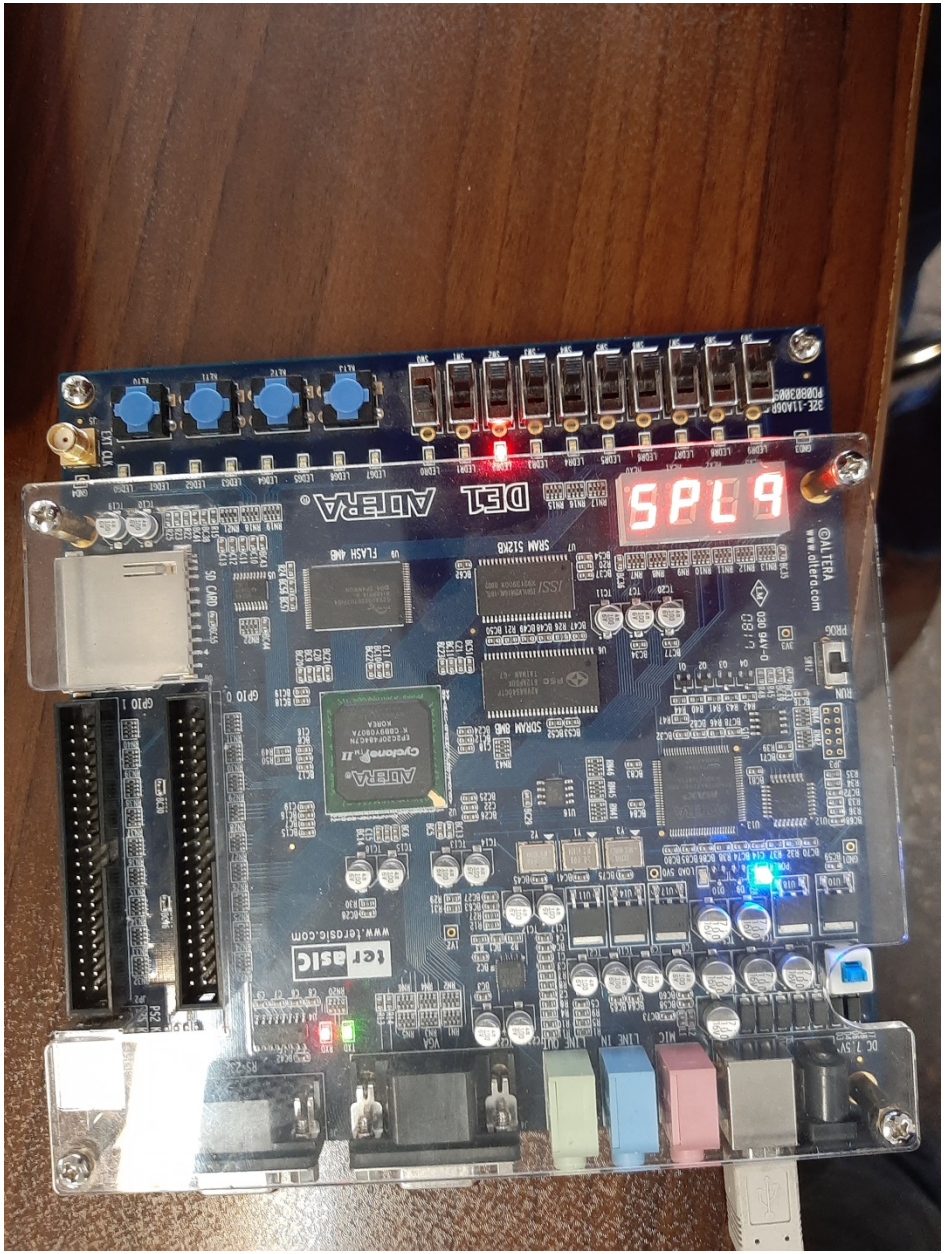
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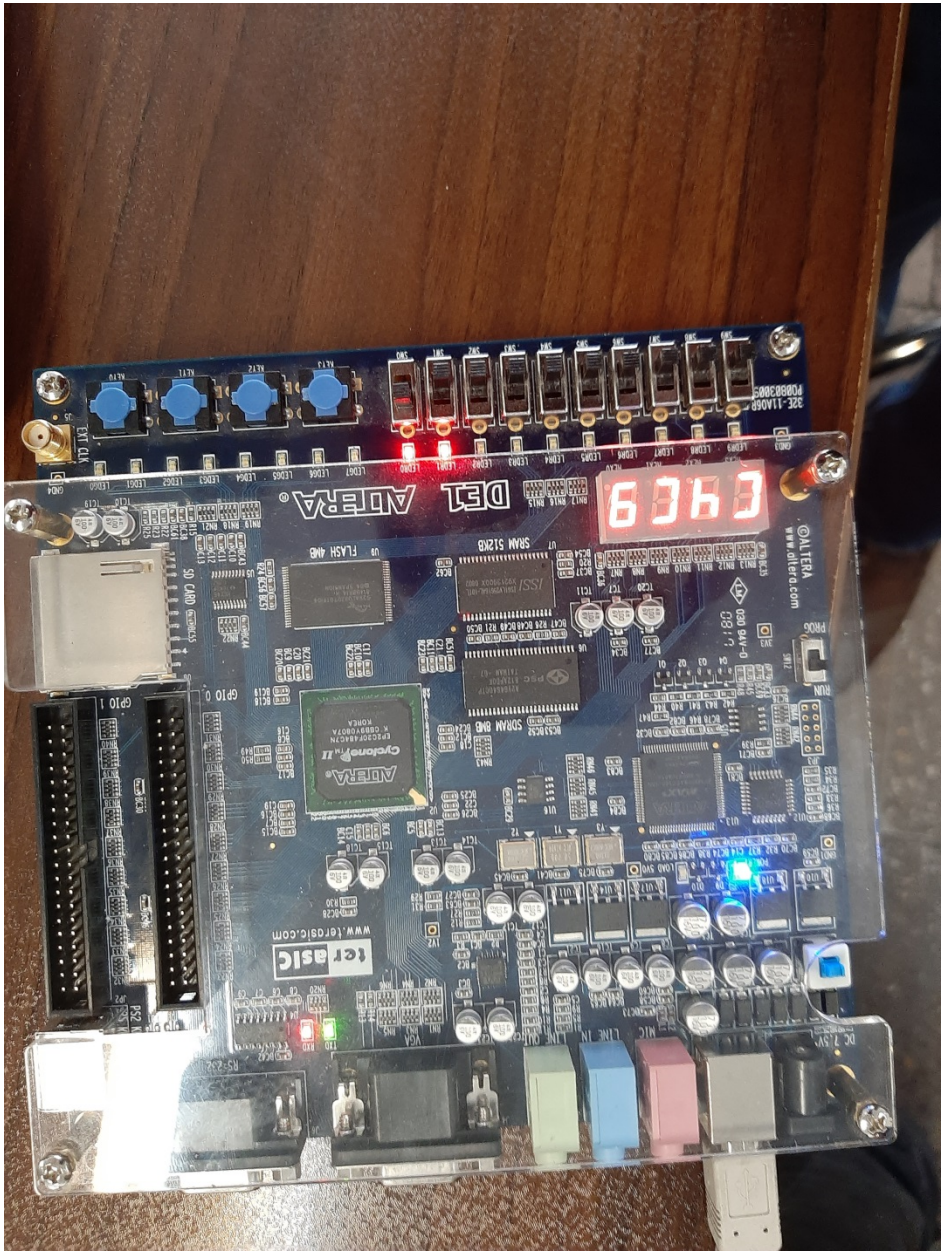
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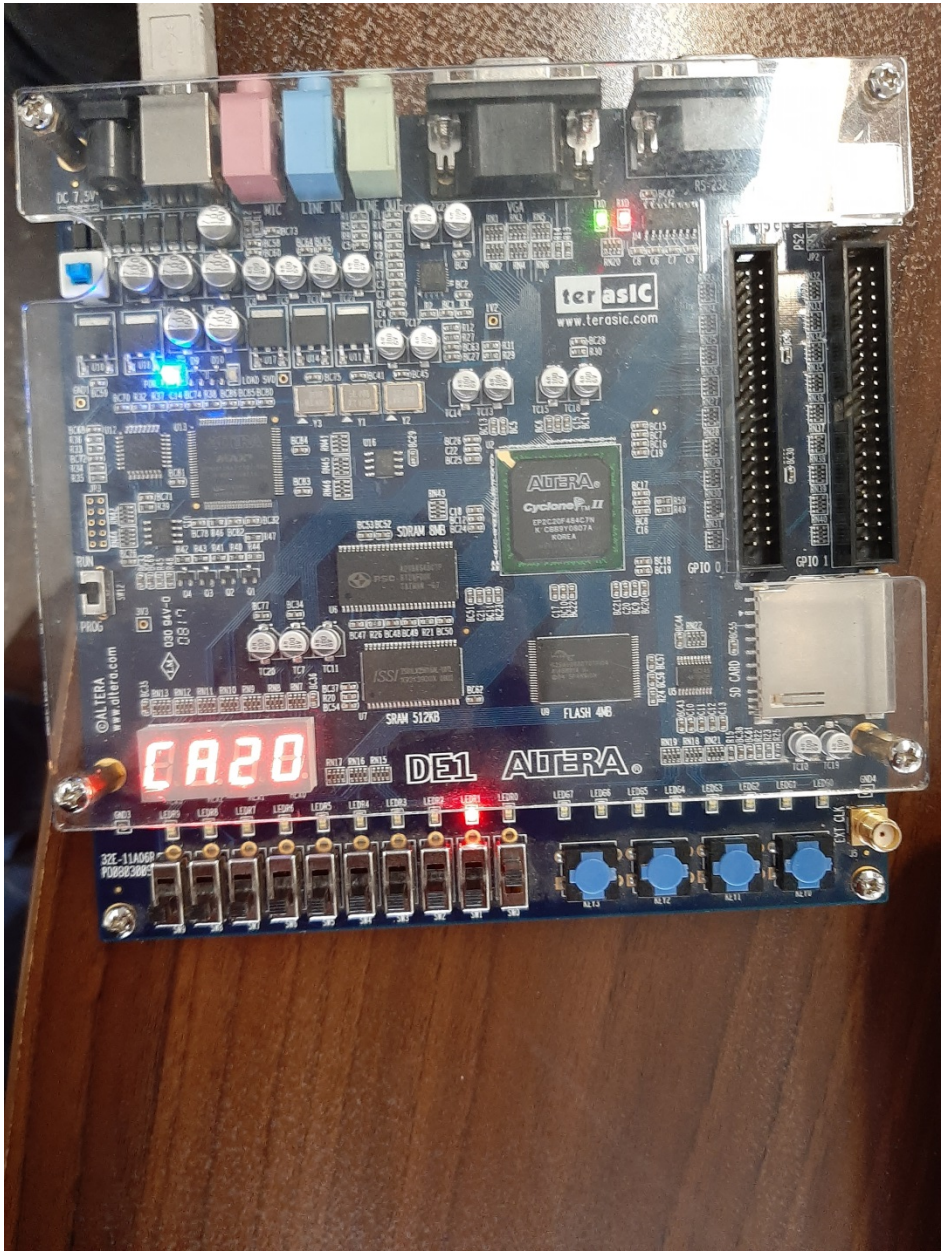
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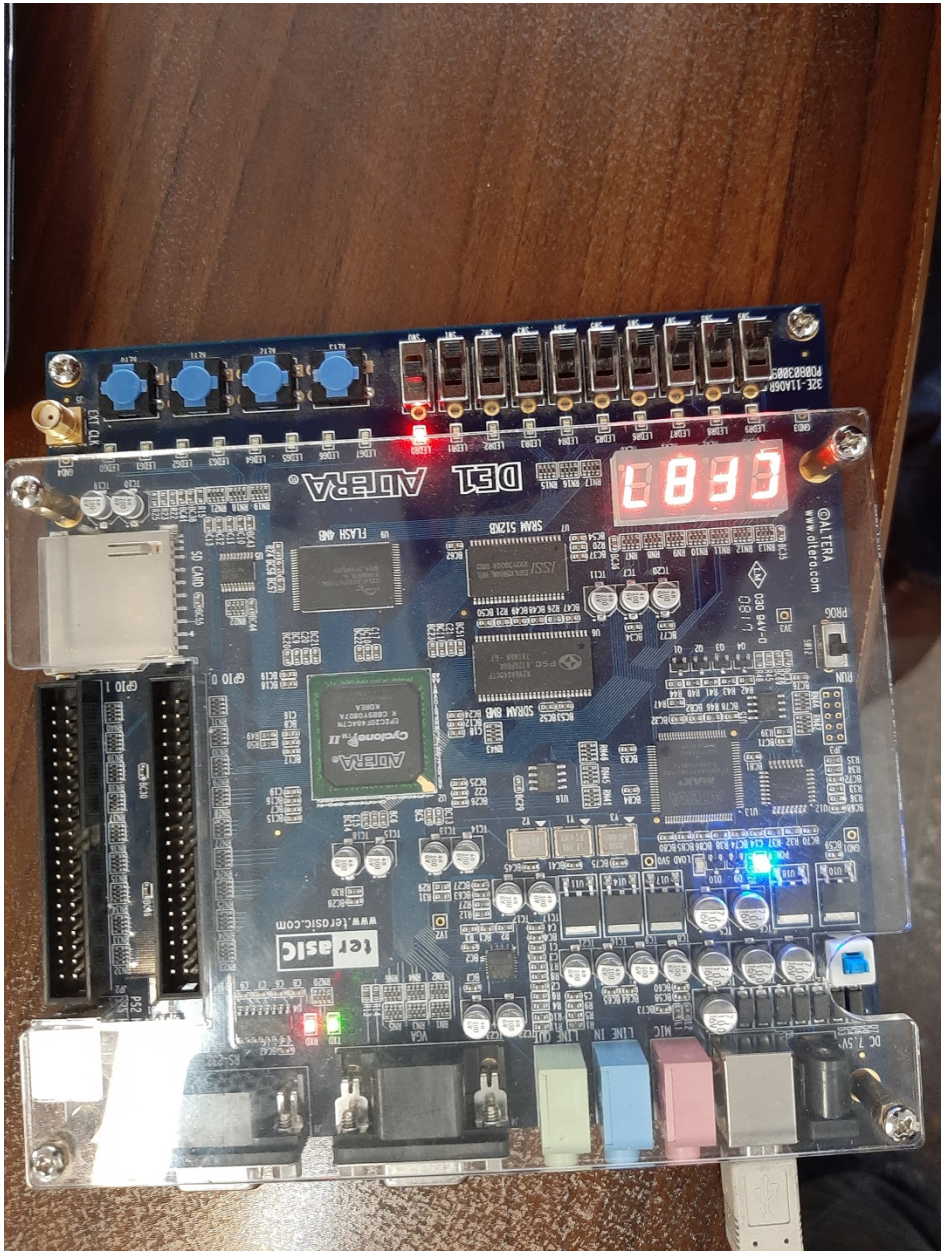
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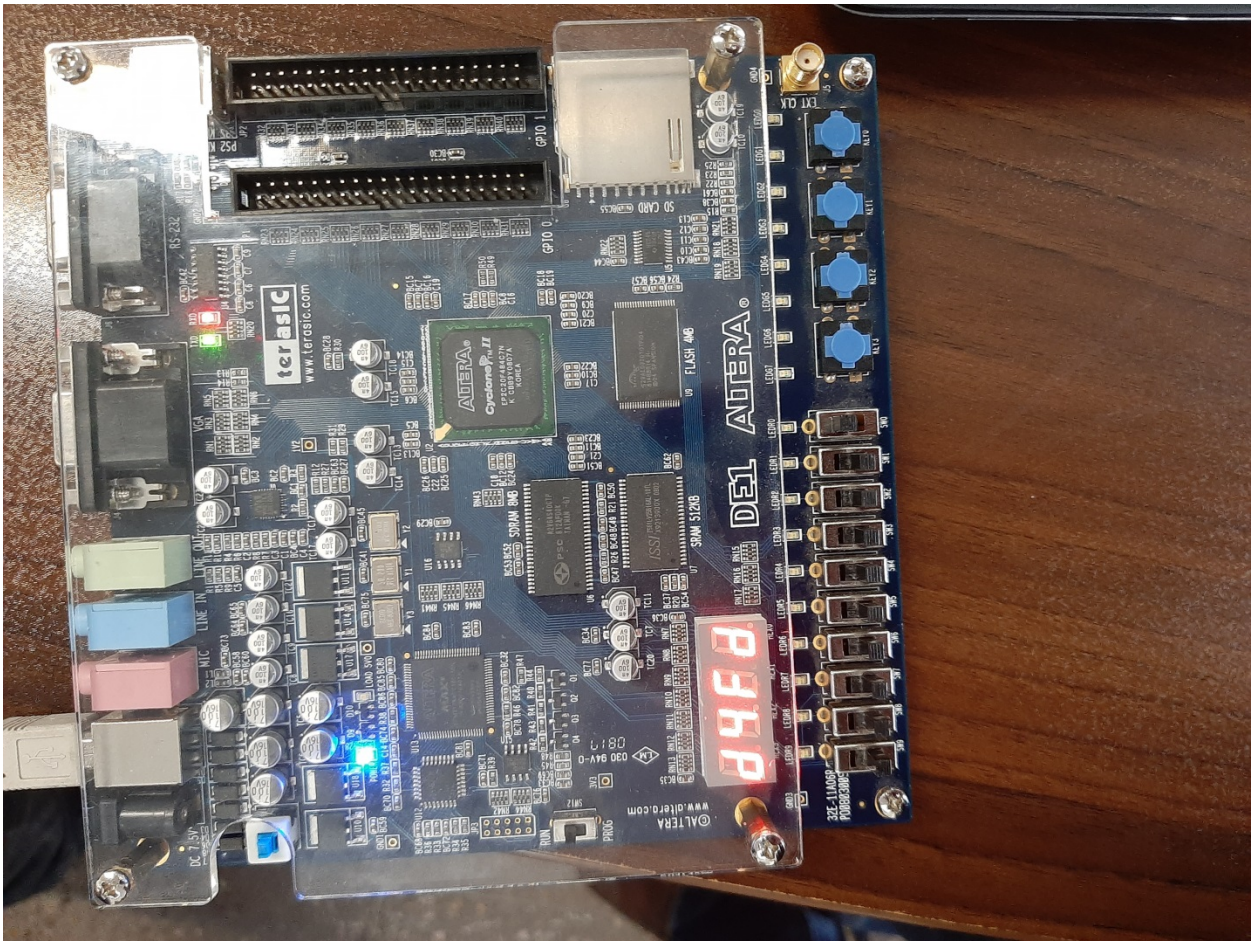

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As you see at first there are 10 used places in FIFO, each time we put FPGA's switch up and down, exponential result is shown on seven segment and one used place is thrown away so used places in FIFO decreases. In the end, there is no used place in FIFO.