EXPERIMENT 1

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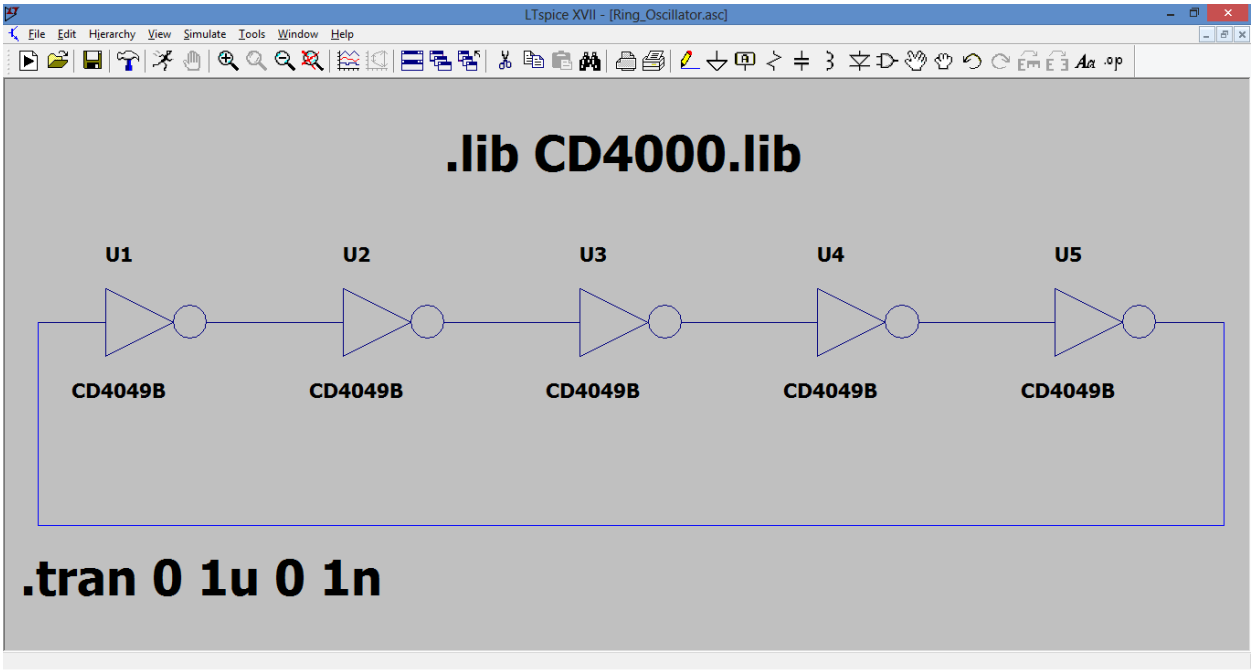
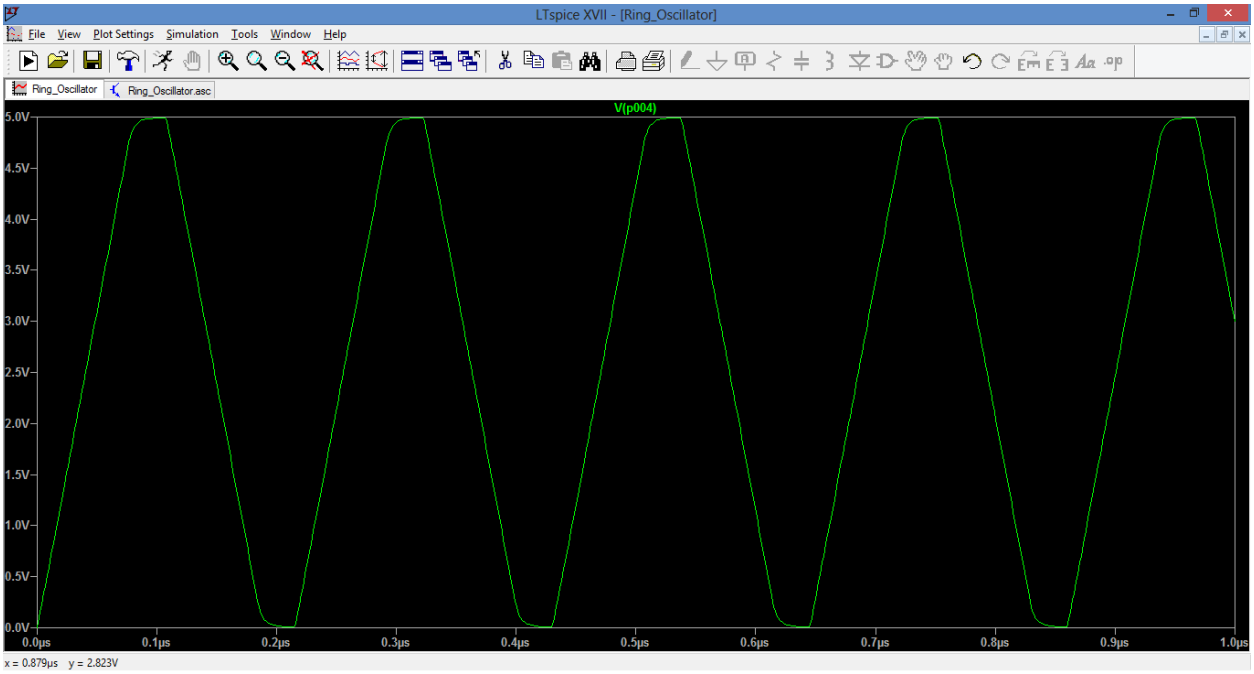
Contents

Ring Oscillator

Circuit:



Simulation of the above Ring oscillator's output:



N = number of inverters used in the Ring Oscillator = 5

Output's period time = 215 ns

1.

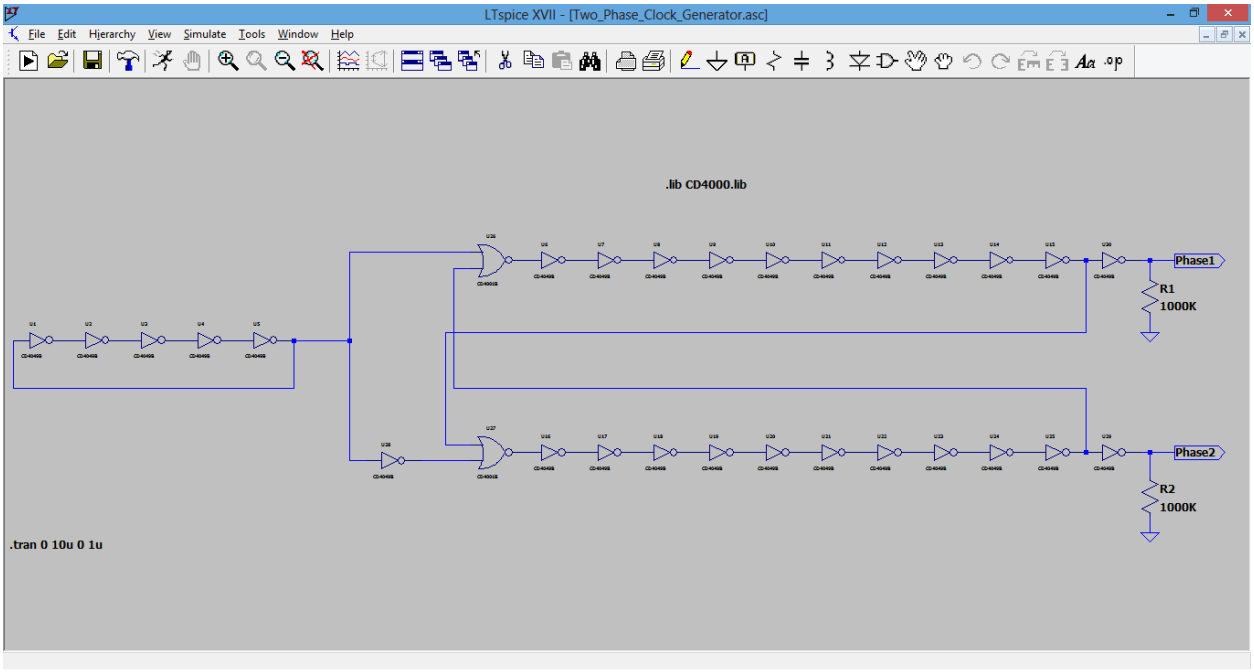
Propagation delay = N * delay of an inverter = output's period time / 2 = 107.69 ns

2.

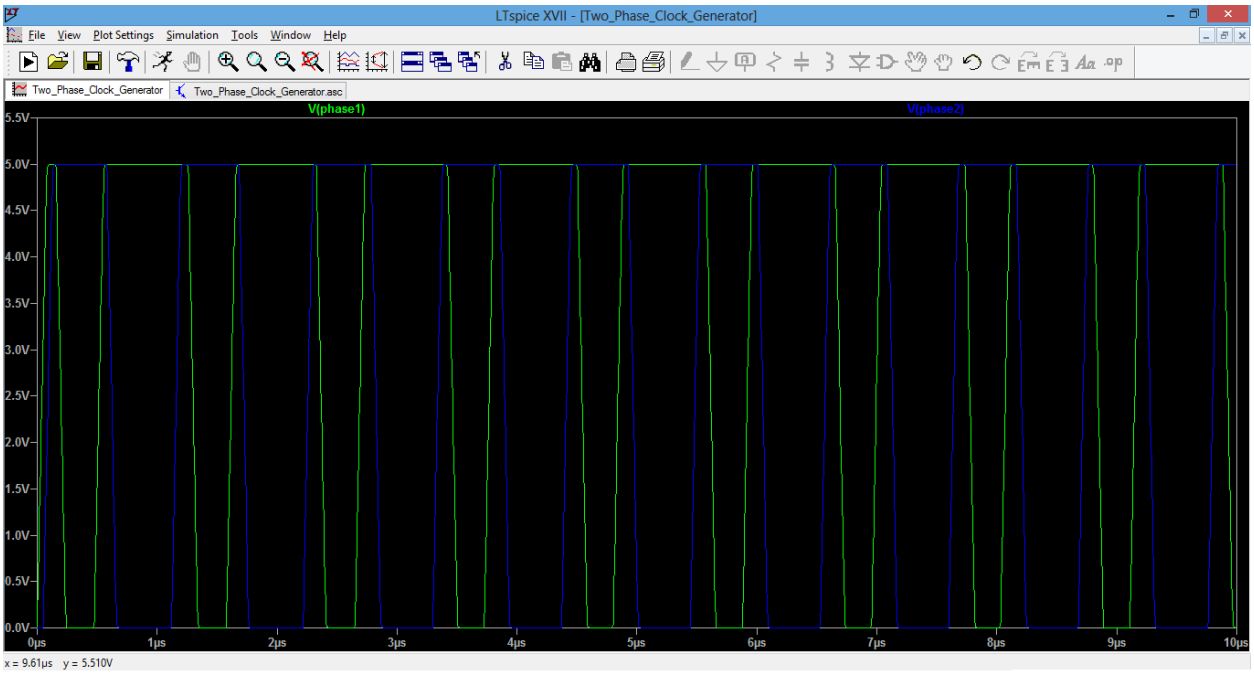
Single inverter's delay = output's period time / N = output's period time / 5 = 21ns

Two Phase Clock Generator

Circuit:

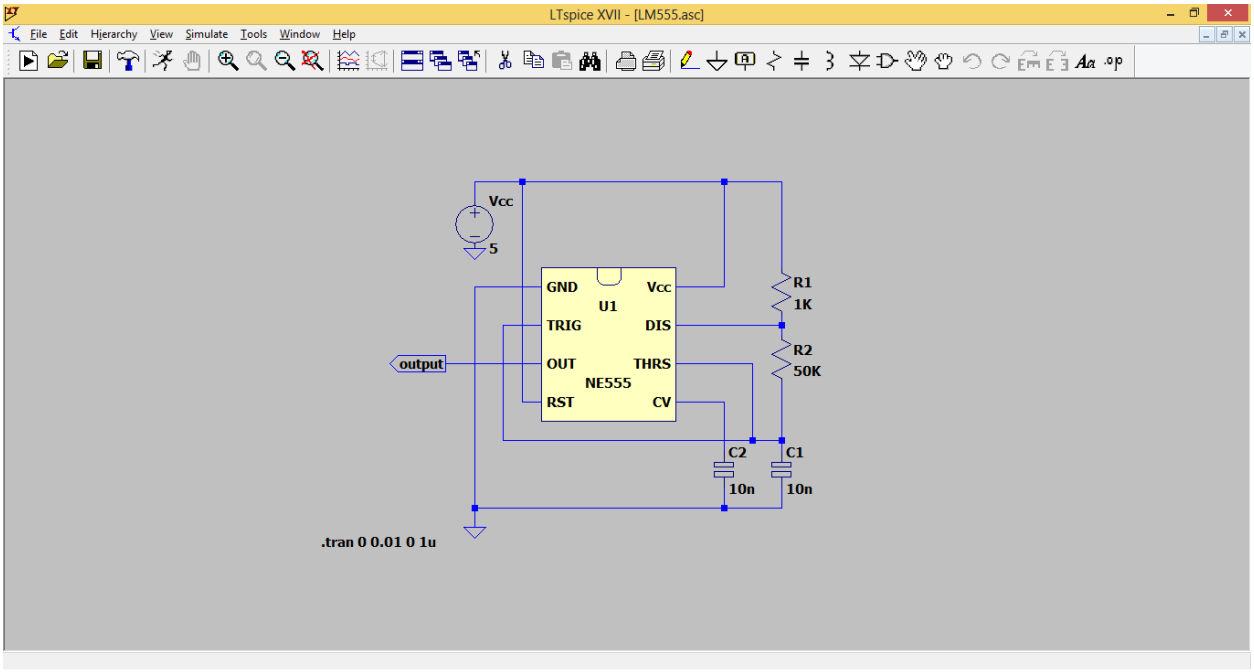


Simulation of the above Two Phase Clock Generator's two phases output:

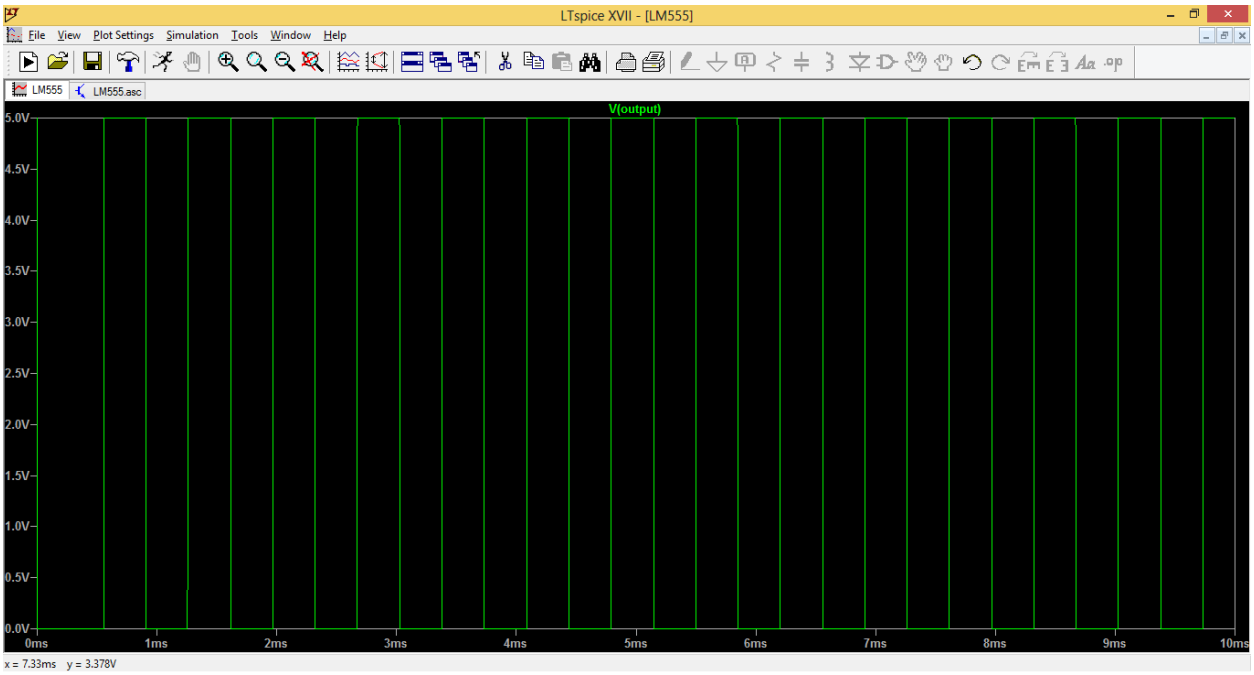


LM555

Circuit:



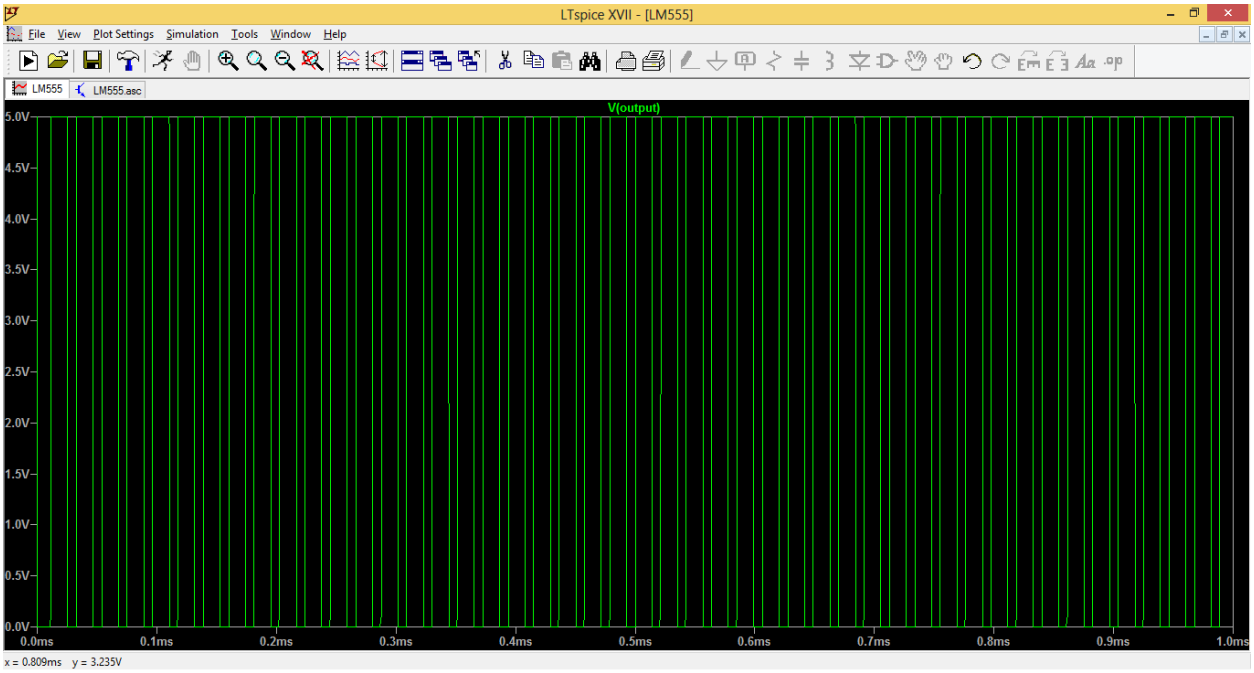
Simulation of the above LM555's output:



Clock frequency = 1428.7143, Duty cycle = 0.50495 ≈ 0.5

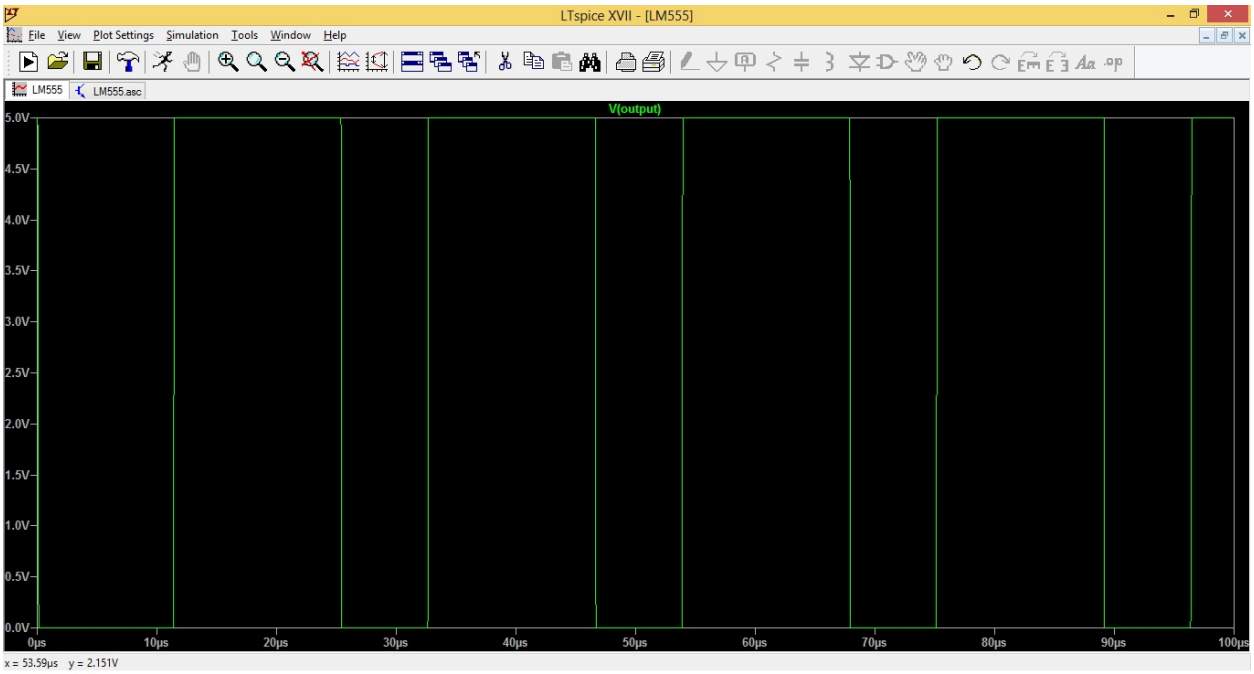
2.

R2 = 1KΩ => frequency = 48100.048, duty cycle = 67%

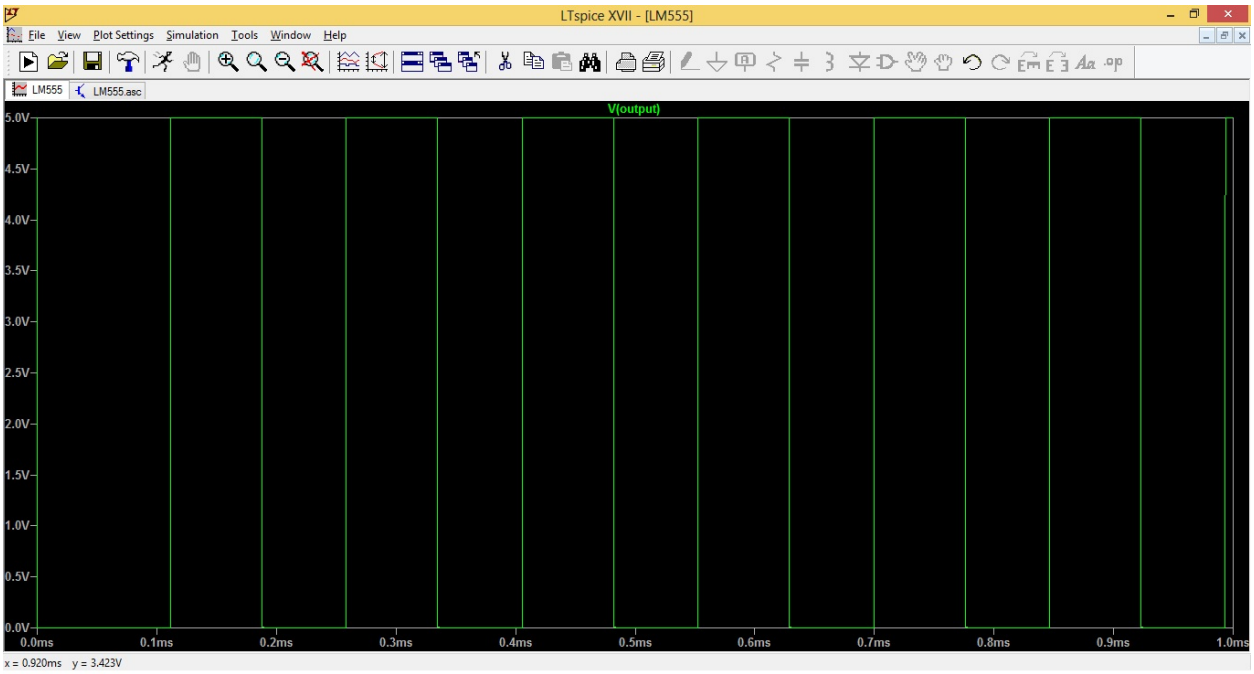


As you see in above diagram, in 0.1ms we almost have 4 periods, so in 1s we will almost have 40000 periods which is close to 48100.048.

As you see in below diagram, duty cycle is almost 2/3 which is close to 67%.

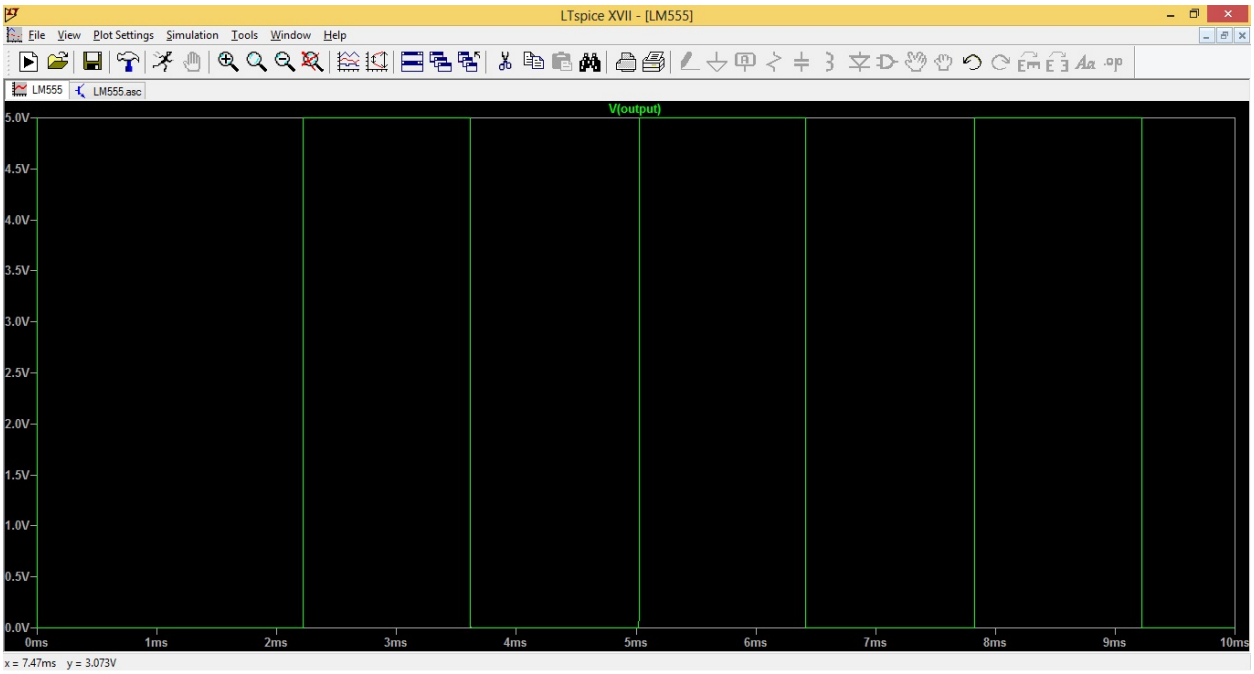


R2 = 10KΩ => frequency = 6871.435, duty cycle = 52.38%



As you see in above diagram, in 1ms we almost have 6 periods, so in 1s we will almost have 6000 periods which is close to 6871.435 and duty cycle is near 50% which is close to 52.38%.

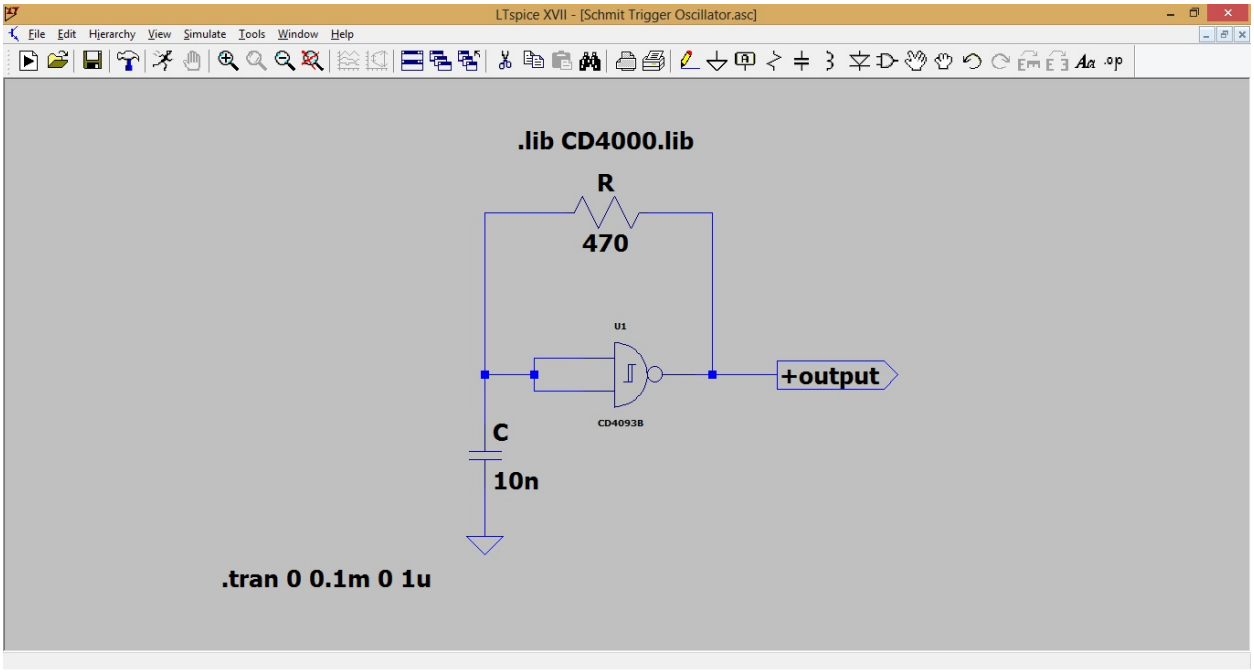
R2 = 200KΩ => frequency = 359.85 , duty cycle = 50.12%



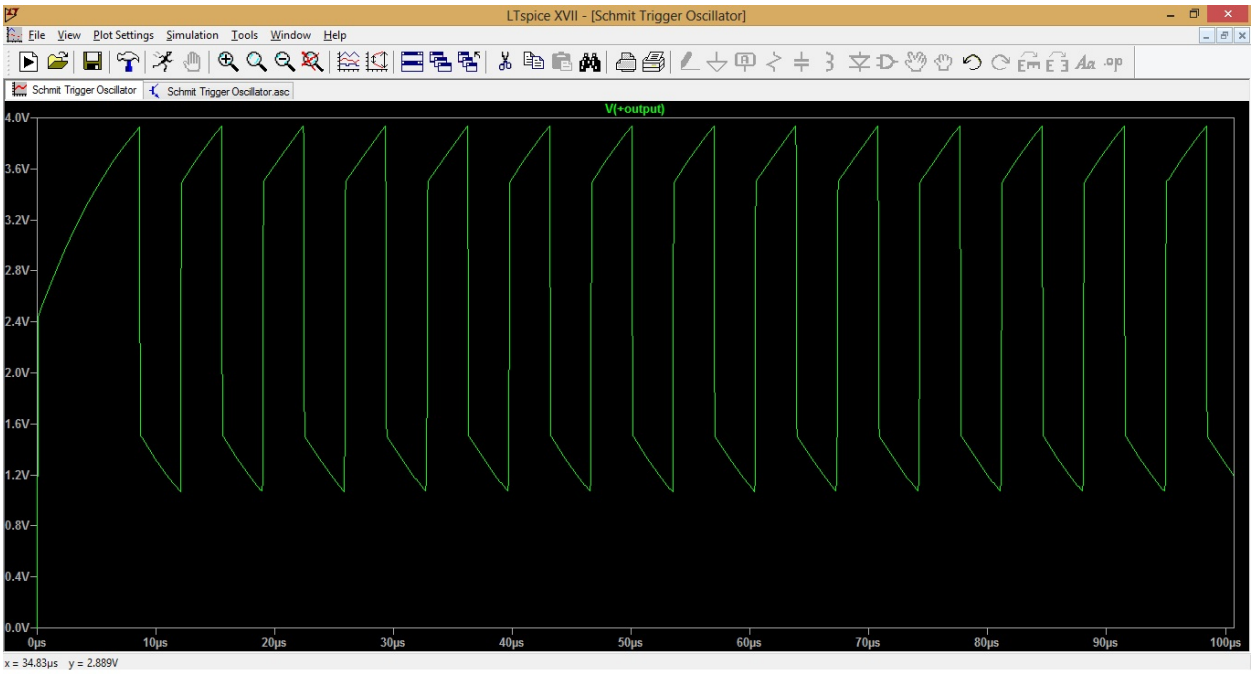
As you see in above diagram, in 10ms we almost have 3 periods, so in 1s we will almost have 300 periods which is close to 359.85 and duty cycle is near 50% which is close to 50.12%.

Schmitt Trigger Oscillator

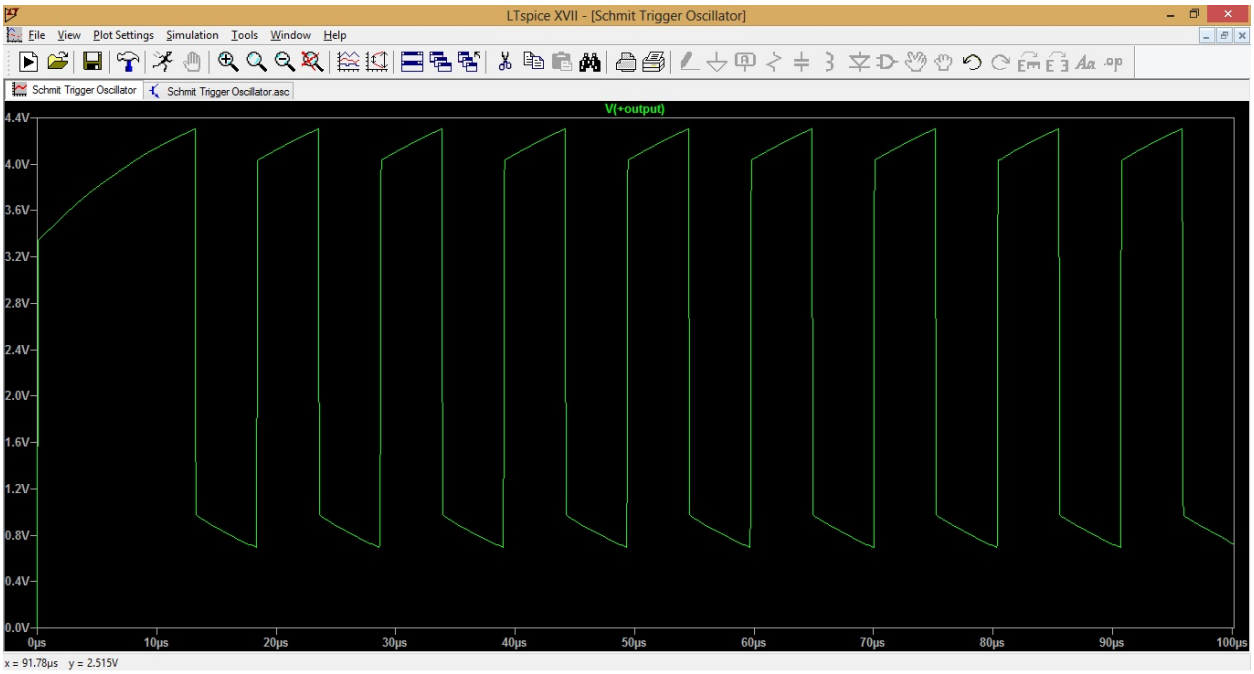
Circuit:



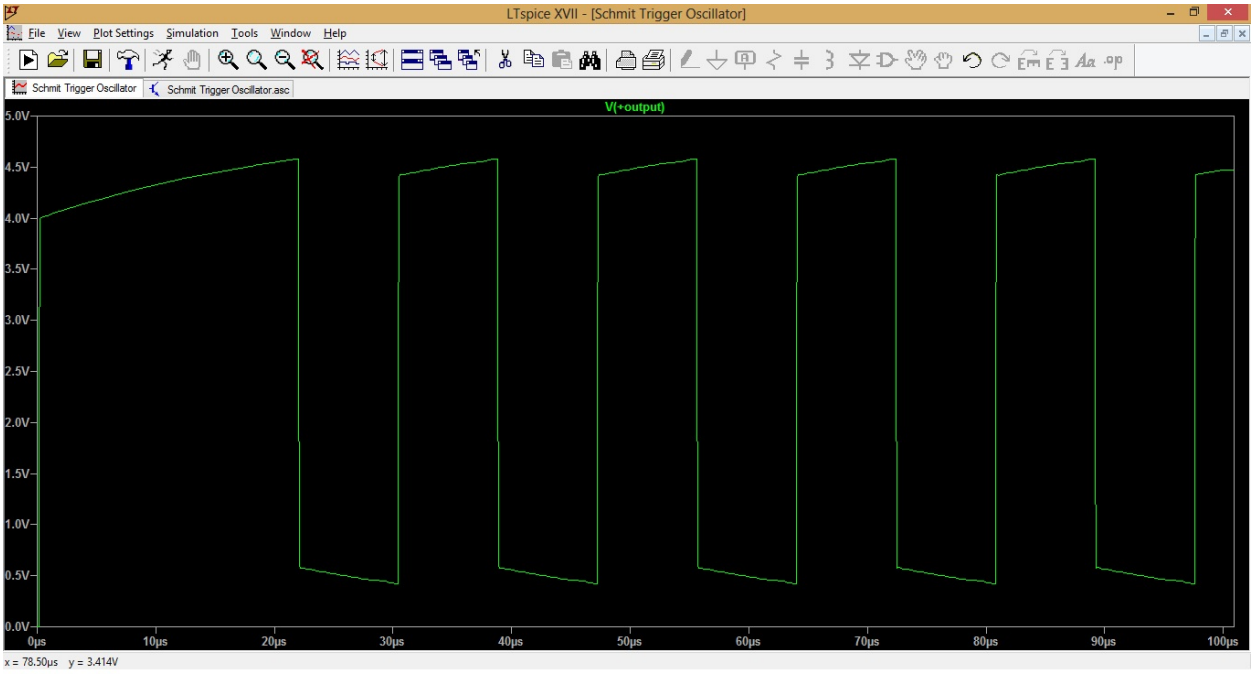
Simulation of the above Schmitt Trigger Oscillator's output for **R = 470Ω**:



Simulation of the Schmitt Trigger Oscillator's output for **R = 1000Ω**:



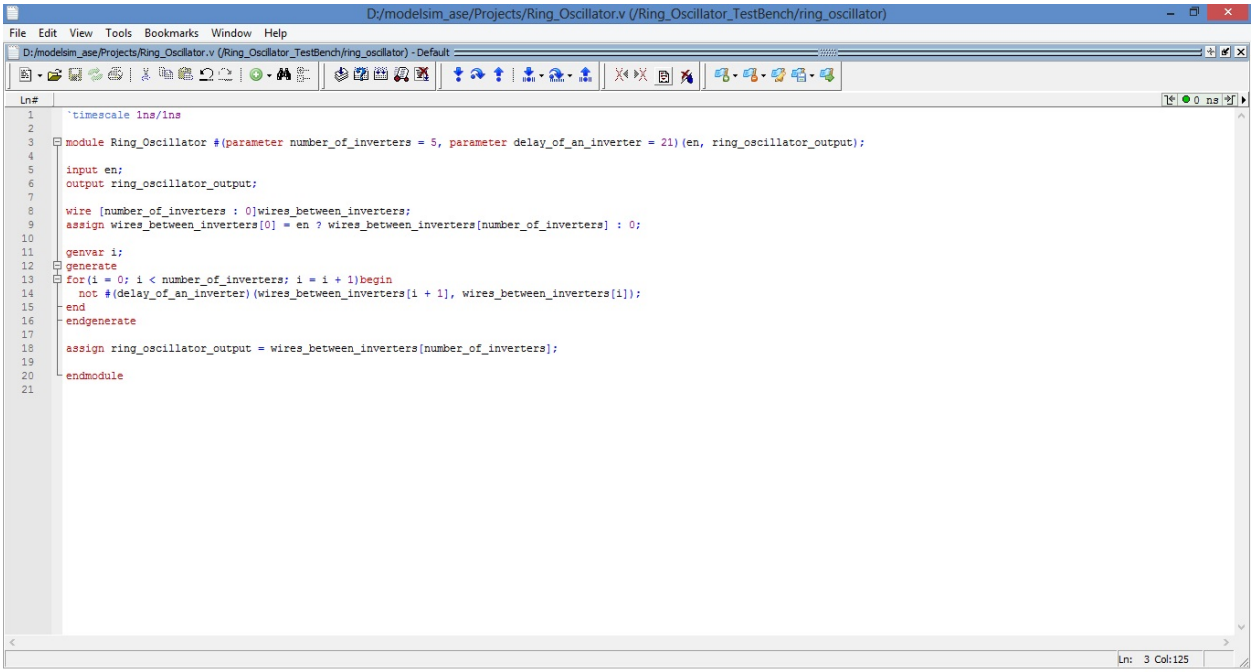
Simulation of the Schmitt Trigger Oscillator's output for **R = 2000Ω**:



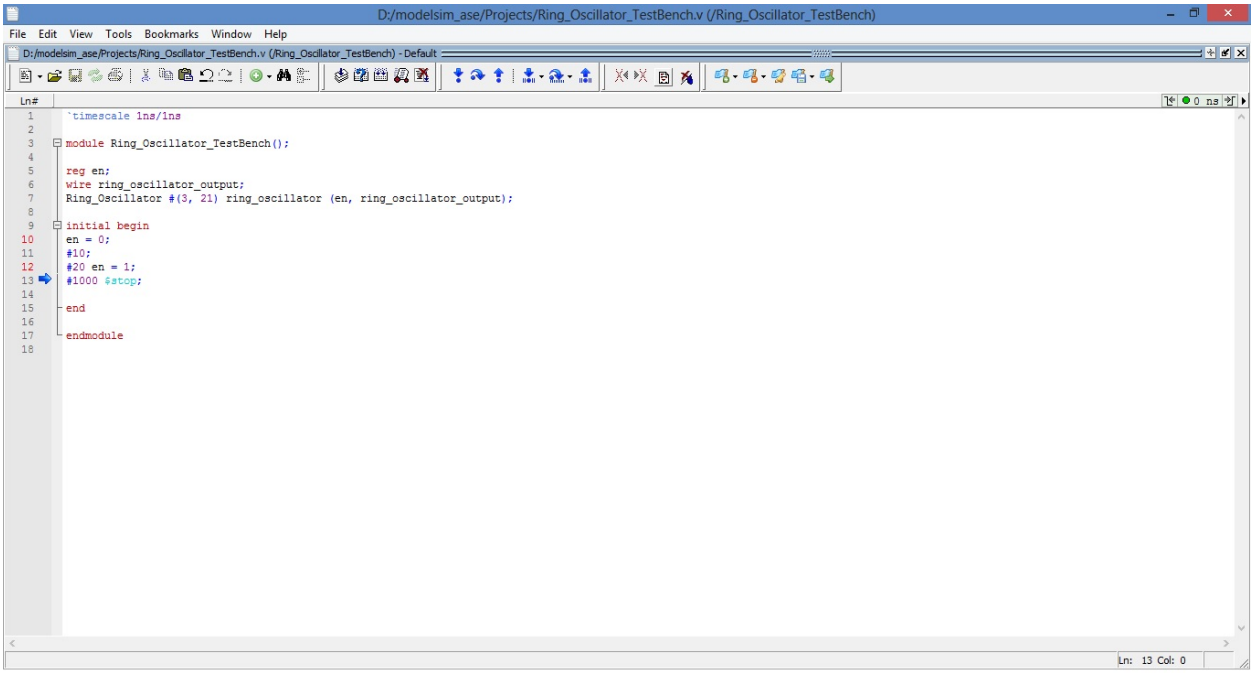
$\alpha_{2000} = 1.195$, $\alpha_{1000} = 0.974$, $\alpha_{470} = 0.6867$ => $\alpha_{\text{average}} = 0.952$

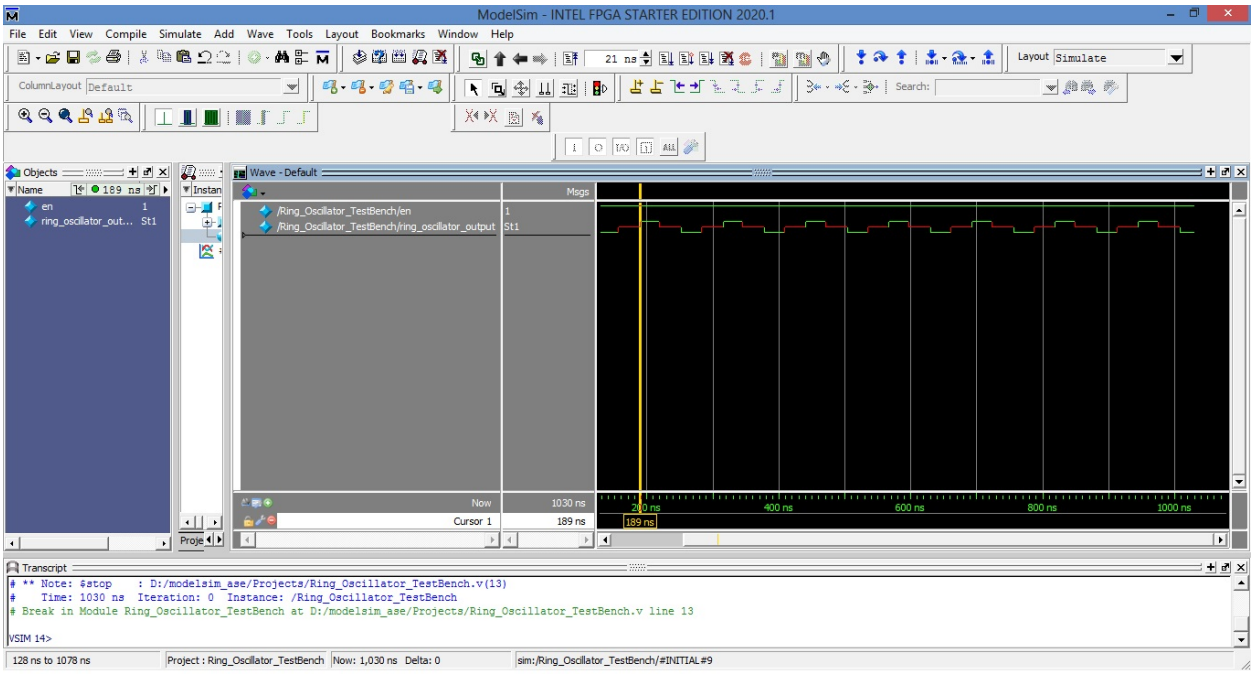
Ring Oscillator(Part 2 - FPGA design)

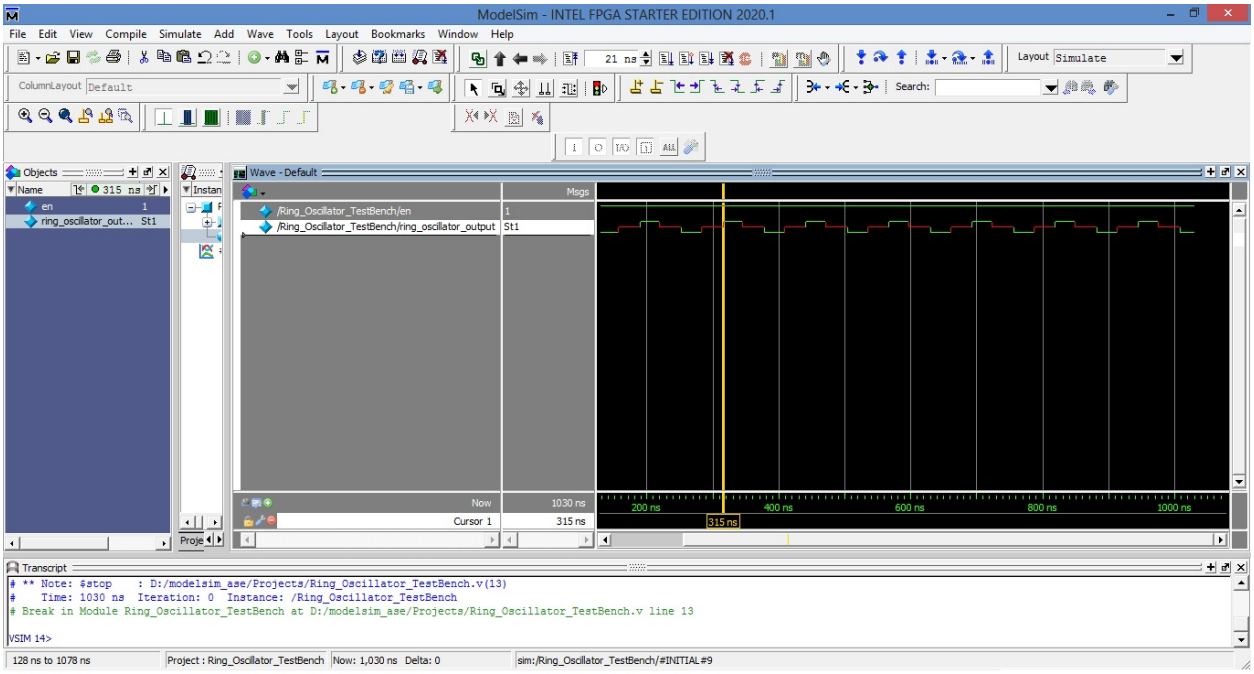
Verilog description of Ring Oscillator circuit:



Test Bench of above Ring Oscillator Verilog code:







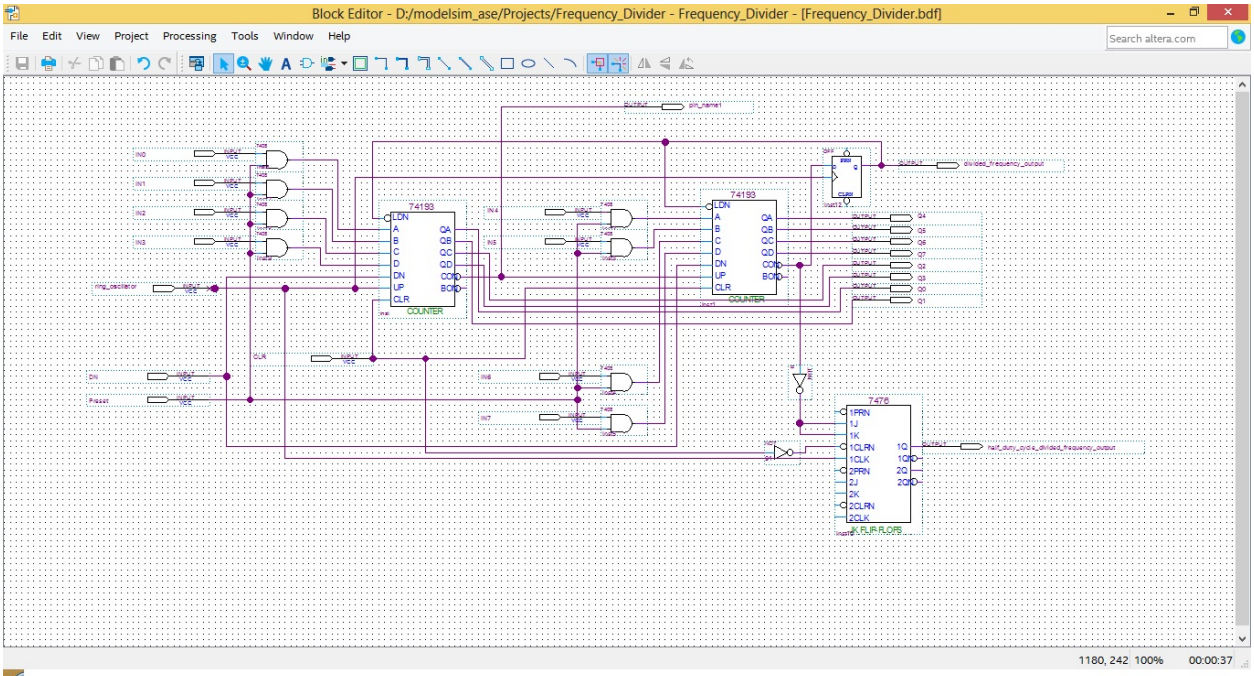
Given N in test bench = 3, given inverter's delay in test bench = 21ns

T = 2× N× inverter's delay = 2× (3) × (21ns) = 6×21 = 126ns = 315 – 189

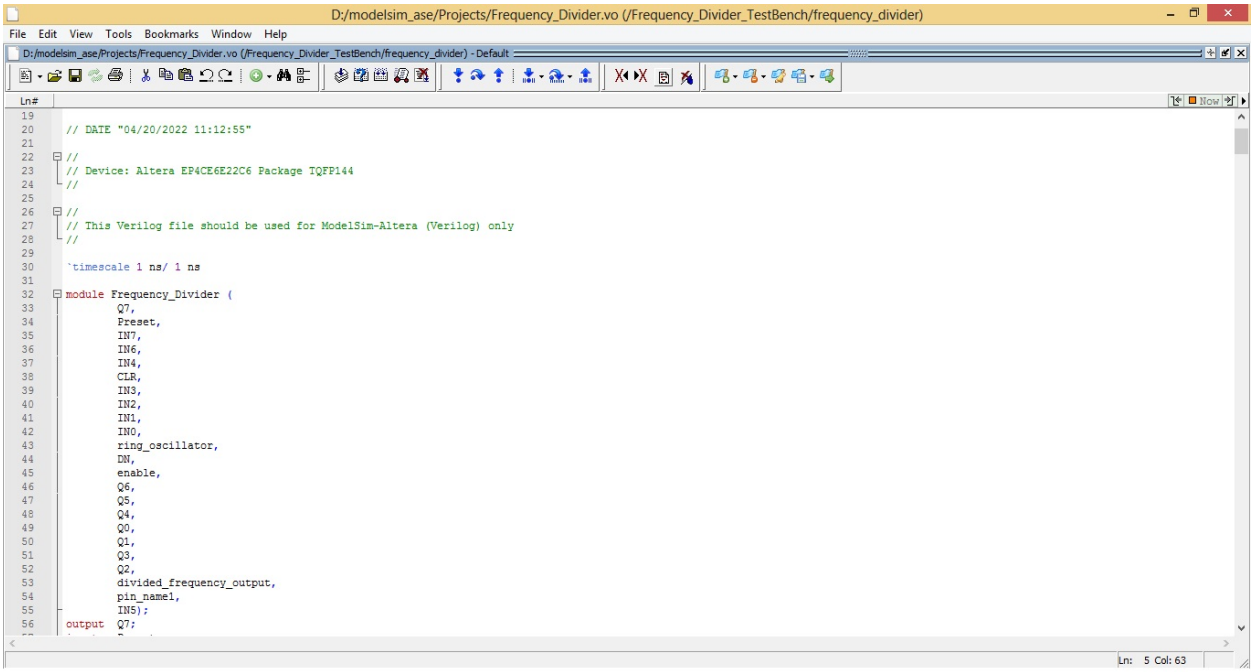
=> f = 1/T = 1/126ns = 7,936,508 Hz

Frequency divider

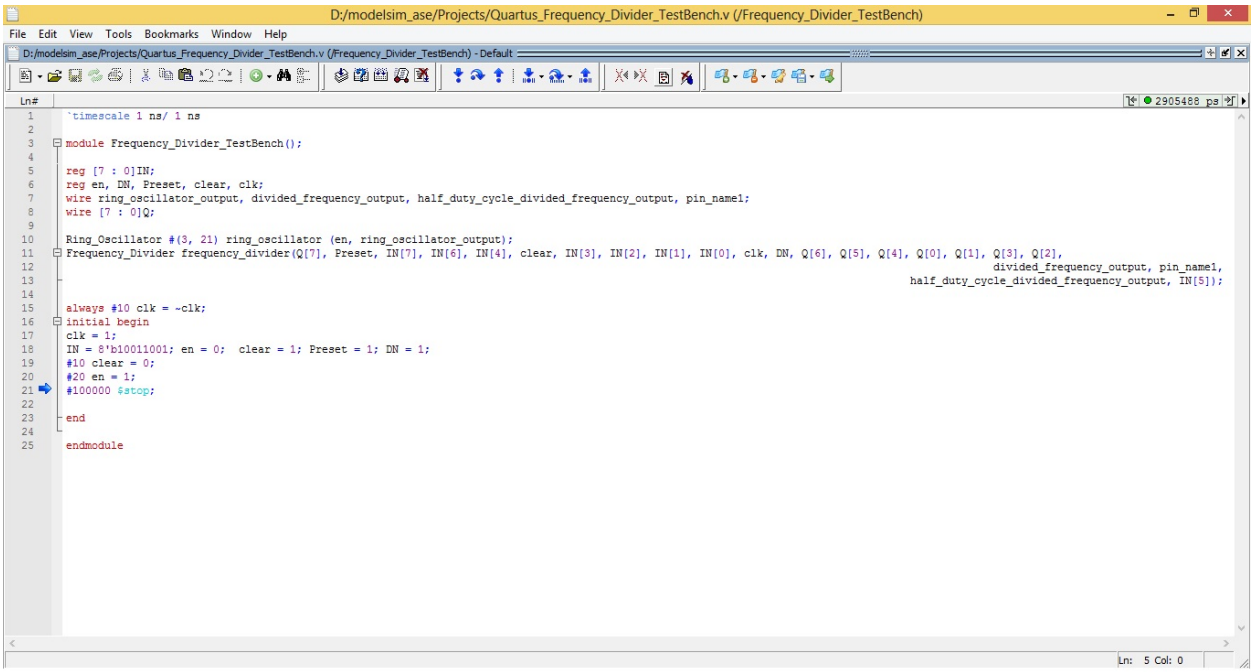
Frequency divider's circuit:



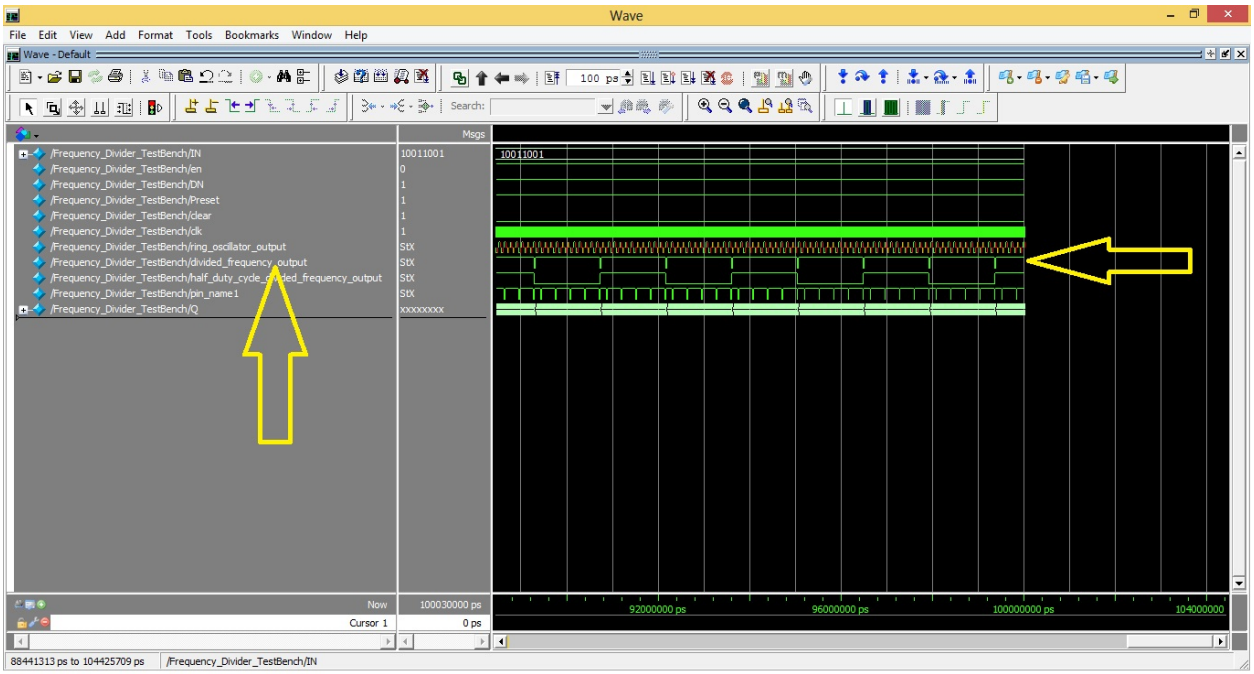
Verilog output of above Frequency divider's circuit:



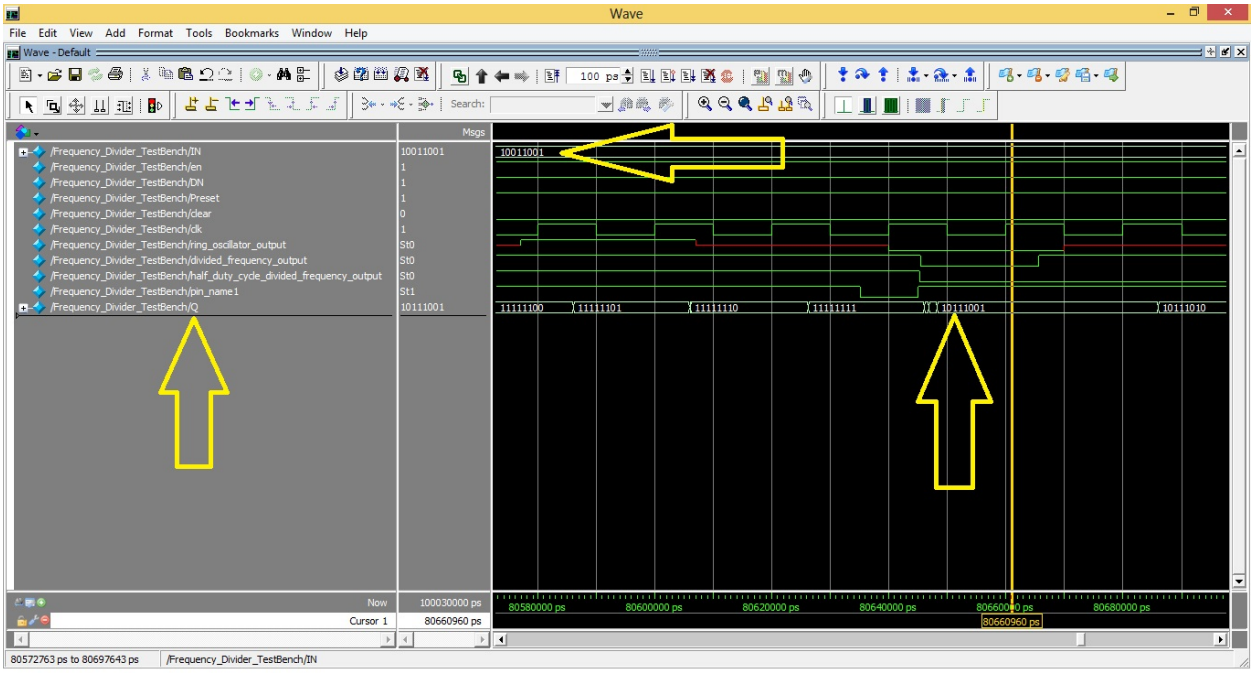
Test Bench of Frequency divider's Verilog output:

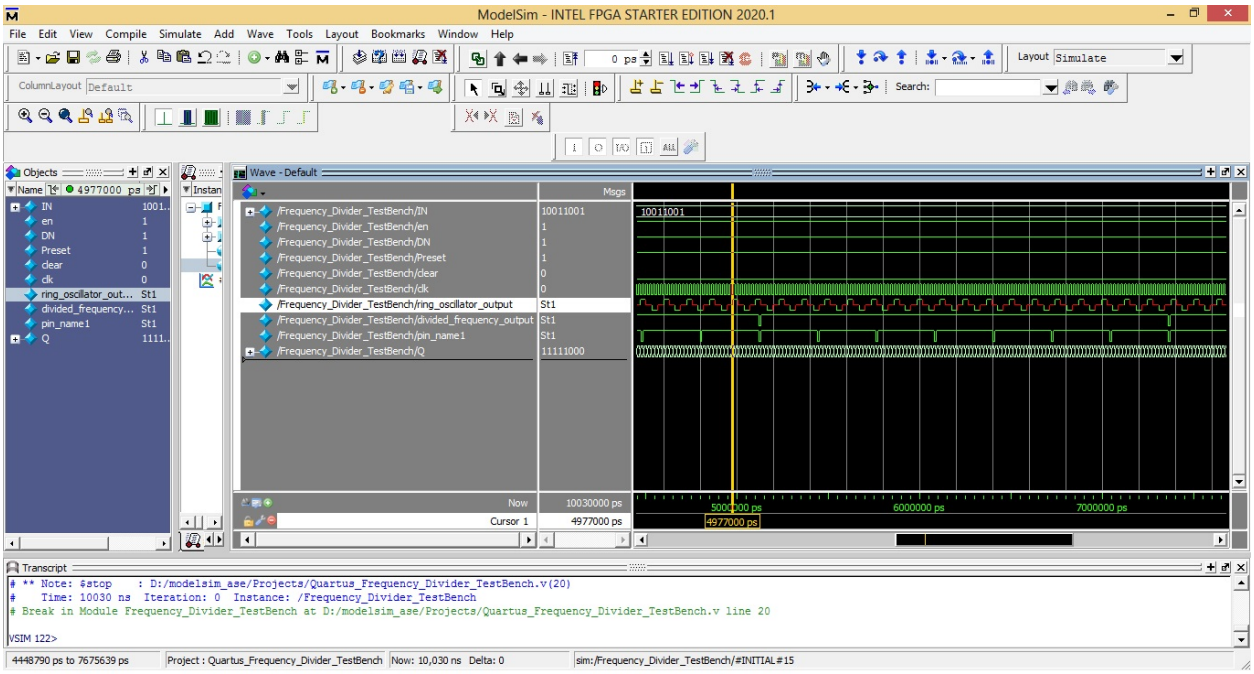


Simulation of the above Frequency divider's output:



Loading the initial value (256 - 103) of Frequency divider:

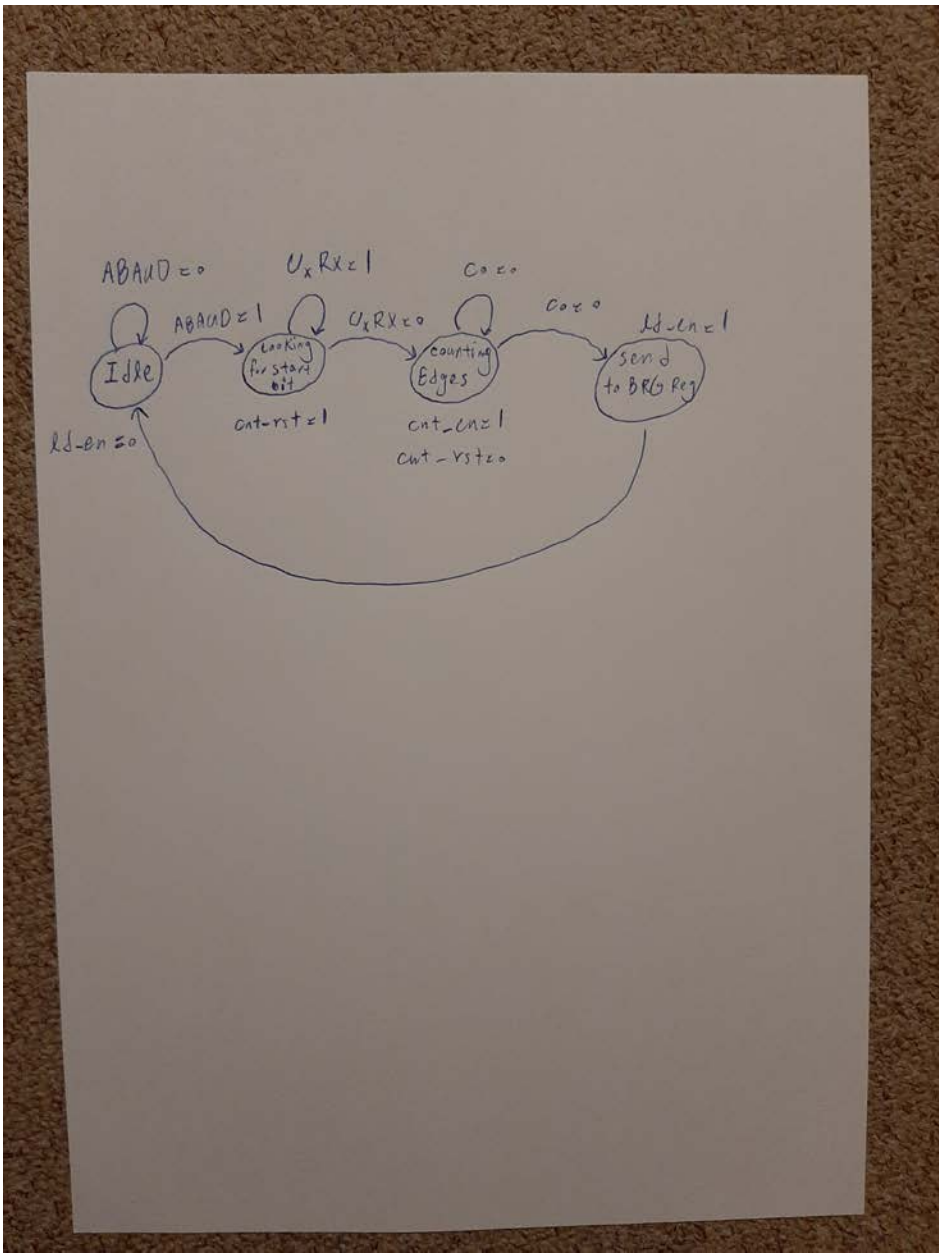




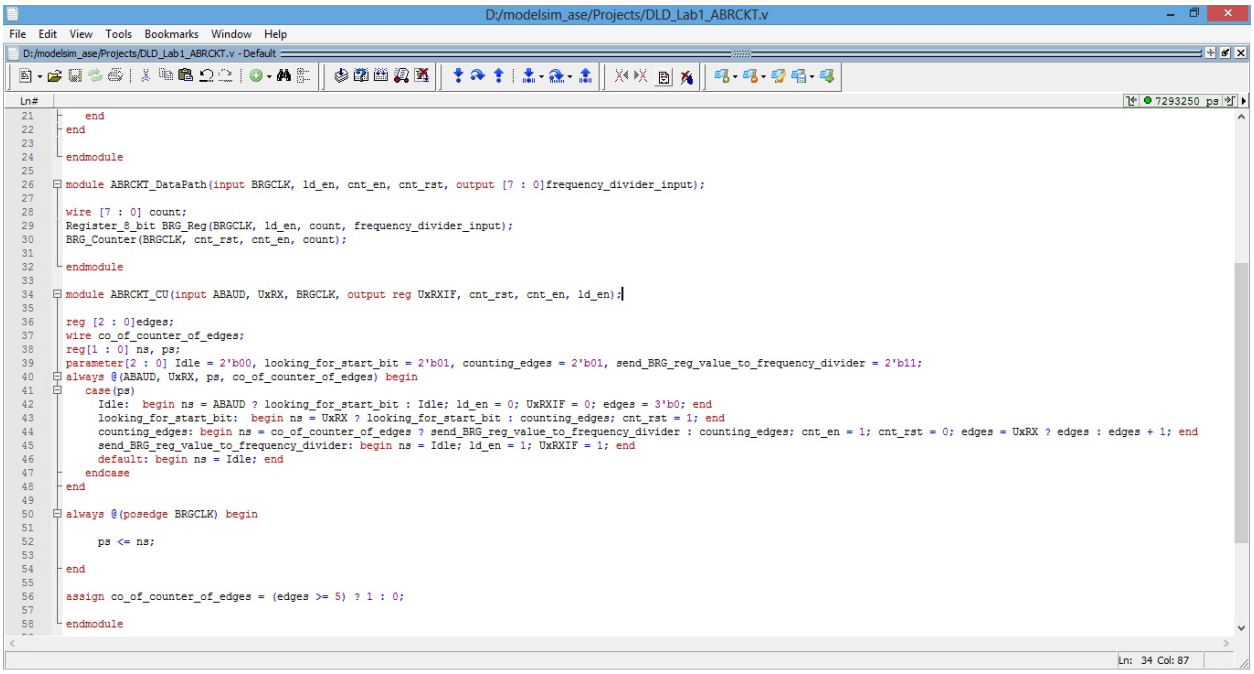
As you see in above diagram there are 7 periods between 2 periods of divided_frequency_output signal. Each period of pin_name1 signal is equal to 16 periods of clock, so period of divided_frequency_output is almost 16×7 clock period $= 102 \times$ clock period, which is very close to $103 \times$ clock period.

Frequency $= 1$ / period $= 1$ / $(103 \times$ clock period$) = 1/103$ clock frequency

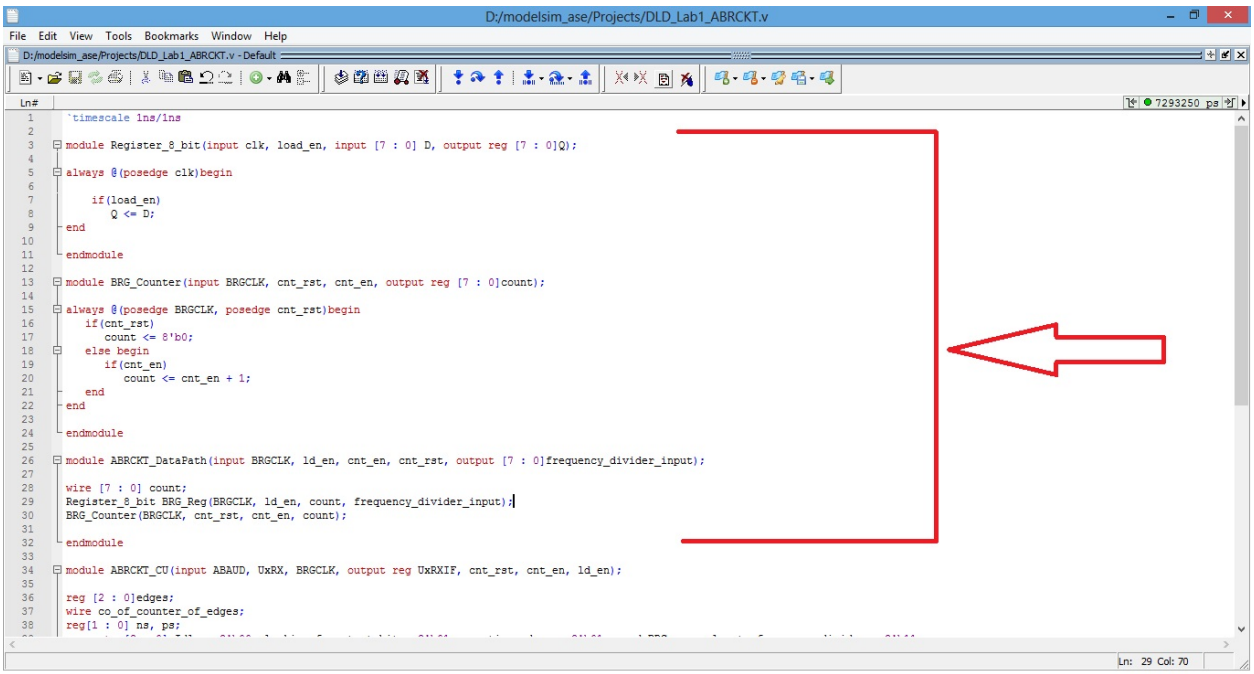
Baud Rate Generator for UART Serial Communication



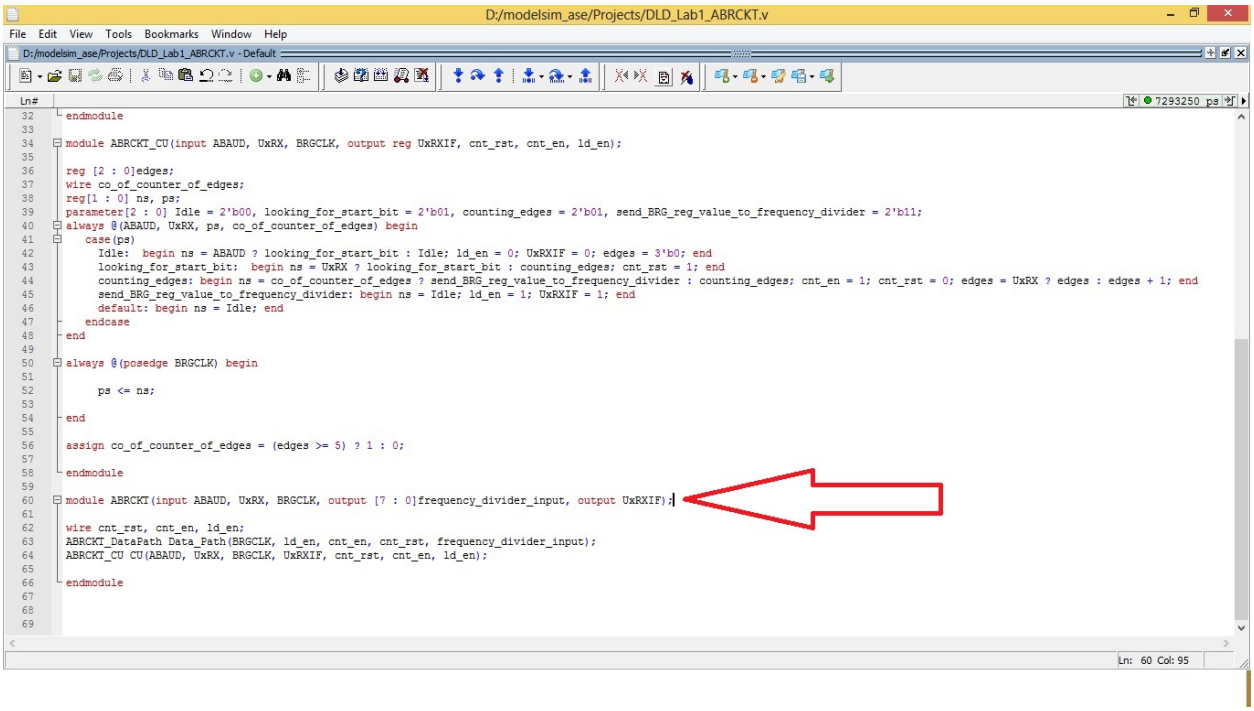
ABRCKT's Controller:



ABRCKT's Data Path:



ABRCKT's Top level:



Schematic symbol of Quartus's synthesized ABRCKT: