University of Tehran

Electrical and Computer Engineering Department

ECE (8101) 342

Object Oriented Modeling of Electronic Circuits – Spring 1401-02

Homework 3: C++ RT-level Design and Modeling
Due Date: Esfand 28

A 4-bit Carry-Lookahead Adder (CLA4) is available and a 64-bit adder is to be built. One way of doing this is to cascade sixteen such adders so that we have sixteen CLA4 units that are cascaded to form a 64-bit adder using Ripple-Carry between the CLAs. An alternative way of doing this is to sequentially use a single CLA4 in sixteen consecutive clock cycles to build a 64-bit adder. The circuit starts its operation with a complete pulse (0-1-0, guaranteed one positive pulse) on the *start* signal. When the operation starts, the sequential adder collects the 64-bit operands form its *dA* and *dB* inputs. After that, the adder starts the adding process using the CLA4 combinational circuit. When this is completed, the 64-bit result of the adder will become available in the output's 64-bit *Result*, and the *done* signal becomes 1. This signal remains active until the next time that the *start* signal becomes 1.

In this homework, you are to design and describe the circuit discussed above in C++ using the RTL *bus* package. You are to

A) Show the schematic diagram of the datapath of the 64-bit adder circuit.
B) Write the circuit datapath in C++ using the RTL *bus* package.
C) Show the controller state diagram of the circuit.
D) Write C++ description of the controller based on **Huffman model**. Use an **asynchronous** reset.
E) Describe the complete circuit by putting together the datapath and the controller.
F) Write a testbench and test your design using at-least five different scenarios.

Deliverables:

1. All C/C++ codes with proper naming
2. A complete report containing
   - Schematic diagrams drawing in Visio or other visualization tools,
   - Enough design illustration and description,
   - Simulation results, input data, and output justification.