University of Tehran

Electrical and Computer Engineering Department

ECE (8101) 342

Object Oriented Modeling of Electronic Circuits – Spring 1401-02

**Homework 1: C++ Logic Modeling**
**Due Date: Esfand 06**

*Benchmarks* are groups of designed circuits that are used for the evaluation and performance of different testing approaches. There are different types of benchmarks. For example, ISCAS-85 series contain combinational benchmarks, ISCAS-89 series contain sequential benchmarks and ITC-99 series are behavioral benchmarks.

C432 is a combinational circuit that belongs to the ISCAS-85 family with thirty-six inputs and seven outputs. As discussed in the course lectures, C++ modeling of C432 requires calling the gates in proper order.

You are to write a C++ model that will not require ordering when used for a combinational circuit. Use the base model from the gates discussed in class, and add a *changed* flag to it. Gates will be used in a loop and iteration through the loop continues until no gate in the loop has had a fresh event in the *changed* flag. Use the *wire* type discussed in the course lectures.

**A)** Write a C++ program for converting a line-oriented Verilog gate netlist to C++ list of gates.
**B)** Simulate the C++ model of C432 in random order. Report the results of the circuit and compare them with the expected values, at least for five scenarios.
**C)** Rewrite the provided gate classes to handle the *changed* flag for unordered implementation.
**D)** Use the modified gates for the C432 model in an event-based loop for unordered implementation of the circuit.
**E)** Verify your unordered implementation using different scenarios (at least five scenarios).