Baseboard
Design Reference Document

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Revision History

Version 1

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1   Introduction

The baseboard module contains all the signal and power IO for the effects pedal. Input voltage of 9 V DC is regulated to 12V to drive an analog switch and the effects board and to 3.3 V to drive the LED indicators and footswitches. A 16 bit microcontroller manages the switching logic, interfaces with peripherals, and supervises the power supply circuit. The audio input and output are routed to the effects modules via the switching circuitry through a cable.

2   Specifications

1. Power

   (a) The Baseboard shall provide a 9–12 V $\pm$1% power supply capable of sourcing $\pm$50 mA each to the audio effect modules

   (b) The Baseboard shall provide low-voltage power circuitry capable of operation from 1.1 V $\pm$1% to 3.3 V $\pm$1%

   (c) The Baseboard shall be capable of sourcing 300 mA peak to drive local peripherals

2. Input/Output

   (a) The Baseboard shall route the audio signal to the baseboard while providing a true bypass path directly to the output

   (b) The Baseboard shall provide input impedance of 1 MΩ $\pm$1% and output impedance of 50 kΩ $\pm$1%

   (c) Input Filter

   (d) Output Filter

3. Switching

   (a) The audio signal shall be switched using high quality analog switches to maximize durability and signal integrity

   (b) The switches shall have an input impedance of no greater than 500 Ω to minimize signal degradation

3   System Architecture

4   Power Supplies

4.1   Overview

Input power is provided from the DC input jack or the USB-C port and is fused with PTC thermistors. A full-bridge rectifier at the DC input jack allows for both center-negative and center-positive connections. Both supplies can be powered by either the DC input at 9–12 V or the 5 V USB VBUS supply, with current OR-ing capability provided by the polarity protection rectifier and a schottky diode in series with the USB VBUS. Following the current OR-ing circuitry and overcurrent protection, the input power flows to the DC/DC converters.

   The Baseboard requires two voltage rails: the analog voltage rail at 12 V and the digital voltage rail at 3.3 V. The analog voltage rail is powered by the Texas Instruments TPS61170 and the digital rail is powered using a voltage regulator for simplicity. The coupled-inductor SEPIC topology was selected for its low ripple and for its ability to act as both a step-up and step-down converter. The TPS61170 supports the SEPIC topology and has a high, fixed switching frequency of 1.2 MHz, allowing for small surface-mount passives to reduce cost and simplify assembly. The analog supply, at 12 V, also employs a linear regulator as a filter to further reduce ripple and improve line regulation. The second regulator stage brings the voltage down to the 12 V required to power the analog rail.
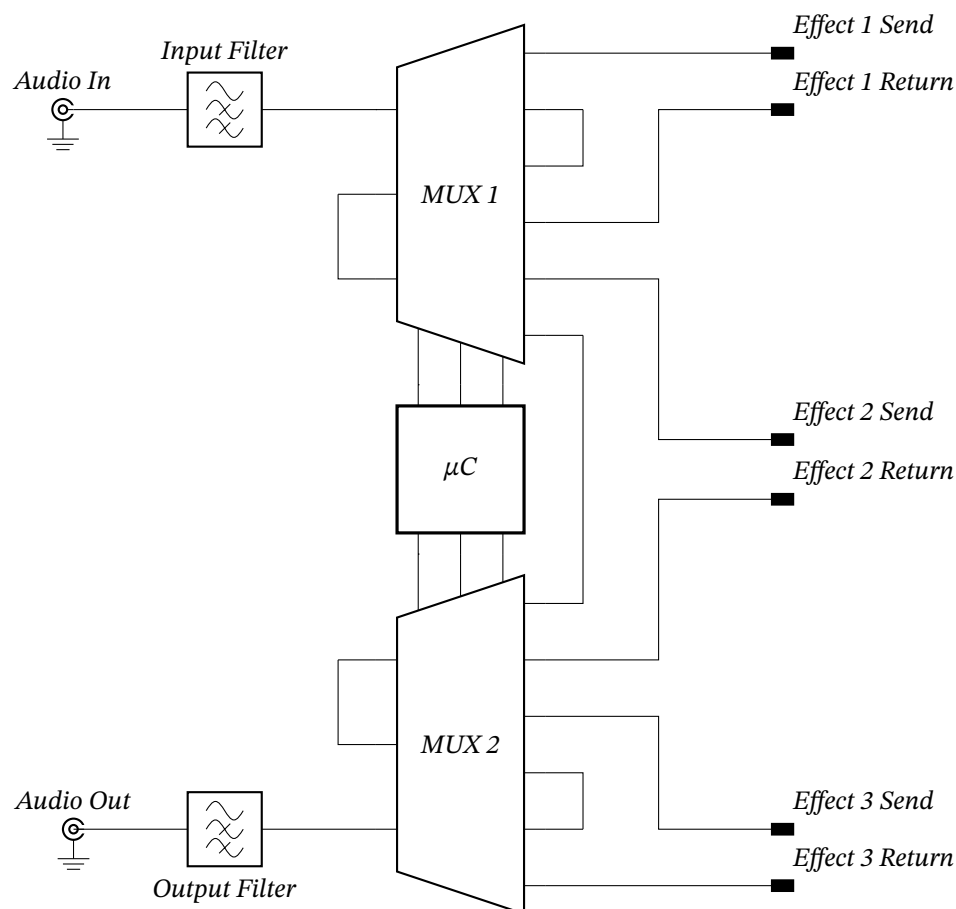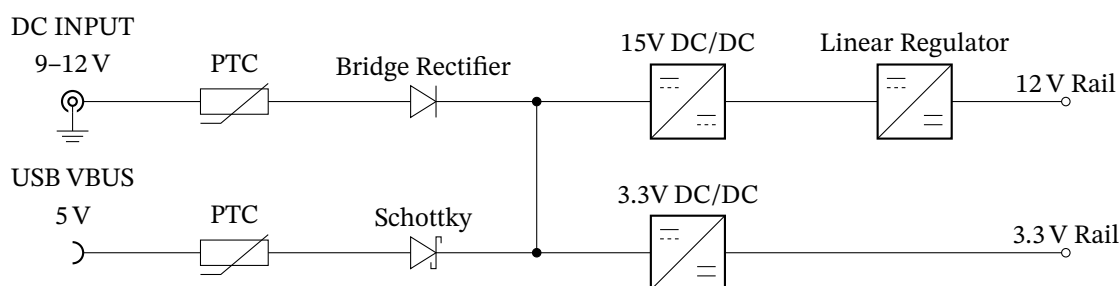
Figure 1: Audio Switching Architecture

Figure 2: Power Supply Architecture

4.2   Analog Supply

4.2.1   Inductor

The design for the analog DC/DC converter begins with inductor selection. Output current capacity is largely determined by the inductor size. For this design, a small inductor is sufficient as the amount of current required by the effects is generally small. A standard compact coupled inductor with series inductance of $22\,\mu\text{H}$ and parallel inductance of $11\,\mu\text{H}$ is predicted to be sufficient to drive loads at up to $80\,\text{mA}$ per effects module, worst-case, by the following Monte Carlo analysis with parameters extracted from the relevant component's datasheets

and with three modules. The analysis was performed for the three specified input voltages: 5 V, 9 V, and 12 V. Based on the analysis, the supply is able to safely drive 200 mA per effects module if powered from a 12 V input, which allows for future expansion using this design.
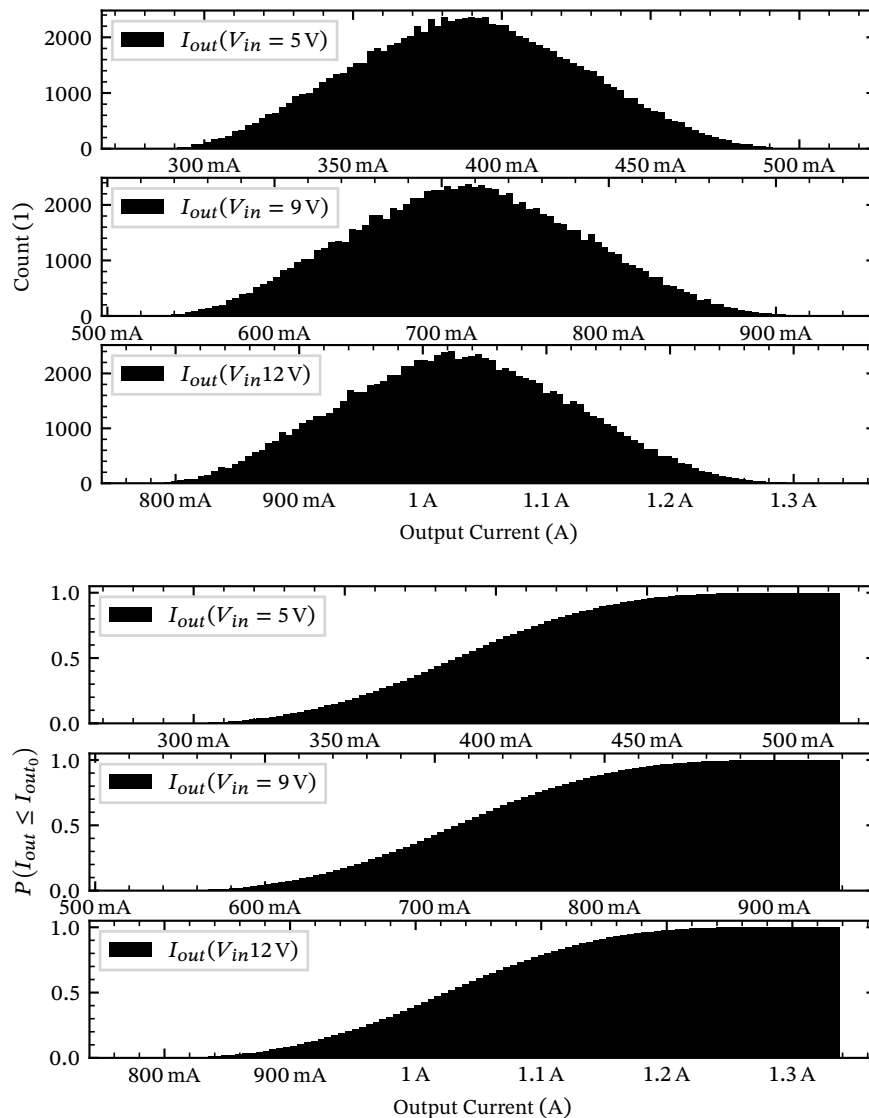

Figure 3: Power Supply Maximum Output Current

The analysis begins by assuming each parameter may be described by a probability distribution function and assigning a reasonable function to each. For the majority of datasheet parameters, the manufacturer only provides three values: an upper bound, a lower bound, and a nominal value - we assume that these datasheet parameters have a triangular PDF based on the given bounds and value for the purpose of this analysis but this may very well not be the case depending on the available components.

4.2.2   Feedback Network

The output voltage of the converter is determined by the following expression.

$$V_{out} = V_{ref}\left(\frac{R_1}{R_2} + 1\right)$$

The output voltage is a function of R_1 and R_2, and their tolerances determine the precision of the output voltage. The minimum possible output voltage, assuming all parts are within specifications, is 13.2 V, so the values shall be chosen to yield an output above that so that 14 V is beyond the lower tail of the output distribution. The value for V_{ref} comes from the datasheet and is the internal feedback reference voltage of the TPS61170. The values chosen for the feedback resistors are below; a 1% tolerance was chosen as the standard design tolerance to reduce variation.

$$R_1 = 86.6\,\text{k}\Omega \pm 1\%$$

$$R_2 = 10.0\,\text{k}\Omega \pm 1\%$$

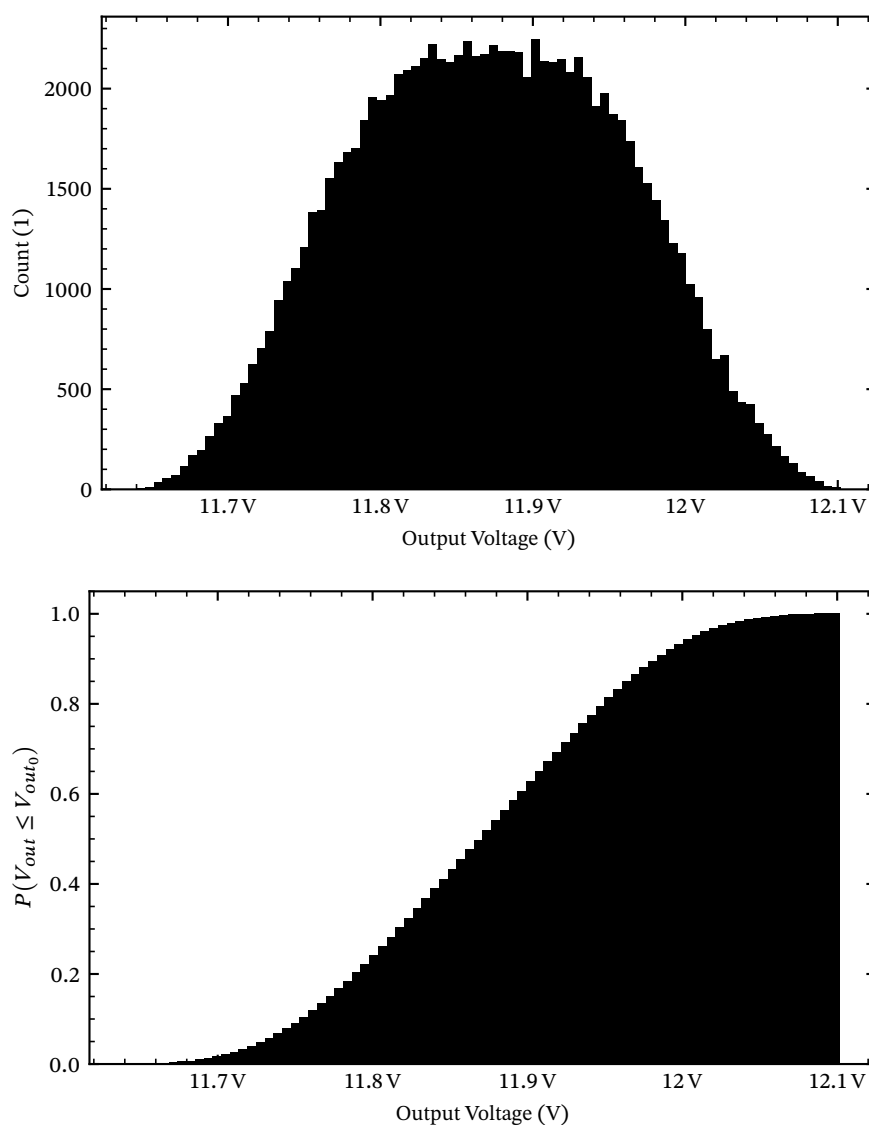$$V_{out,\,min.} \approx 11.6\,\text{V}$$

Figure 4: Power Supply Output Voltage

4.2.3 Diode

The switching diode used must have a fast recovery time and support a larger reverse-voltage than that of the TPS61170 (40 V). A robust component for this application is the Diodes Incorporated DFLS240L-7 in a PowerDI-123 package, which meets the requirements, has a low forward-voltage of around 20 mV at low currents, and is a standard part with many alternates available. The Diodes Incorporated DFLS260L-7, also in a PowerDI-123 package, is promoted as a robust alternate from the same family with a higher voltage rating.

$$I_D = I_S \left(e^{\frac{q_e - V_D}{n k_B T}} - 1 \right)$$

$$V_D = \frac{n k_B T}{q_{e^-}} \ln \left(\frac{I_D}{I_S} + 1 \right)$$

4.2.4 Input/Output Capacitors

Input and output capacitors are selected based on the upper limits of the datasheet recommendations and are chosen to be 12 μF MLCC-type surface-mount capacitors. In order to minimize derating, a medium-voltage and physically large capacitor is selected with a voltage rating of greater than 50 V.

$$C_{out,min.} = 26.1 \, \mu F$$

4.2.5 SEPIC Coupling Capacitor

The SEPIC coupling capacitor is chosen to be 1 μF. Similar to the output capacitors, to minimize derating due to applied DC bias voltage, a medium-voltage and physically large capacitor is selected with a voltage rating of greater than 50 V. The figure below suggests that a 500 nF capacitor would be sufficient, but the datasheet recommends 1 μF and there are already other 1 μF capacitors used in the design.

$$C_{s,min.} = 0.523 \, \mu F$$

4.2.6 Compensation Network

The compensation network for the DC/DC converter shall be tuned with the first prototypes.

4.2.7 Linear Regulator

The generic 1117-style three-terminal regulator was chosen as the post-regulator for the analog voltage rail for its low dropout voltage, low cost, and wide availability and compatibility with offerings from several manufacturers. The BOM specifies an Onsemi part number but any 1 A 1117-style regulator should be compatible.

The output voltage is determined via the typical three-terminal voltage regulator equation, shown below.

$$V_{out} = V_{ref} \left(1 + \frac{R_2}{R_1} \right) + I_{adj} R_2$$

Setting $R_1 = 120 \, \Omega$ sets the current through the feedback network to 10 mA, which is nominally twice the required current to maintain regulation. With R_1 defined, the other parameters are determined from the datasheet and a value for R_2 is obtained.
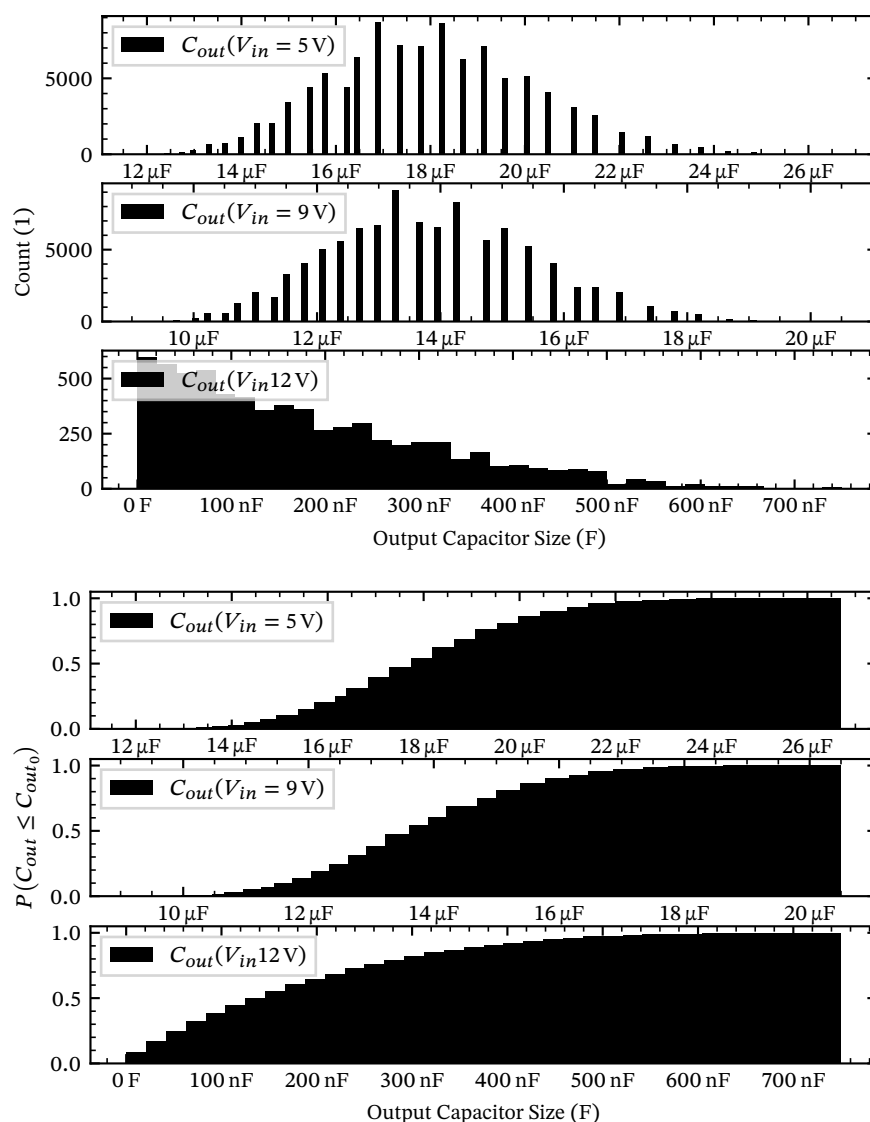
Figure 5: Power Supply Output Capacitor Size

4.3   Low-Voltage Supply

4.3.1   Linear Regulator

The low voltage supply is provided by a linear voltage regulator for simplicity. In the future, a second switching converter may be designed to replace it, in the interest of efficiency. To consolidate the bill of materials the same regulator is used as for the analog supply. The output voltage is determined by the same relationship as that shown above. By letting $V_{out} = 3.3\,\text{V}$, $R_1 = 120\,\Omega$, and $I_{adj} = 120\,\mu\text{A}$, the above relationship yields approximately $R_2 = 196\,\Omega$. The low-voltage supply can be run at lower voltages. A study should be performed to determine how low - $1.8\,\text{V}$ is supported by all digital circuits in the system.
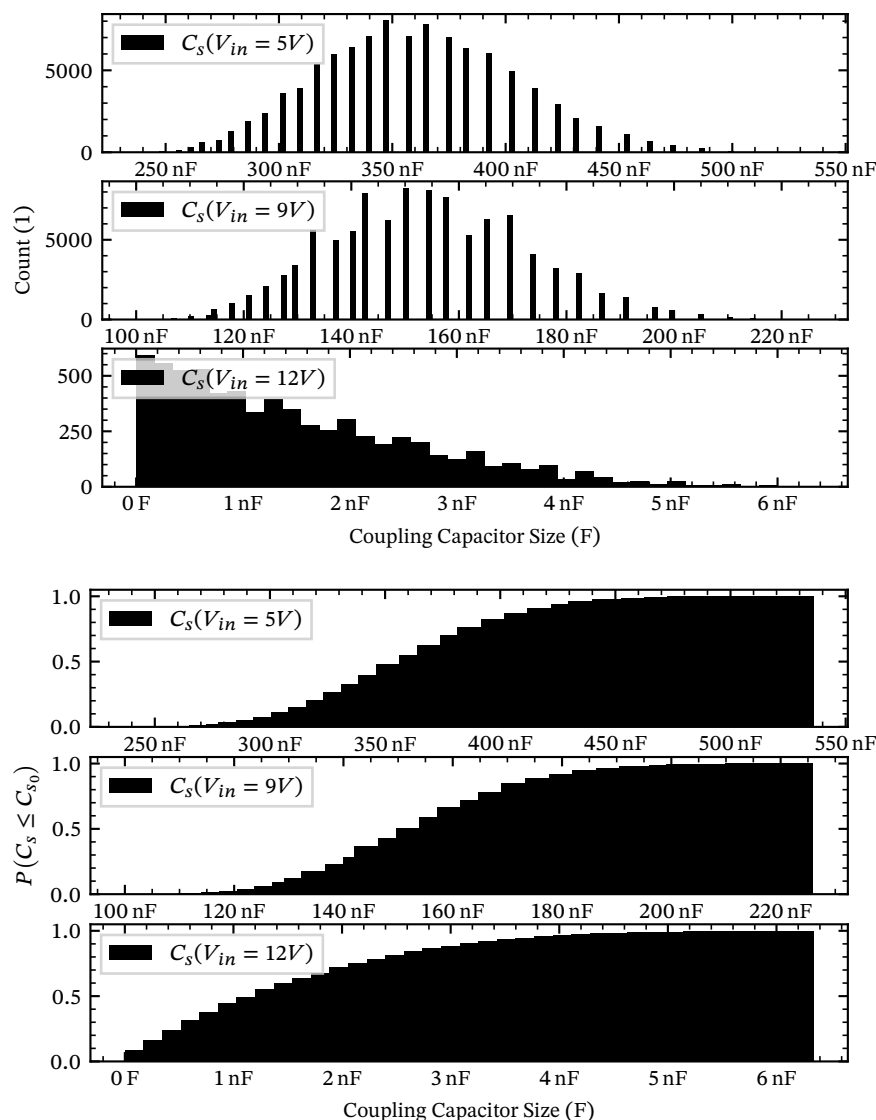
Figure 6: Power Supply SEPIC Coupling Capacitor Size

5 Effects Interface

The effects interface connects three external effects modules through two TMUX4053 analog multiplexers. The TMUX4053 is an upgraded version of the standard 4053 CMOS multiplexer with a higher voltage rating and improved impedance parameters. The signals are sent to the external modules and return via the same connectors, then are routed through the multiplexer circuit to the next effects module or to the main output.

5.1 Switching

The TMUX4053 was selected for two main reasons. Primarily, it supports the 12V supply with comfortable margin. As a second reason, the TMUX4053 is offered in a compact SMD package which improves reliability. The control signals for the multiplexers are generated by the RP2040 microcontroller which polls the footswitches and accordingly manages the switching logic for the multiplexers.
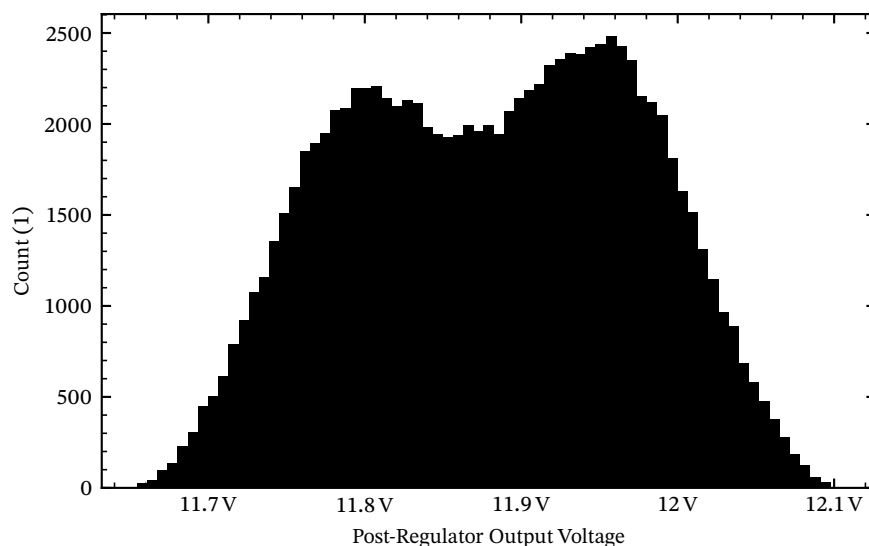
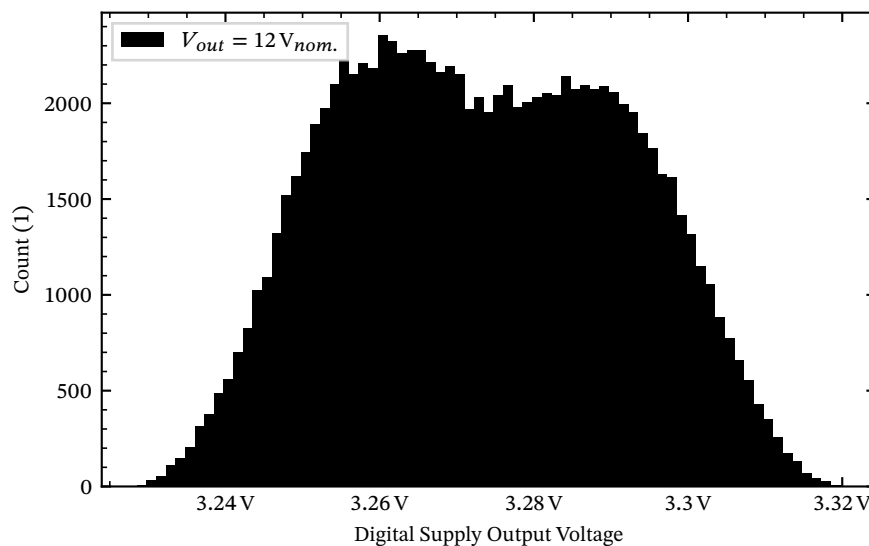Figure 7: Analog Supply Post-Regulator Output Voltage

Figure 8: 3.3 V Regulator Output Voltage

5.2 Interface

6 Microcontroller

The Raspberry Pi RP2040 dual-core ARM microcontroller was selected for two primary reasons: its extremely good cost per performance ratio despite being much more powerful than this application demands, and for the excellent documentation provided by the manufacturer.

In this design, the microcontroller performs the functions listed below, along with some other minor tasks.

- Manage audio switching logic and control analog switches

- Monitor footswitch status

- Control indicator LEDs

- USB 2.0 controller

6.0.1   Power

The microcontroller has a peak current draw of approximately 100 mA from the 3.3 V rail, yielding a power consumption of approximately 330 mW. The RP2040's internal low-voltage levels are generated using the integrated LDO which uses two external capacitors (C411 and C413), shared between pin 45 and pin 23 of the IC. The remaining external capacitors are used as decoupling capacitors for the 3.3 V rail.

6.1   Memory

Any standard AT25xxx memory may be used for this design, assuming it has the correct package and memory layout. A DFN package was selected for mechanical reliability and for being widely available. The design specifies the maximum possible memory of 128 Mbit to ease the software development process, but may be reduced in the future as an exercise in cost reduction.

6.2   Clocks and Timing

The manufacturer's recommend crystal, the ABM8-272-T3, was selected to generate the clock signals. The crystal has an SMD package and is widely available. If unavailable, a new crystal will have to be selected and rigorously tested.

6.3   GPIO

7   Peripherals

7.1   Overview

7.2   Footswitches

7.3   USB