# Baseboard Design Reference Document

The baseboard module contains all the signal and power IO for the effects module. Input voltage of 9V DC is regulated to +/- 9V to drive an analog switch and the effects board and to +3.3V to drive the LED indicators and footswitches. A 16-bit microcontroller manages the switching logic, interfaces with peripherals, and supervises the power supply circuit. The audio input and output are routed to the effects board via the switching circuitry through a flat flex cable.

[BLOCK DIAGRAM]

In order to generate plots and perform design analysis, libraries must be imported below:

# iec16022 for qr codes

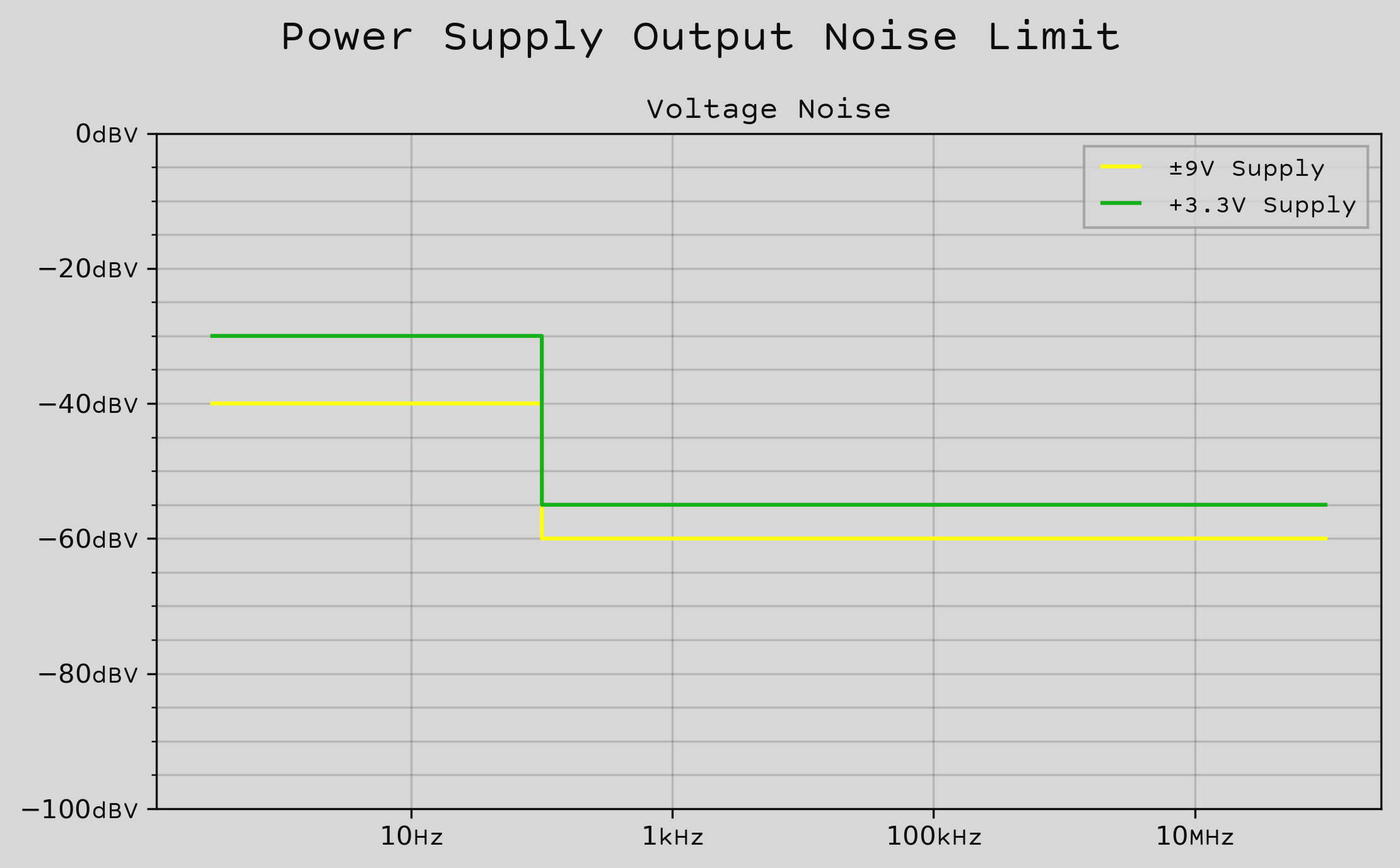
import numpy as np  
  
from matplotlib import pyplot as plt  
plt.style.use('refdoc.mplstyle')  
from matplotlib.ticker import EngFormatter  
  
# define formatter for frequency  
formatter\_Hz = EngFormatter(unit='Hz', sep="")  
  
# define formatter for time  
formatter\_s = EngFormatter(unit='s', sep="")  
  
# define formatter for resistance  
formatter\_Ohm = EngFormatter(unit='Ω', sep="")  
  
#define formatter for dBV  
formatter\_dBV = EngFormatter(unit='dBV', sep="")

### Specifications

1. Power
   1. The Baseboard shall provide a ± 9V, ± 1% power supply capable of sourcing ± 200mA peak to the audio effects board
   2. The Baseboard shall provide low-voltage power circuitry capable of operation from +1.2V, ± 1% to +5V, ± 1%
   3. The Baseboard shall be capable of sourcing 150mA peak to drive local peripherals
   4. Noise from any power supply must be below -40dB at all frequencies and below -60dB above 100Hz
2. Input/Output
   1. The Baseboard shall route the audio signal to the baseboard while providing a true bypass path directly to the output
   2. The Baseboard shall provide input impedance of 1MΩ ± 1% and output impedance of 49.9kΩ ± 1%
   3. Input Filter
   4. Output Filter
3. Switching
   1. The audio signal shall be switched using high quality analog switches to maximize durability and signal integrity
   2. The switches shall have an impedance of no greater than 500Ω to minimize impedance matching losses

#### Output Power Noise

min\_freq = 0.3  
max\_freq = 100E6  
frequency = np.logspace(np.log10(min\_freq), np.log10(max\_freq), 30000, base=10)  
  
noise\_spec\_9V = []  
noise\_spec\_LV = []  
  
corner\_freq\_9V = 100  
corner\_freq\_LV = 100  
  
for freq in frequency:  
 if freq < corner\_freq\_9V:  
 noise\_spec\_9V.append(-40)  
 else:  
 noise\_spec\_9V.append(-60)  
   
 if freq < corner\_freq\_LV:  
 noise\_spec\_LV.append(-30)  
 else:  
 noise\_spec\_LV.append(-55)  
  
fig, ax = plt.subplots(1, 1)  
  
ax.plot(frequency, noise\_spec\_9V, label='±9V Supply')  
ax.plot(frequency, noise\_spec\_LV,label='+3.3V Supply')  
  
ax.set\_xscale('log')  
ax.xaxis.set\_major\_formatter(formatter\_Hz)  
  
ax.yaxis.set\_major\_formatter(formatter\_dBV)  
ax.set\_ylim(-100, 0)  
ax.set\_title("Voltage Noise")  
fig.suptitle("Power Supply Output Noise Limit")  
ax.legend()  
fig.tight\_layout()



## System Block Diagram

## Circuit Design

Overview

### Power

ADP5070 Datasheet: <https://www.analog.com/media/en/technical-documentation/data-sheets/ADP5070.pdf>

I\_OUT1 = 200E-3  
I\_OUT2 = -200E-3

#### Feedback Resistors

To select the appropriate feedback resistors, the following relationships were taken from the datasheet to compute the correct values.

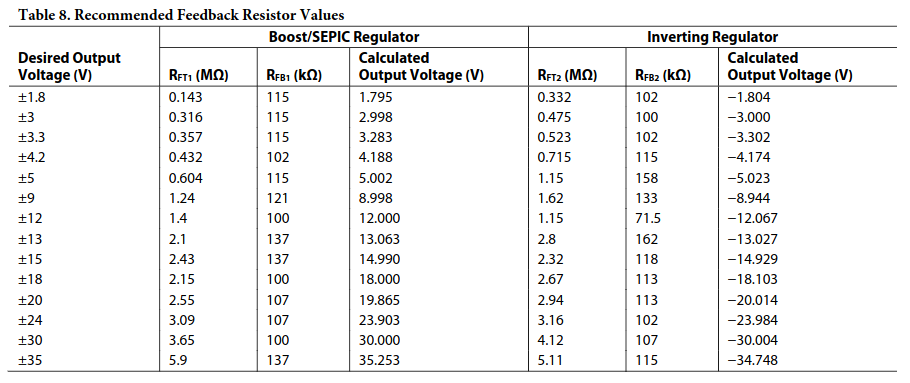
The positive output for the boost regulator can be set using the relationship

where is the positive output voltage, is the reference voltage, is the feedback resistor from to , and is the feedback resistor from to .

The negative output for the inverting regulator can be set using the relationship

where is the negative output voltage, is the reference voltage, is the feedback resistor from to , is the feedback resistor from to , and is the pin reference voltage.

Recommended values can also be selected from the table below, from the manufacturer's datasheet.



In order to have the correct margin to allow for the linear regulator drop-out voltage, output voltages of were selected, yielding the following values for the feedback resistors as taken from the table.

The low-noise precision resistors chosen for the design do not support values above , so these ratios must be reconfigured to have the largest value resistor be . The relationships above can be rewritten to solve for the other resistor value.

V\_POS = 12  
V\_NEG = -12  
  
V\_IN = 8.55  
  
V\_FB1 = 0.8 # from datasheet page 3  
V\_FB2 = 0.8 # from datasheet page 4  
V\_REF = 1.6 # from datasheet page 4  
  
R\_FT1 = 1E6  
R\_FT2 = 1E6  
  
R\_FB1 = R\_FT1 / ( (V\_POS / V\_FB1) - 1 )  
R\_FB2 = R\_FT2 \* (V\_REF - V\_FB2) / (V\_FB2 - V\_NEG)  
  
print(f"R\_FT1 = {R\_FT1} Ω")  
print(f"R\_FB1 = {R\_FB1} Ω")  
print(f"R\_FT2 = {R\_FT2} Ω")  
print(f"R\_FB2 = {R\_FB2} Ω")

R\_FT1 = 1000000.0 Ω  
R\_FB1 = 71428.57142857143 Ω  
R\_FT2 = 1000000.0 Ω  
R\_FB2 = 62500.0 Ω

#### Output Capacitors

The capacitor dielectric is chosen to be X5R or X7R to provide adequate temperature and DC bias characteristics. The worst-case capacitance considering temperature variation, tolerance, and voltage can be found using the following equation from the datasheet

where is the effective capacitance at the specified operating voltage, is the nominal datasheet capacitance, is the worst-case capacitor temperature derating coefficient, is the DC bias derating at the specified output voltage, and is the worst-case component tolerance.

The datasheet suggests a value of as a compromise between performance and size - a value of was selected to provide additional filtering without compromising performance by a large amount. This value will provide extremely comfortable margins at the worst-case values determined above, and will provide better filtering than the recommended value with better response time. Thus,

C\_OUT = 20E-6  
  
D\_TEMP = 0.014  
D\_BIAS = 0.120  
D\_TOL = 0.200  
  
C\_OUT\_ESR = 2.5E-3  
  
C\_OUT\_EFF = C\_OUT \* ( 1 - D\_TEMP ) \* ( 1 - D\_BIAS ) \* ( 1 - D\_TOL )

#### Input Capacitors

Larger value input capacitors reduce input voltage ripple and improve transient response of the system. Component placement should be optimized to minimize supply noise by placing the input capacitors as close as possible to the power input pins. For stability, and effective capacitance of at least is required, with a minimum of required for the PVIN1 and PVIN2 pins and required for the PVINSYS pin.

To minimize the number of componentes in the BOM, the same capacitor will be used to decouple the power input pins - one for PVIN1 and PVIN2 and another for PVINSYS.

C\_PVIN = 22E-6  
C\_PVINSYS = 22E-6

#### Capacitor

The datasheet requires a ceramic capacitor between the VREG pin and AGND.

C\_VREG = 1E-6

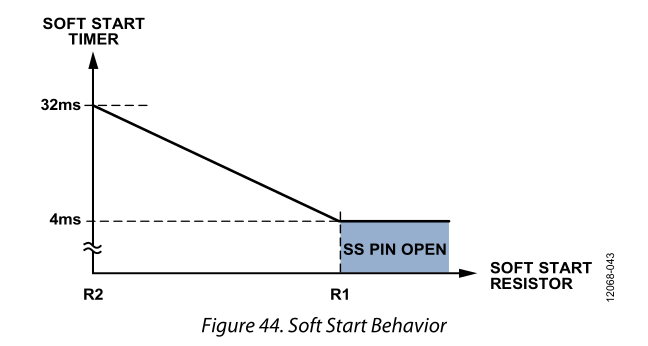
#### Capacitor

The datasheet requires a ceramic capacitor between the VREF pin and AGND.

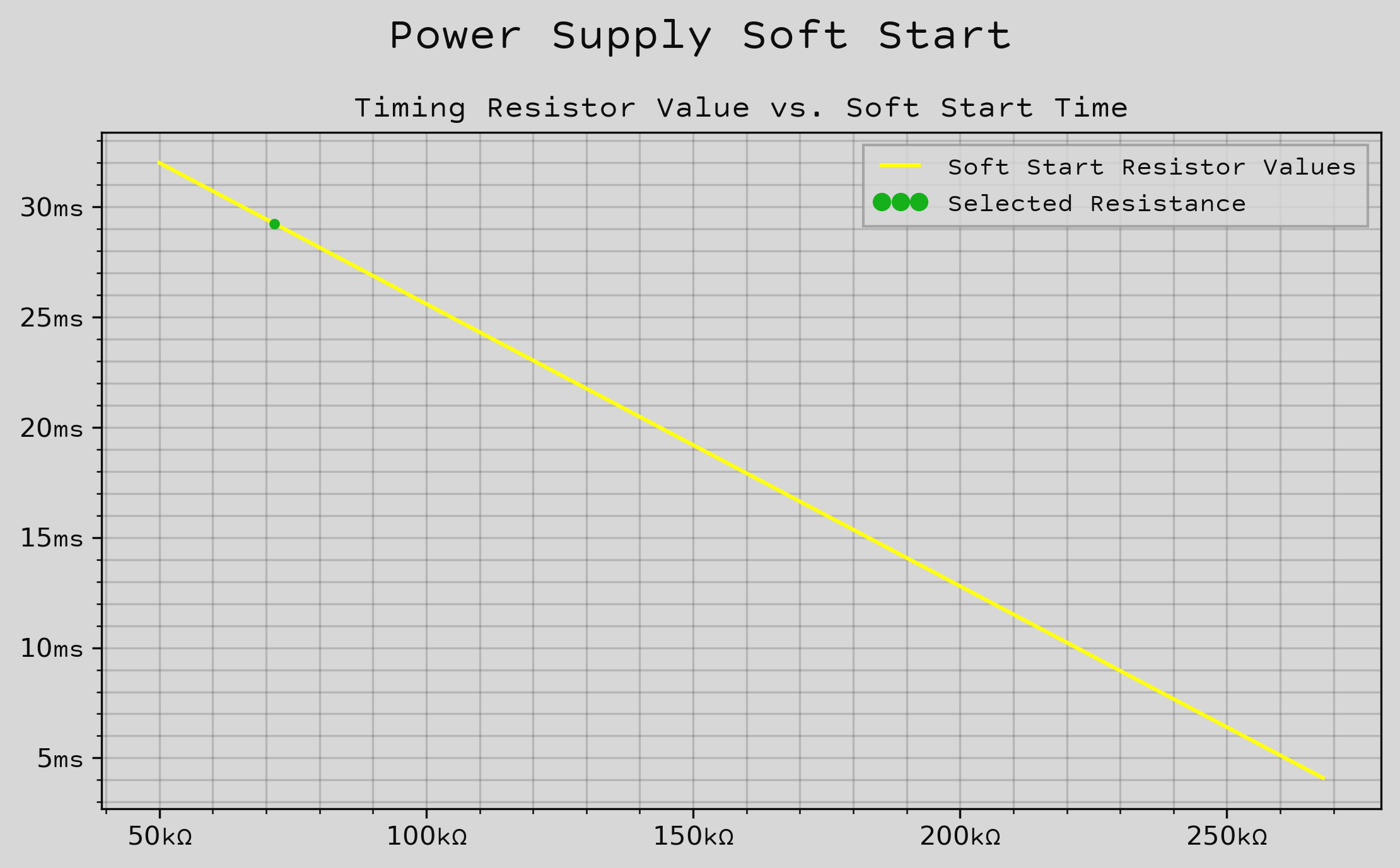
C\_VREG = 1E-6

#### Soft Start Resistor

Soft start is not a required feature, but it can be implemented and the resistor DNP'ed to save on cost if desired. The plot below shows the relationship between the soft start time and the value of the timing resistor. A resistor value of yields a soft start time of approximately and is already being used in the circuit as .



fig, ax = plt.subplots(1, 1)  
  
R\_SOFT\_START = np.linspace(50E3, 268E3, 800)  
t\_SOFT\_START = 38.4E-3 - 1.28E-7 \* R\_SOFT\_START  
  
ax.plot(R\_SOFT\_START, t\_SOFT\_START, label='Soft Start Resistor Values')  
  
R\_SOFT\_START = 71.5E3  
t\_SOFT\_START = 38.4E-3 - 1.28E-7 \* R\_SOFT\_START  
  
ax.plot(R\_SOFT\_START, t\_SOFT\_START, '.', label='Selected Resistance')  
  
ax.yaxis.set\_major\_formatter(formatter\_s)  
ax.xaxis.set\_major\_formatter(formatter\_Ohm)  
ax.set\_title("Timing Resistor Value vs. Soft Start Time")  
fig.suptitle("Power Supply Soft Start")  
ax.legend()  
fig.tight\_layout()



#### Diodes

A low forward voltage Schottky diode with less than junction capacitance is recommended for D1 and D2. The selected diode, the Diodes Incorporated DFLS240L-7, has a typical forward voltage and a typical junction capacitance of . This capacitance is higher than recommended, but the efficiency losses will be minimal.

V\_DF = 450E-3  
C\_D = 90E-12

#### Boost Regulator Inductor

The datasheet recommends an inductor value between and as a good compromise between inductor current ripple and efficiency. The inductor ripple current in the worst-case, the continuous conduction mode, can be calculated. The switch duty cycle, , can be found from the relationship below.

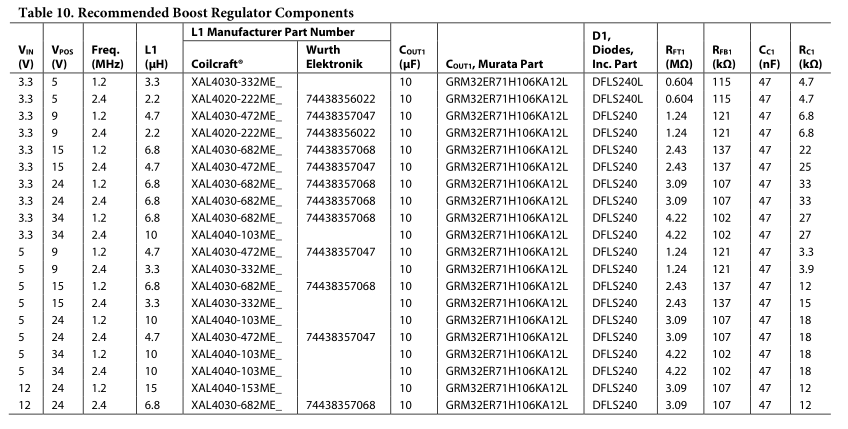
The DC input current during the constant current mode can be found from the equation below.

Using the duty cycle and switching frequency, the switch on time can be obtained as follows. The switching frequency is chosen here to be either or .

Finally, the on time is then used to find the inductor size as a function of inductor ripple current at steady-state.

Assuming inductor ripple current of 30% the maximum DC input current yields the following expression.

To ensure stability, the minimum inductance is given by the below equation from the datasheet.



f\_SW = 2.4E6  
  
DUTY\_1 = ( V\_POS - V\_IN + V\_DF ) / (V\_POS + V\_DF)  
I\_IN = I\_OUT1 / ( 1 - DUTY\_1 )  
t\_ON1 = DUTY\_1 / f\_SW  
L1 = V\_IN \* t\_ON1 \* ( 1 - DUTY\_1) / ( 0.3 \* I\_OUT1)  
L1\_MIN = 1E-6 \* V\_IN \* ( ( 0.27 / (1 - DUTY\_1)) - 0.33)  
  
print("L1 =", L1)  
print("L1\_MIN =", L1\_MIN)

L1 = 1.2773080272898825e-05  
L1\_MIN = 5.399999999999998e-07

#### Inverting Regulator Inductor

Similarly, the inductor value for the inverting regulator's inductor can be derived. Again starting with the duty cycle, we obtain the following expression.

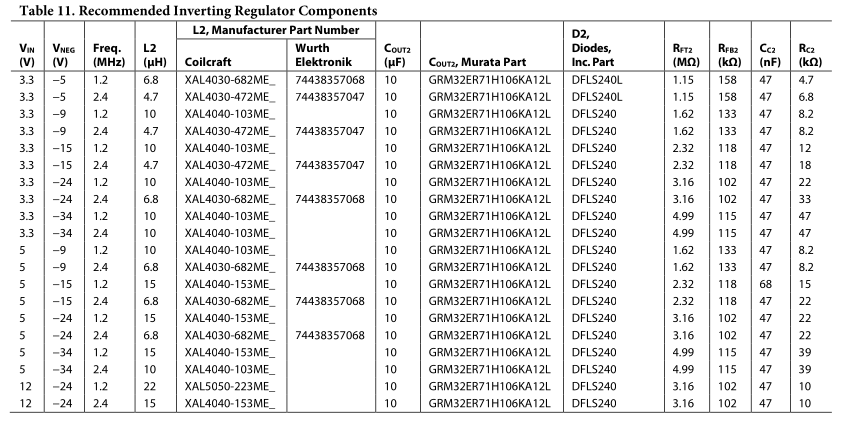
The DC current in the constant current mode can then be found as a function of the duty cycle.

The switch on time is also expressed as a function of the duty cycle.

And again, the inductance value can be obtained from the on time and the inductor ripple current.

Again assuming a ripple current of the maximum DC current will allow the expression to be solved as follows.

To ensure stability, the inductor value must be greater than the minimum inductance obtained below.

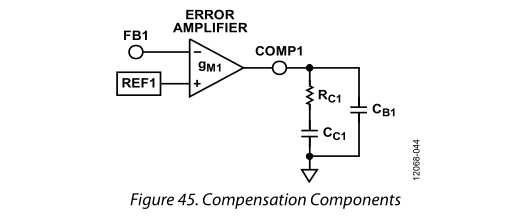


DUTY\_2 = ( np.abs(V\_NEG) + V\_DF ) / ( V\_IN + np.abs(V\_NEG) + V\_DF )  
I\_L2 = I\_OUT2 / ( 1 - DUTY\_2 )  
t\_ON2 = DUTY\_2 / f\_SW  
L2 = V\_IN \* t\_ON2 \* ( 1 - DUTY\_2 ) / ( 0.3 \* np.abs(I\_OUT2) )  
L2\_MIN = 1E-6 \* V\_IN \* ( ( 0.27 / ( 1 - DUTY\_2)) - 0.33 )  
   
print("L2 =", L2)  
print("L2\_MIN =", L2\_MIN)

L2 = 1.4331792091836734e-05  
L2\_MIN = 2.8485000000000008e-06

#### Boost Regulator Compensation

The ADP5070 allows for external loop compensation to optimize the dynamics for a given application. The design of the compensation network for the boost regulator is performed following the datasheet recommendations as follows.



The boost regulator requires compensation such that the crossover frequency occurs below the frequency of the right-half plane zero introduced by the topology of the converter. The zero is can be determined as shown,

where is the right half plane zero frequency and is the equivalent load resistance. The datasheet recommends that the regulator crossover frequency be less than or equal to one-tenth the right half plane zero frequency. The boost regulator loop gain is

where is the loop gain, is the feedback regulation voltage, is the regulated positive output voltage, is the input voltage, is the error amplifier transconductance gain, is the output impedance of the error amplifier and is , is the impedance of the series RC network from to , is the current sense transconductance gain (the inductor current divided by the voltage at ), which is internally set by the ADP5070 to 6.25 A/V, and finally is the impedance of the load in parallel with the output capacitor.

To solve for the crossover frequency, the equation may be simplified to

where is the crossover frequency.

To solve for , the datasheet provides the following equation, where .

From the datasheet, this equation can be simplified.

For best accuracy, the datasheet recommends using the effective capacitance of the output capacitor under DC bias conditions that will be seen in operation.

Once the compensation resistor has been found, the zero can be set to one-fourth the crossover frequency, per the datasheet's recommendation.

The parallel capacitor is then chosen to cancel the zero introduced by the output capacitor ESR.

From the datasheet, for most applications, must be within the range of to , and must be within the range of to .

R\_LOAD1 = V\_POS / I\_OUT1  
f\_Z1\_RHP = ( R\_LOAD1 \* ( 1 - DUTY\_1 )\*\*2 ) / ( 2\*np.pi \* L1 )  
f\_C1 = f\_Z1\_RHP \* 95E-3  
V\_FB1 = V\_POS \* R\_FB1 / ( R\_FB1 + R\_FT1 )  
G\_M1 = 300E-6 # from datasheet  
G\_CS1 = 6.25 # from datasheet  
R\_C1 = ( 2\*np.pi \* f\_C1 \* C\_OUT\_EFF \* V\_POS\*\*2 ) / ( V\_FB1 \* V\_IN \* G\_M1 \* G\_CS1 )  
C\_C1 = 2 / ( np.pi \* f\_C1 \* R\_C1 )  
C\_B1 = C\_OUT\_ESR \* C\_OUT / R\_C1  
  
print("R\_C1 =", R\_C1)  
print("C\_C1 =", C\_C1)  
print("C\_B1 =", C\_B1)

R\_C1 = 32806.31335384616  
C\_C1 = 5.793350733506955e-10  
C\_B1 = 1.5240968852764458e-12

#### Inverting Regulator Compensation

The design of the inverting regulator compensation network is similar to that of the boost regulator compensation network. For the sake of brevity, the detailed explanation has been omitted, but the process is the same as above.

R\_LOAD2 = V\_NEG / I\_OUT2  
f\_Z2\_RHP = ( R\_LOAD2 \* ( 1 - DUTY\_2 )\*\*2 ) / ( 2\*np.pi \* L2 \* DUTY\_2 )  
f\_C2 = f\_Z2\_RHP \* 95E-3  
V\_FB2 = V\_NEG \* R\_FT2 / ( R\_FB2 + R\_FT2 )  
G\_M2 = 300E-6 # from datasheet  
G\_CS2 = 6.25 # from datasheet  
R\_C2 = ( 2\*np.pi \* f\_C2 \* C\_OUT\_EFF \* np.abs(V\_NEG) \* ( V\_IN + ( 2 \* np.abs(V\_NEG) ) ) ) / ( np.abs(V\_FB2) \* V\_IN \* G\_M2 \* G\_CS2 )  
C\_C2 = 2 / ( np.pi \* f\_C2 \* R\_C2 )  
C\_B2 = C\_OUT\_ESR \* C\_OUT / R\_C2  
  
print("R\_C2 =", R\_C2)  
print("C\_C2 =", C\_C2)  
print("C\_B2 =", C\_B2)

R\_C2 = 3330.504725701844  
C\_C2 = 1.0800204962904543e-08  
C\_B2 = 1.5012739544893877e-11