AIML	COMPUTER ORGANIZATION AND ARCHITECTURE	3	0	0	3

Course Objectives

- To understand the architecture of computers and to analyze the performance using various addressing modes.
- To familiarize with hierarchical memory system including cache memories and virtual memory.
- To impart knowledge about different ways of communicating with I/O devices and standard I/O interfaces.

UNIT I BASIC STRUCTURE OF COMPUTERS 9

Functional units – Basic operational concepts – Bus structures – Performance and metrics – Instructions and instruction sequencing – Hardware – Software Interface – Instruction set architecture – Addressing modes – RISC – CISC – ALU design – Fixed point and floating point operations : Floating Point Numbers and Operations.

UNIT II BASIC PROCESSING UNIT 9

Some Fundamental concepts – Execution of a complete instruction: Branch instructions – Multiple bus organization – Hardwired control: A Complete Processor – Micro programmed control: Microinstructions – Micro program Sequencing – Wide-Branch Addressing – Microinstructions with next address field – Prefetching and emulation – Nano programming.

UNIT III PIPELINING 9

Basic concepts: Role of Cache Memory – Pipeline Performance – Data Hazards – Instruction Hazards – Influence on Instruction Sets: Addressing modes – Condition Codes – Datapath and Control Considerations – Superscalar Operation: Out-of-Order Execution – Execution Completion – Dispatch Operation – Performance Considerations – Exception Handling.

UNIT IV MEMORY SYSTEM 9

Basic concepts – Semiconductor RAM – ROM – Speed – Size and cost – Cache Memories: Mapping Functions – Replacement Algorithms – Example – Performance Considerations: Interleaving – Hit Rate and Miss Penalty– Caches on the Processor Chip – Virtual Memories – Memory Management Requirements – Associative Memories – Secondary Storage devices.

UNIT V I/O ORGANIZATION 9

Accessing I/O devices – Interrupts : Interrupt Hardware – Enabling and Disabling Interrupts – Handling Multiple Devices – Controlling Device Requests – Exceptions – Direct Memory Access: Bus Arbitration – Buses: Synchronous Bus – Asynchronous Bus – Interface circuits: Parallel Port – Serial Port – Standard I/O Interfaces (PCI, SCSI, and USB), I/O devices and processors.

Total: 45h