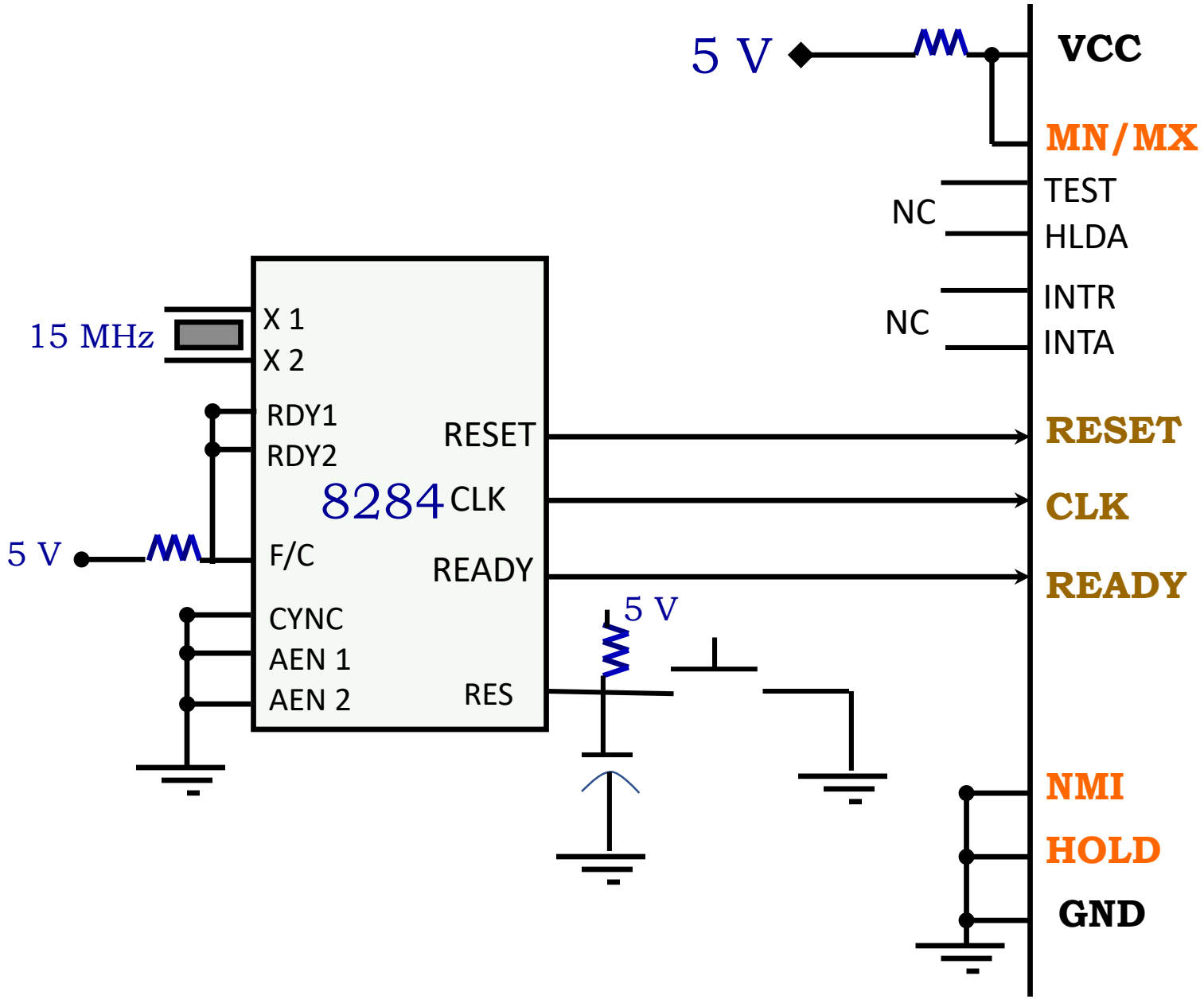
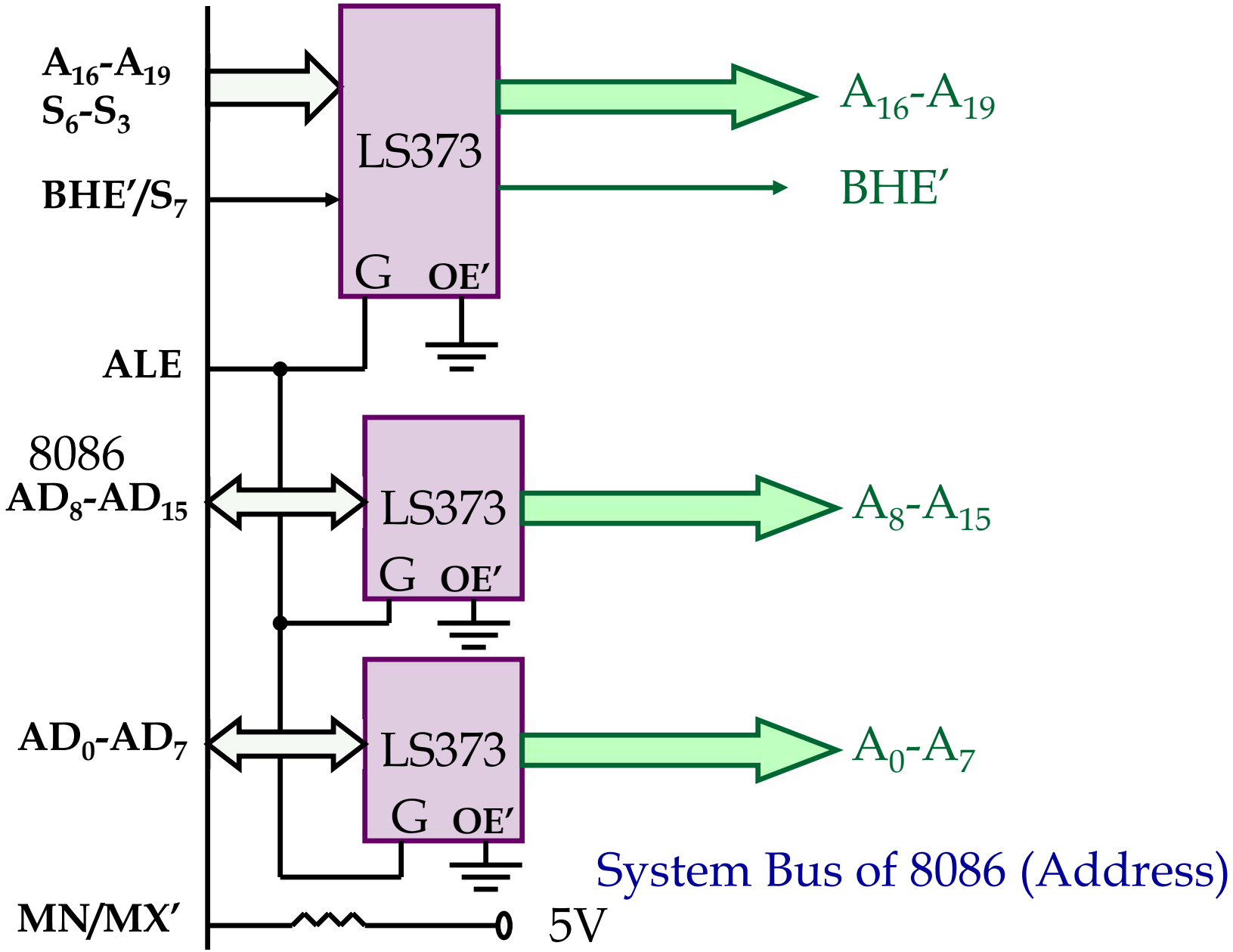
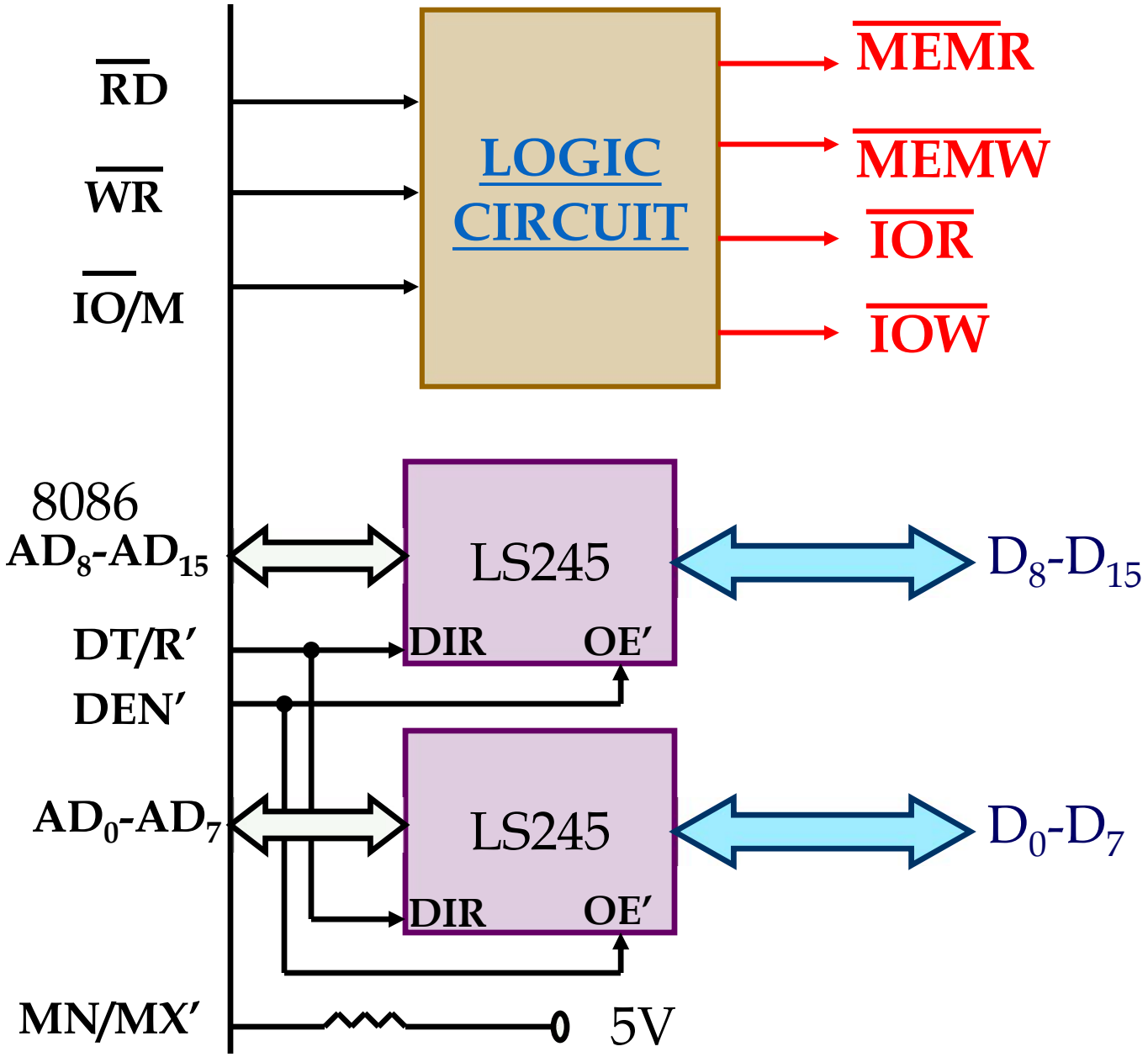
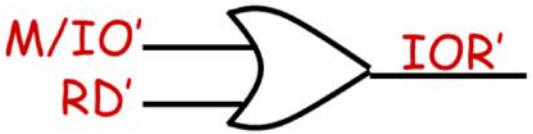

5 V
VCC
MN/MX
TEST
NC
HLDA
INTR
NC
INTA
15 MHz
X 1
X 2
RDY1
RDY2
RESET
8284
CLK
5 V
F/C
READY
CYNC
AEN 1
AEN 2
RES
5 V
RESET
CLK
READY
NMI
HOLD
GND

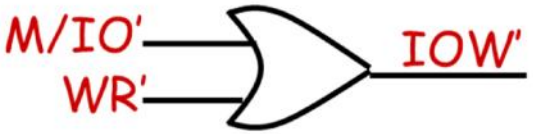
8086 Inputs


A16-A19
S6-S3
BHE'/S7
LS373
G
OE'
ALE
8086
AD8-AD15
LS373
G
OE'
AD0-AD7
LS373
G
OE'
MN/MX'
5V
A16-A19
BHE'
A8-A15
A0-A7
System Bus of 8086 (Address)

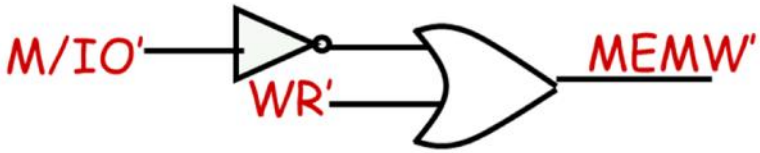


System Bus of 8086(Data + Control)

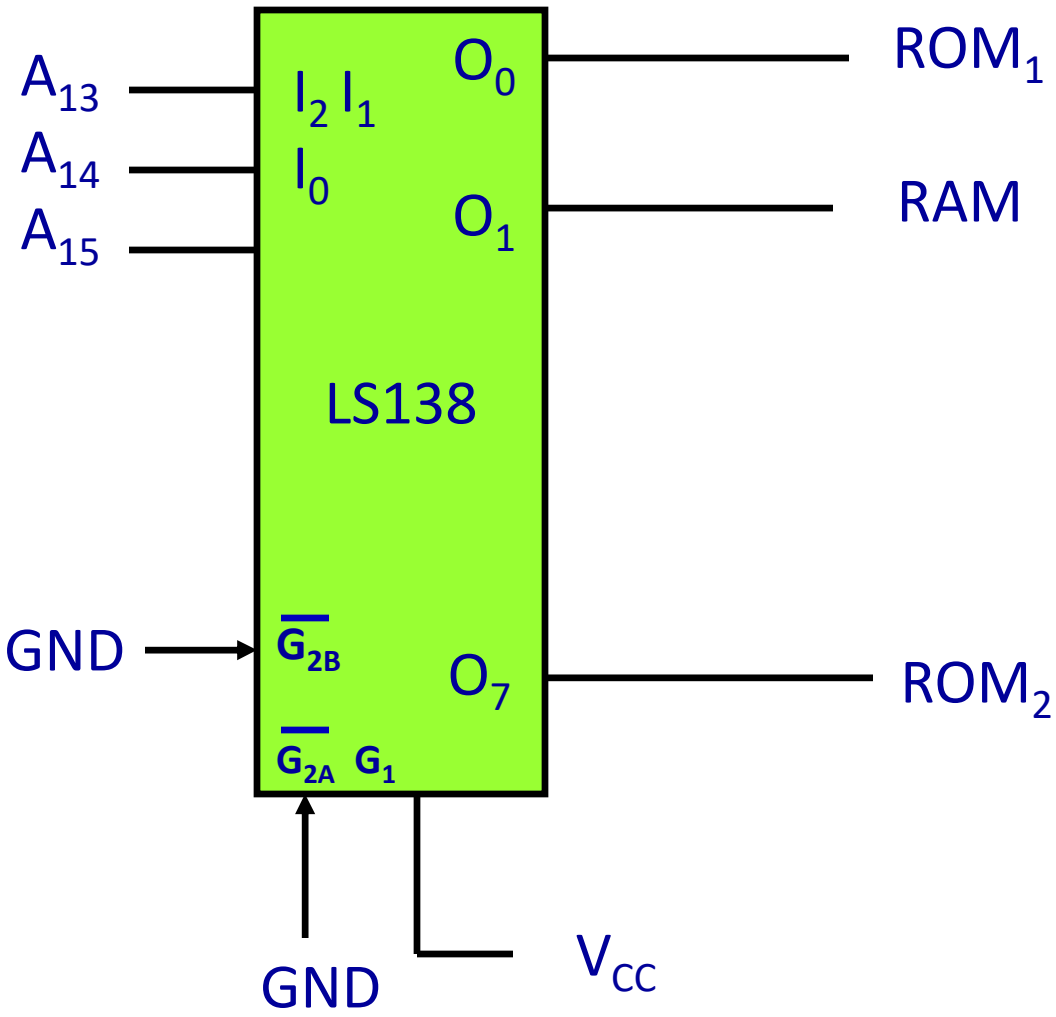




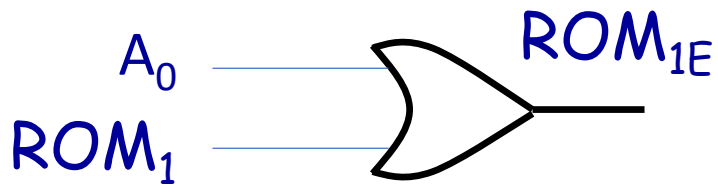
M/IO'	RD'	WR'	Bus cycle
1	0	1	MEMR'
1	1	0	MEMW'
0	0	1	IOR'
0	1	0	IOW'

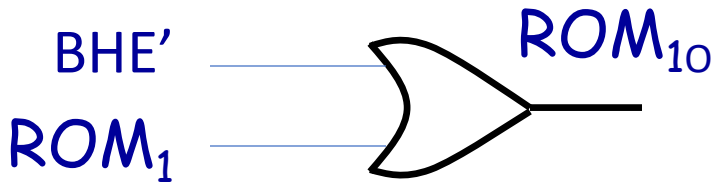


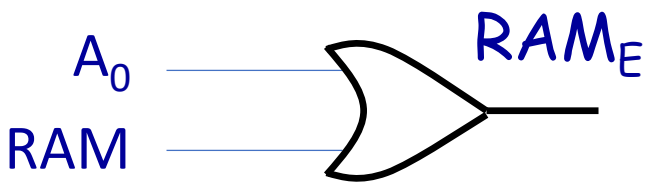
back

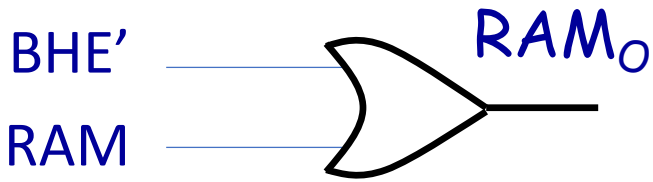


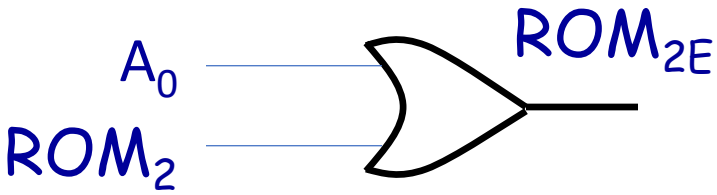
Memory Decoder

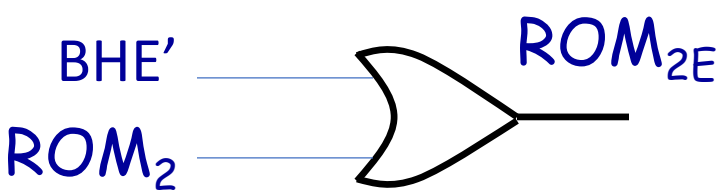

A0
ROM1
ROM1E

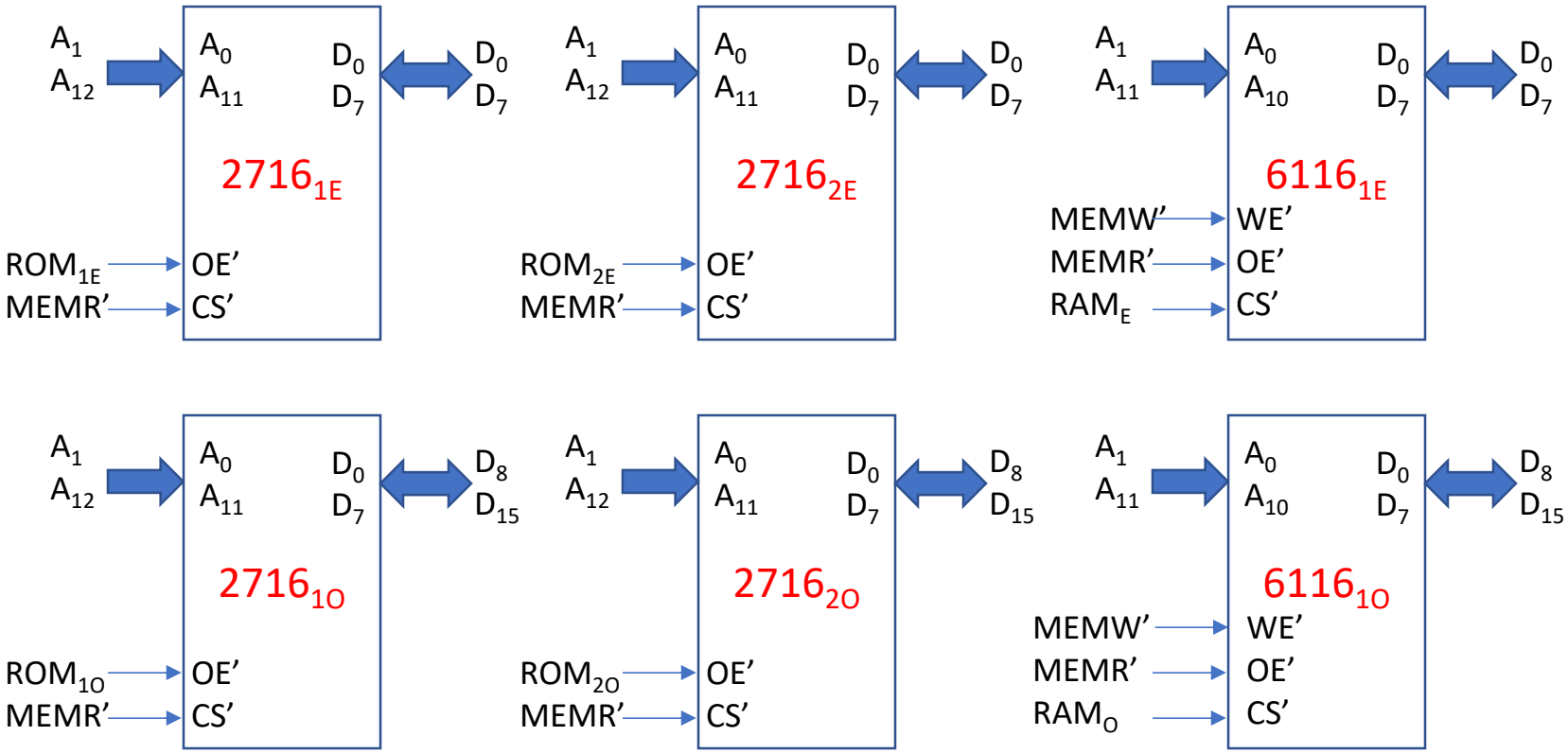

BHE'
ROM1
ROM1O


A0
RAM
RAME

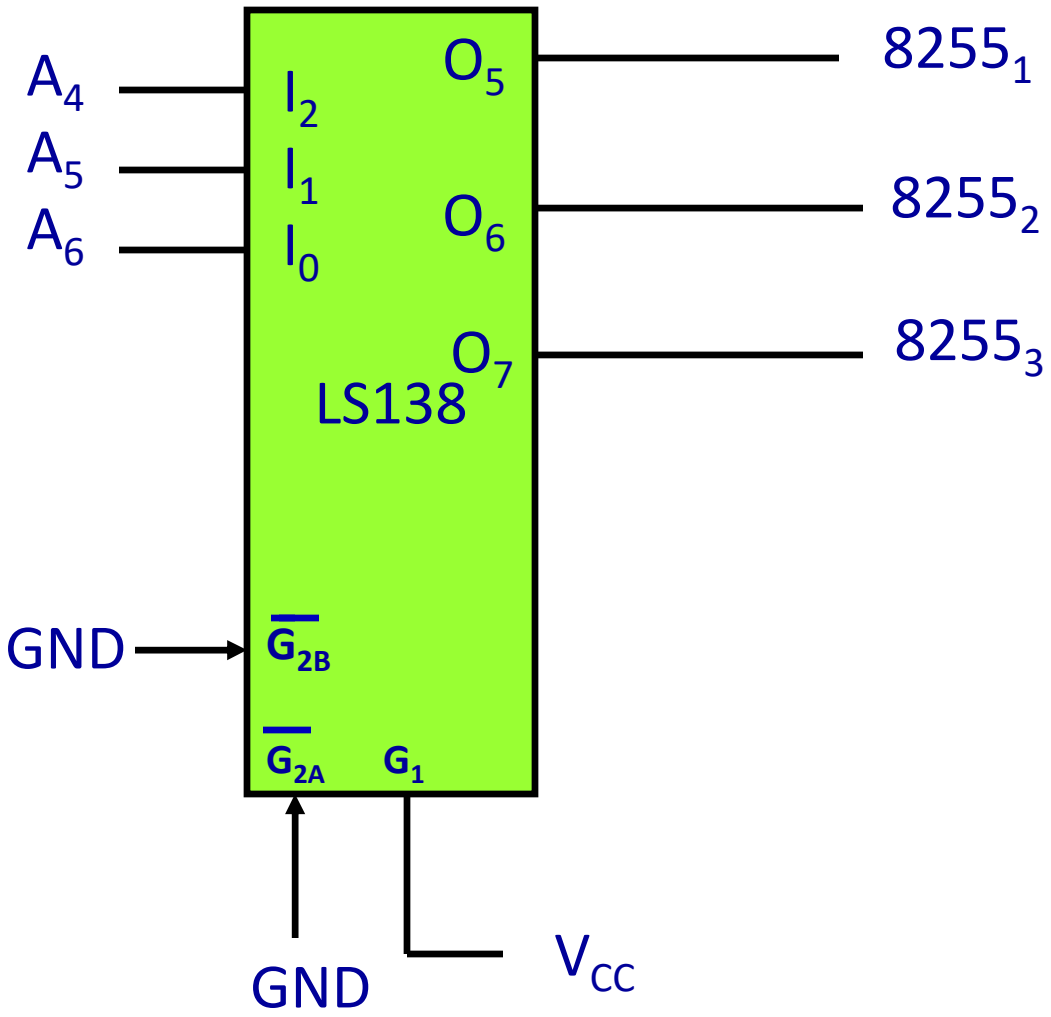

BHE'
RAM
RAMO


A0
ROM2
ROM2E


BHE'
ROM2
ROM2E

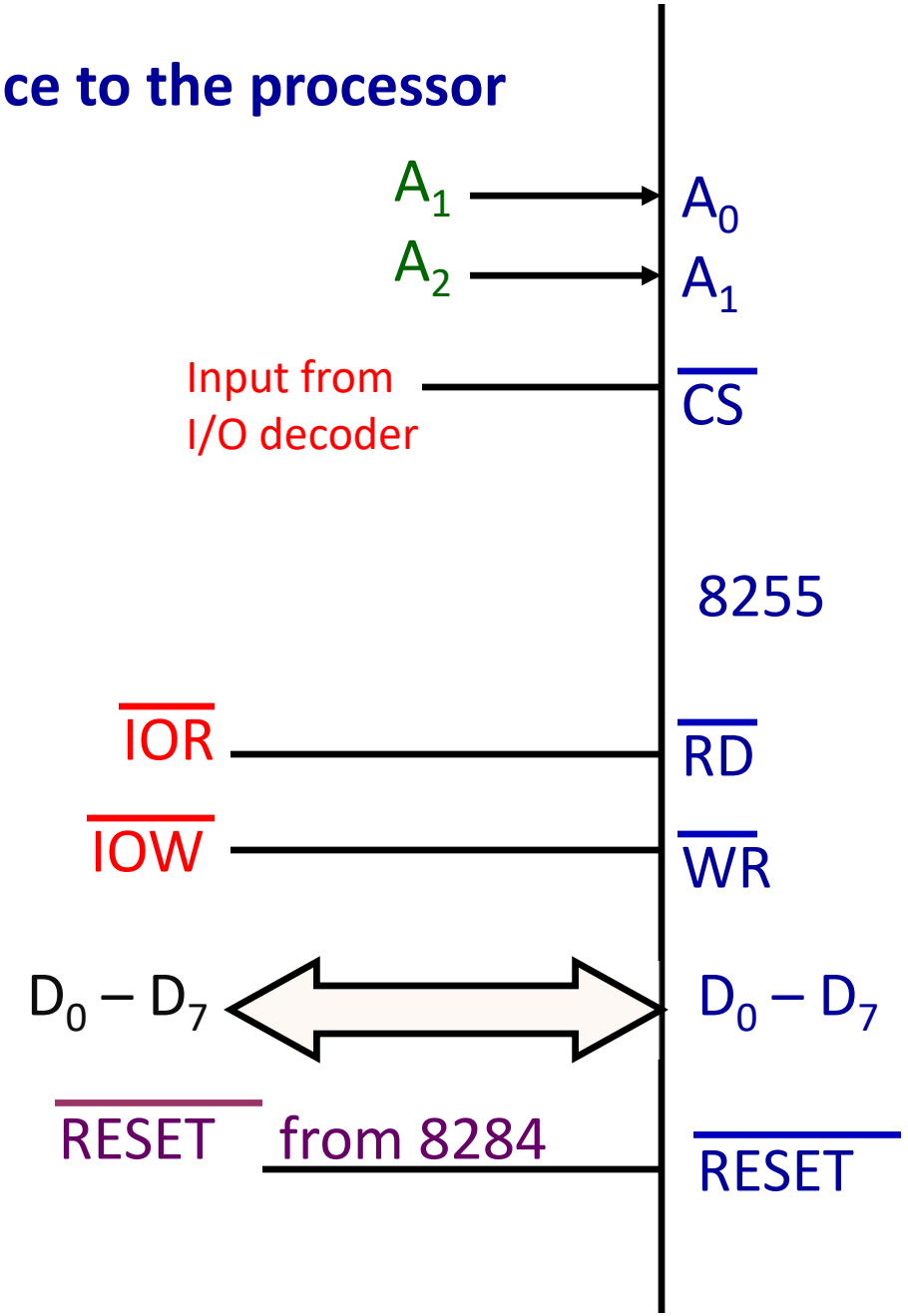


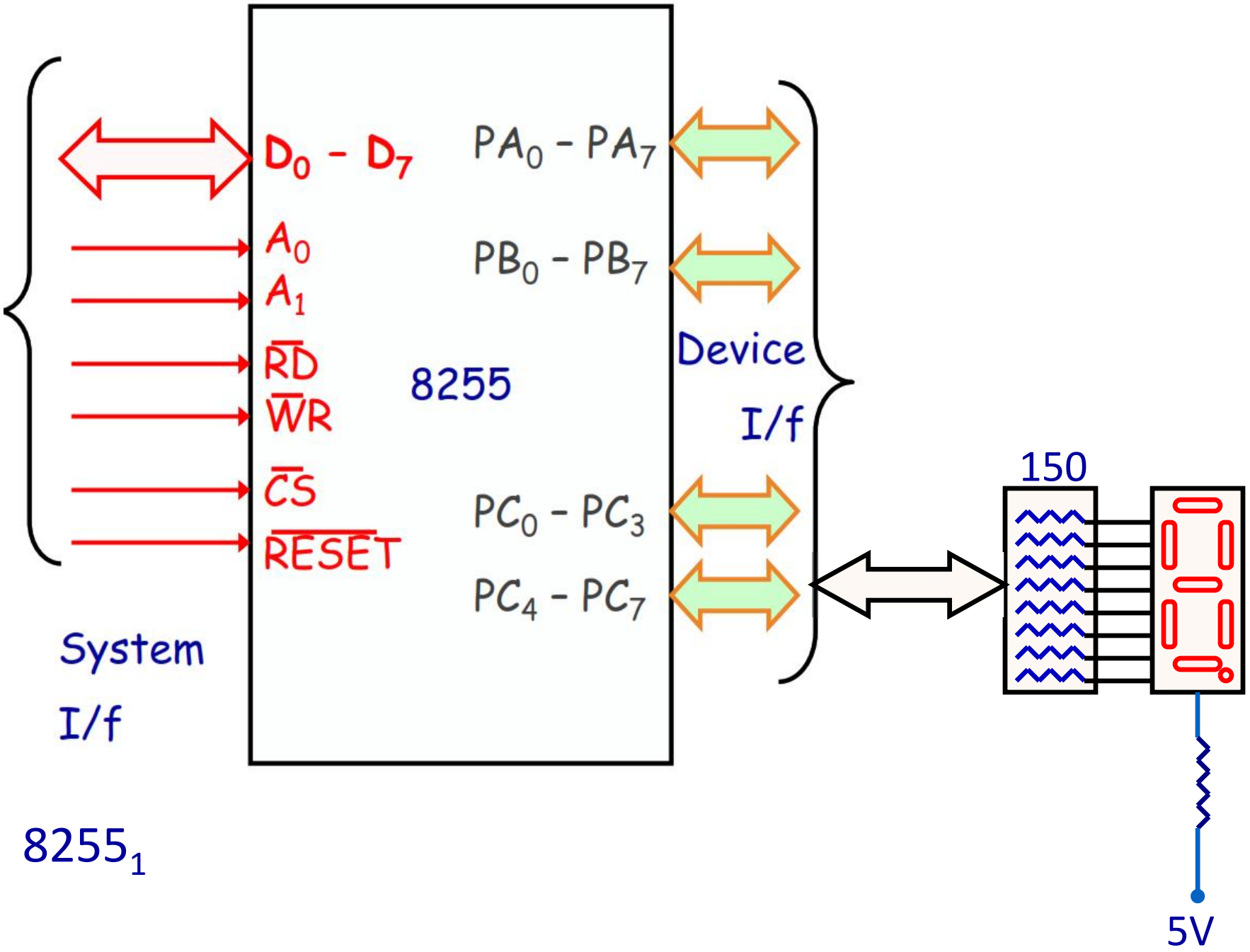
Memory Interfacing


A4
A5
A6
I2
I1
I0
O5
O6
O7
LS138
8255 1
8255 2
8255 3
GND
G2B
G2A
G1
GND
VCC

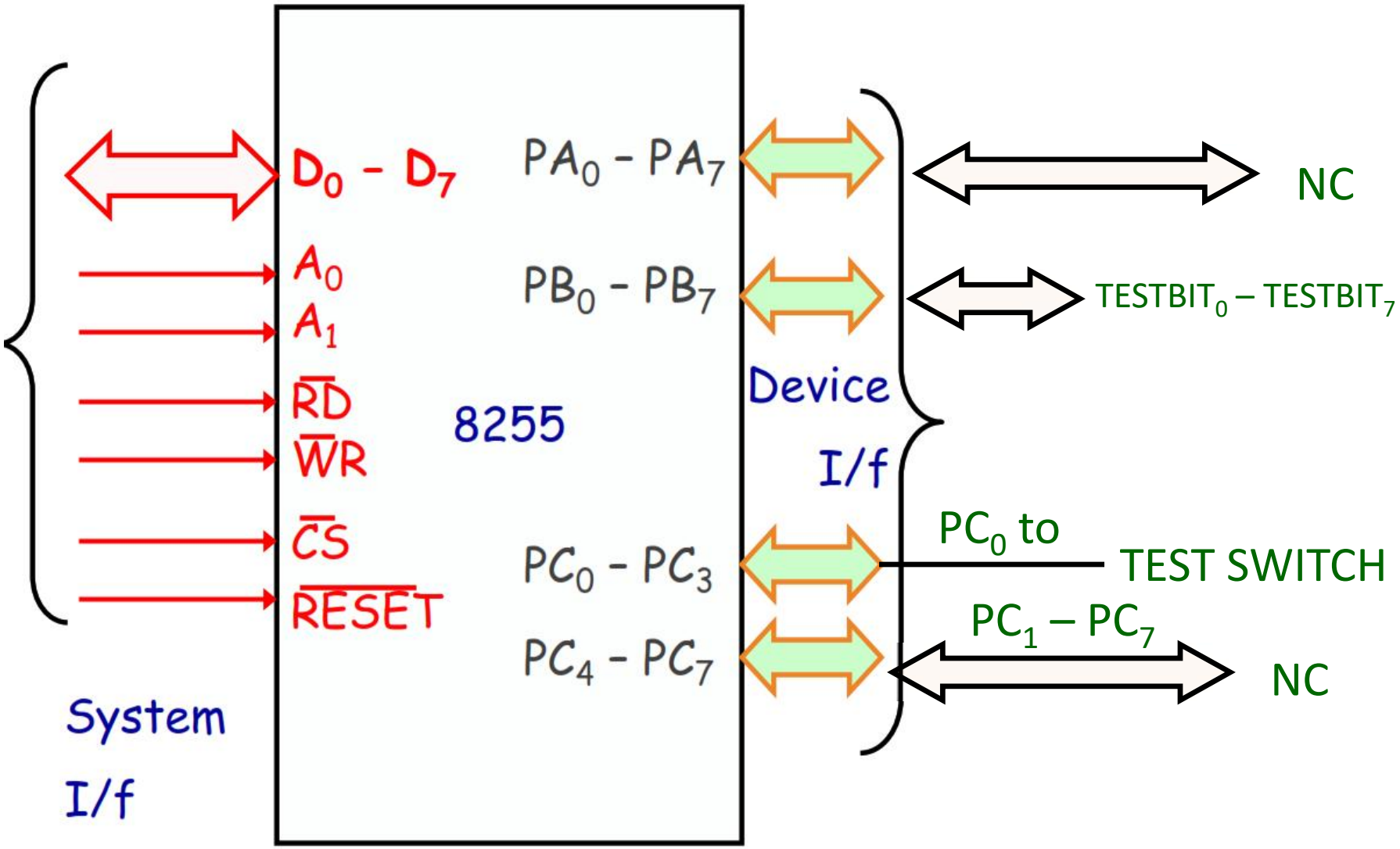
I/O Decoder

8255_1, 8255_2, 8255_3 Interface to the processor

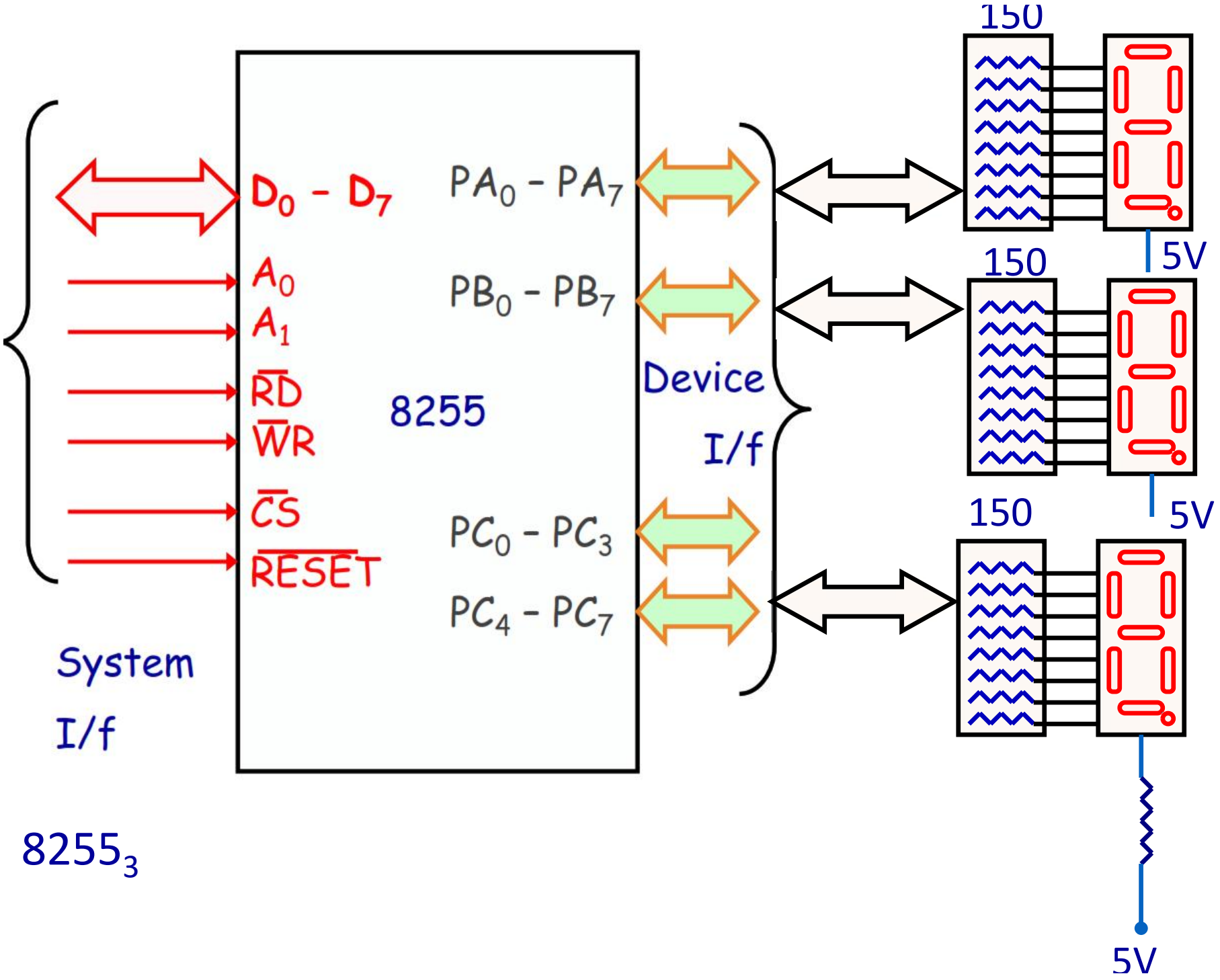



D0 - D7
A0
A1
RD
WR
CS
RESET
8255
PA0 - PA7
PB0 - PB7
PC0 - PC3
PC4 - PC7
Device
I/f
System
I/f
150
5V

8255_1


D0 - D7
A0
A1
RD
WR
CS
RESET
8255
PA0 - PA7
PB0 - PB7
PC0 - PC3
PC4 - PC7
Device
I/f
System
I/f
NC
TESTBIT0 – TESTBIT7
PC0 to
TEST SWITCH
PC1 – PC7
NC

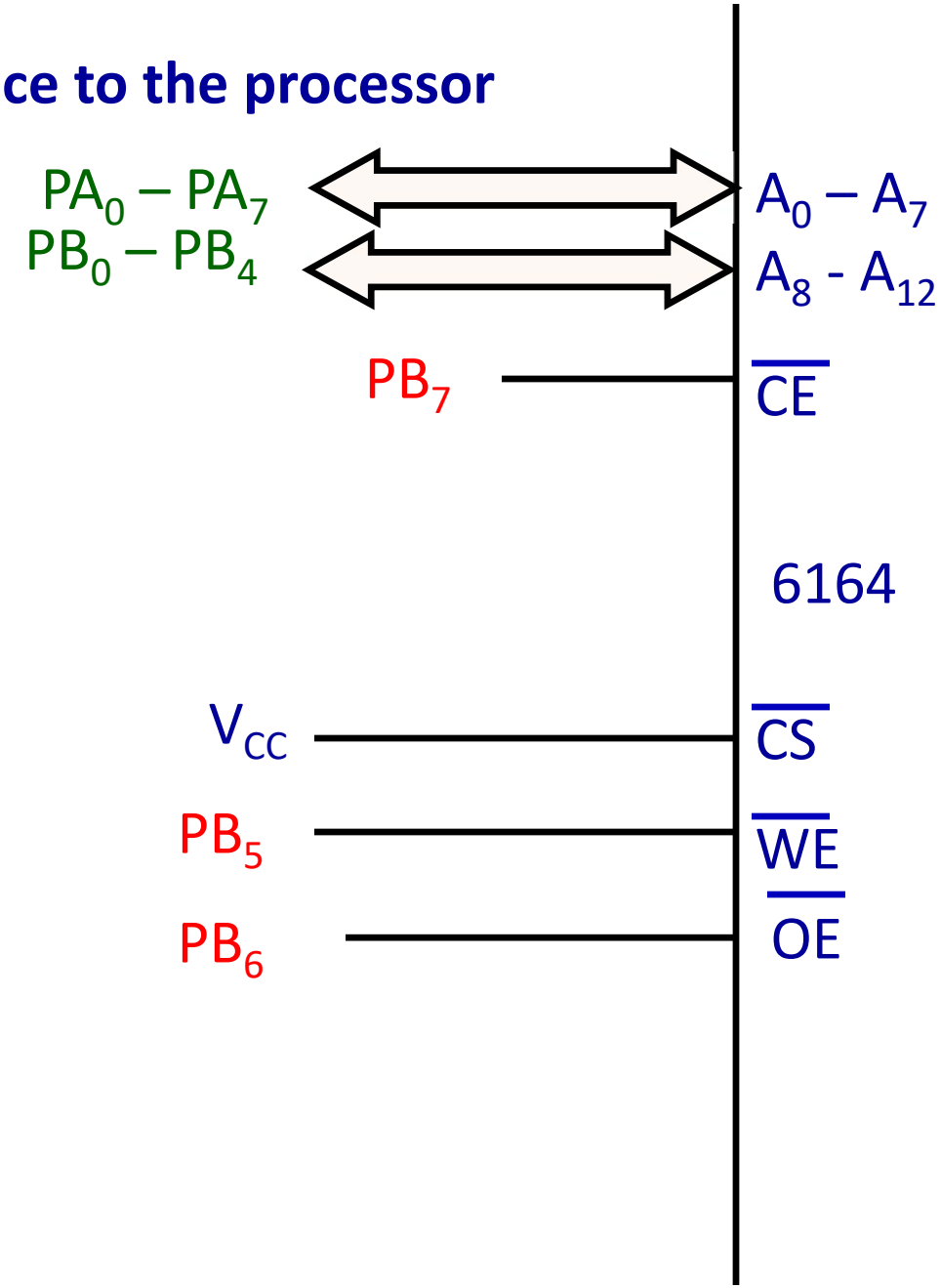
8255_2

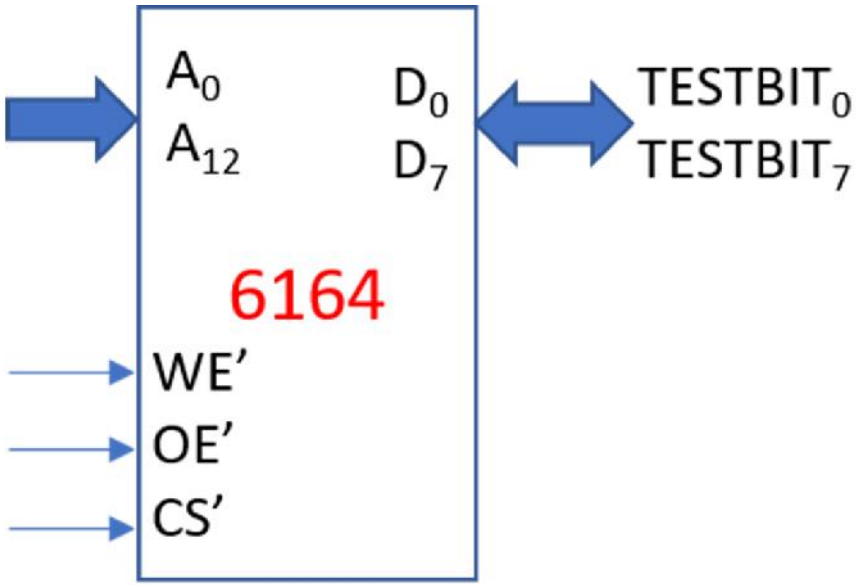

150
150
150
5V
5V
5V
D_0 - D_7
A_0
A_1
$\overline{RD}$
$\overline{WR}$
$\overline{CS}$
$\overline{RESET}$
8255
PA_0 - PA_7
PB_0 - PB_7
PC_0 - PC_3
PC_4 - PC_7
Device
I/f
System
I/f

8255_3

TEST RAM 6164 Interface to the processor

All inputs from 8255_1




A0
A12
D0
D7
TESTBIT0
TESTBIT7
6164
WE'
OE'
CS'