RAM TESTER

Submitted by: Group 70

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Contents

User Requirements & Technical Specifications

Design a microprocessor-based RAM tester.

The tester should be able to test 6164 RAM chips. The tester tests each bit of the RAM individually.

For a byte of RAM, the first bit (D0) is written as zero and read back, now a one is written into the bit and again it is read back.

If the two read operations result in bit D0 to contain a zero and one respectively then the bit is inferred as good. Any other result indicates a faulty bit.

The test is repeated for all bits of a byte and for all bytes of the RAM. The summary result, PASS/FAIL should be displayed.

User will place the 6164 chip in the zip socket, then press a switch labelled TEST.

The RAM is tested and the result is displayed on the 7-segement display as PASS/FAIL.

Assumptions & Justifications

- At the memory location FFFF0H where the processor returns on reset is provided with a JMP statement taking it to the start of the code.
- HOLD and NMI signals are grounded since no DMAC or non-maskable interrupt is used.
- INT signal is not used and hence IVT and ISR is not used. So is INTA'. Polling is used. Whenever TEST switch is pressed, testing starts.
- Ready signal is held high always. Data transfer into TEST RAM is taken care by introducing software delays.
- All addresses used are even addresses as D0-D7 data lines are used in interfacing all 8255As.

Components used with justification wherever required

- 8086
- 8284: Clock generator for 8086
- 6164 TEST RAM – 8K ram placed in the test socket to test all pins – Manual Attached
- Common Anode Seven Segment Display – 4 Nos. As PASS/FAIL are to be displayed
- 8255 – 3 nos. used for I/O interfacing
- 2716 – 4 nos. Smallest ROM chip available is 2K and as we need to have even and odd bank and ROM is required at reset address which is at $FFFF0_H$ and 00000_H - where there is the IVT
- 6116 – 2 nos. Smallest RAM chip available is 2 K and we need odd and even bank. We need RAM for stack and temporary storage of data
- LS 138 – 2 decoders
- LS 373, LS 245 and required gates
- SPDT Momentary switches – 2 used for RESET and TEST

Address Map

Memory Map

ROM1 – 00000_H – $00FFF_H$

RAM 1– 01000_H – $01FFF_H$

ROM2 – $FF000_H$ – $FFFFF_H$

I/O Map

8255_1 – 50 – 56_H

8255_H – 60 – 66_H

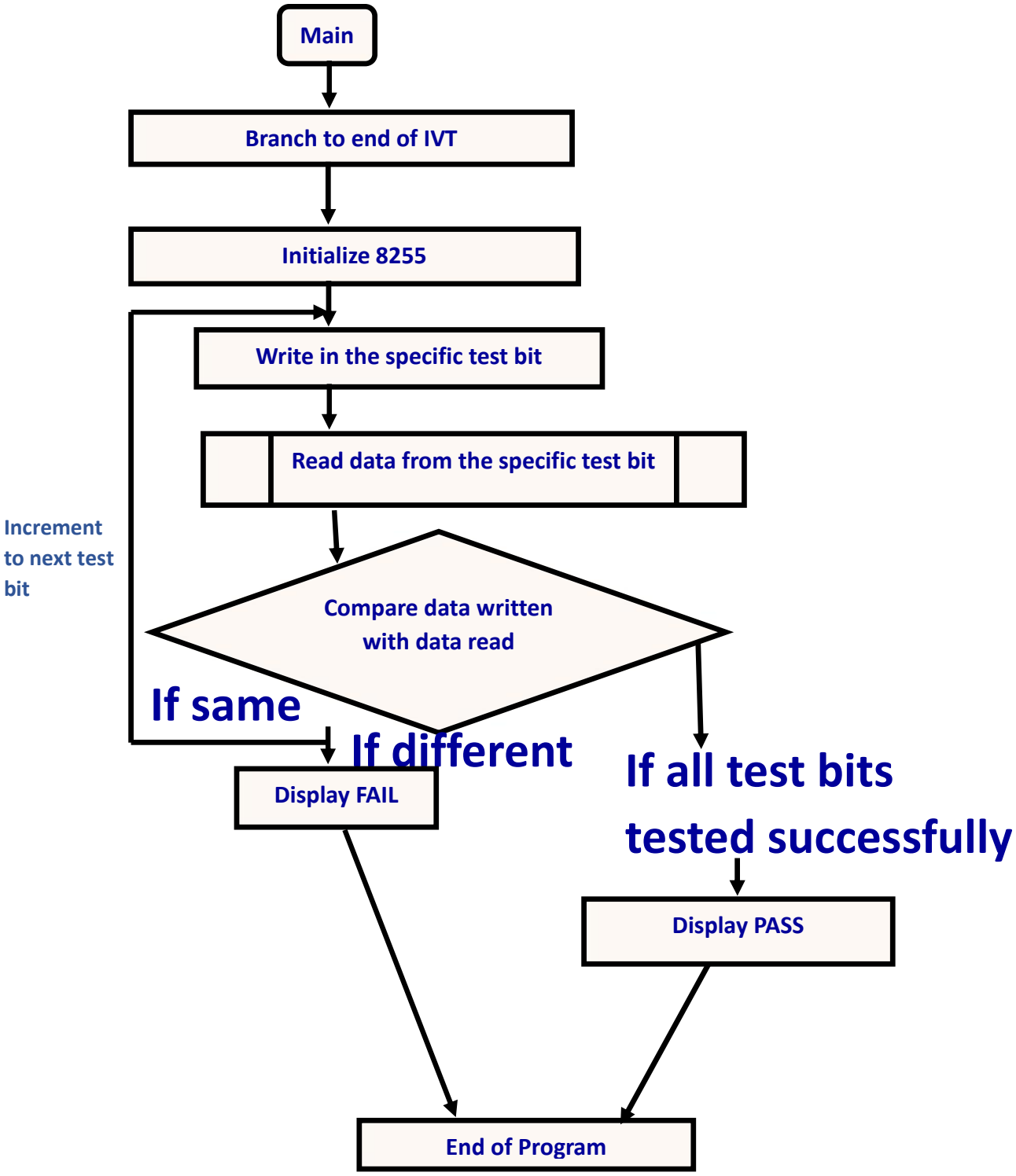
8255_H – 70 – 76_H

Design

Complete design shown with proper labelling (design attached)

Flow Chart

Main Program



Variations in Proteus Implementation with Justification

1. 6264 RAM used instead of 6164 as specified in question due to module loading issues in proteus
2. ROM in only 00000 – as proteus allows to change reset address.

Firmware

Implemented using emu8086 attached.

List of Attachments

1. Complete Hardware Real World Design – ram_tester_design.pdf
2. Manuals
    a. 6164 RAM
3. Proteus File – FinalSubmission.dsn
4. EMU8086 ASM File – ram_tester_code.asm
5. Binary File after assembly – test2.bin