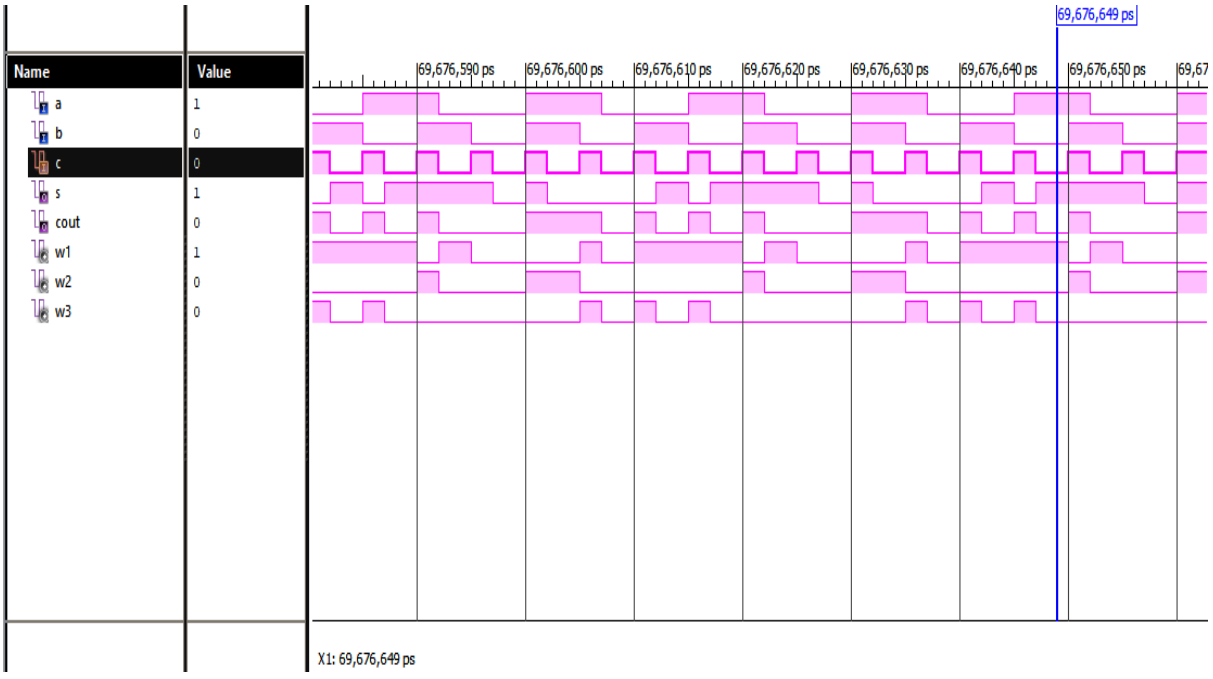
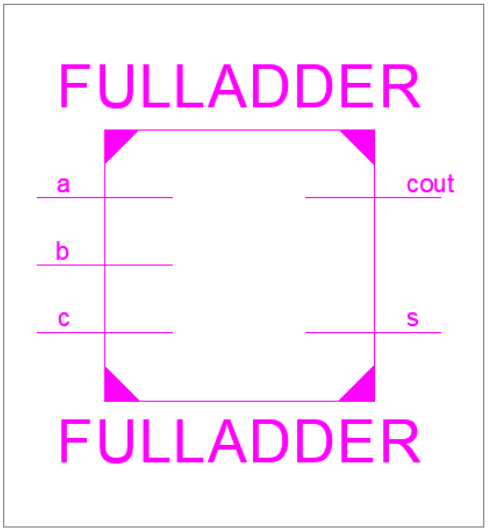
VERILOG CODE FOR FULL ADDER

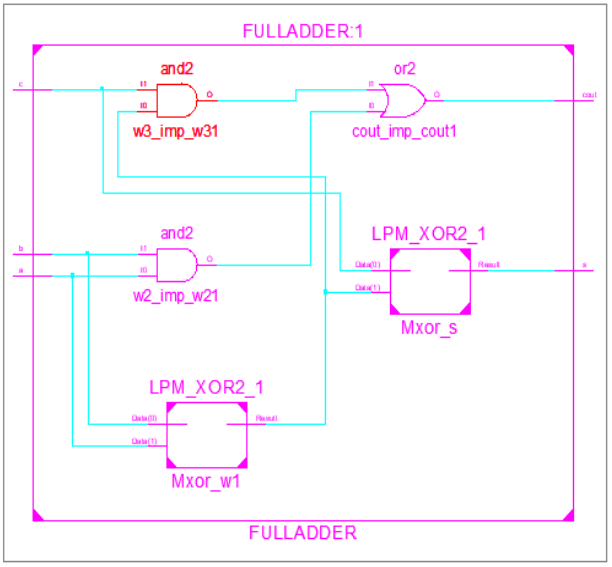
```
//Full adder using structural modeling
module full_adder_s (
    input a,b,cin,
    output sum,carry
);
wire w1,w2,w3,w4;          //Internal connections
xor(w1,a,b);
xor(sum,w1,cin);           //Sum output
and(w2,a,b);
and(w3,b,cin);
and(w4,cin,a);
or(carry,w2,w3,w4);        //carry output

endmodule
```

OUTPUT WAVEFORM:

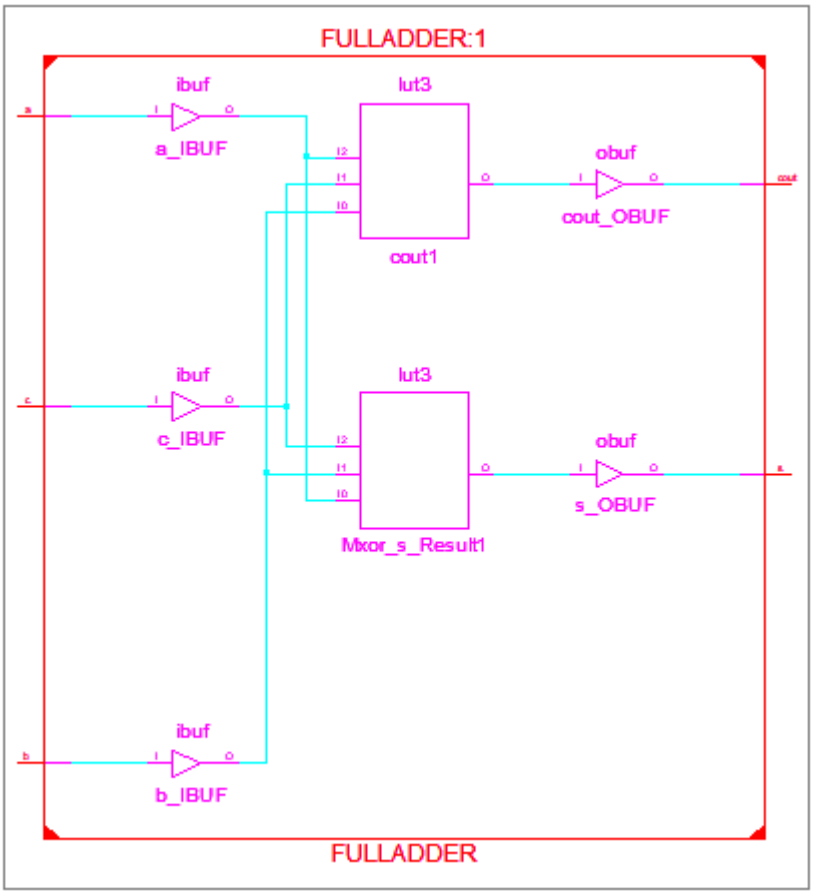


Rtl schematic view:





Technology schematic view:



Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	1	2448	0%
Number of 4 input LUTs	2	4896	0%
Number of bonded IOBs	5	172	2%

Timing Summary:

Speed Grade: -4

Minimum period: No path found

Minimum input arrival time before clock: No path found

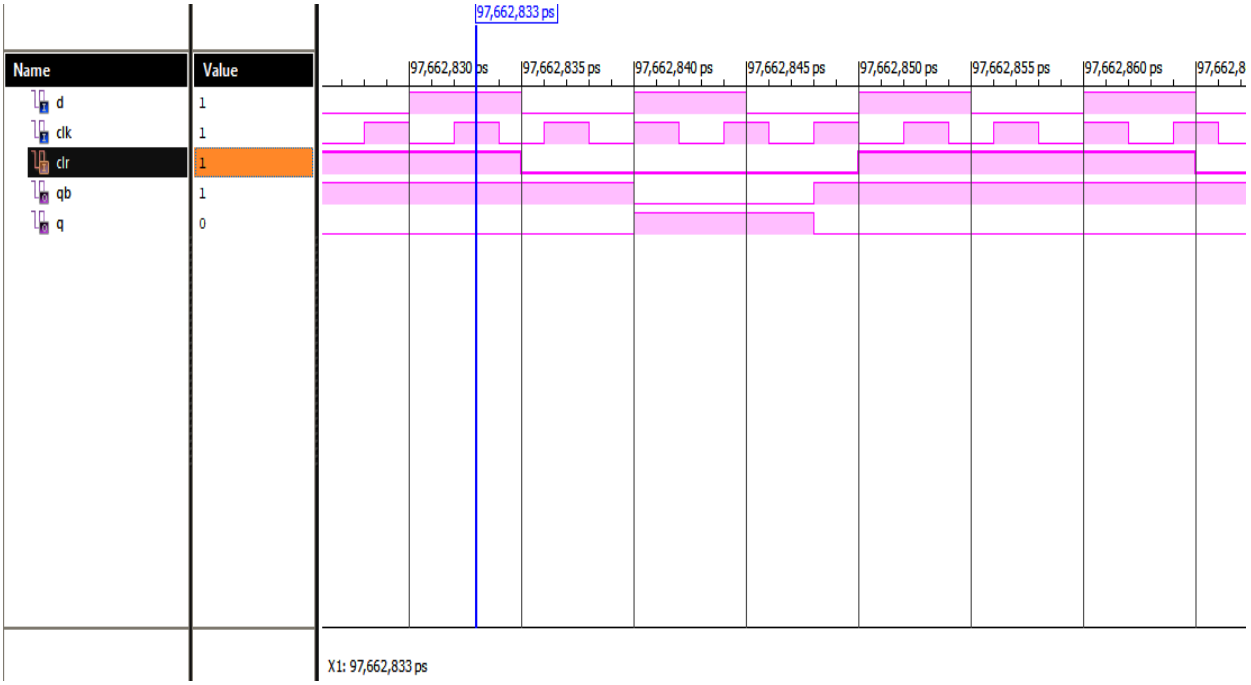
Maximum output required time after clock: No path found

Maximum combinational path delay: 6.236ns

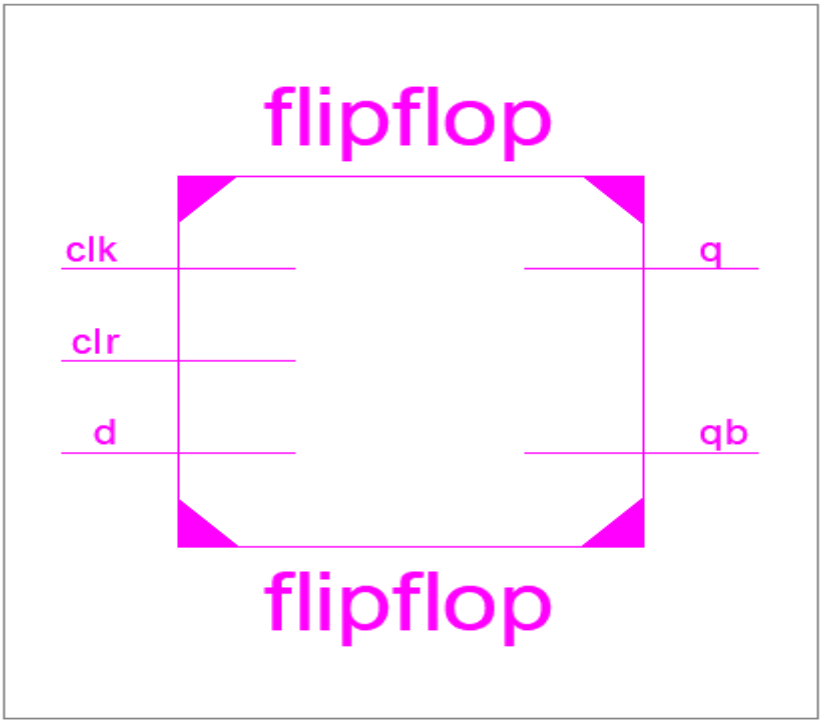
VERILOG CODE FOR D-FLIP FLOP

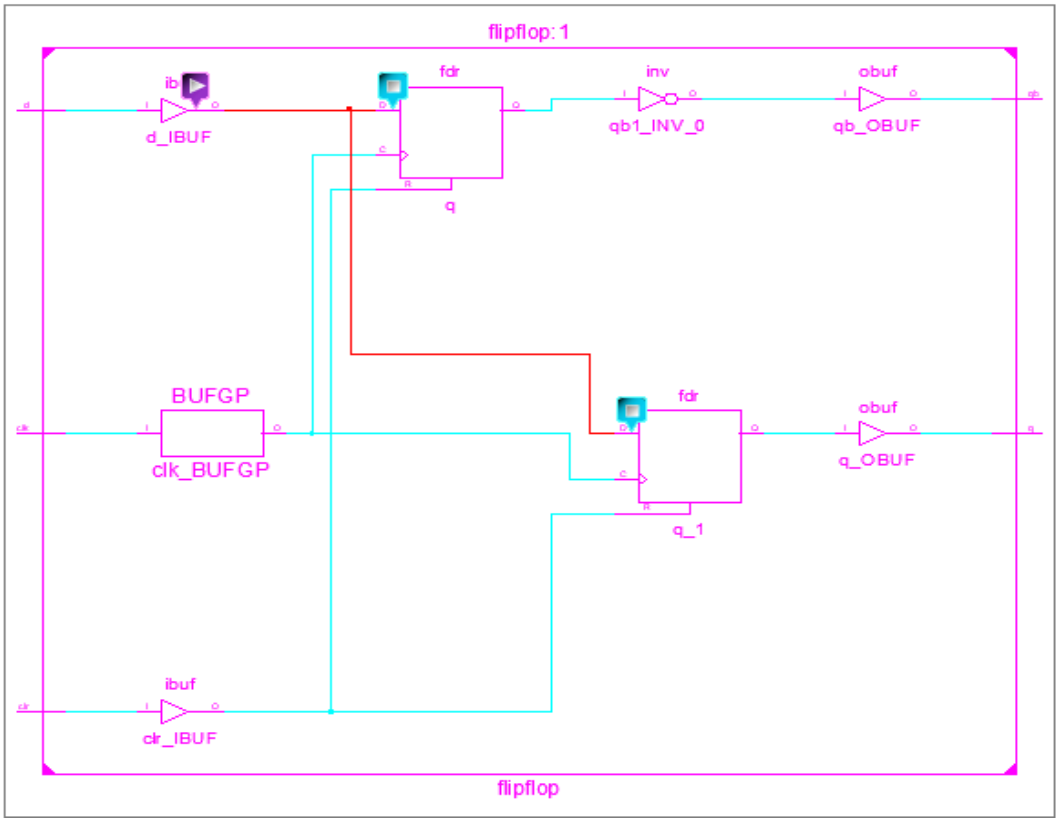
```
module flipflop(d,clk,clr,q,qb);

input d,clk,clr;

output reg q;

output qb;

assign qb=~q;

always@(posedge clk)

begin

if(clr==1)

q=0;

else

q=d;

end

endmodule
```

OUTPUT WAVEFORM:

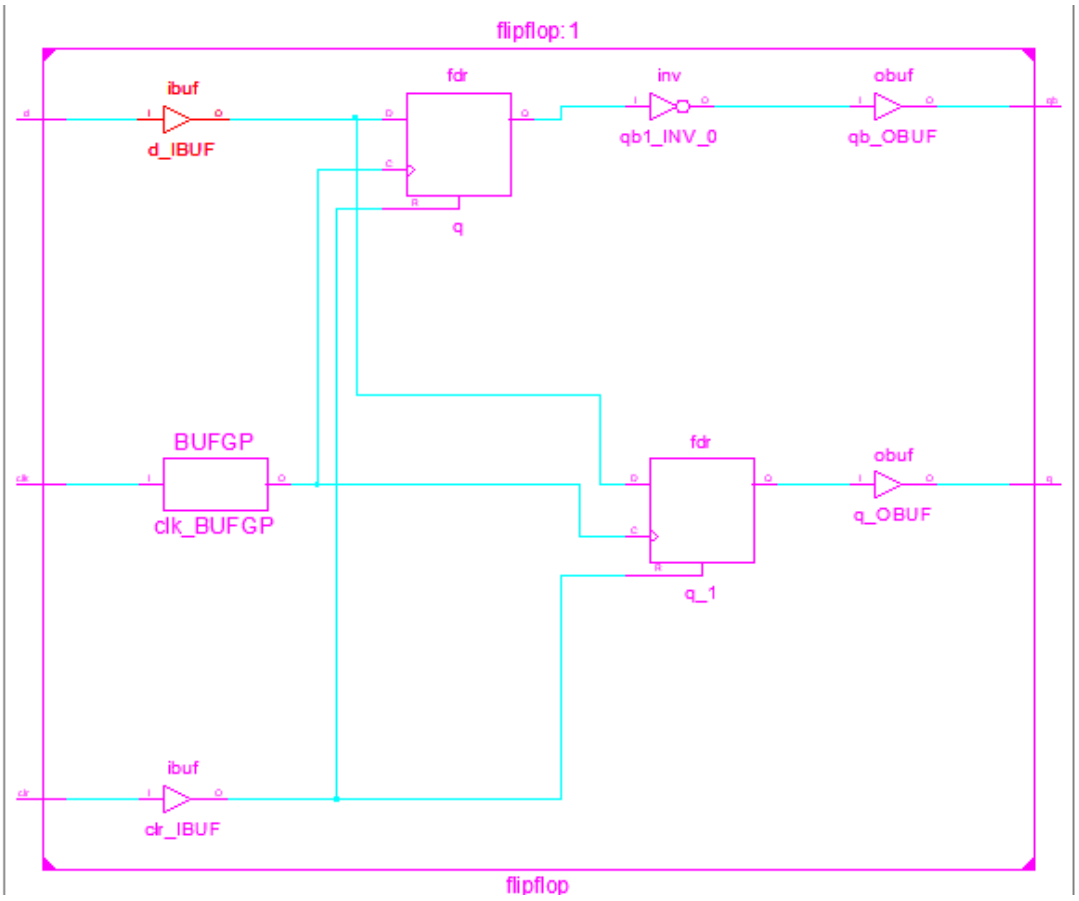


Rtl schematic view:





Technology schematic view:



Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	1	2448	0%
Number of 4 input LUTs	1	4896	0%
Number of bonded IOBs	5	172	2%
Number of GCLKs	1	24	4%

Timing Summary:

Speed Grade: -4

Minimum period: No path found

Minimum input arrival time before clock: 2.576ns

Maximum output required time after clock: 5.407ns

Maximum combinational path delay: No path found