# North Carolina State University

# Fall 2016 Semester

# CSC/ECE 506: Architecture of Parallel Computers

# Program 2

# Report

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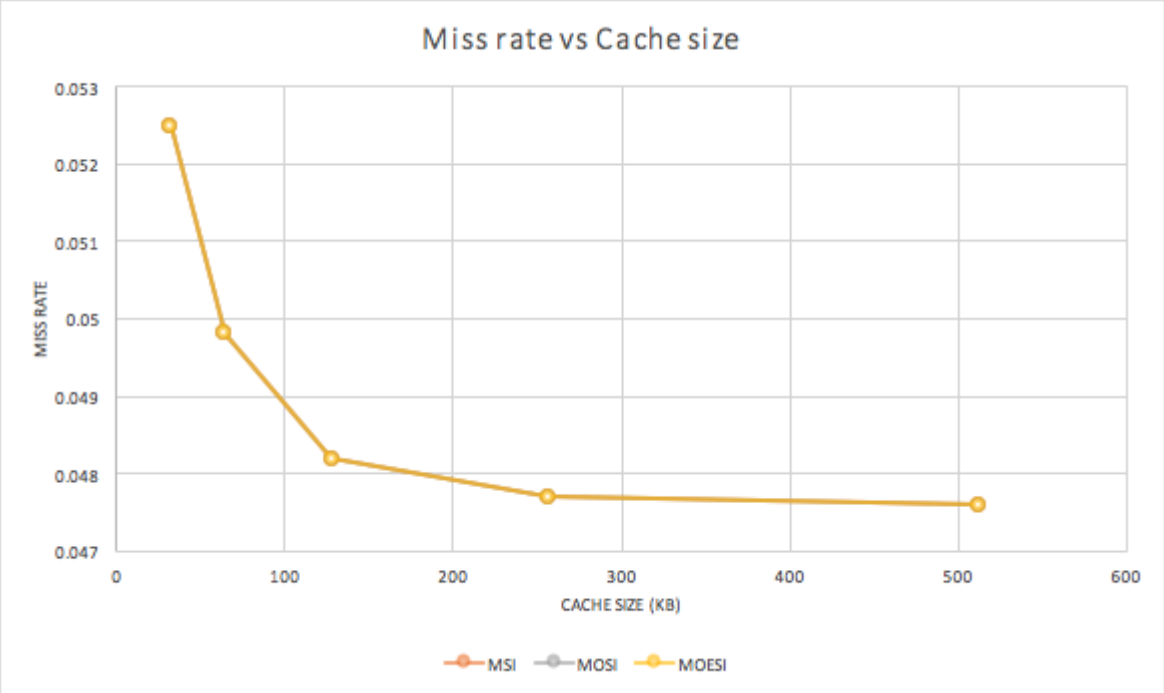
1. Cache performance (using Long trace). Analysis: Discuss the various aspects of the coherence protocols- number of memory transactions, complexity of the protocols and how the performance is impacted. As you vary the configuration, discuss the trends within a system and across protocol.

a. Plot a graph showing the trend for miss rate vs cache size (assoc and block size constant) for each protocol.

**Miss Rate vs Cache Size, with block size of 64 kB and associativity of 8**

| Cache Size (kB) | MSI | MOSI | MOESI |
|---|---|---|---|
| **32** | 0.052489 | 0.052489 | 0.052489 |
| **64** | 0.049812 | 0.049812 | 0.049812 |
| **128** | 0.048197 | 0.048197 | 0.048197 |
| **256** | 0.047707 | 0.047707 | 0.047707 |
| **512** | 0.047601 | 0.047601 | 0.047601 |

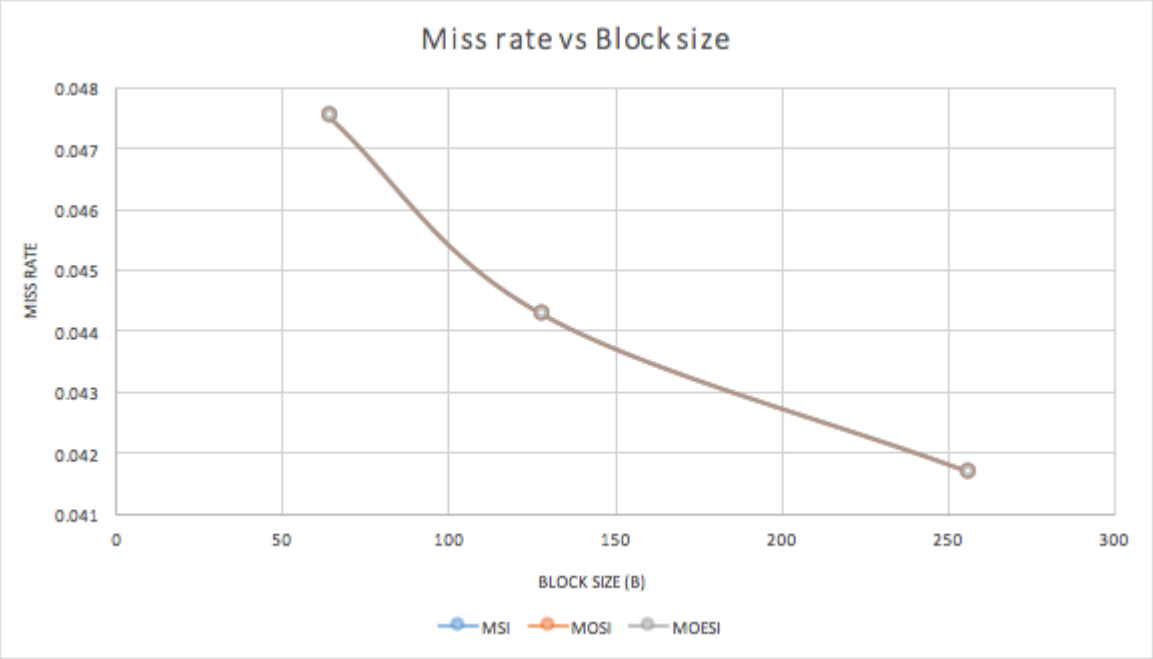



Very much predictably, miss rates decrease with increase in cache size due to reduced capacity misses. Saturation of the decreasing trend is due to cold misses. The interesting thing to note here is that the miss rates are same across protocols since they do not affect the cache accesses by trace files used.

b. Plot a graph showing the trend for miss rate vs cache block size (assoc and cache size constant) for each protocol.

**Miss Rate vs Block Size, with cache size of 1 MB and associativity of 8**

| Block Size (B) | MSI | MOSI | MOESI |
|---|---|---|---|
| **64** | 0.047511 | 0.047511 | 0.047511 |
| **128** | 0.044279 | 0.044279 | 0.044279 |
| **256** | 0.041701 | 0.041701 | 0.041701 |

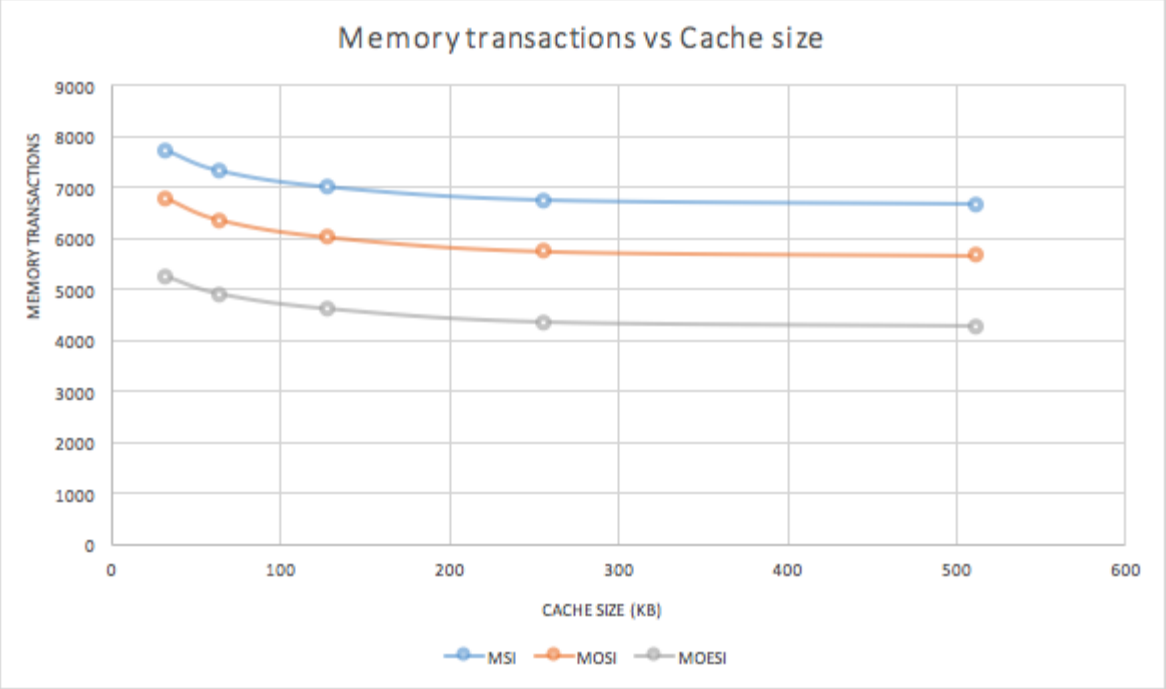



Same as before, we observe same miss rates for all protocols and a decreasing trend as block size increases. This is because cold misses go down due to bringing in more blocks at a time. Increasing this beyond a point could have lead to cache pollution, due to bringing in a lot of unwanted blocks each time and evicting useful ones. This probably doesn't reflect here due to the high cache size we have used.

c. Plot a graph showing the trend for number of memory transactions vs cache size (assoc and block size constant) for each protocol.

**Memory Transactions vs Cache Size, with block size of 64 kB and associativity of 8**

| Cache Size (kB) | MSI | MOSI | MOESI |
|---|---|---|---|
| **32** | 7726 | 6783 | 5259 |
| **64** | 7318 | 6362 | 4912 |
| **128** | 6999 | 6032 | 4619 |
| **256** | 6740 | 5759 | 4358 |
| **512** | 6662 | 5677 | 4280 |

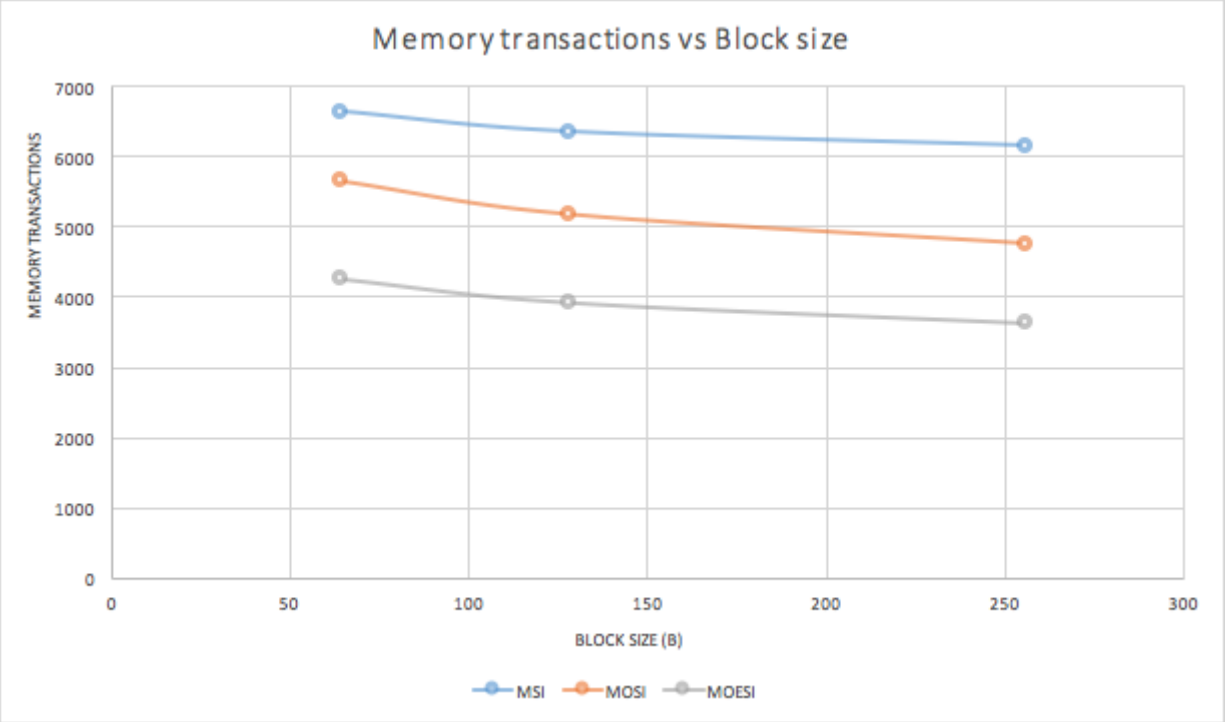



Memory transactions go down with increasing cache size according to expectations. There will be less evictions and requests in a larger cache. Number of memory transactions in decreasing order is MSI, MOSI, MOESI. This is because of the difference in the frequency of memory writebacks. MSI requires most frequent write-backs since it has fewest states, so that any changes to those states require writebacks. MOESI has the most states in its FSM which means the logic for determining the next state of the FSM, that includes determining when to evict a block in owner state or to make a write back or to make another processor as the owner is all very complicated. There is medium complexity for MOSI. This plays a direct role in performance counters as we can see in the graph above, with less memory transactions for the more complex protocols.

d. Plot a graph showing the trend for number of memory transactions vs cache block size (assoc and cache size constant) for each protocol.

**Memory Transactions vs Block Size, with cache size of 1 MB and associativity of 8**

| Block Size (B) | MSI | MOSI | MOESI |
|---|---|---|---|
| **64** | 6636 | 5649 | 4254 |
| **128** | 6347 | 5173 | 3924 |
| **256** | 6147 | 4753 | 3635 |




Memory transactions go down with increasing block size according to expectations. There will be requests since we bring in more blocks per request. Number of memory transactions in decreasing order is MSI, MOSI, MOESI. Similar to the reasons stated in graph 1c., the more complicated protocols directly result in lesser memory transactions.

2. Bus Transactions: Out of the listed Metrics, only report numbers from 17 (cache to cache transfers) to 23 (busUpgrs). Use only Long trace. Analysis: Discuss the trend about bus traffic. For various configurations, discuss the trend across protocols. Report these metrics for the experiments you do for generating the graphs, no other additional experiments are needed.

| Protocol | Cache-to-Cache Transfers | Inter-ventions | Invalid-ations | Flushes | BusRds | BusRdxs | Bus-Upgrs |
|---|---|---|---|---|---|---|---|
| **Cache Size : 32 KB, Block Size : 64 B** | | | | | | | |
| **MSI** | 0 | 0 | 2034 | 87 | 6391 | 700 | 0 |
| **MOSI** | 197 | 42 | 2034 | 169 | 6391 | 41 | 659 |
| **MOESI** | 1721 | 42 | 2034 | 169 | 6391 | 41 | 650 |
| **Cache Size : 64 KB, Block Size : 64 B** | | | | | | | |
| **MSI** | 0 | 0 | 2034 | 89 | 6063 | 700 | 0 |
| **MOSI** | 208 | 44 | 2034 | 175 | 6063 | 41 | 659 |
| **MOESI** | 1658 | 44 | 2034 | 175 | 6063 | 41 | 650 |
| **Cache Size : 128 KB, Block Size : 64 B** | | | | | | | |
| **MSI** | 0 | 0 | 2034 | 91 | 5865 | 700 | 0 |
| **MOSI** | 217 | 46 | 2034 | 181 | 5865 | 41 | 659 |
| **MOESI** | 1630 | 46 | 2034 | 181 | 5865 | 41 | 650 |
| **Cache Size : 256 KB, Block Size : 64 B** | | | | | | | |
| **MSI** | 0 | 0 | 2034 | 92 | 5805 | 700 | 0 |
| **MOSI** | 230 | 47 | 2034 | 184 | 5805 | 41 | 659 |
| **MOESI** | 1631 | 47 | 2034 | 184 | 5805 | 41 | 650 |
| **Cache Size : 512 KB, Block Size : 64 B** | | | | | | | |
| **MSI** | 0 | 0 | 2034 | 92 | 5792 | 700 | 0 |
| **MOSI** | 234 | 47 | 2034 | 184 | 5792 | 41 | 659 |
| **MOESI** | 1631 | 47 | 2034 | 184 | 5792 | 41 | 650 |
| **Cache Size : 1 MB, Block Size : 64 B** | | | | | | | |
| **MSI** | 0 | 0 | 2034 | 93 | 5781 | 700 | 0 |
| **MOSI** | 235 | 48 | 2034 | 187 | 5781 | 41 | 659 |
| **MOESI** | 1630 | 48 | 2034 | 187 | 5781 | 41 | 650 |
| **Cache Size : 1 MB, Block Size : 128 B** | | | | | | | |
| **MSI** | 0 | 0 | 2089 | 129 | 5386 | 711 | 0 |
| **MOSI** | 374 | 84 | 2089 | 293 | 5386 | 40 | 671 |
| **MOESI** | 1623 | 84 | 2089 | 293 | 5386 | 40 | 663 |
| **Cache Size : 1 MB, Block Size : 256 B** | | | | | | | |
| **MSI** | 0 | 0 | 2157 | 178 | 5070 | 735 | 0 |
| **MOSI** | 521 | 133 | 2157 | 436 | 5070 | 40 | 695 |
| **MOESI** | 1639 | 133 | 2157 | 436 | 5070 | 40 | 687 |

MSI protocol has no cache-to-cache transfers, Interventions and BusUpgrs. Invalidations do not change with protocol and cache size, as long as block size is the same. BusRds do not change with protocol either. MOSI and MOESI protocols have the same number of interventions, flushes, and BusRdxs. BusRdxs however, is really high for MSI since there are no bus upgrade requests for MSI. The trend is reversed in case of flushes since a lot of writebacks mean that data is fresh from the memory and requires very less flushes. MOESI has a higher number of cache-to-cache transfer compared to MOSI as cache blocks in 'E' state can also do such transfers.

With an increase in cache size with a fixed block size, in case of MSI protocol, the number of bus reads decreases due to more blocks in the cache, and the number of flushes increases, again due to all the blocks in the cache. For MOSI and MOESI protocol, similarly, bus reads decrease whereas interventions and flushes increase due to reasons similar to MSI protocol. Cache to cache transfers increases first for MOSI before showing a declining trend, whereas it simply decreases for MOESI. The reasons for the trend is that initial increases in cache size contributes to more blocks in cache which leads to increased cache to cache transfers effect with wears out and thereafter starts declining since more size means more sets so that blocks are mapped to different sets.

With an increase in block size with a fixed cache size, in case of MSI protocol, similar to the previous paragraph, bus reads decrease while invalidations and BusRdxs increase. And for cache-to-cache transfers, similar to previous paragraph, there is an initial decreasing trend for MOSI while it continuously decreases for MOESI.