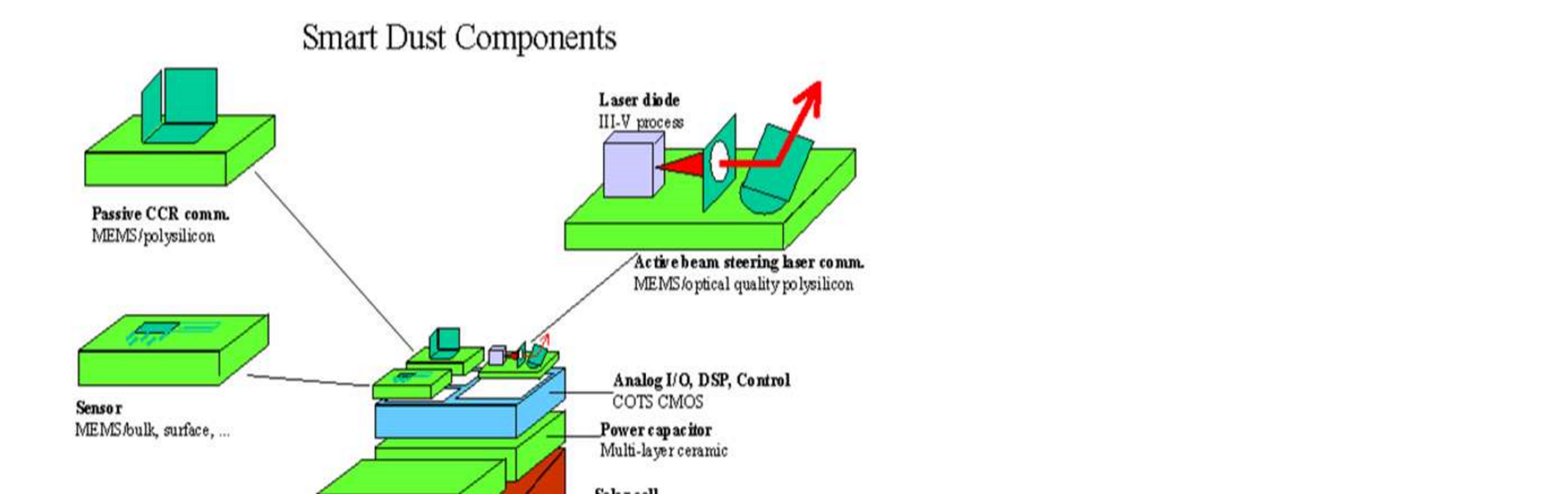
# **1.INTRODUCTION**

The goal of the Smart Dust project is to build cubic milli meter scale sensing and communication platforms (figure 1) that form a distributed sensor network and can monitor environmental conditions in both military and commercial applications. These networks will consist of hundreds to thousands of “dust motes” and a few interrogating transceivers. The dust motes are comprised of various subsystems from different fabrication technologies. Many sensors, including temperature, pressure, and acceleration sensors, from MEMS and CMOS processes can be attached to a mote. An ASIC handles measurement recording, data storage, and system control. A receiver circuit converts photocurrent from an incoming laser into a data stream to be used to interrogate or reconfigure the mote. Several transmission systems can also be utilized, such as a passive corner cube reflector (CCR) for communication to a base station, or an integrated laser with beam steering MEMS structures for inter-mote communication. Finally, all of the components are mounted onto a thick-film battery charged by a solar cell. The most difficult constraints in the Smart Dust design are those regarding the minimum energy consumption necessary to drive the circuits and MEMS devices. When fitting the entire mote within a 1mm volume, the energy density of the power supply is the primary issue. Current technology yields batteries with ~1J/mm3 of energy and a high series resistance. Modern capacitors can achieve as much as ~10mJ/mm3 with a low series resistance.

Series resistance affects the peak power that can be pulled from the source. In typical low power mixed-signal systems, most designers consider performance in terms of cycles, samples, or bits, maximizing performance first and minimizing power second. With the strict power constraints for Smart Dust, we are forced to consider performance in terms of Joules: given a cubic-milli meter battery, there is one Joule of energy to use. With the CCR, communication costs about 1nJ/bit, while sensing can be achieved at ~1nJ/sample. Modern processors, such as the Strong ARM SA1100 can perform computations as low as ~1nJ/instruction. With these energy figures, one can make cost trade-off between the amount of computation, the amount of data transmitted and the sensor sampling frequency. However, by using a closer mapping of the application needs to the architecture and targeting ultralow energy from the start, we believe we can achieve orders of magnitude reduction in the energy cost per instruction. Keeping this in mind, the goals of the project were: scenario including necessary signal processing.

* Determine the exact functional needs for a particular computation functions. In addition, the exact amount of re-configurability needed was to be determined.
* Map the necessary functionality of the core into various possible architectures.
* Evaluate the choices using Watt watcher (Verilog power estimator) and/or power mill.



# **2.CORE FUNCTIONALITY SPECIFICATION**

In order to allow us to make realistic trade-offs, a particular application scenario was chosen to guide the design. We chose the case of military base monitoring wherein on the order of a thousand.

Smart Dust motes are deployed outside a base by a micro air vehicle to monitor vehicle movement. The motes can be used to determine when vehicles were moving, what type of vehicle it was, and possibly how fast it was travelling. The motes may contain sensors for vibration, sound, light, IR, temperature, and magnetization. CCRs will be used for transmission, so communication will only be between a base station and the motes, not between motes. A typical operation for this scenario would be to acquire data, store it for a day or two, then upload the data after being interrogated with a laser. However, to really see what functionality the architecture needed to provide and how much re-configurability would be necessary, an exhaustive list of the potential activities in this scenario was made. The operations that the mote must perform can be broken down into two categories: those that provoke an immediate action and those that reconfigure the mote to affect future behaviour.

## **2.1 Immediate Operations**

* Transmit ID – provides a mote health report.
* Transmit current reading from sensor x.
* Transmit current readings from all sensors.
* Send logged data for sensor x.
* Are you logging data?
* Do you have data logged?
* Store the following value as the real time clock counter reference time.
* Turn on/off the transmission training sequence – the base station is going to move or has stopped.

**2.2 Reconfiguration Operations**

* Start logging data from sensor x with samples every t seconds.
* Stop logging data.
* Set the receiver wakeup interval to t seconds – may be from a second to a day.
* Set logging threshold.
* Set filter coefficients.
* Set FFT bin width and positions.
* Apply a FIR filter to the data stream from sensor x.
* Broadcast logged data every t seconds (Scatter cast mode) – don’t waste energy turning on the receiver.
* Take an FFT on sensor x and immediately transmit if the spectral content in band y is above z.
* Take an FFT on sensor x and store any bands that exceed the threshold.
* If sensor x exceeds z, then turn on sensor y and transmit/log its information.

From this list of operations, a list of basic activities that the various logical portions would need to do (i.e. receiver – timing recovery, data recovery, decode packet). The list of activities was then broken down into a list of specific functions that the architecture would need to support, such as selecting a sensor, move the time stamp to memory, calculate the CRC, compare a value to a threshold, etc.The comprehensive list can be found at

[http://wwwbsac.eecs.berkeley.edu/~warneke/cs252/Military\_Base\_Scen ario.html](http://wwwbsac.eecs.berkeley.edu/~warneke/cs252/Military_Base_Scen%20ario.html)

**3. THE MEMS TECHNOLOGY IN SMART DUST**

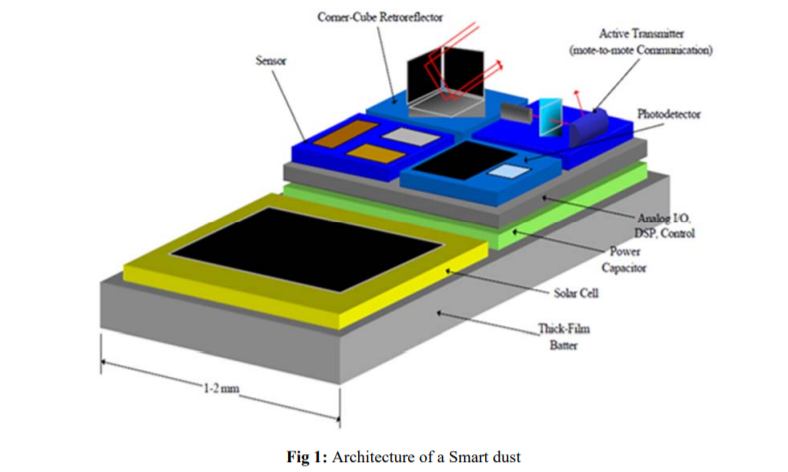
Smart dust requires mainly revolutionary advances in miniaturization, integration & energy management. Hence designers have used MEMS technology to build small sensors, optical communication components, and power supplies. Micro electro mechanical systems consists of extremely tiny mechanical elements, often integrated together with electronic circuitry. They are measured in micrometers, that is millions of a meter. They are made in a similar fashion as computer chips. The advantage of this manufacturing process is not simply that small structures can be achieved but also that thousands or even millions of system elements can be fabricated simultaneously. This allows systems to be both highly complex and extremely low-cost.

Micro-Electro-Mechanical Systems (MEMS) is the integration Of mechanical elements, sensors, actuators, and electronics on a common silicon substrate through micro fabrication technology. While the electronics are fabricated using integrated circuit (IC) process sequences (e.g., CMOS, Bipolar processes), the micromechanical components are fabricated using compatible "micromachining" processes that selectively etch away parts of the silicon wafer or add new structural layers to form the mechanical and electromechanical devices. MEMS realizes a complete System On chip technology.

Microelectronic integrated circuits can be thought of as the "brains" of a system and allow microsystems to sense and control the environment. Sensors gather information from the environment through measuring mechanical, thermal, biological, chemical, optical, and magnetic phenomena. The electronics then process the information derived from the sensors and through some decision making capability direct the actuators to respond by moving, positioning, regulating, and filtering, thereby controlling the environment for some desired purpose.

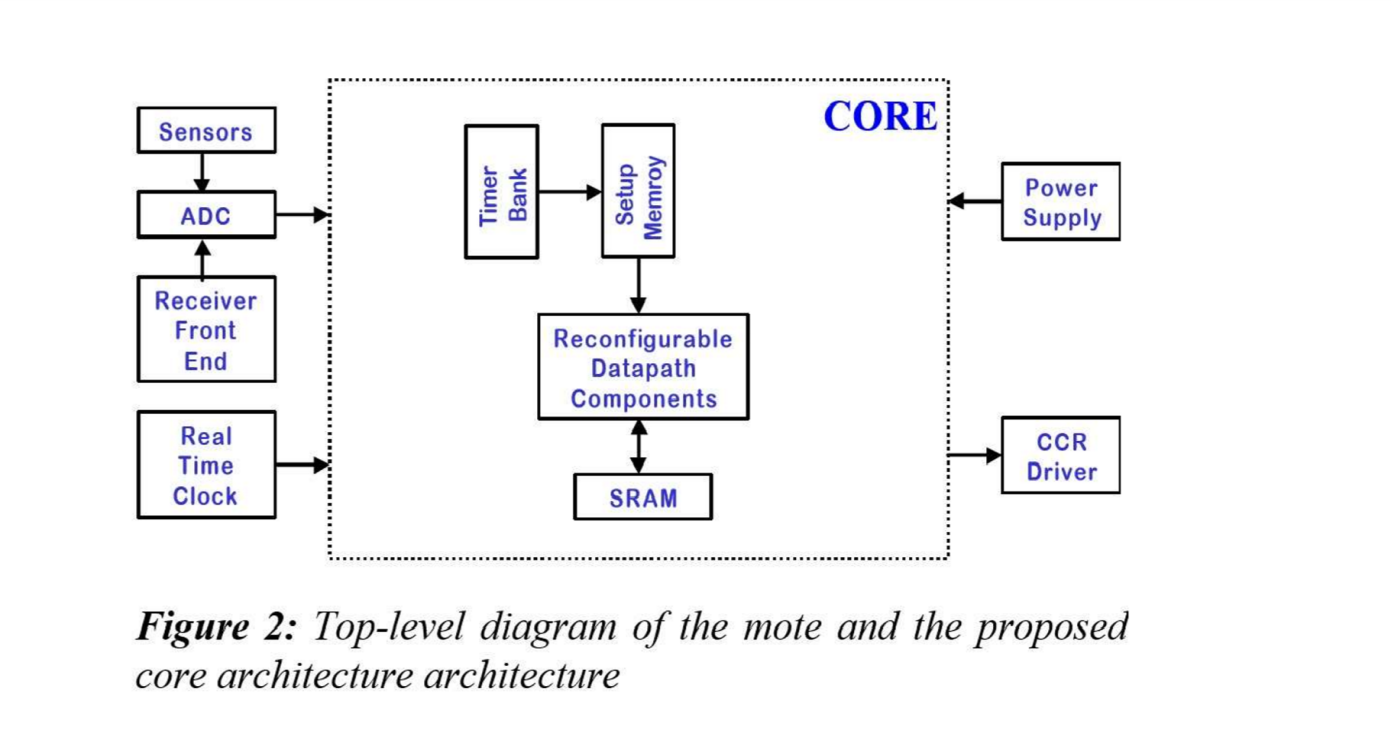
Because MEMS devices are manufactured using batch fabrication techniques similar to those used for integrated circuits, unprecedented levels of functionality, reliability, and sophistication can be placed on a small silicon chip at a relatively low cost. The deep insight of MEMS is as a new manufacturing technology, a way of making complex electromechanical systems using batch fabrication techniques similar to those used for integrated circuits, and uniting these electromechanical elements together with electronics.

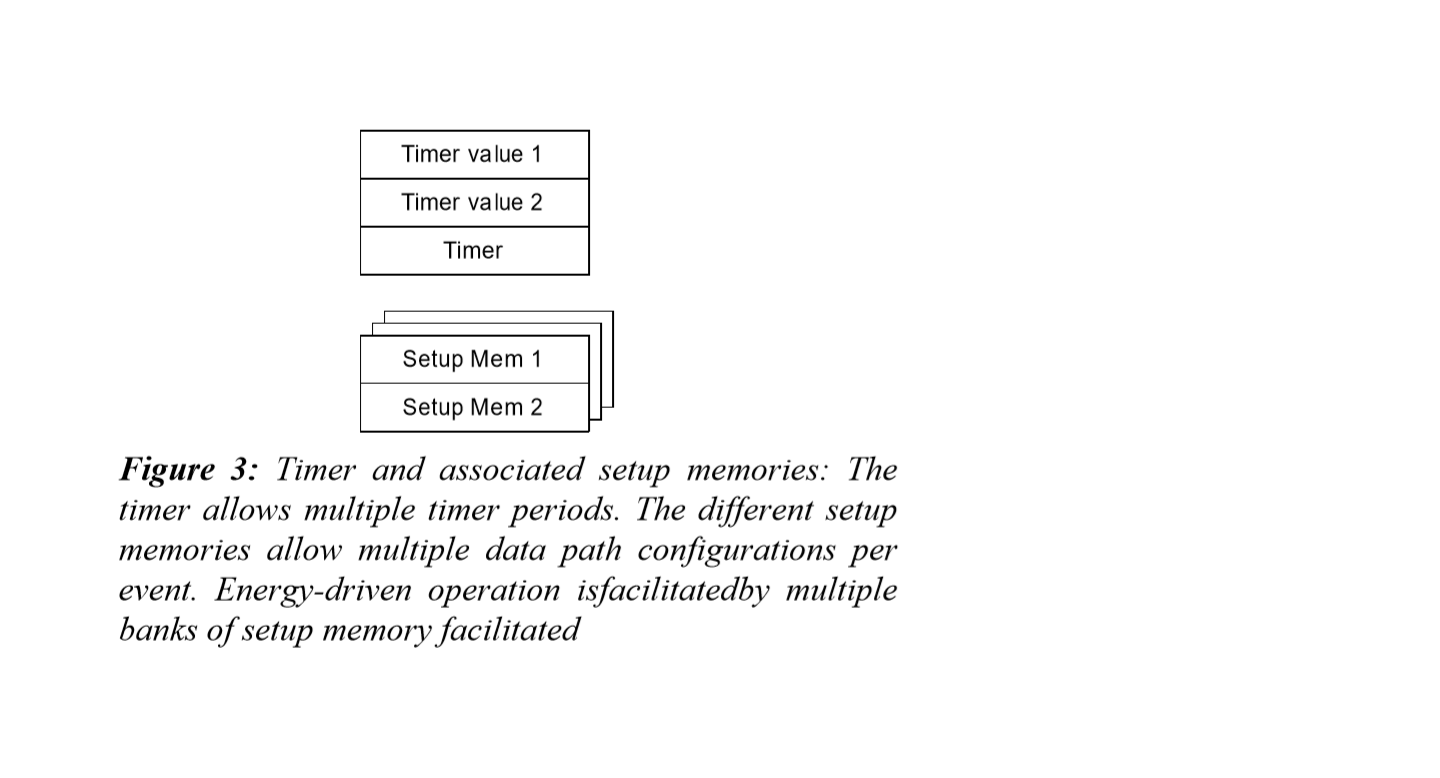
Historically, sensors and actuators are the most costly and unreliable part of a sensor-actuator-electronics system. MEMS technology allows these complex electromechanical systems to be manufactured using batch fabrication techniques, increasing the reliability of the sensors and actuators to equal that of integrated circuits. The performance of MEMS devices and systems is expected to be superior to macro scale components and systems , the price is predicted to be much lower.



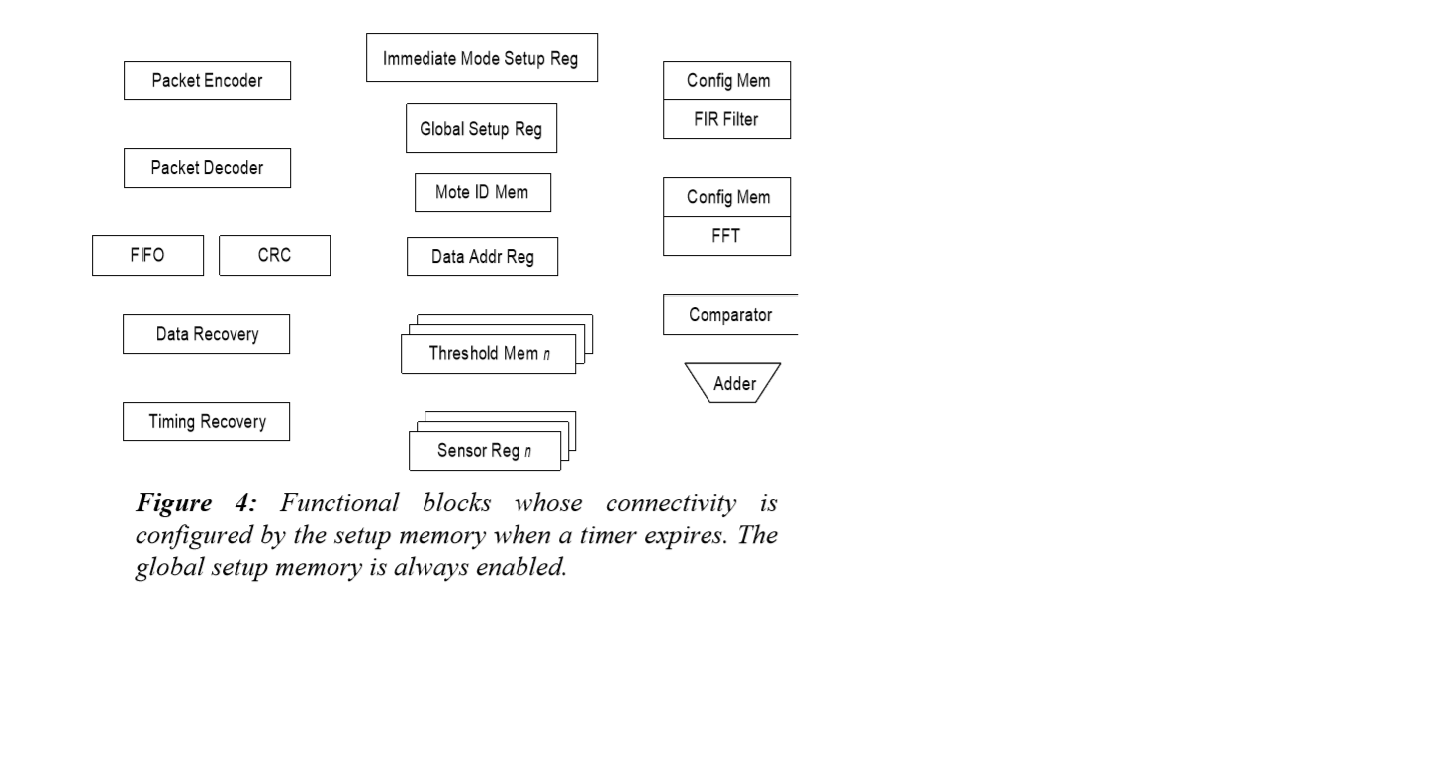
# **4. PROPOSED ARCHITECTURE**

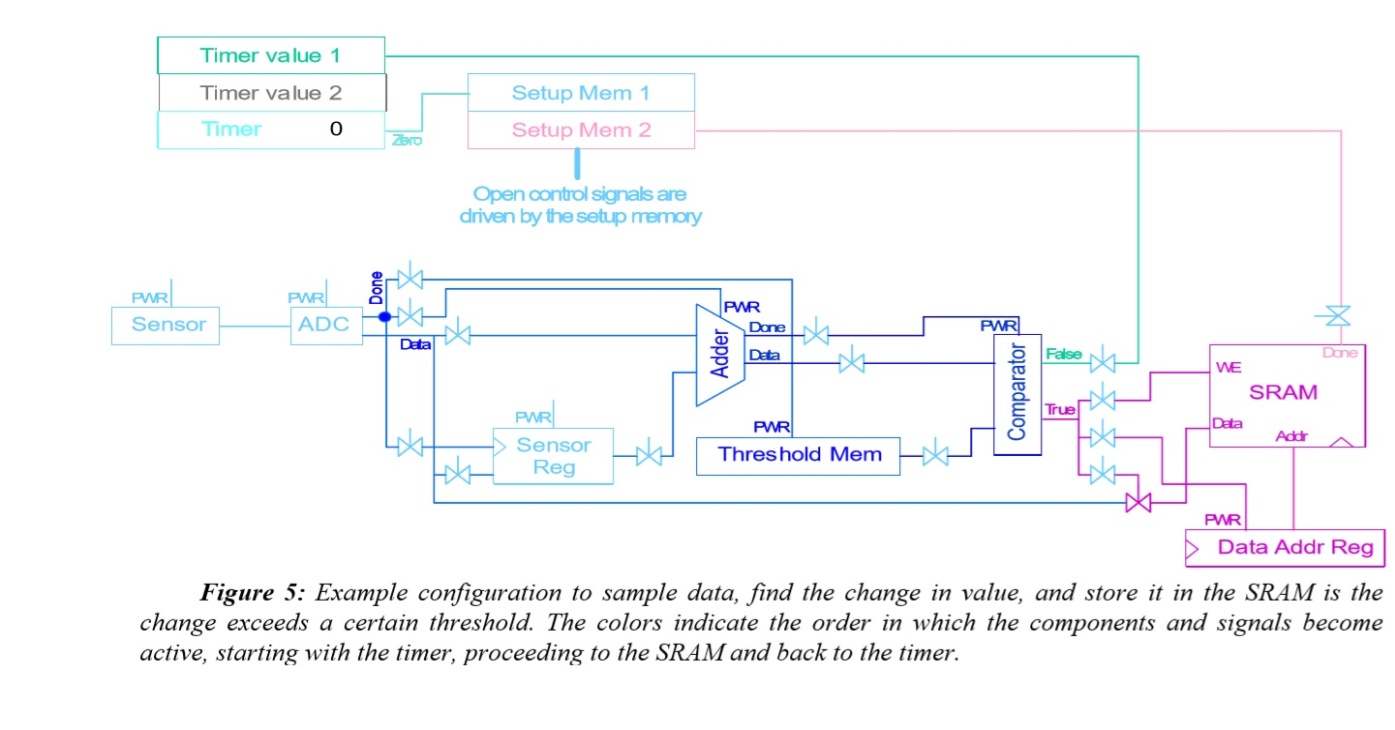
Trimming the application space of a general purpose microprocessor can achieve only so much in terms of energy savings. Instead we propose to implement an ultra-low power ASIC design with on-the-fly re-configurability of the computational blocks. Looking through the functional specifications for the core, we realized that each operation is regulated by a timed event; hence a bank of timers forms the basis of the architecture. For minimum energy, a direct mapping of a particular function into hardware is generally best, but from the list of specifications it was clear that a certain amount of re-configurability would be necessary. Thus, the timers enable setup memories that configure functional blocks into data paths that provide only the capabilities necessary for that event. These paths are data-driven so that functional blocks are only powered up when their inputs are ready, minimizing standby power and glitching. A block diagram of this new architecture is shown in figure 2. Figure 3 details a section of the timer bank and setup memory. The timer is loaded from the timer value memory, setting its period. When the timer expires, it enables setup memory 1, which configures the data path to perform the desired function.





When the data path has finished its operation, either the timer value can be loaded into the timer and the countdown restarted or setup memory 2 can be enabled. Setup memory 2 will then configure the data path for another operation, thus facilitating multiple operations per timer event. Additional setup memory can be added for more involved sequences. Multiple timer periods are desirable for several situations. For example, one might want to sample a sensor at a slow rate until an interesting signal is detected. At that point, the sampling rate should increase. In addition, the motes might be deployed without anyone coming back to talk to them for a day, so it would be desirable to be able to set the receiver wake-up timer to not wake-up for 24 hours, but then it should decrease the period dramatically to 10’s of seconds in case one doesn’t make it back to talk to the mote at exactly the right time. The proposed architecture facilitates this by providing multiple timer values that can be loaded into the timer depending on the results of the data path computation. Another feature of this architecture is energy-driven operation modes. An energy-monitoring unit selects between multiple banks of setup memory and timer values depending on the current level of the energy stores. Each bank can have different timer periods and algorithms to control energy expenditure. Two types of packets can be sent to the mote, corresponding to the two types of operations.

 Figure 4 shows the functional blocks included in the reconfigurable data path. For the communications back end, there is a data recovery block, timing recovery block, FIR filter, packet encoder that does bits stuffing and adds the flag byte, packet decoder that does bit un stuffing, CRC block, and a FIFO. Incoming packets are stored in the FIFO until the CRC can be verified, at which point the packet body will be used as described above. The global setup memory holds certain timer-independent configuration bits, such as timer enables. The sensor registers are used to store previous sensor readings to use in computing data changes. Various computation blocks can be included in the data path, such as an adder, comparator, and FFT unit. All of the functional units in the data path are data driven. The setup memory only powers up and enables the first set of units that are needed, such as the sensor and ADC. Once these units have done their job, they assert a done signal that is routed, based on the configuration memory, to the next unit, such as the adder, and powers it up and enables it. Likewise, when this unit has finished its job, it will power up and enable the next device in the chain. The last unit in the path will cause the timer to reload its value and cause the setup memory to stop configuring the data path. The advantages of this data driven technique include minimizing the standby power by keeping components powered down until exactly when they are needed, and ensuring that the inputs are stable before the next device is powered up, which minimizes glitches. It is significant to note that since this architecture does not use shared busses as in traditional microcontrollers, the functional components can be configured for certain parallel operations. For example, a sensor reading could be both stored in SRAM and transmitted with the CCR, although this is not necessarily a desirable capability. A large number of wires will be necessary to implement this architecture in order to allow configurable connectivity between so many units and to distribute all the control signals. Two potential choices for implementing the wires include point-to-point routing of control and data wires between each block and a mesh of wires with routing switches, similar to an FPGA. We focused on the former approach in this work since at this point the design seemed small enough that the point-to-point wiring would not be too onerous and the mesh would not show significant advantages.

 Figure 5 delineates the operation of the architecture by show the configuration for one of the most common tasks, acquiring sensor data, checking if it has changed more than a threshold value, then storing the result to memory. The colors indicate the order that components and signals become active, clearly showing the data driven nature. One potential hazard of this architecture is that the done signals can glitch as the blocks are powered up, which would provide a false trigger to the next stage. A second issue is that despite the fact that the blocks are powered down, the internal nodes do not discharge immediately. For example, an 8-bit comparator whose 1V VDD line is supplied by a PFET, will only discharge 13mV in 100µs with the PFET turned off. If the inputs change while powered off in this manner, a new calculation can be performed and only drop VDD by 170mV. An advantage of this is that less charge will be needed when the block is powered up again. However, this stored charge will also allow the block to continue to drive its outputs despite being powered down, so the outputs will generally need tri-state buffers. These hazards will require some extra work at the circuit level to make this architecture work. H spice simulations were used to determine the power and energy consumption of some of the blocks to test the feasibility of the proposed architecture. We used a standard cell library for the National Semiconductor 0.25µm process as the basis of the design. A 1V supply was used with a VT of 0.55V. Initially we simulated the timer since it runs continuously and thus is a significant portion of the power consumption. A 12-bit, loadable countdown timer running at 10 kHz consumes 5.4nW, or 540fJ per cycle. The same simulation in Power Mill gave 5.2nW, demonstrating comparable results to H spice while running more than 100 times faster. Next, we simulated the 8-bit comparator with a power-up/down PFET. We adjusted the rise and fall time of the power control signal between 1ns and 10µs and the W/L of the PFET from 1/0.24 to 100/0.24. The circuit was power cycled from the initial operating point to charge up the internal nodes, the comparator inputs were changed to effect a new comparison, and a second power cycle was run. The energy was computed for the second power cycle, including 1µs of on-time. The energy consumption only varied by about 10% and was approximately 95fJ. The average power consumption during the 1µs of on-time was measured to be about 2.9nW with about 30% variation. The average power consumption for the off-time with the internal nodes charged, was about 6.4pW with 3% variation. From these numbers we can determine when it is worthwhile to perform power cycling. By dividing the energy consumed in the power cycling by the static power consumed when the module is powered up, we find the maximum amount of time that the circuit can be on before it is beneficial to turn it off. In this case, we find that the comparator should be turned off if it is idle more than 33µs, or running slower than 31 kHz. Since the maximum speed that anything in the core would run at is 10 kHz, and most operations would occur at speeds on the order of 100Hz down to 0.01Hz (100sec), this power cycling scheme is very advantageous. We are currently in the process of estimating the energy consumption for the configuration shown in figure 5 using Power Mill. A corresponding subroutine on an ARM8 would consume 1.44nJ at 1V and 10 kHz[6]. The preliminary results from the H spice simulations above indicate that we should be able to achieve at least two orders of magnitude lower energy consumption with the proposed architecture. In addition, a microcontroller being designed for ultra-low energy operation and targeted at the same scenario as the proposed architecture will provide a more realistic comparison between a conventional microprocessor architecture and the proposed architecture.

**Communicating with a smart dust Communicating From a Grain of Sand**

Smart Dust’s full potential can only be attained when the sensor nodes communicate with one another or with a central base station. Wireless communication facilitates simultaneous data collection from thousands of sensors. There are several options for communicating to and from a cubic milli meter computer. Radio-frequency and optical communications each have their strengths and weaknesses.

Radio-frequency communication is well under-stood, but currently requires minimum power levels in the multiple milli swatt range due to analog mixers, filters, and oscillators. If whisker-thin antennas of centimeter length can be accepted as a part of a dust mote, then reasonably efficient antennas can be made for radio-frequency communication. While the smallest complete radios are still on the order of a few hundred cubic milli meters, there is active work in the industry to produce cubic-milli meter radios. Moreover RF techniques cannot be used because of the following disadvantages: -

* Dust motes offer very limited space for antennas, thereby demanding extremely short wavelength (high frequency transmission). Communication in this regime is not currently compatible with low power operation of the smart dust.
* Furthermore radio transceivers are relatively complex circuits making it difficult to reduce their power consumption to required microwatt levels.   
  They require modulation, band pass filtering and demodulation circuitry.
* So an attractive alternative is to employ free space optical transmission. Studies have shown that when a line of sight path is available, well defined free space optical links require significantly lower energy per bit than their RF counter paths.
* There are several reasons for power advantage of optical links.
* Optical transceivers require only simple base band analog and digital circuitry.
* No modulators, active band pass filters or demodulators are needed.

**5.ADVANTAGES AND DISADVANTAGES**

**5.1 Advantages**

**For an industry:**

* Improving safety, efficiency, and compliance.
* Reducing system and infrastructure costs.
* Increasing productivity.

**For farmers or farming purpose:**

* Detecting the needs of the crop resulting in a better fertilization management.
* It gives farmers a better management of time.
* Reduction of inputs and Increase of outputs resulting an increase in productivity.

**For  factories and plants:**

* It automates many manual error-prone tasks which involve calibration and monitoring.
* Provide accurate data of motor health in order to perform more timely maintenance when needed.
* Detection of  corrosion in aging pipes before they leak.

**For  an office environment:**

* It  eliminates  wired routers entirely and replacing them with a single Smart Dust chip which would handle all hardware and software functions for distributed networks, using five times less power than conventional networks.
* Smart Dust nodes can even be equipped with GPS receivers. Can be used to track  the movements of visitors as they roam around the office to see if they are going to any restricted locations.

**For military purpose:**

* A military application like monitoring activities in inaccessible areas, accompany soldiers and alert them to any poisons or dangerous biological substances in the air.
* Security and Tracking.
* In the military, they can perform as a remote sensor chip to track enemy movements, detect poisonous gas or radioactivity.

**5.2 Disadvantages**

**Privacy Issue**

* One of the major disadvantages of Smart Dust is the privacy issue for organizations using it. Detecting even the most subtle changes, Smart Dust leaves little to the imagination. Smart Dust are miniature sensors. They can record whatever you want them to record. Because this new technology is so small, people are scared that they would be spied on by companies.
* That brings the main disadvantage to any company who would use Smart Dust. They would have to advise everybody who is part of the study or experiment. It could also bring ethical issues. For example, which employees would you let analyze the data that the sensors are giving and what information would they have access to Privacy is likely going to be an ongoing and difficult debate in the coming years, and Smart Dust may be right at its center.

**Cost**

* Although Smart Dust is gaining popularity in many fields, it remains costly to implement such a system in an organization. The little chips themselves saw their prices go down by a lot in the recent years, however implementing all the satellites and other elements needed may cost a company a lot of money.

**6. MAJOR CHALLENGES**

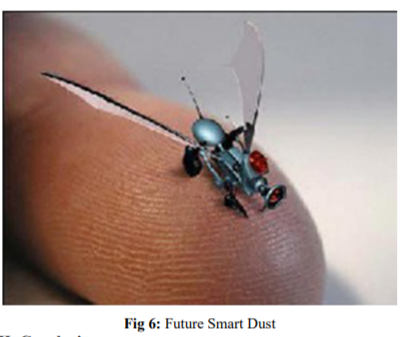
* It is difficult to fit all these devices in a small smart dust both size wise and energy wise.
* As the device are so small, batteries present a massive addition of weight .
* To incorporate all these functions while maintaining a low power consumption.
* Maximizing operating life given the limited volume of energy storage.
* The functionality can be achieved only if the total power consumption is limited to microwatt levels.
* An unbroken line of sight of path should be available for free space optical links.

**7.FUTURE ASPECTS**

Smart dust is a devise in the order of a cubic milli-meter, which contains four basic components: power, computation, sensor and communication. There are a number of research institutions that are currently working on centimeter-scale distributed sensor network. Several research groups at UCLA are developing an entire radio on a single CMOS substrate and a low power wireless MEMS.

The future of smart dust lies on both optical communication and fiber-optic communication. The MEMS is one of the main technologies that can improve both communication systems. There are several obstacles in the developing a communication system for the cubic milli meter-scale distributed sensor network. Nevertheless, it stands in the way of the future commercialization of smart dust.

To improve performances of the free-space optical and fiber-optic communication systems, it needs to achieve a high data rate. This can be achieved by improving MEMS techniques and a data rate of the imaging receiver. Power consumption is also one of the major components that play a key role in design of the smart dust. While microcontroller consumes less power, battery energy densities have not improved significantly over the years.



In the future, a custom circuit design of the microcontroller with the choice of electronics will allow to employ additional functionality. The additional functionality will make future smart dust to be able to perform more complex functions. As it has mentioned in conclusion, this design suffers from a low triggering edge comparing with the traditional design. It also has a bottleneck on computational part of the design that can considerably increase the response time. This can be a major weakness for application with a really high margin of sensitivity and/or also applications which demand a fast reply. So implementing this algorithm using another programming language can be quite interesting. Also this algorithm can be implemented using more than one programming languages and the results can be compared. This can show which language can serve Smart Dust network best in this case.

Changing the mote behaviour obviously is not the best and the most complicated solution for decreasing the power consumption in a Smart Dust network. Of course, there can be more works to be done to improve the algorithm which is suggested in this work but also looking to the network as a whole, can give more solutions to be worked on. One of the most interesting features that can make Smart Dust network adopted to, is AI or Artificial Intelligence. Earlier in this work, there is a short chapter on this subject however we couldn't work more detail in this area but it can offer really high measures for the applications that is adopted to these technologies. Based on experience and earlier studies, neural networks and fuzzy logic are two AI technologies that can be well applied to Smart Dust networks.

**8.CONCLUSION**

Smart dust is made up of thousands of sand-grain-sized sensors that can measure ambient light and temperature. The sensors each one is called a "mote" have wireless communications 47 devices attached to them, and if you put a bunch of them near each other, they'll network themselves automatically. These sensors, which would cost pennies each if mass produced, could be plastered all over office buildings and homes.

Each room in an office building might have a hundred or even a thousand light- and temperature-sensing motes, all of which would tie into a central computer that regulates energy usage in the building. Taken together, the motes would constitute a huge sensor network of smart dust, a network that would give engineers insight into how energy is used and how it can be conserved. In a dust-enabled building, computers would turn off lights and climate control in empty rooms. During peak energy usage times, air conditioners that cool servers -- which drain a lot of the tech world's power -- would be automatically shut off, and then turned on again if the servers get too hot. Thus it can very lead to world’s energy conservation solutions.

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