Class D Audio Power Amplifier - Overview

Version 1.0

XMOS

Publication Date: 2010/02/15

1 Overview

Class D power amplifiers (PA) offer excellent power efficiency when compared to other classes of PA. The output stage switches at high frequency between fully on and fully off and can be controlled by a pulse width modulation (PWM) signal.

The XS1 can readily convert audio samples to high frequency PWM to drive a class D PA directly without the need for a digital to analog converter (DAC). This keeps the audio signal in the digital domain right up until the final PA stage, and thus avoids degrading the audio through analog stages that can be bypassed. The additional bill of materials cost of a high quality DAC is also avoided.

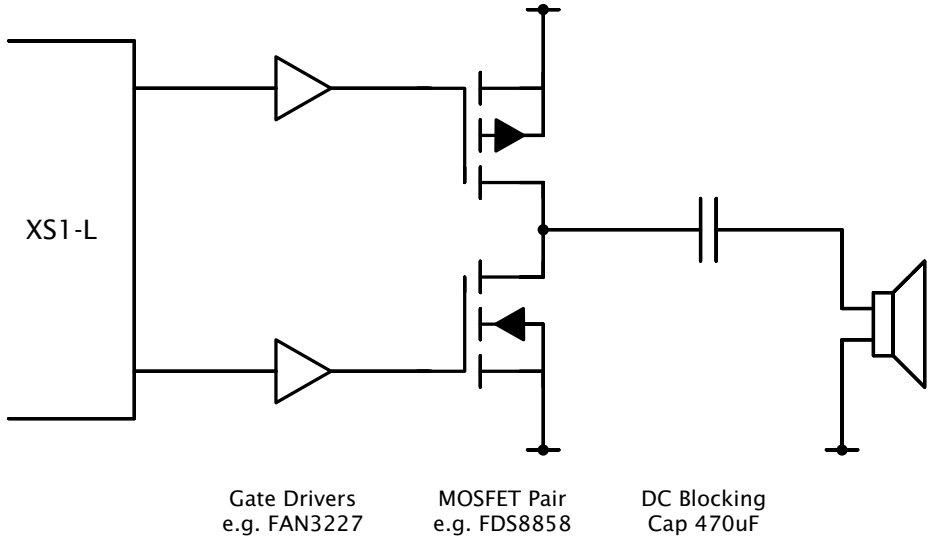

Figure 1: Example single ended class D circuit

Working backwards from the speaker, the basic stages involved in a single ended class-D PA are as follows:

1. A pair of power MOSFETs drive the speaker through a dc blocking capacitor for a single ended implementation. Expensive inductors for low pass filtering can often be avoided if the circuit is located close to the speaker.
2. The MOSFETs are driven with slightly different timing to avoid *shoot through* current when both of the MOSFETs are partially on. Two related PWM signals are therefore required from the XS1 device for each audio channel.

3. To drive the gates of the MOSFETs, the logic level PWM signals from the XS1 signals are amplified by gate drivers.
4. The XS1 PWM signals are created from audio samples at the PWM frequency (e.g. 384kHz) and driven to 1 bit ports on the XS1 device.
5. To obtain the audio samples at the PWM frequency, the audio input sample stream is interpolated to increase its frequency (e.g. from 48kHz to 384kHz).

Thread	Thread Speed	Description
Left sample interpolation	50 MIPS	Upsample and filter the left audio input samples to the PWM frequency (e.g. from 48kHz to 384kHz).
Right sample interpolation	50 MIPS	Upsample and filter the right audio input samples to the PWM frequency (e.g. from 48kHz to 384kHz).
PWM port driver	50 MIPS	Drives both PWM ports from each channel using the PWM frequency samples.

The power of the amplifier is determined by the choice of MOSFET and the available power supply rail.

Single ended (half bridge) and bridge tied load (full bridge) implementations can both be driven by the same XS1 application code.

The signal to noise ratio (SNR) of the PA depends on the external circuitry implementation, but 90dB should be easily achieved.

2 Example Bill of Materials

The table below provides an example bill of materials for a stereo implementation which provides 3W (rms) per channel. Each single ended channel drives a 4 Ohm load and exceeds a SNR of 90dB.

Manufacturer	Description	Part No	Qty	Cost($)*	Total Cost($)
Fairchild	Dual N-type and Ptype MOSFET	FDS4897C	2	0.21	0.42
Fairchild	MOSFET driver	FAN3227T	2	0.44	0.88
Panasonic	470uF DC Blocking Cap	EEU-FM1A471	2	0.08	0.16
Panasonic	220uF Reservoir Cap	EEU-FM1E2211	1	0.08	0.08
					1.54

* 1000 off prices obtained from Digikey.com on 2009/12/18

Figure 2 shows the class D amplifier with the bill of materials above on the PCB on the left of the image. The XCore on the PCB on the right of the image acquires the audio samples from USB and performs the class D computation driving the amplifier.

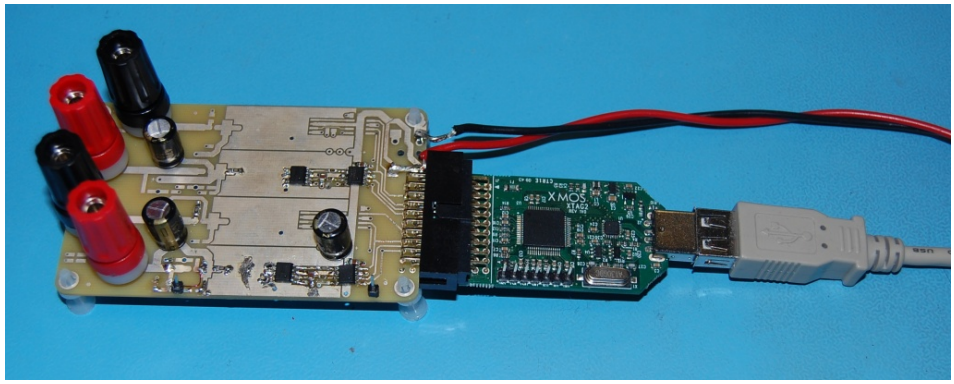

Figure 2: Example Class D Amplifier

3 Low Cost Implementation Example

If the output does not need to be high power (for example 0.2W) a lower cost implementation is possible. MOSFETs can be used which have logic level gate threshold voltages. The gates of these devices can then be driven from the XCore directly rather than requiring a separate gate driver chip. A ~50c per channel solution is possible using devices MOSFET such as FDC602P and FDC637BNZ. This approach also has the advantage that it does not need a separate power supply since the 3V3 power supply rail can be carefully reused for the PA.

4 Document History

Date	Release	Comment
2010-02-15	1.0	First release

Disclaimer