EE5311: Digital IC Design
Assignment 2

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The drive folder containing the libraries for the designs can be accessed using this link.

1 Experiment

This assignment involves schematic and layout design for the Carry-Out circuit of an adder. The circuit takes in three inputs A, B and C_{in} and generates $\overline{C_{out}}$.

$$\overline{C_{out}} = \overline{AB + BC_{in} + C_{in}A}$$

The schematic and layout design for the logic gates were performed using the Electric VLSI tool and the SPICE simulations were performed using LTSpice. Three sets of gate sizes were analysed (λ = 11nm):

1. _1X **Design** *(Arjun)*
   - **LHS Stack** L = 2λ, W_n = 8λ, W_p = 16λ
   - **RHS Stack** L = 2λ, W_n = 8λ, W_p = 16λ
2. _2X **Design** *(Srinivas)*
   - **LHS Stack** L = 2λ, W_n = 16λ, W_p = 32λ
   - **RHS Stack** L = 2λ, W_n = 8λ, W_p = 16λ
3. _4X **Design** *(Ashwanth)*
   - **LHS Stack** L = 2λ, W_n = 24λ, W_p = 48λ
   - **RHS Stack** L = 2λ, W_n = 8λ, W_p = 16λ

In order to maintain a fixed V_{DD}—GND pitch of 50λ, the larger transistors are divided into fingers. NMOS transistors in all the designs use a width of 8λ while PMOS transistors use a width of 16λ. Thus, fingers are not used in the _1X design.

2 Schematic

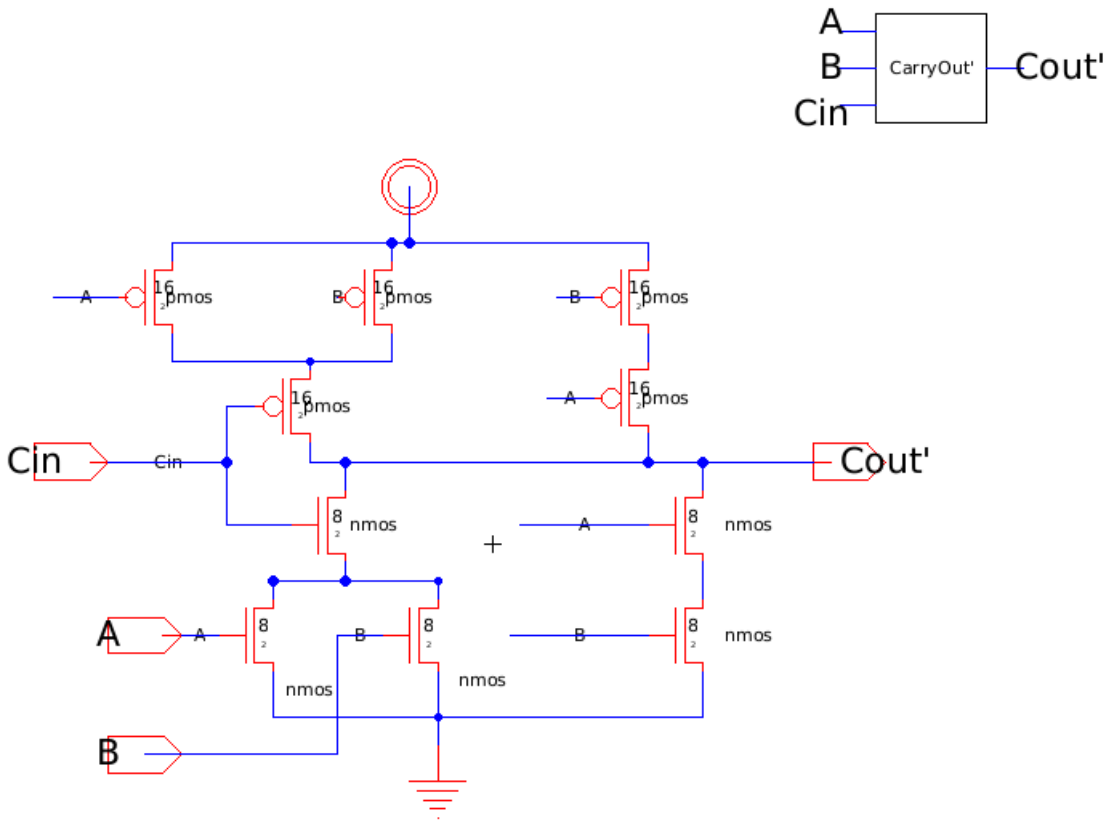

Figure 1: Schematic of Carry-Out Circuit for _1X dimensions

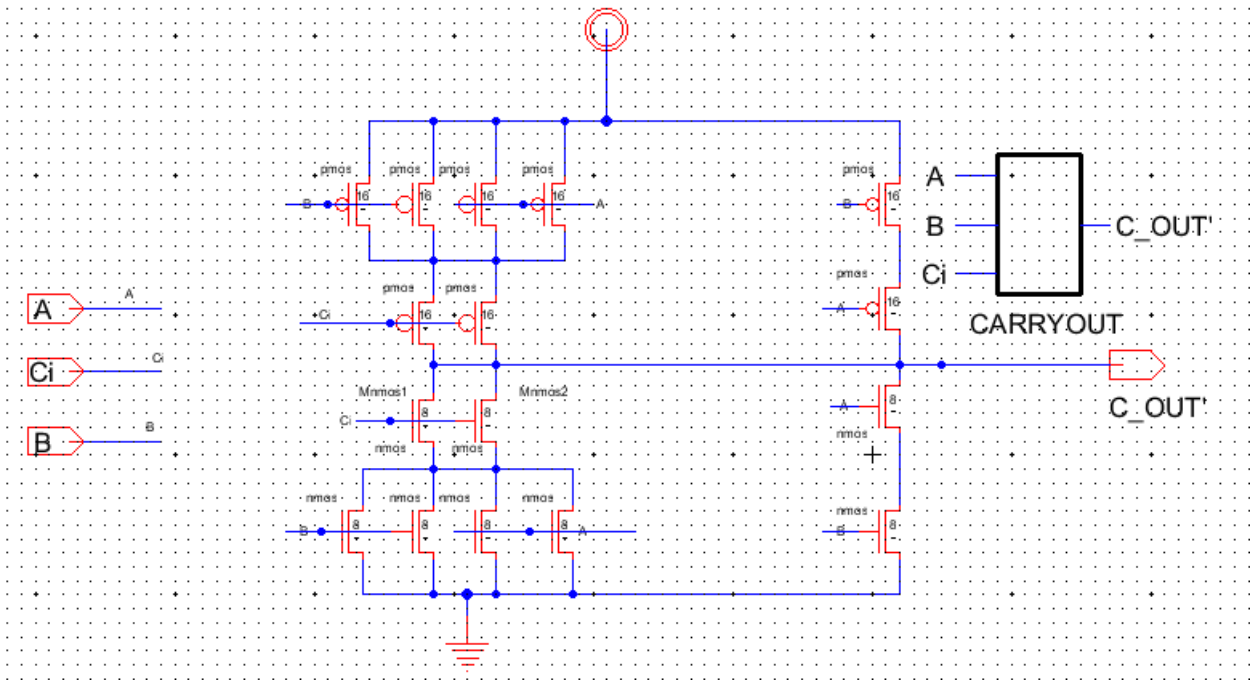

Figure 2: Schematic of Carry-Out Circuit for _2X dimensions

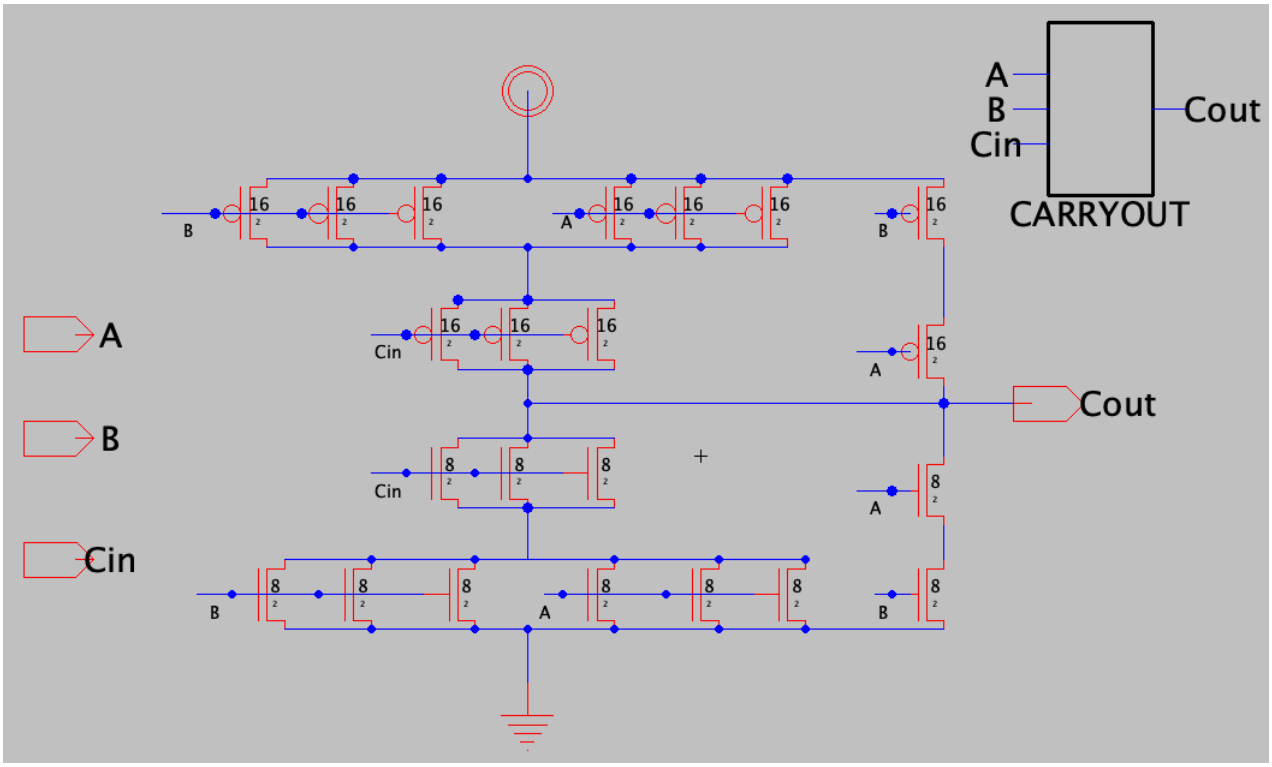

Figure 3: Schematic of Carry-Out Circuit for _4X dimensions

3 Layout

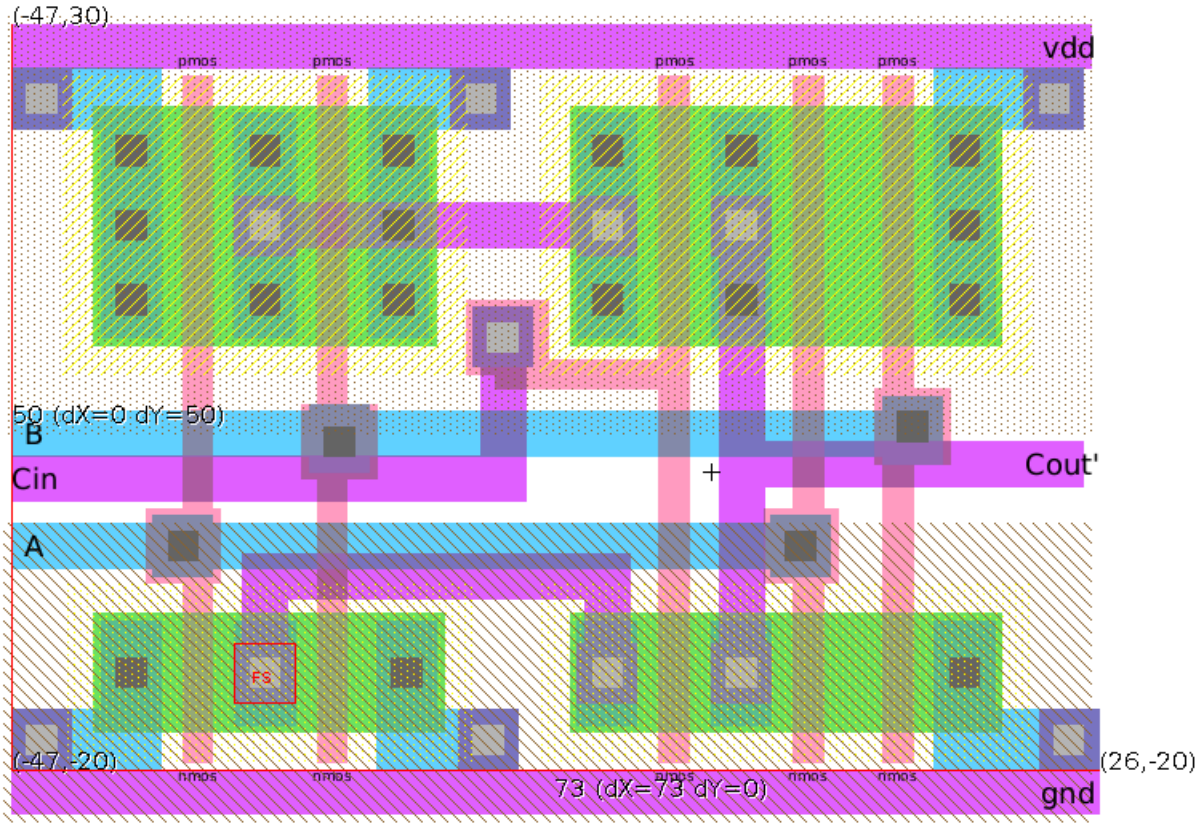

Figure 4: Layout of Carry-Out Circuit for _1X dimensions

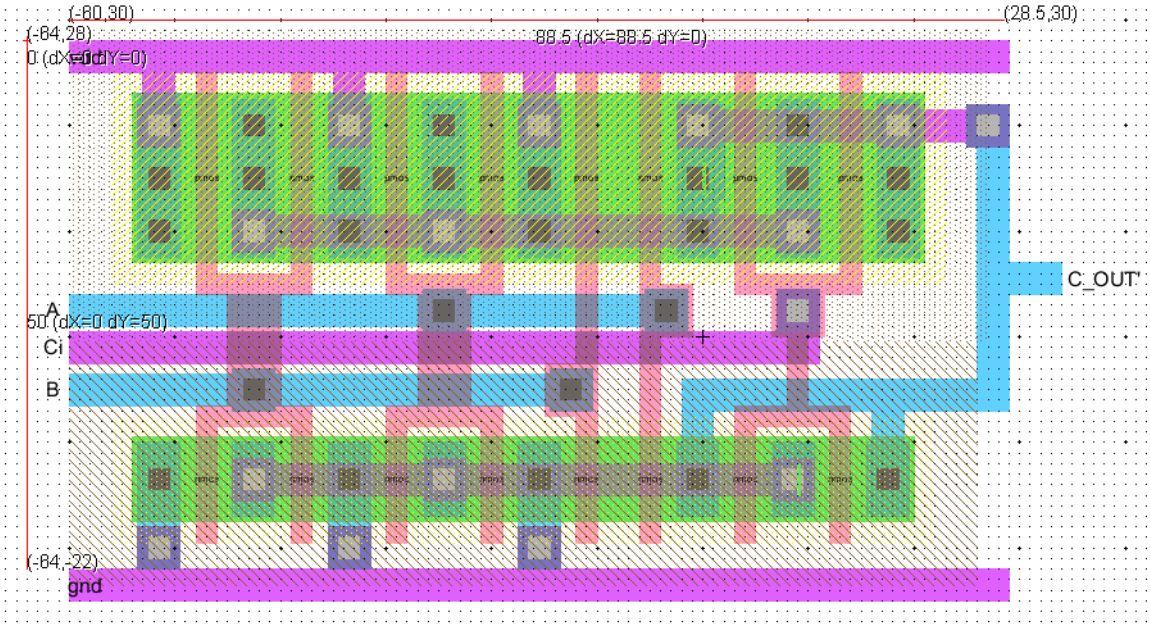

Figure 5: Layout of Carry-Out Circuit for _2X dimensions

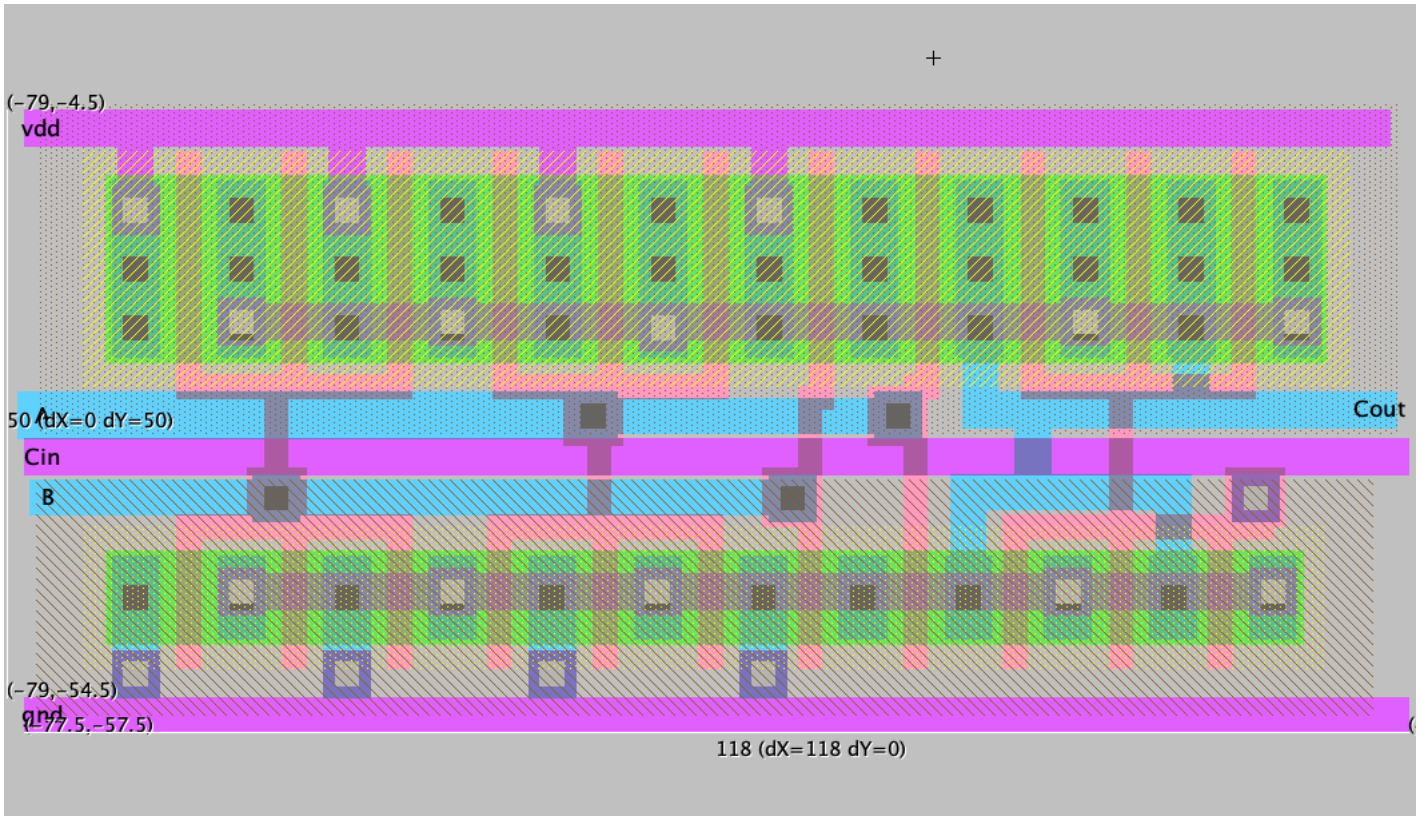

Figure 6: Layout of Carry-Out Circuit for _4X dimensions

4 Functional Simulation

Verification of Truth Table of the logic gates.

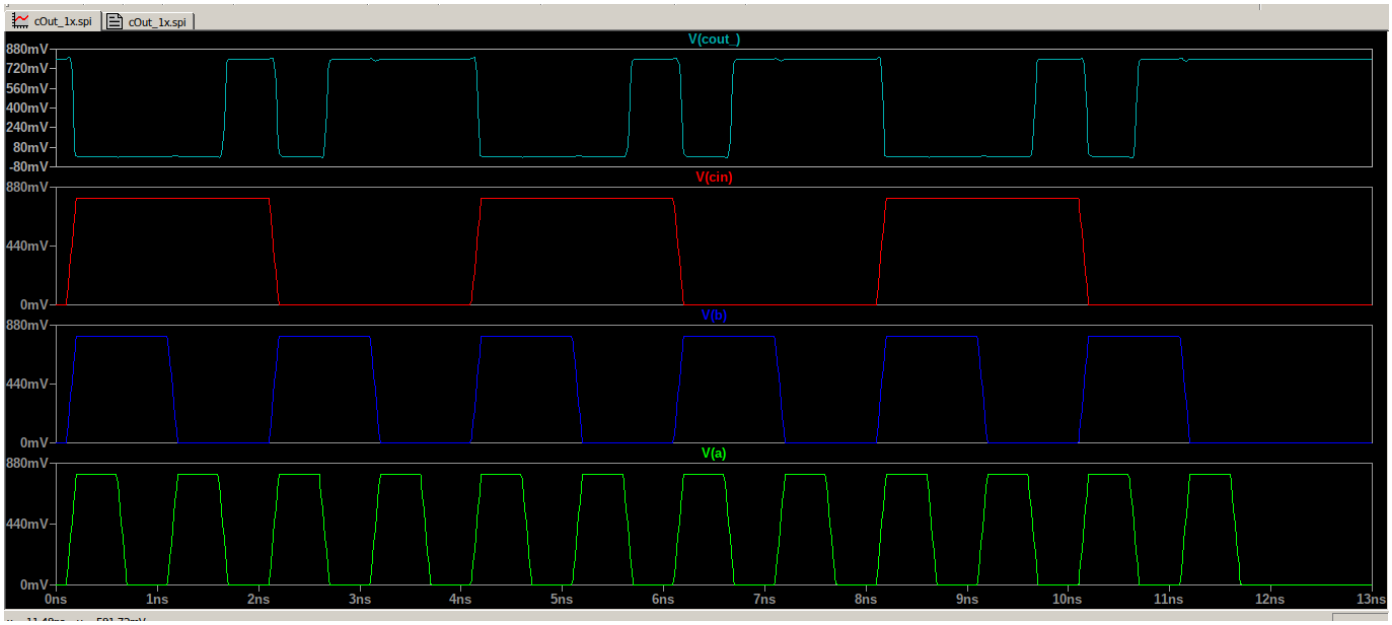

Figure 7: Functionality of Carry-Out Circuit

5 DRC and LVS results

DRC and LVS results of the layouts

5.1 1X

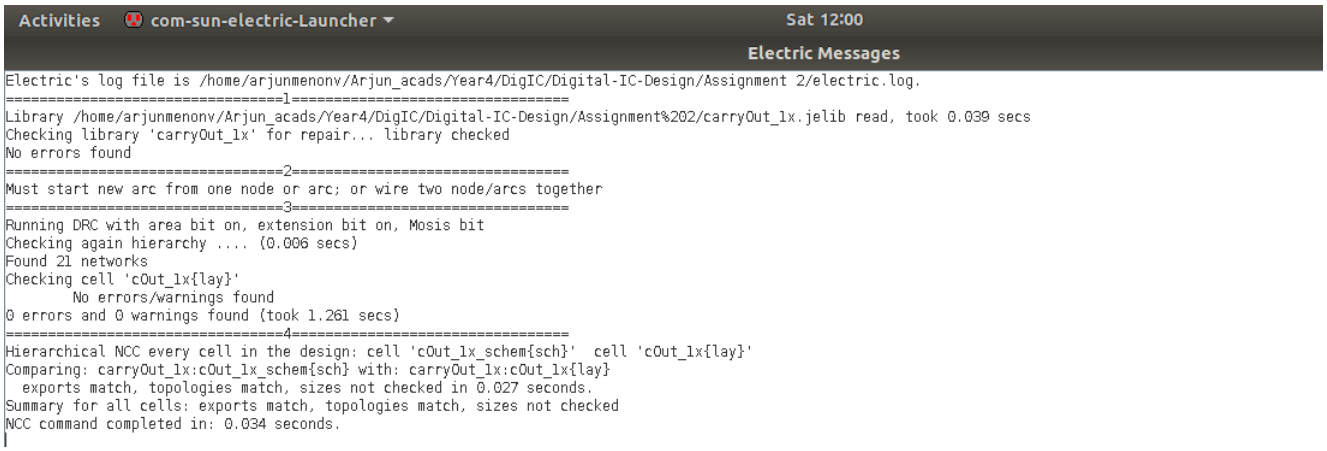

Figure 8: DRC and LVS of 1X

5.2 2X

```
================================2================================
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 29 networks
Checking cell 'CARRYOUT{lay}'
        No errors/warnings found
0 errors and 0 warnings found (took 0.17 secs)
================================3================================
Hierarchical NCC every cell in the design: cell 'CARRYOUT{sch}'  cell 'CARRYOUT{lay}'
Comparing: EXPT2_2x:CARRYOUT{sch} with: EXPT2_2x:CARRYOUT{lay}
  exports match, topologies match, sizes not checked in 0.131 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.131 seconds.
```

Figure 9: DRC and LVS of 2X

5.3 4X

```
================================2609================================
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 33 networks
0 errors and 0 warnings found (took 0.002 secs)
================================2610================================
Hierarchical NCC every cell in the design: cell 'cout{sch}'  cell 'cout{lay}'
Comparing: cout:cout{sch} with: cout:cout{lay}
  exports match, topologies match, sizes not checked in 0.008 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.01 seconds.
```

Figure 10: DRC and LVS of 4X

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