EE5311: Digital IC Design
Assignment 4

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November 7, 2021

The drive folder containing the libraries for the designs can be accessed using this link.

1 Introduction

The cells designed in the previous assignments are now used to assemble a signed 8-bit multiplier. The architecture used for the multiplier is the signed Carry-Save architecture (CSM) with a ripple adder in the vector merge stage. The sizes of the NAND and Full Adder cells that result in the least delay without compromising on the area is also found by evaluating a model of the critical path of the CSM circuit.

To optimise the delay, inverting Full Adders were used in the circuit. Using the mirroring property of Full Adders, the number of inverters in the circuit were minimised, with no inverter being present in the critical path. Two kinds of Half Adder icons were derived from the FA in order to make use of the FA's mirroring property:

- For non-inverting inputs to HA, the C_{in} terminal of the FA was tied to gnd so that inverting outputs are generated.
- For inverting inputs to the HA, the C_{in} terminal of the FA was tied to V_{DD} so that non-inverting outputs are generated.

2 Critical Path Model

Since the Full Adder topology used requires $\overline{C_{out}}$ to be computed for evaluating $\overline{Sum}$, the critical delay is dominated by the propagation of the $\overline{Sum}$ signal. In order to characterise the critical delay of the CSM corresponding to a combination of cell sizes, the critical path of the multiplier is simulated separately; the delay from the input to the MSB of the product is evaluated for all possible sizes to find

the optimal set of sizes.

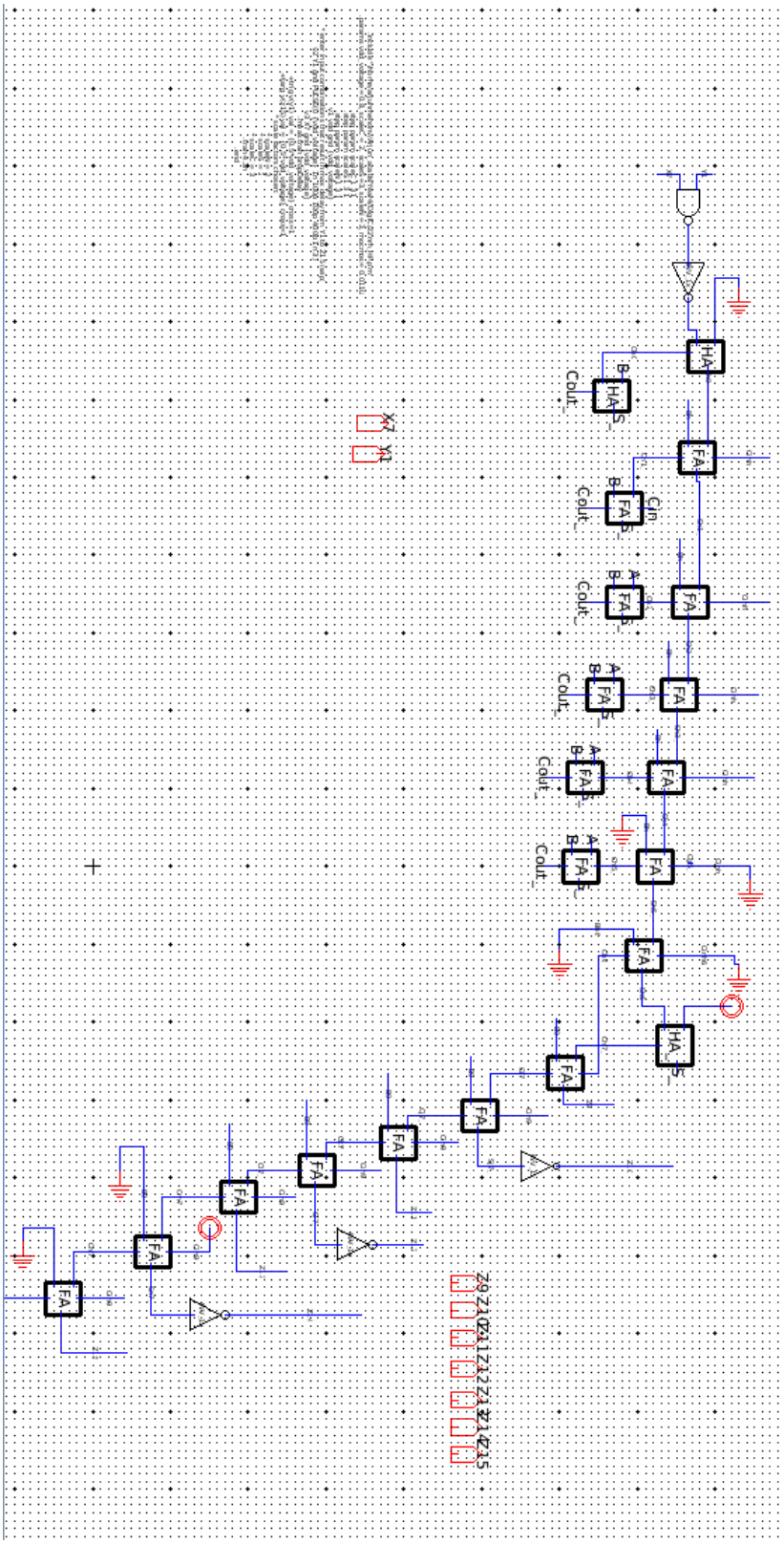

Figure 1: Critical Path Model for CSM

Parameters in simulation:

- scaleN: NAND size; `.step param scaleN 1 3 1`

- scaleS: size of Sum-Gen stage of FA; `.step param scaleS 1 3 1`
- scaleC: size of Carry-Out stage of FA; `.step param scaleC 1 3 1`

3 Schematic

Due to the large size of the circuit, the schematic is presented here in chunks.

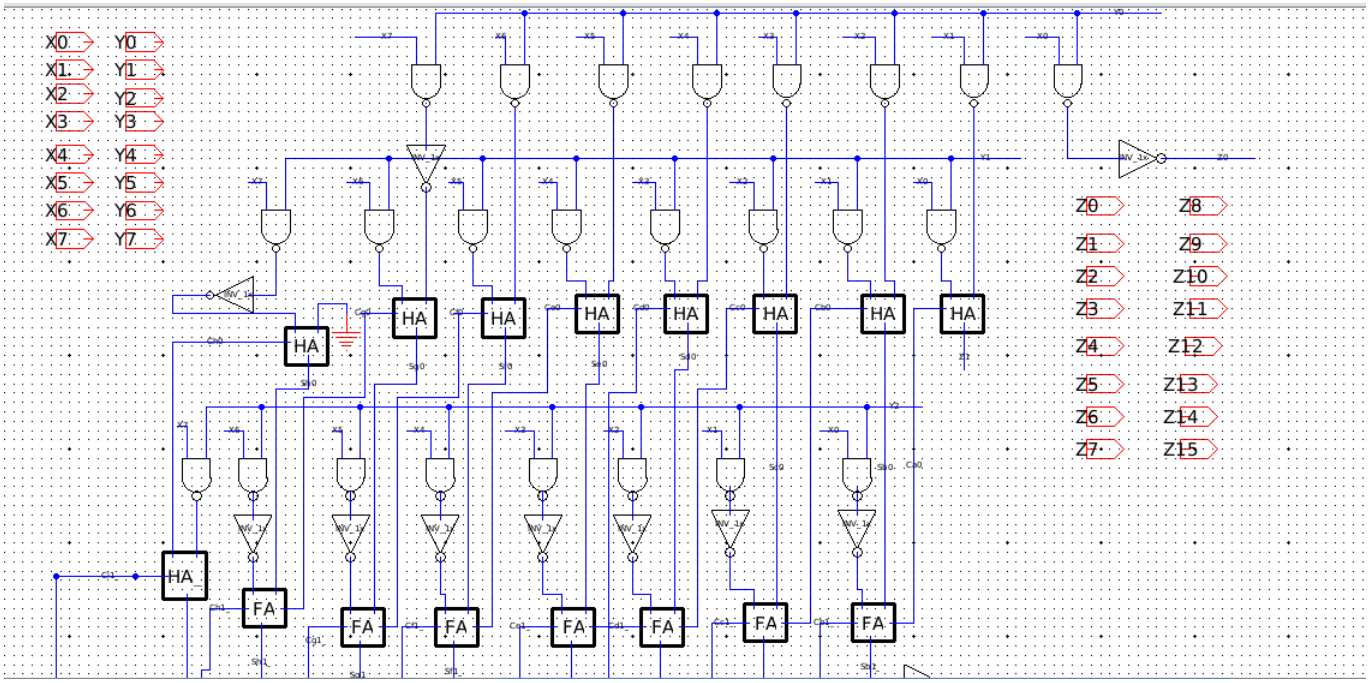

Figure 2: Rows 0 and 1 of CSM

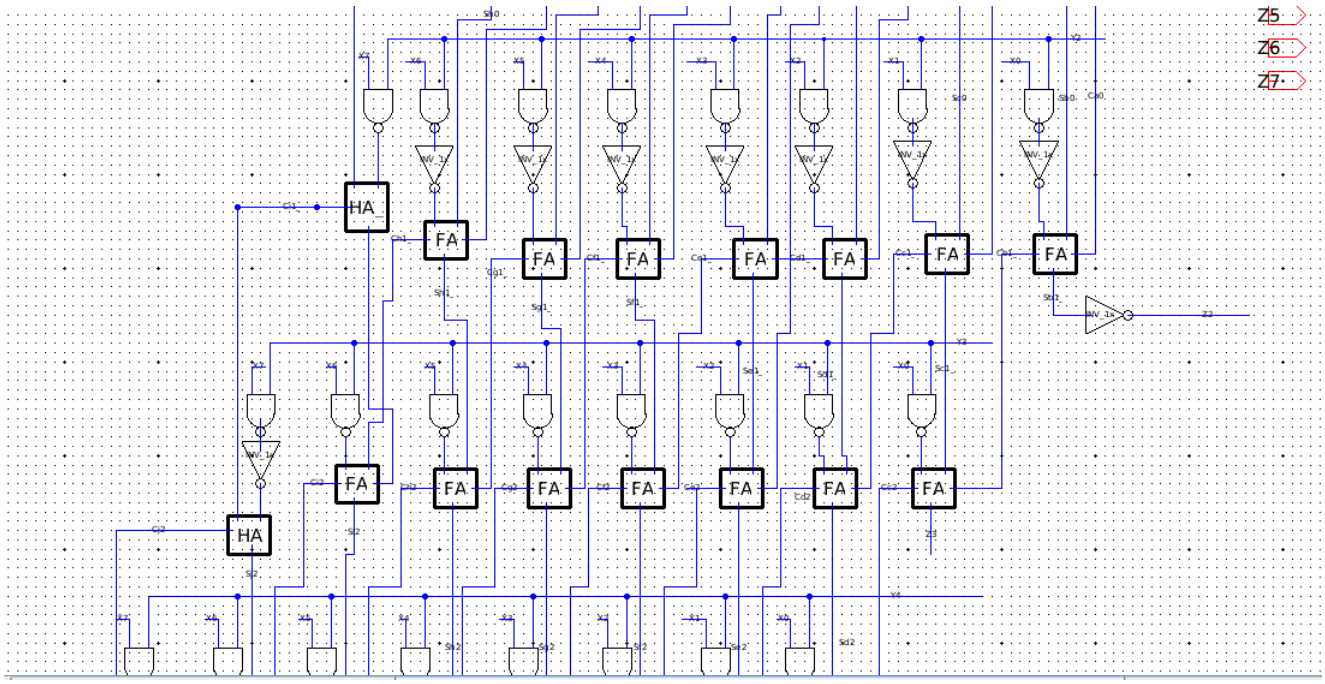

Figure 3: Rows 2 and 3 of CSM

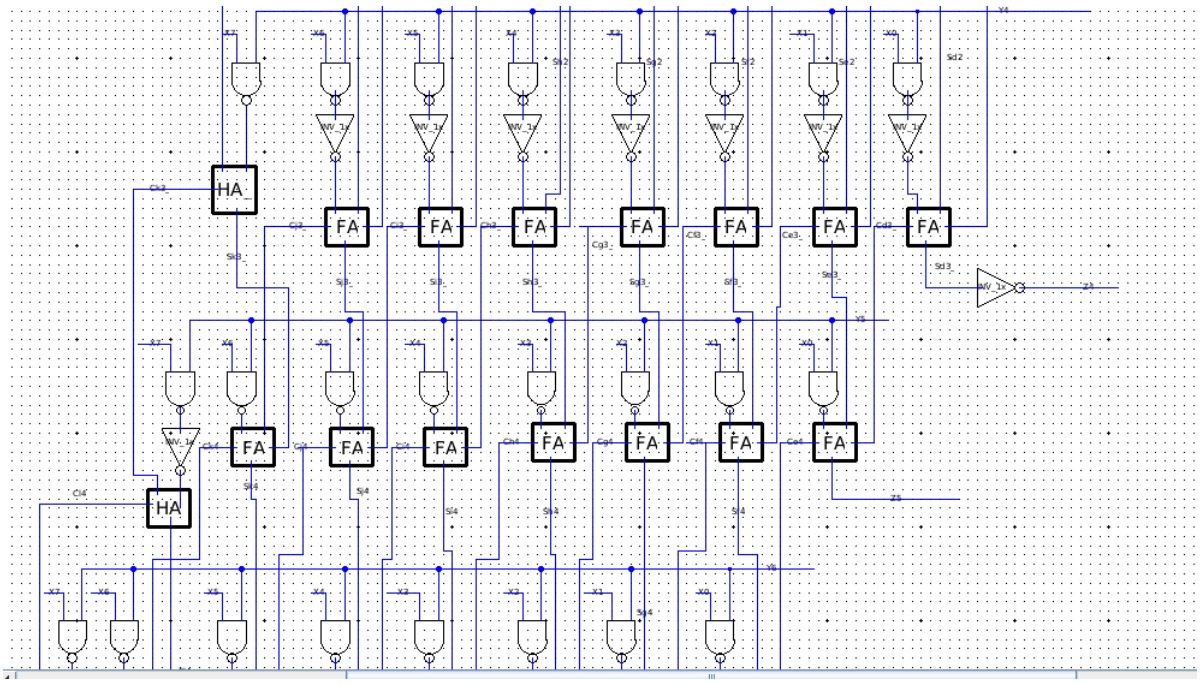

Figure 4: Rows 4 and 5 of CSM

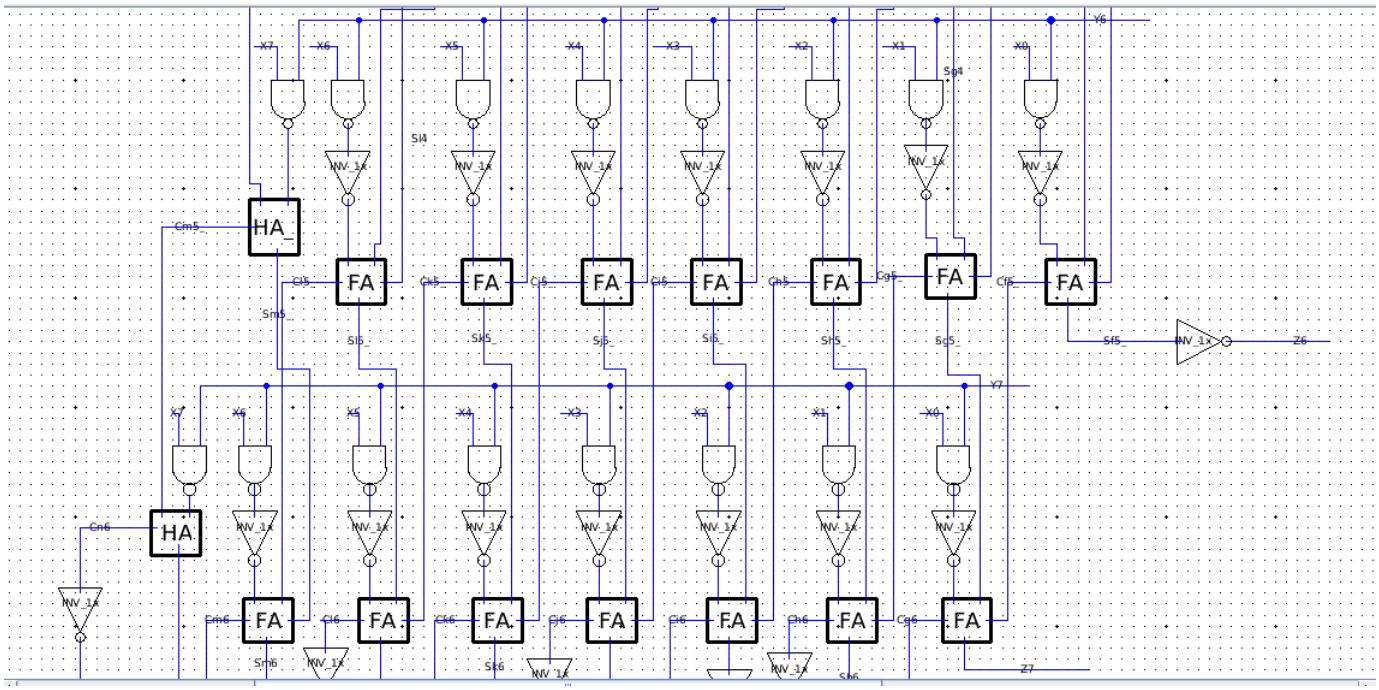

Figure 5: Rows 6 and 7 of CSM

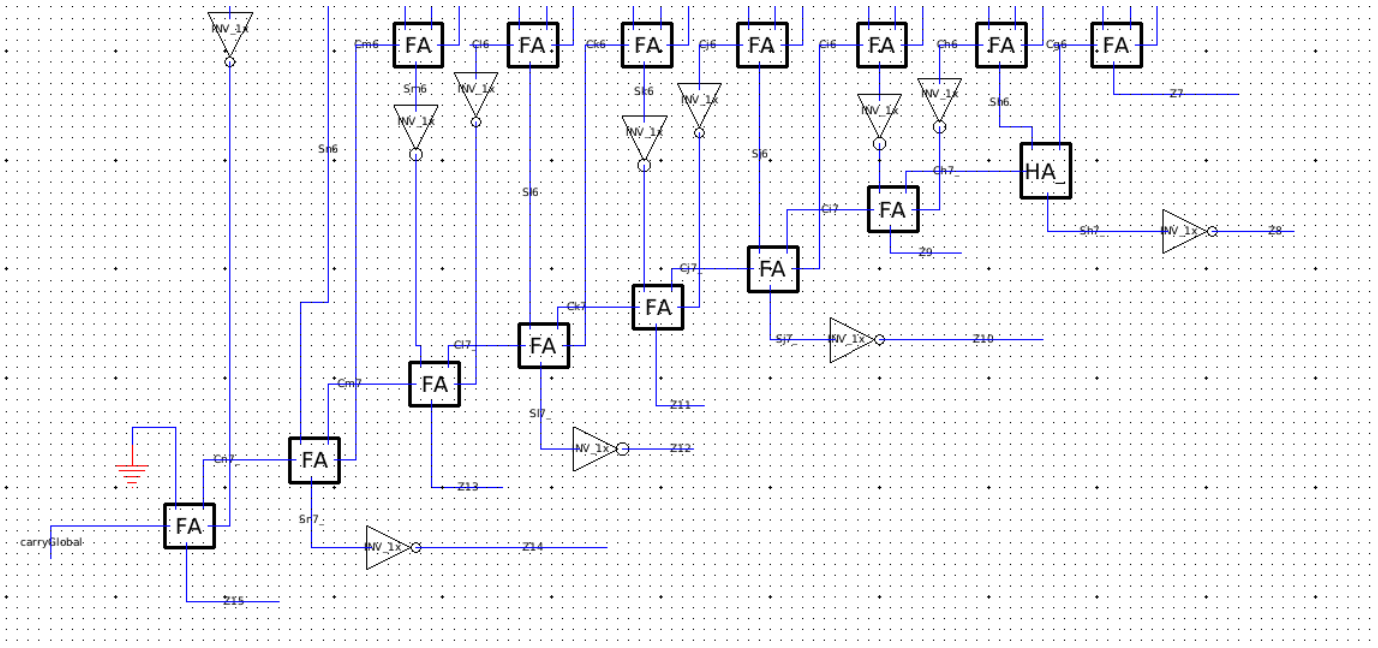

Figure 6: Vector Merge Stage of the CSM: a ripple carry adder is used here

4 Determining Optimal Sizes

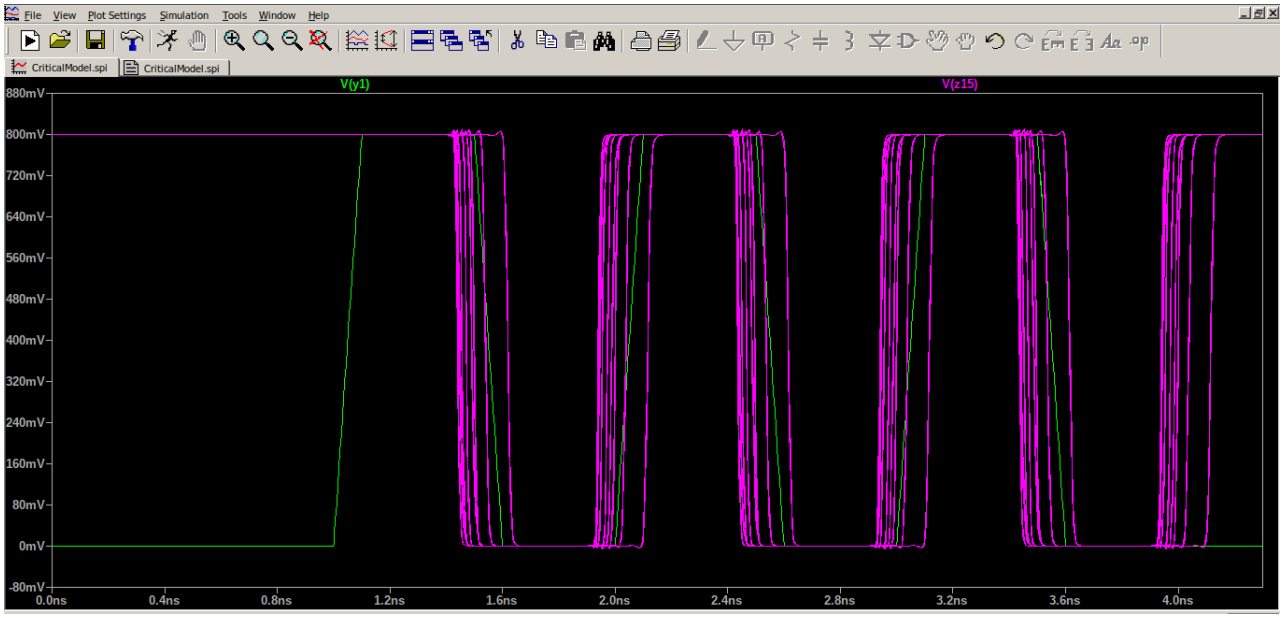

Figure 7: Y1-Z15 delay of the Critical Model circuit for all 27 size combinations

4.1 Table of Delays

Sl No	NAND	Sum	Cout	Delay (op fall)	Delay (op rise)	SumGen area	Cout area	Net FA area	CSM area (ign. NAND, inv)
1	1	1	1	4.42E-10	4.40E-10	5125	3650	8775	561600
2	1	1	2	3.97E-10	3.95E-10	5125	4425	9550	611200
3	1	1	3	3.99E-10	3.97E-10	5125	5900	11025	705600
4	1	2	1	4.91E-10	4.89E-10	10470	3650	14120	903680
5	1	2	2	4.06E-10	4.07E-10	10470	4425	14895	953280
6	1	2	3	3.92E-10	3.92E-10	10470	5900	16370	1047680
7	1	3	1	5.70E-10	5.68E-10	11050	3650	14700	940800
8	1	3	2	4.51E-10	4.51E-10	11050	4425	15475	990400
9	1	3	3	4.23E-10	4.24E-10	11050	5900	16950	1084800
10	2	1	1	4.40E-10	4.38E-10	5125	3650	8775	561600
11	2	1	2	3.95E-10	3.93E-10	5125	4425	9550	611200
12	2	1	3	3.97E-10	3.95E-10	5125	5900	11025	705600
13	2	2	1	4.89E-10	4.87E-10	10470	3650	14120	903680
14	2	2	2	4.05E-10	4.05E-10	10470	4425	14895	953280
15	2	2	3	3.90E-10	3.90E-10	10470	5900	16370	1047680
16	2	3	1	5.68E-10	5.66E-10	11050	3650	14700	940800
17	2	3	2	4.49E-10	4.49E-10	11050	4425	15475	990400
18	2	3	3	4.21E-10	4.22E-10	11050	5900	16950	1084800
19	4	1	1	4.39E-10	4.37E-10	5125	3650	8775	561600
20	4	1	2	3.94E-10	3.92E-10	5125	4425	9550	611200
21	4	1	3	3.96E-10	3.94E-10	5125	5900	11025	705600
22	4	2	1	4.88E-10	4.86E-10	10470	3650	14120	903680
23	4	2	2	4.04E-10	4.04E-10	10470	4425	14895	953280
24	4	2	3	3.89E-10	3.89E-10	10470	5900	16370	1047680
25	4	3	1	5.68E-10	5.65E-10	11050	3650	14700	940800
26	4	3	2	4.48E-10	4.48E-10	11050	4425	15475	990400
27	4	3	3	4.20E-10	4.21E-10	11050	5900	16950	1084800

Table 1: Cell Size vs Delay: Top 5 combinations with least delay are highlighted

The combination of sizes that was picked for the CSM circuit was combination 11- NAND: 2X, Sum-Gen: 1X, Carry-Out: 2X. This was chosen despite combination 24 having the least delay as this combination offers low delay on relatively lower area than combination 24.

Note that the area calculation considers only the area of FAs (evaluated from the dimensions of the layout of the corresponding FA). Therefore, comparing configurations 11 and 20, while config 20 offers a lower delay (an advantage of 1ps) than config 11, its area is larger as the NAND gate is now twice the size of that used in config 11 (not reflected in the calculations).

5 Functional Simulation

The functionality of the circuit was simulated for three sets of input vectors.

5.1 16 X 16

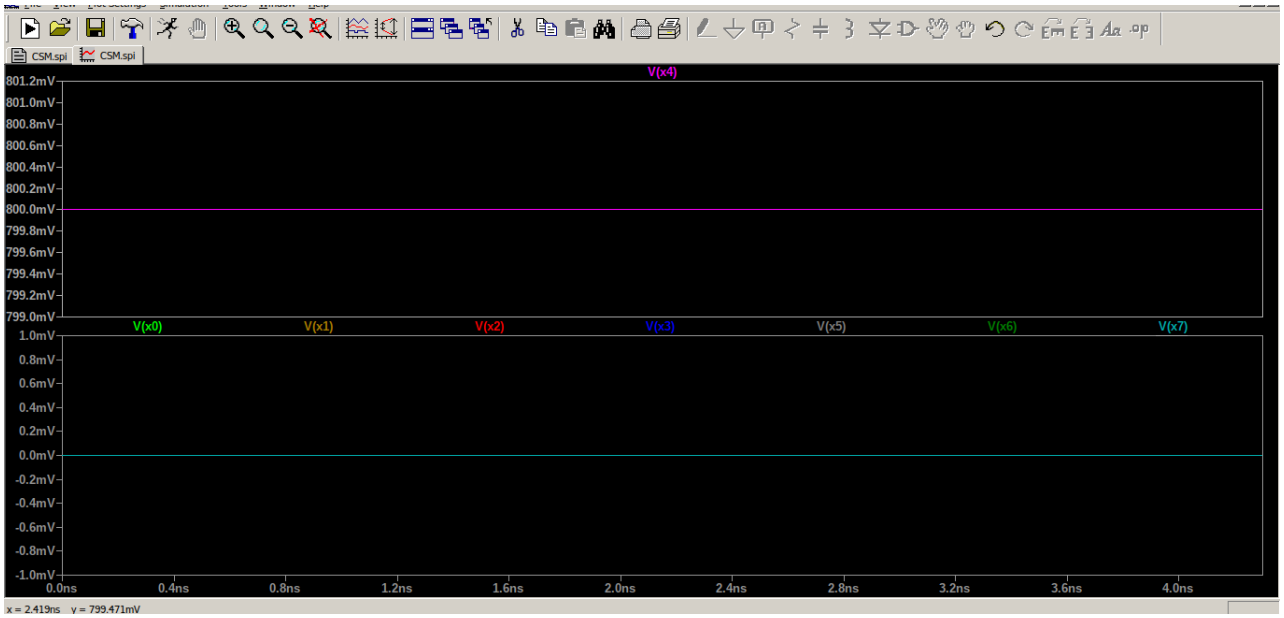

Figure 8: x = $(0001\ 0000)_2 = 16_{10}$

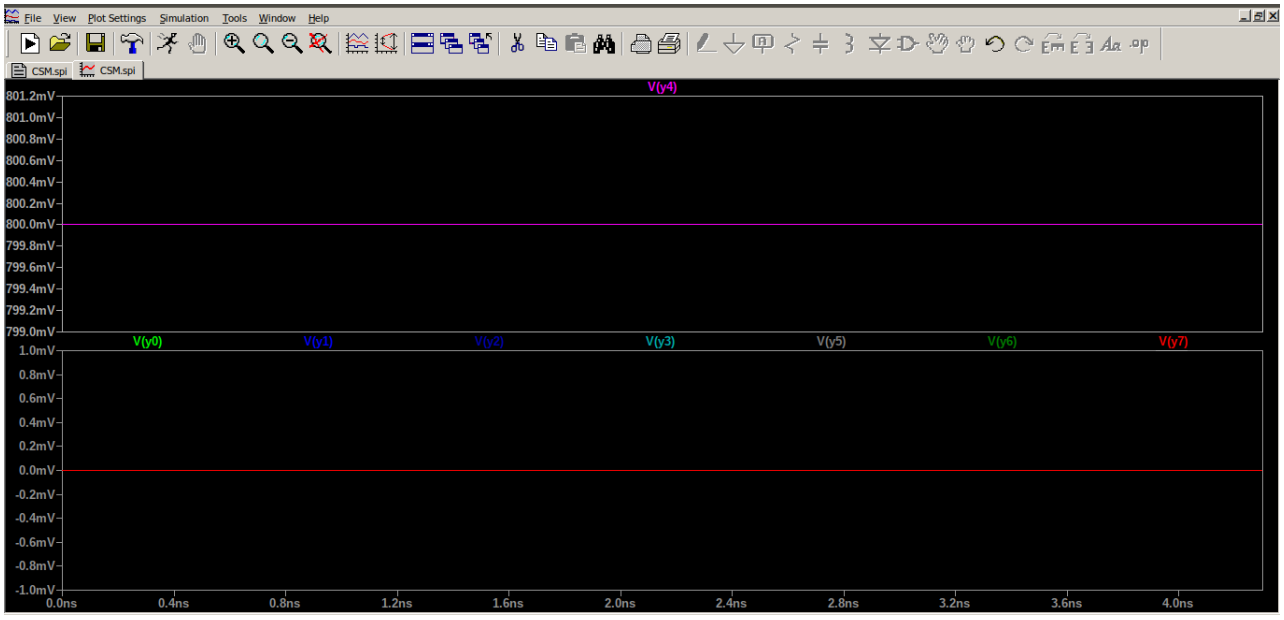

Figure 9: y = $(0001\ 0000)_2 = 16_{10}$

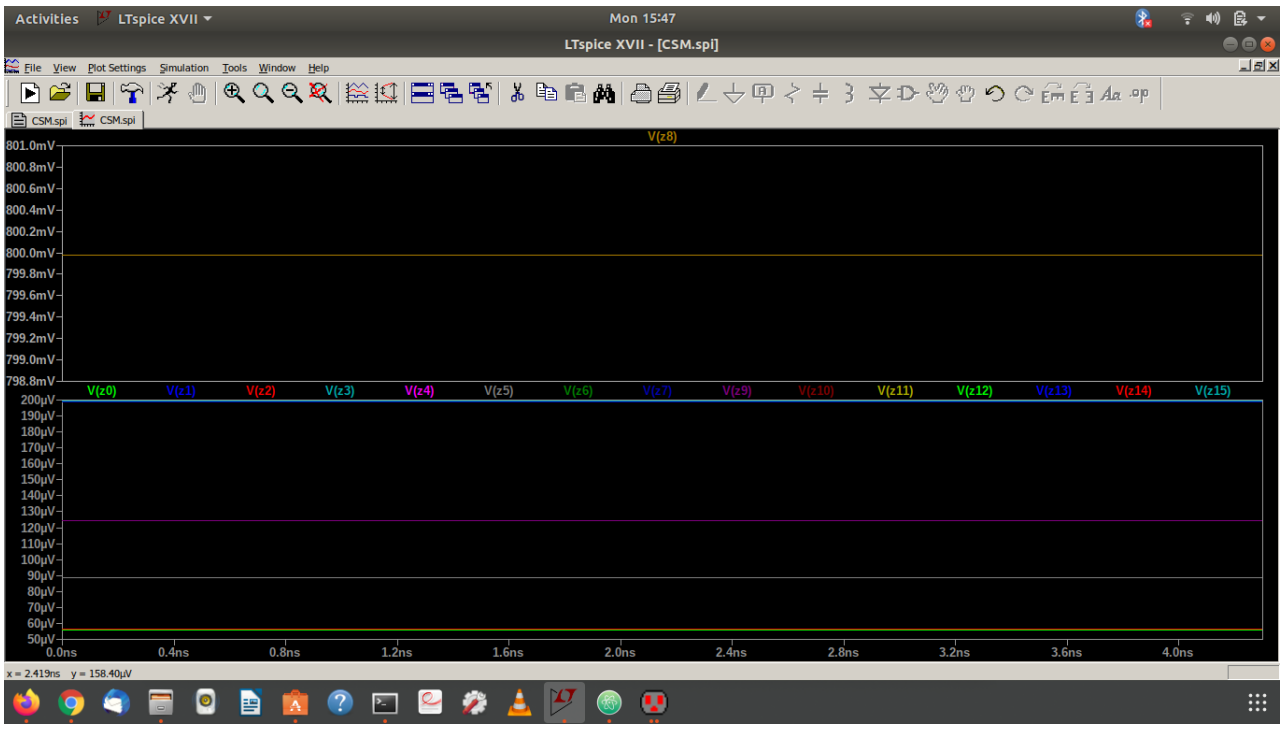

Figure 10: z = $(0000\ 0001\ 0000\ 0000)_2 = 256_{10}$

5.2 -1 X -1

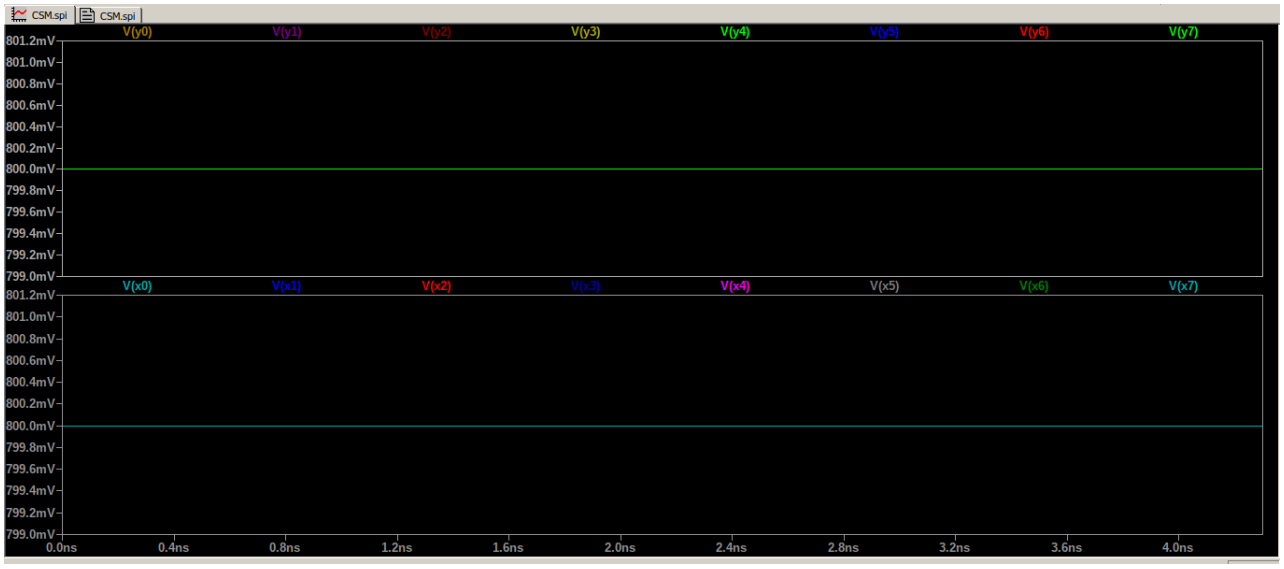

Figure 11: x = y = $(1111\ 1111)_2 = -1_{10}$

Figure 12: z = $(0000\ 0000\ 0000\ 0001)_2 = 1_{10}$

5.3 80 X -109

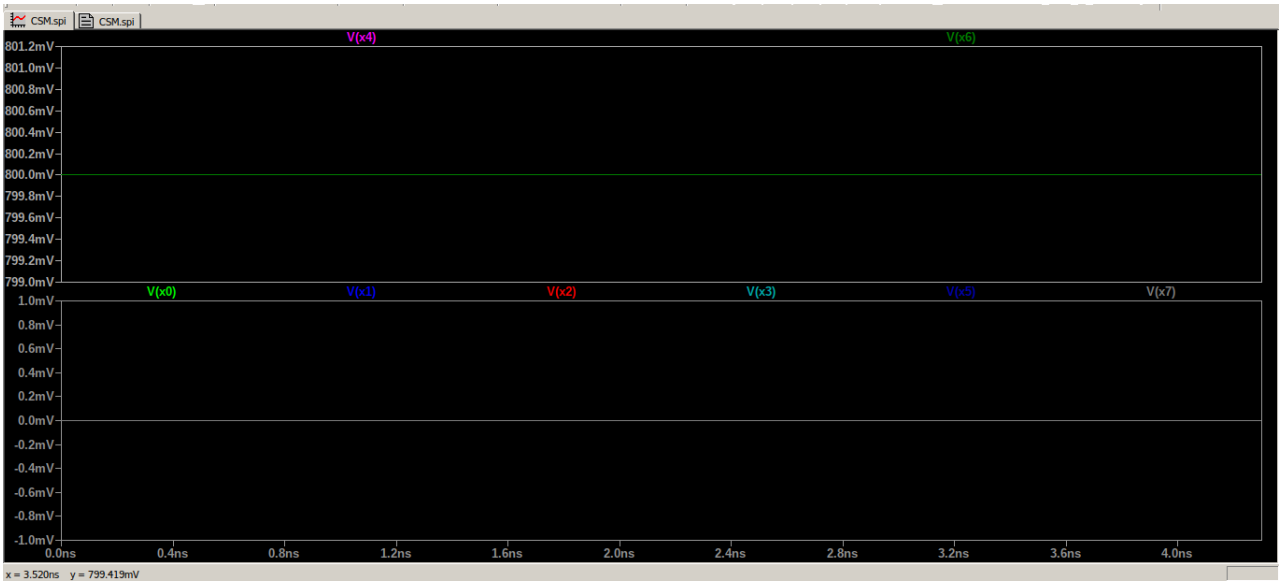

Figure 13: x = $(0101\ 0000)_2 = 80_{10}$

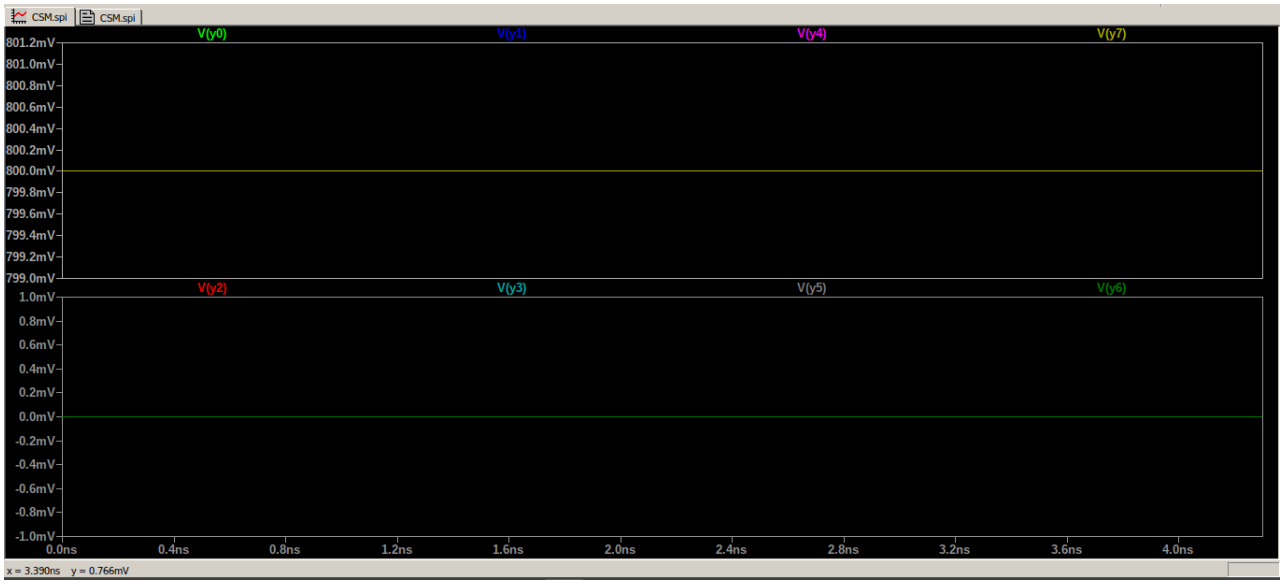

Figure 14: y = $(1001\ 0011)_2 = -109_{10}$

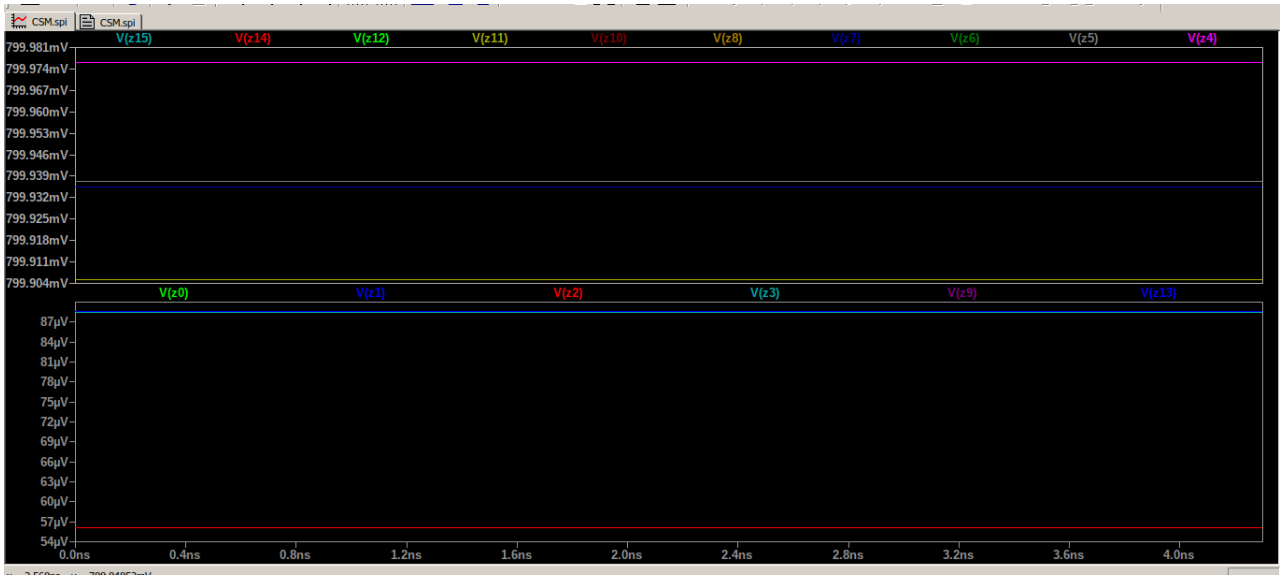

Figure 15: z = $(1101\ 1101\ 1111\ 0000)_2 = -8720_{10}$ = -109 * 80

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