EE5311: Digital IC Design
Assignment 1

Arjun Menon V Srinivas R Ashwanth S
EE18B104 EE18B136 EE18B040
Electrical Engineering
IIT Madras

September 19, 2021

The drive folder containing the libraries for the designs can be accessed using this link.

1 Experiment

In this experiment, we have simulated the functional and timing behaviour of Inverter, NAND2 and AND2 logic gates using the HP 22nm CMOS spice model. The schematic and layout design for the logic gates were performed using the Electric VLSI tool and the SPICE simulations were performed using LTSpice. Three sets of gate sizes were analysed (λ = 11nm):

1. _1X **Design** *(Arjun)*
   - **Inverter** L = 2λ, W_n = 4λ, W_p = 8λ
   - **NAND2** L = 2λ, W_n = 8λ, W_p = 8λ
2. _2X **Design** *(Srinivas)*
   - **Inverter** L = 2λ, W_n = 8λ, W_p = 16λ
   - **NAND2** L = 2λ, W_n = 16λ, W_p = 16λ
3. _4X **Design** *(Ashwanth)*
   - **Inverter** L = 2λ, W_n = 16λ, W_p = 32λ
   - **NAND2** L = 2λ, W_n = 32λ, W_p = 32λ

2 Schematic

2.1 Inverter

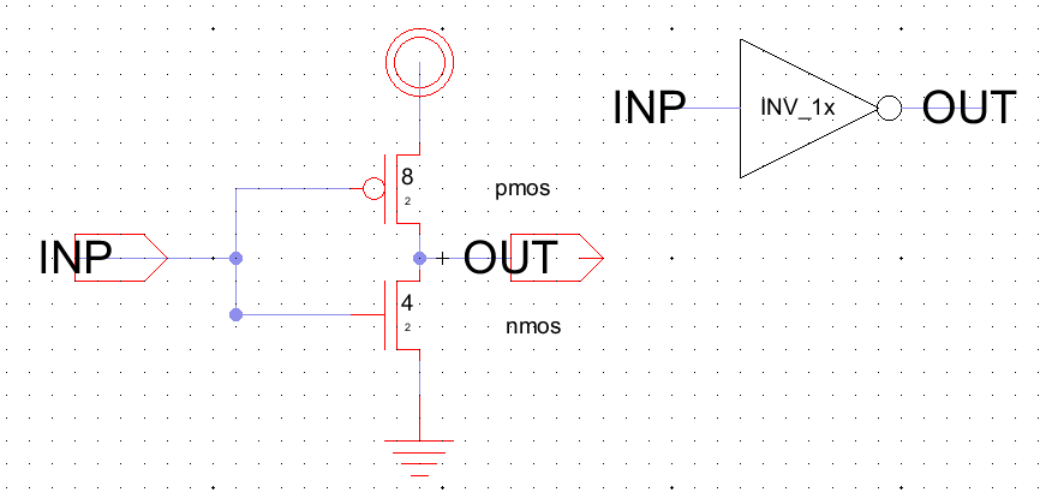

Figure 1: Schematic of Inverter_1X

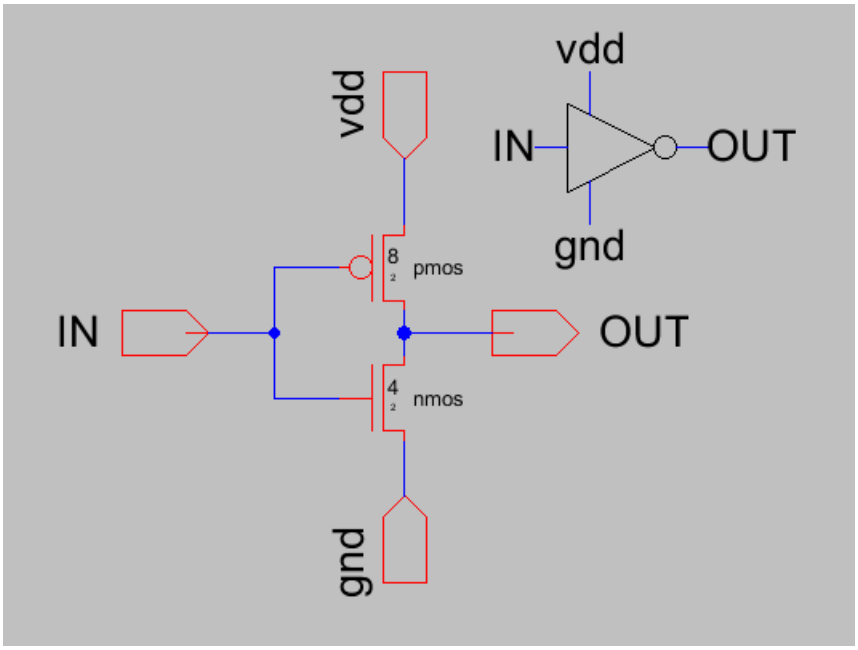

Figure 2: Schematic of Inverter_2X

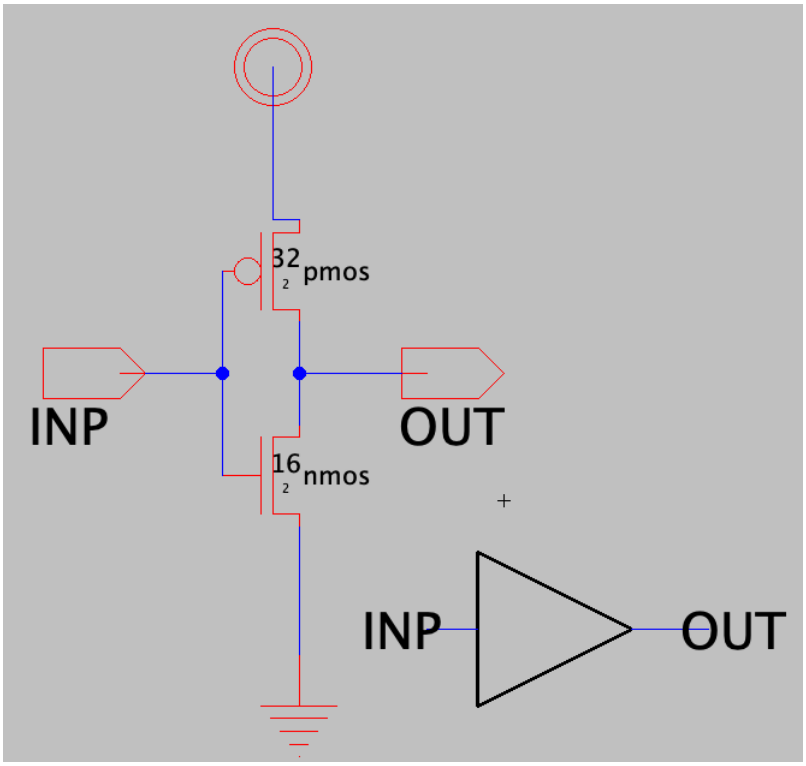

Figure 3: Schematic of Inverter_4X

2.2 NAND2

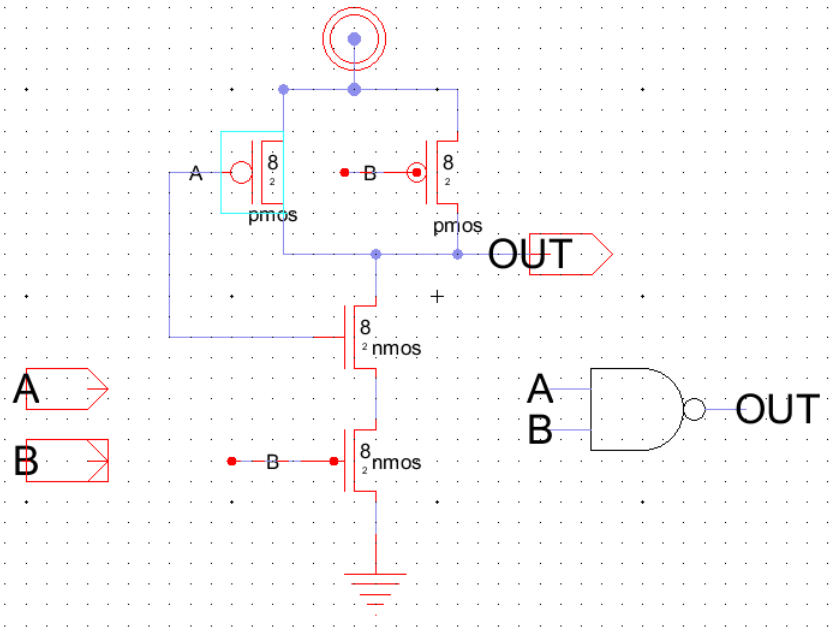

Figure 4: Schematic of NAND2_1X

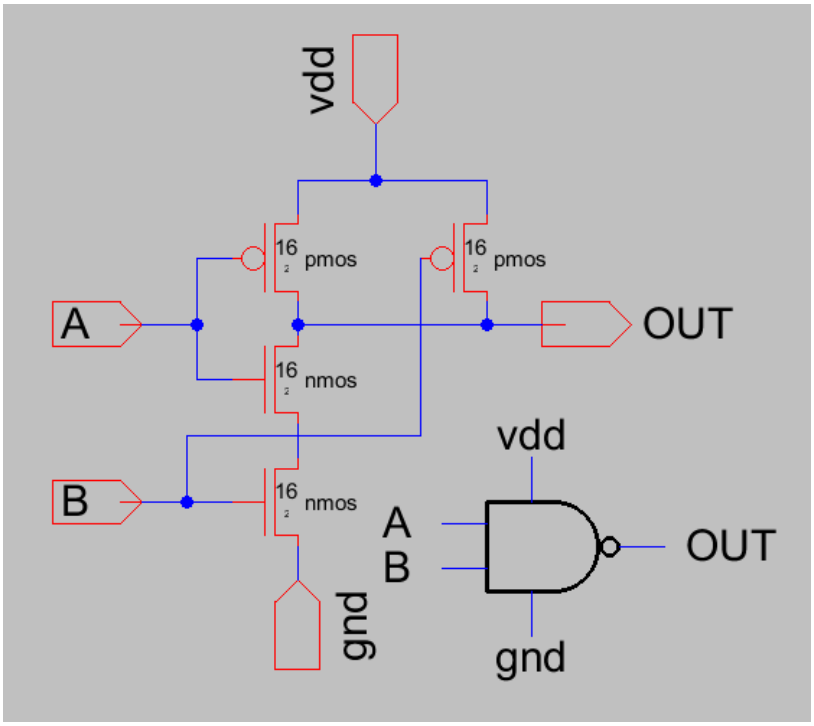

Figure 5: Schematic of NAND2_2*X*

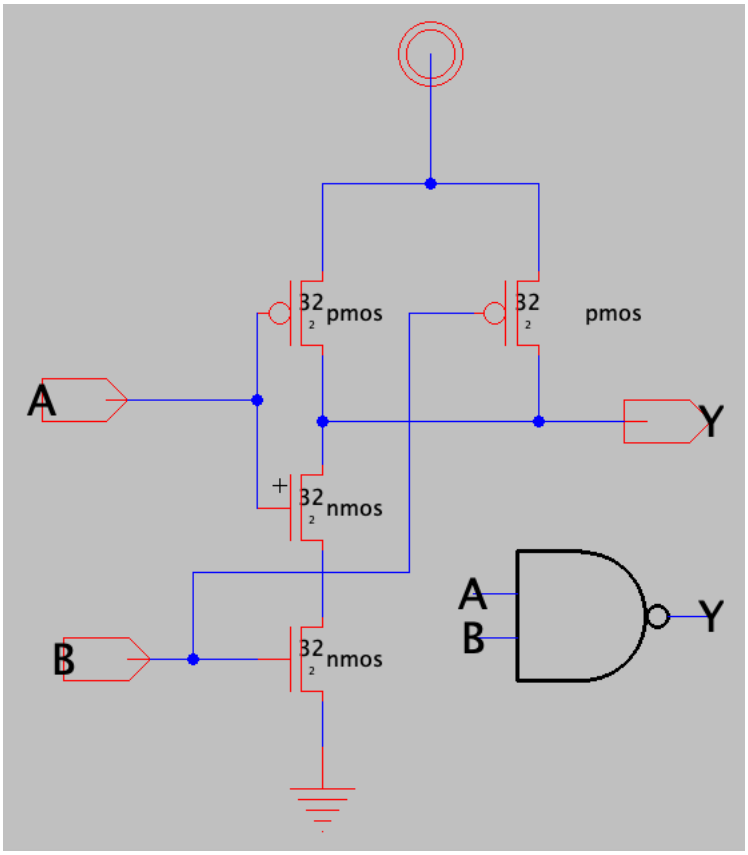

Figure 6: Schematic of NAND2_4*X*

2.3 AND2

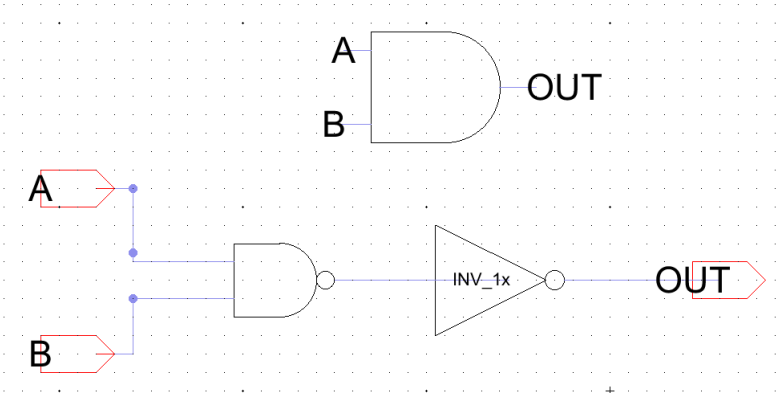

Figure 7: Schematic of AND2_1*X*

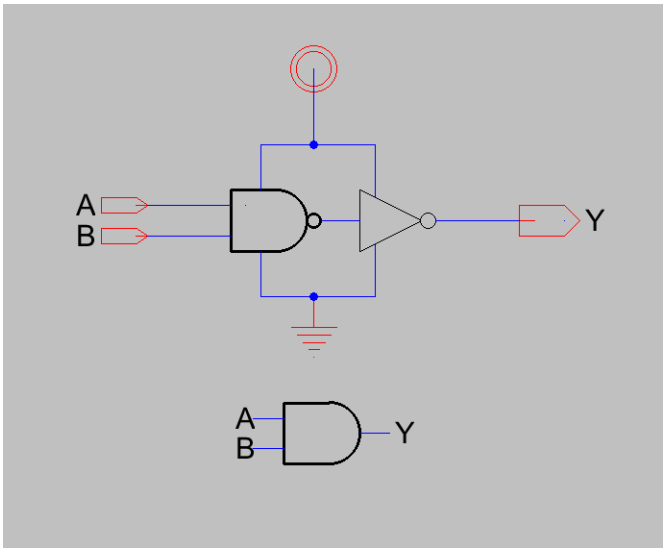

Figure 8: Schematic of AND2_2*X*

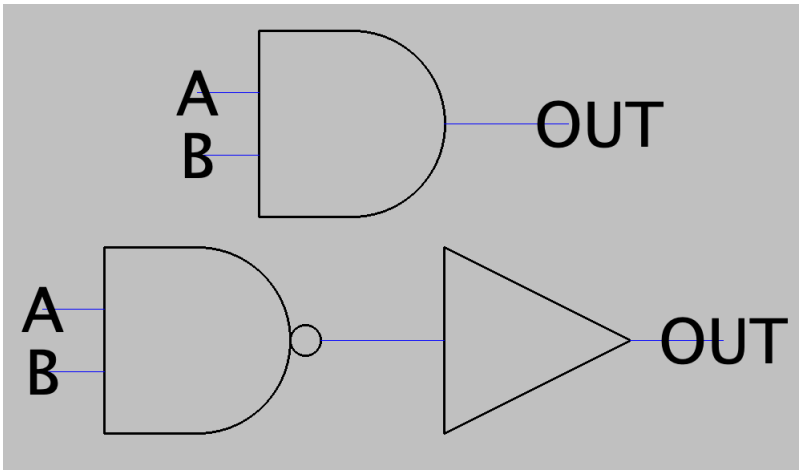

Figure 9: Schematic of AND2_4*X*

3 Layout

3.1 Inverter

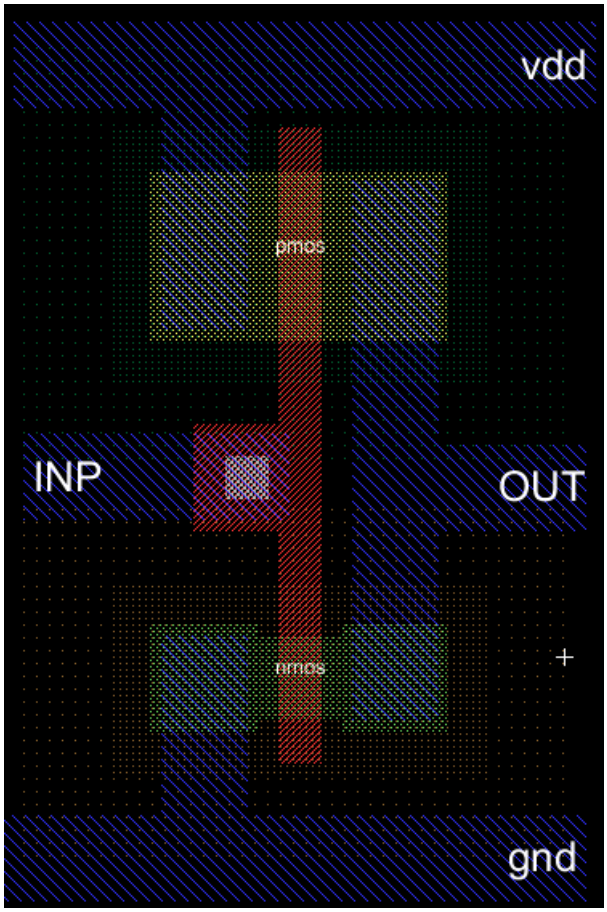

Figure 10: Layout of Inverter_1X

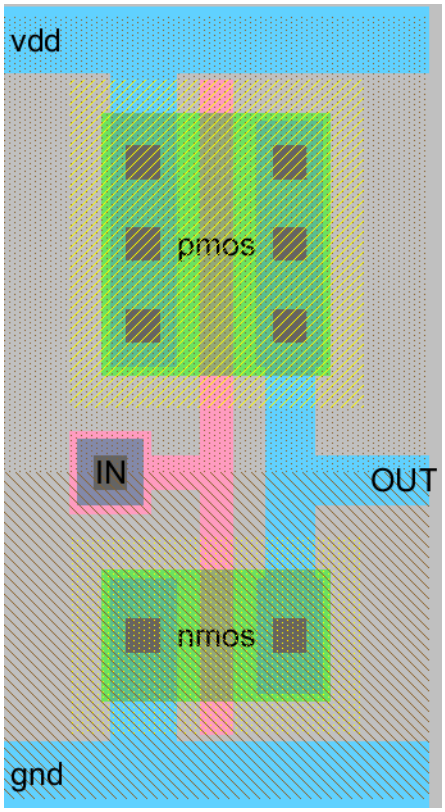

Figure 11: Layout of Inverter_2X

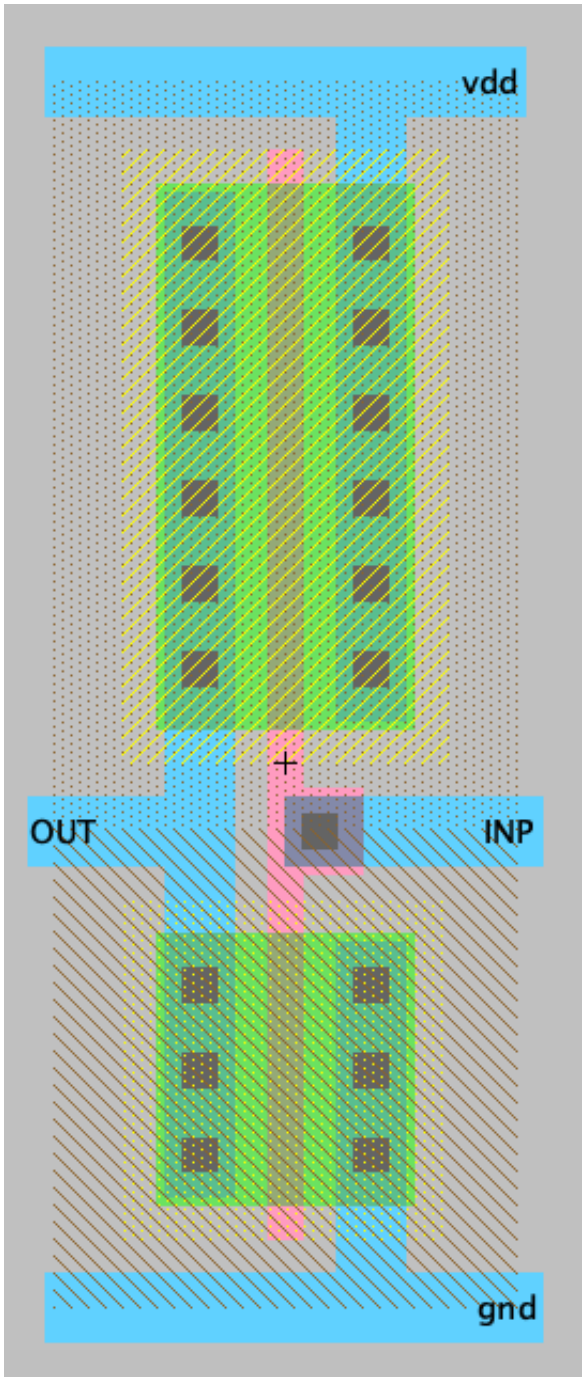

Figure 12: Layout of Inverter_4X

3.2 NAND2

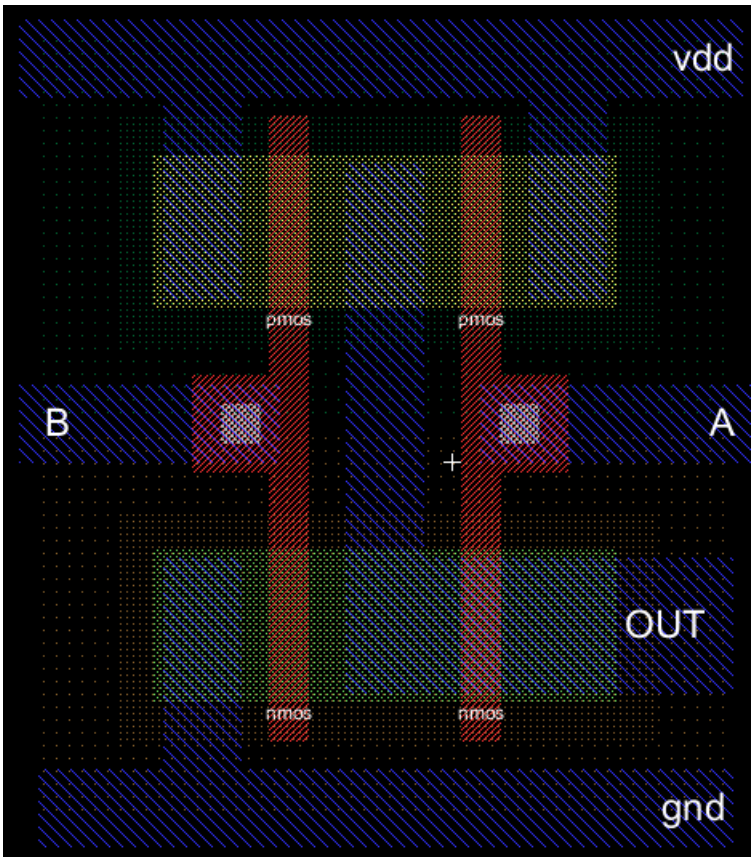

Figure 13: Layout of NAND2_1*X*

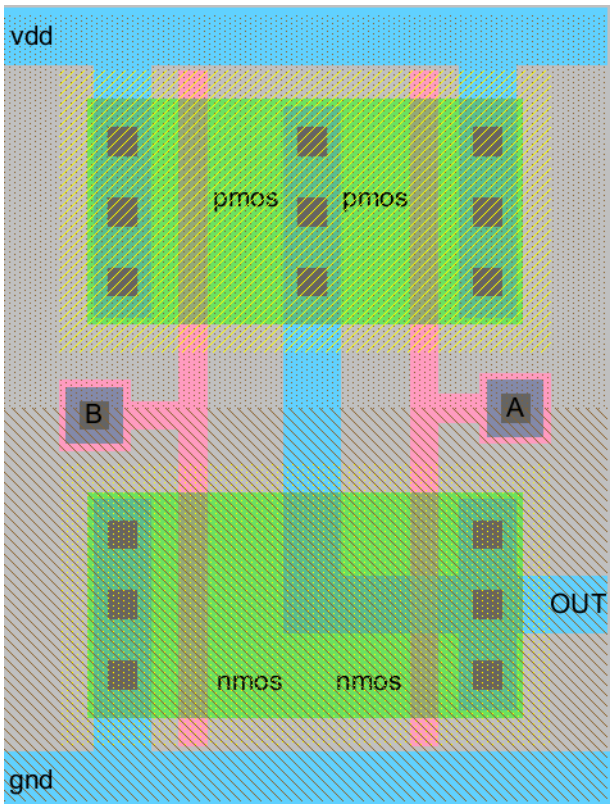

Figure 14: Layout of NAND2_2*X*

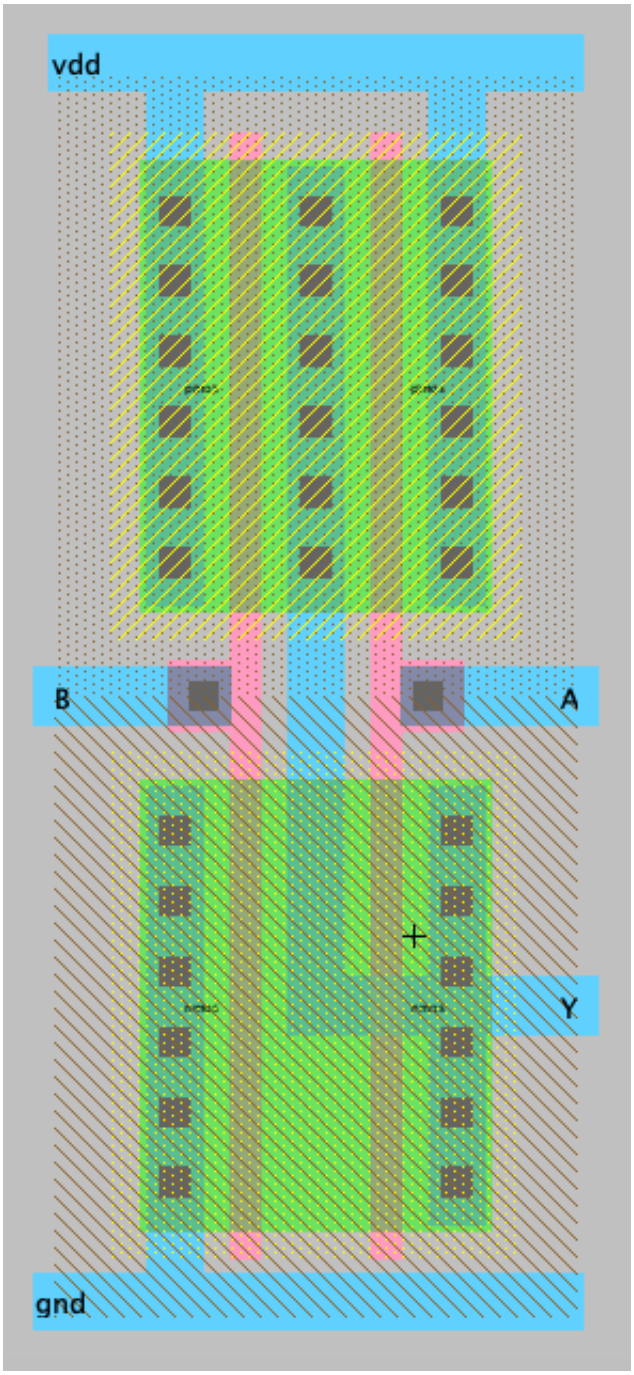

Figure 15: Layout of NAND2_4X

3.3 AND2

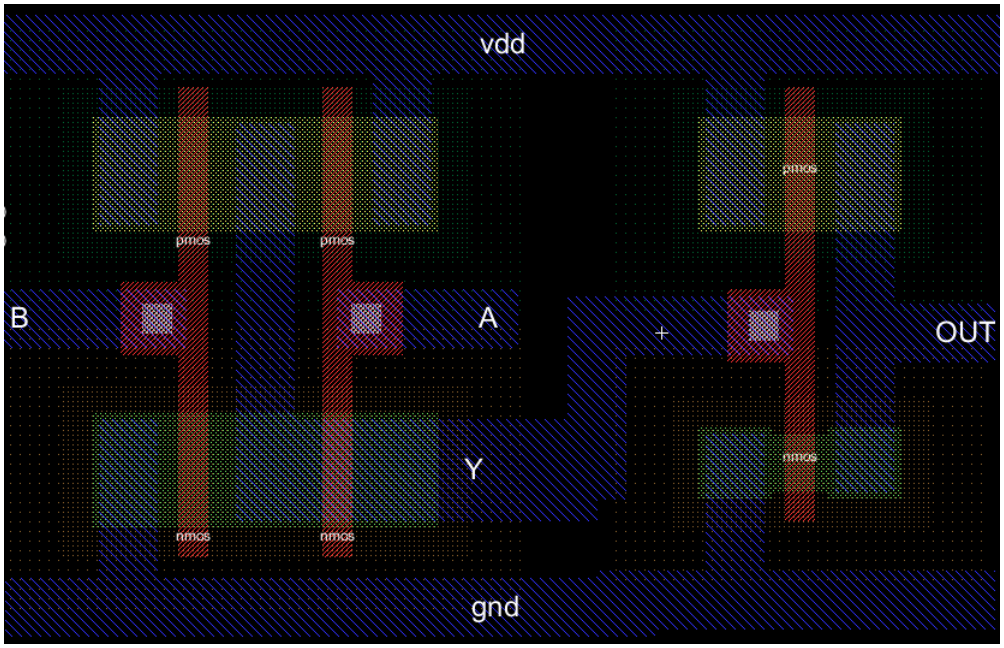

Figure 16: Layout of AND2_1*X*

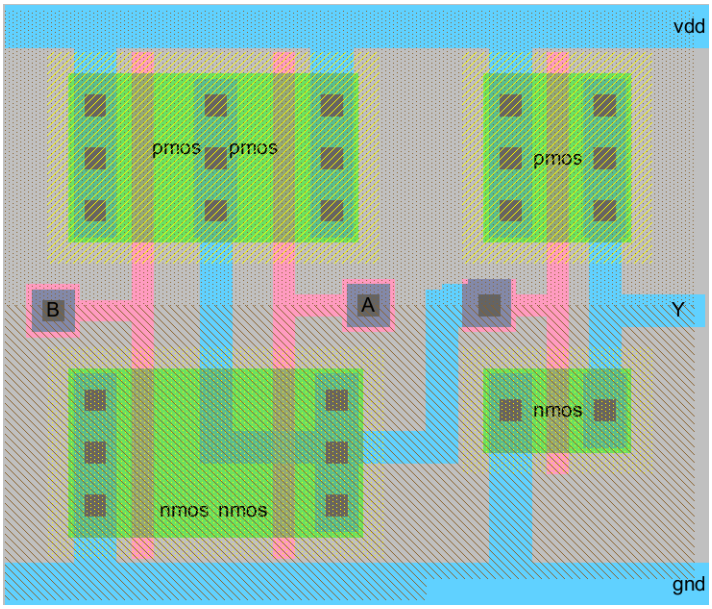

Figure 17: Layout of AND2_2*X*

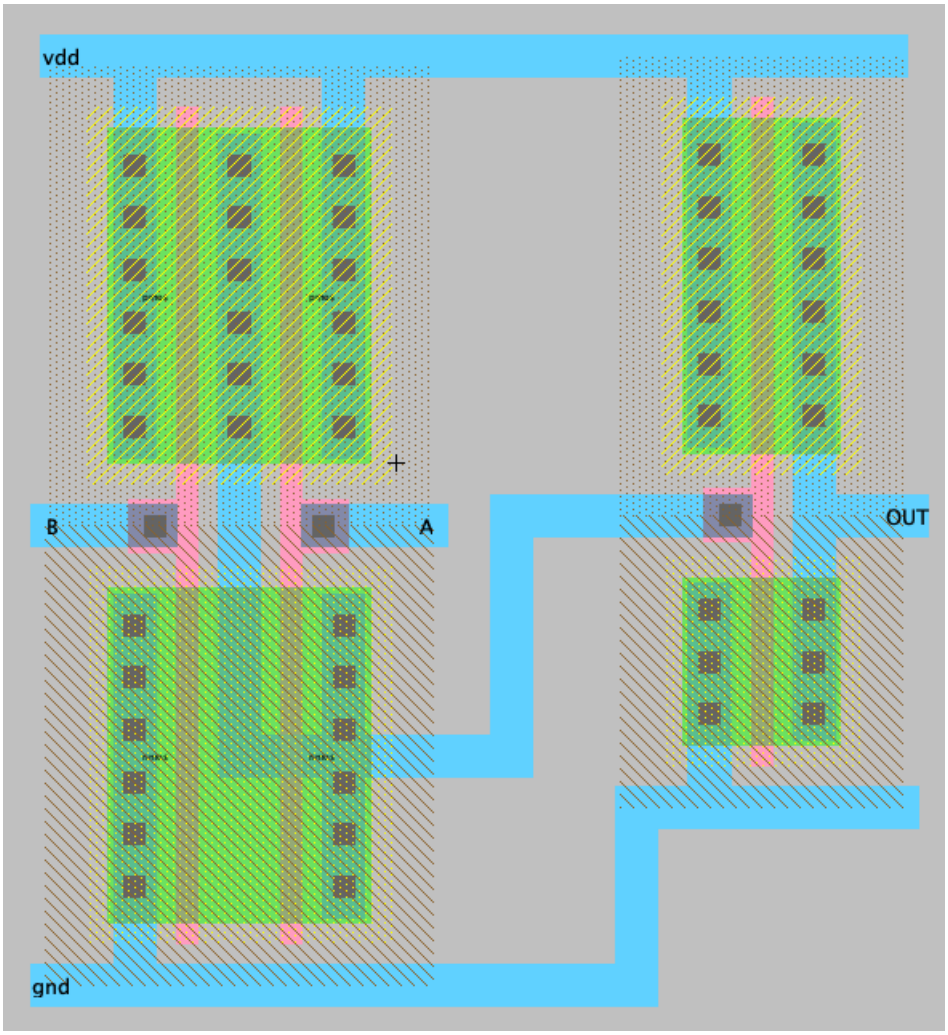

Figure 18: Layout of AND2_4*X*

4 Functional Simulation

Verification of Truth Table of the logic gates.

4.1 Inverter

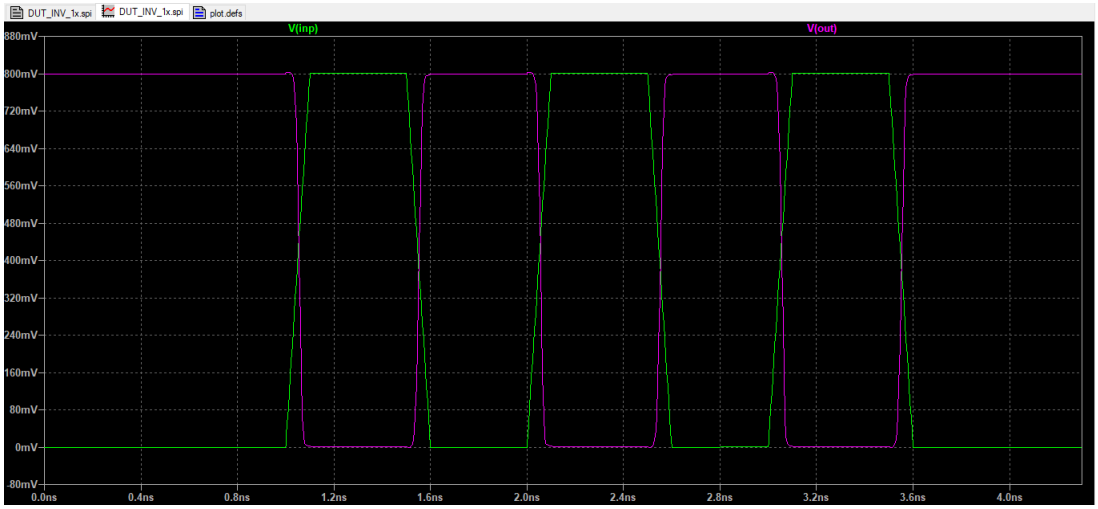

Figure 19: Functionality of Inverter

4.2 NAND2

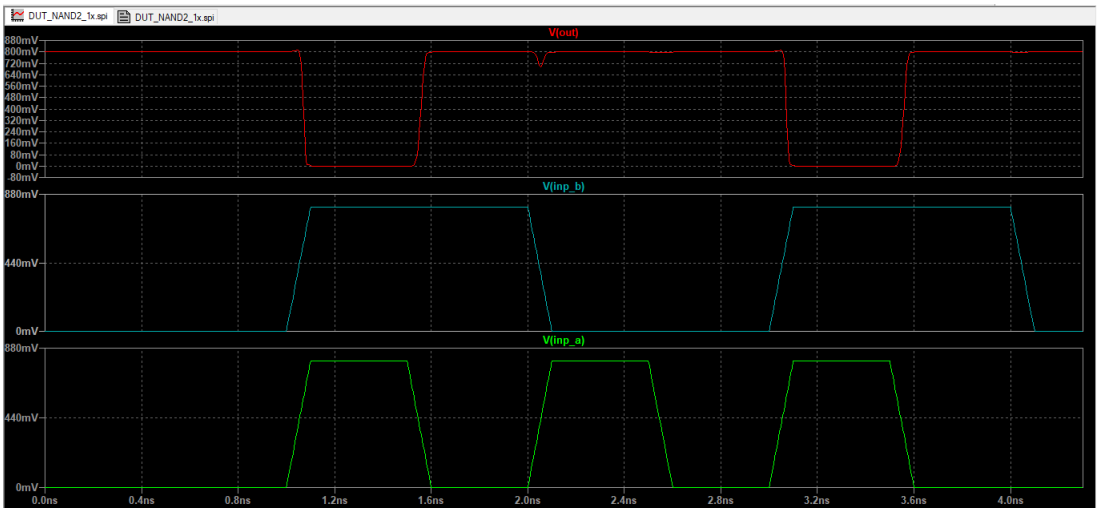

Figure 20: Functionality of NAND2

4.3 AND2

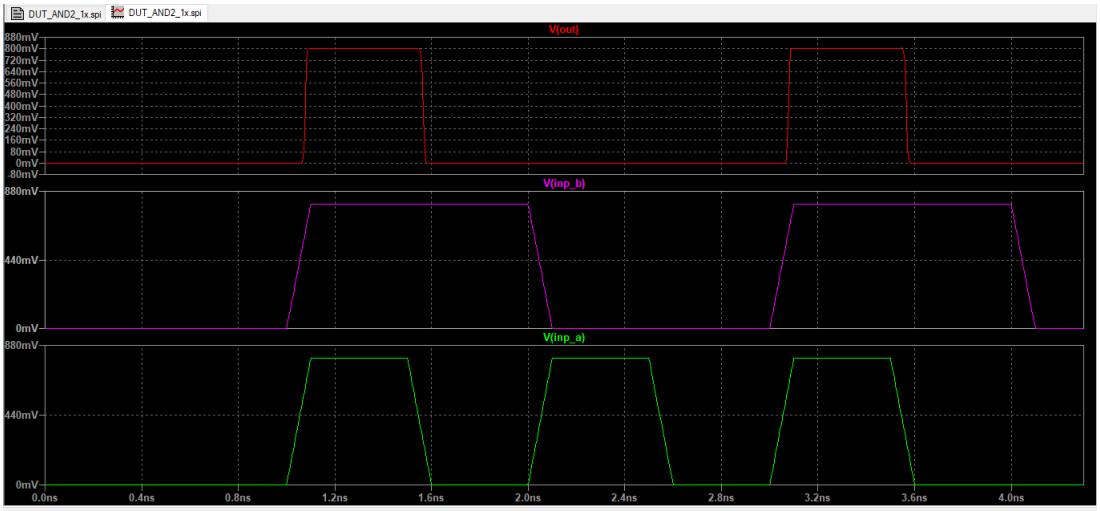

Figure 21: Functionality of AND2

5 DRC and LVS results

DRC and LVS results of the layouts

5.1 1X

```
================================9================================
Running DRC with area bit off, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 7 networks
0 errors and 0 warnings found (took 0.001 secs)
================================10================================
Running DRC with area bit off, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 11 networks
0 errors and 0 warnings found (took 0.003 secs)
================================11================================
Running DRC with area bit off, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 14 networks
0 errors and 0 warnings found (took 0.001 secs)
================================12================================
Hierarchical NCC every cell in the design: cell 'INV_1x{sch}'  cell 'INV_1x_layout{lay}'
Comparing: Assign1:INV_1x{sch} with: Assign1:INV_1x_layout{lay}
  exports match, topologies match, sizes not checked in 0.081 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.098 seconds.
================================13================================
Hierarchical NCC every cell in the design: cell 'NAND2_1x{sch}'  cell 'NAND2_1x_layout{lay}'
Comparing: Assign1:NAND2_1x{sch} with: Assign1:NAND2_1x_layout{lay}
  exports match, topologies match, sizes not checked in 0.06 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.061 seconds.
================================14================================
Hierarchical NCC every cell in the design: cell 'AND2_1x{sch}'  cell 'AND2_1x_layout{lay}'
Comparing: Assign1:AND2_1x{sch} with: Assign1:AND2_1x_layout{lay}
  exports match, topologies match, sizes not checked in 0.004 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.006 seconds.
```

Figure 22: DRC and LVS of 1X

5.2 2X

```
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 7 networks
Checking cell 'INVERTER_LAYOUT{lay}'
        No errors/warnings found
0 errors and 0 warnings found (took 0.109 secs)
================================3================================
Hierarchical NCC every cell in the design: cell 'INVERTER{sch}'  cell 'INVERTER_LAYOUT{lay}'
Comparing: EXPT1_2x:INVERTER{sch} with: EXPT1_2x:INVERTER_LAYOUT{lay}
  exports match, topologies match, sizes not checked in 0.032 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.047 seconds.
================================4================================
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 11 networks
0 errors and 0 warnings found (took 0.0 secs)
================================5================================
Hierarchical NCC every cell in the design: cell 'NAND2{sch}'  cell 'NAND2_LAYOUT{lay}'
Comparing: EXPT1_2x:NAND2{sch} with: EXPT1_2x:NAND2_LAYOUT{lay}
  exports match, topologies match, sizes not checked in 0.016 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.016 seconds.
================================6================================
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 15 networks
Checking cell 'AND2_LAYOUT{lay}'
        No errors/warnings found
0 errors and 0 warnings found (took 0.094 secs)
================================7================================
Hierarchical NCC every cell in the design: cell 'AND2{sch}'  cell 'AND2_LAYOUT{lay}'
Comparing: EXPT1_2x:AND2{sch} with: EXPT1_2x:AND2_LAYOUT{lay}
  exports match, topologies match, sizes not checked in 0.0 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.0 seconds.
```

Figure 23: DRC and LVS of 2X

5.3 4X

```
================================922================================
Hierarchical NCC every cell in the design: cell 'Inverter:inv{sch}'  cell 'Inverter:inverter__inv{lay}'
Comparing: Inverter:inv{sch} with: Inverter:inverter__inv{lay}
  exports match, topologies match, sizes not checked in 0.002 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.002 seconds.
================================923================================
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 7 networks
0 errors and 0 warnings found (took 0.002 secs)
================================924================================
Hierarchical NCC every cell in the design: cell 'NAND:NAND{sch}'  cell 'NAND:NAND{lay}'
Comparing: NAND:NAND{sch} with: NAND:NAND{lay}
  exports match, topologies match, sizes not checked in 0.005 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.006 seconds.
================================925================================
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 11 networks
0 errors and 0 warnings found (took 0.001 secs)
================================926================================
Hierarchical NCC every cell in the design: cell 'AND{sch}'  cell 'AND{lay}'
Comparing: AND:AND{sch} with: AND:AND{lay}
  exports match, topologies match, sizes not checked in 0.005 seconds.
Summary for all cells: exports match, topologies match, sizes not checked
NCC command completed in: 0.007 seconds.
================================927================================
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 14 networks
0 errors and 0 warnings found (took 0.001 secs)
```

Figure 24: DRC and LVS of 4X

6 Timing Simulation

From the following table, it can be seen that the increase in delays with respect to Fan-Out is almost linear, suggesting that the first order back-of-the-envelope calculations of input capacitance of a logic gate is quite accurate. The linear behaviour is more apparent from the following figure. Further, the delay at Fan-Out = 0 is due to the parasitic capacitance of the logic gate at the output.

6.1 Characterising Delays vs Fan-Out for NAND2_1X gate

Fan out	Rise Delay (ps)		Fall Delay (ps)	
	A to OUT	B to OUT	A to OUT	B to OUT
0	7.761	10.325	7.073	13.449
1	10.474	12.82	10.029	16.444
2	12.896	15.084	12.652	18.951
3	15.028	17.062	15.064	21.12
4	17.041	18.954	17.217	23.104
5	18.848	20.646	19.277	24.901
6	20.581	22.275	21.151	26.566
7	22.199	23.824	22.958	28.165
8	23.725	25.26	24.655	29.642

Table 1: Rise and Fall Delays vs Fan-Out of NAND2_1X gate.

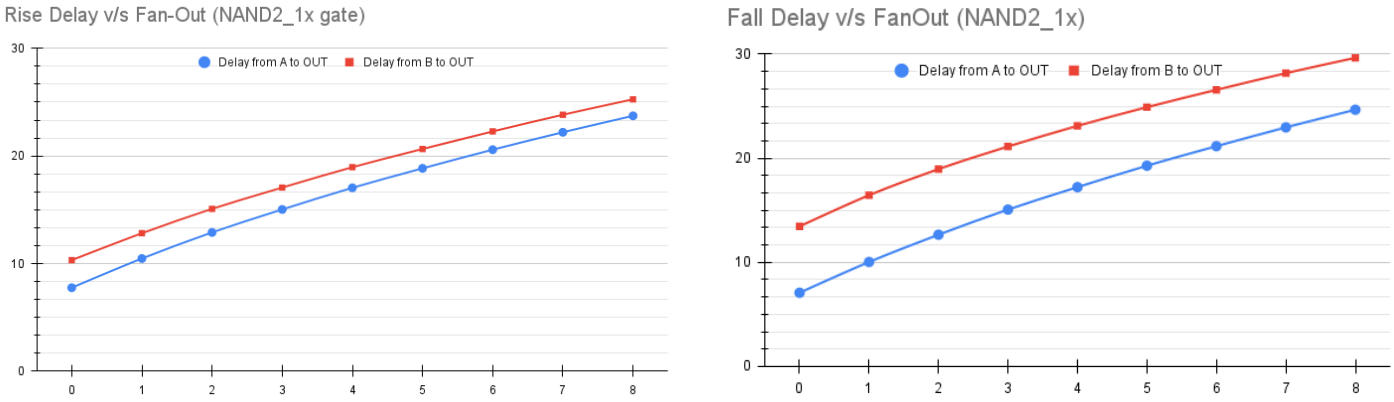

Figure 25: Rise and Fall Delays vs Fan-Out for the NAND2_1X gate

6.2 Characterising Delays vs Fan-Out for NAND2_2X gate

Fan out	Rise Delay (ps)		Fall Delay (ps)	
	A to OUT	B to OUT	A to OUT	B to OUT
0	7.579	10.133	7.019	13.338
1	10.311	12.681	10.057	16.396
2	12.718	14.923	12.743	18.943
3	14.884	16.945	15.163	21.157
4	16.864	18.802	17.387	23.144
5	18.697	20.531	19.452	24.963
6	20.411	22.157	21.386	26.645
7	22.468	23.669	24.002	28.225
8	23.979	25.158	25.697	29.729

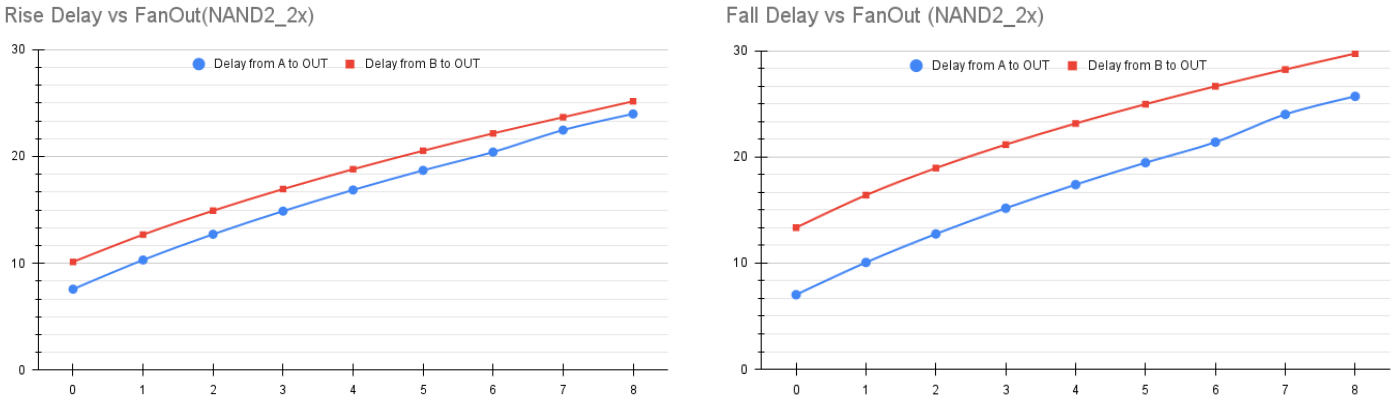

Figure 26: Rise and Fall Delays vs Fan-Out for the NAND2_2X gate

6.3 Characterising Delays vs Fan-Out for NAND2_4X gate

Fan out	Rise Delay		Fall Delay	
	A to OUT	B to OUT	A to OUT	B to OUT
0	7.486	10.025	6.9769	13.162
1	10.262	12.597	10.059	16.271
2	12.698	14.845	12.785	18.867
3	14.884	16.879	15.242	21.115
4	16.885	18.752	17.5	23.132
5	18.739	20.49	19.597	24.977
6	20.466	22.122	21.562	26.684
7	22.092	23.67	23.415	28.287
8	23.637	25.146	25.175	29.811

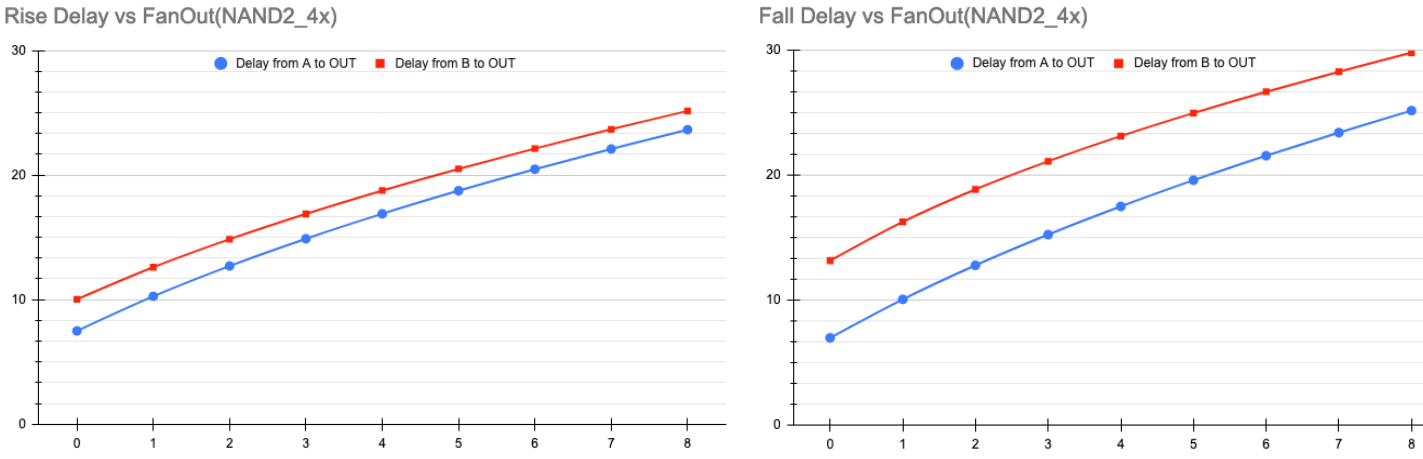

Figure 27: Rise and Fall Delays vs Fan-Out for the NAND2_4X gate

6.4 Some inferences from the above figures:

- The no-load delay is approximately the same for all three gate sizes. This is as expected from analysis- as the gate size increases by a factor of k, the effective resistance along the charging/discharging path reduces by a factor of k while the output capacitance increases by a factor of k. The overall delay ($\propto RC$) remains constant.

- The delay from input node A to the output node is consistently lower than the delay from input node B to output. This is because when input B is maintained at V_{DD}, the drain of the bottom NMOS transistor in the NAND2 gate is almost at 0 volts. Hence when input A is raised to V_{DD}, only one node (drain of the top NMOS transistor) has to be discharged to ground.
  On the other hand, when input A is maintained at V_{DD} and input B is raised from 0V to V_{DD}, the drains of both the NMOS transistors must be discharged to 0V, resulting in a larger delay.

★ ★ ★