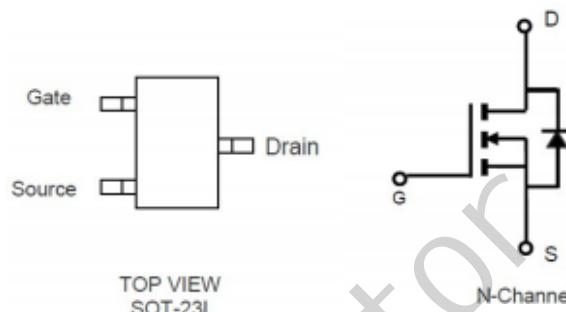


■ FEATURE

- ◆ 20V/4.5A, $R_{DS(ON)}=25m\Omega$ (typ.)@ $V_{GS}=4.5V$
- ◆ 20V/2.5A, $R_{DS(ON)}=55m\Omega$ (typ.)@ $V_{GS}=2.5V$
- ◆ 20V/2.0A, $R_{DS(ON)}=80m\Omega$ (typ.)@ $V_{GS}=1.8V$
- ◆ Super high design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and Maximum DC current capability
- ◆ Full RoHS compliance
- ◆ SOT23-3L package design



■ DESCRIPTION

The 2502 is the N-Channel logic enhancement mode power field effect transistor is produced using high cell density advanced trench technology.. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, and low in-line power loss are needed in a very small outline surface mount package.

■ APPLICATIONS

- ◆ Power Management
- ◆ Portable Equipment
- ◆ DC/DC Converter
- ◆ Load Switch
- ◆ DSC
- ◆ LCD Display inverter

■ ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ Unless otherwise noted)

Symbol	Parameter		Typical	Unit
V_{DSS}	Drain-Source Voltage		20	V
V_{GSS}	Gate-Source Voltage		± 10	V
I_D	Continuous Drain Current ($T_c=25^\circ C$)	$V_{GS}=10V$	4.5	A
	Continuous Drain Current ($T_c=70^\circ C$)		3.0	
I_{DM}	Pulsed Drain Current		20	A
I_S	Continuous Source Current (Diode Conduction)		1.5	A
P_D	Power Dissipation	$T_A=25^\circ C$	1.5	W
		$T_A=70^\circ C$	0.9	
T_J	Operation Junction Temperature		150	$^\circ C$
T_{STG}	Storage Temperature Range		-55~+150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient		90	$^\circ C/W$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress rating only and functional device operation is not implied

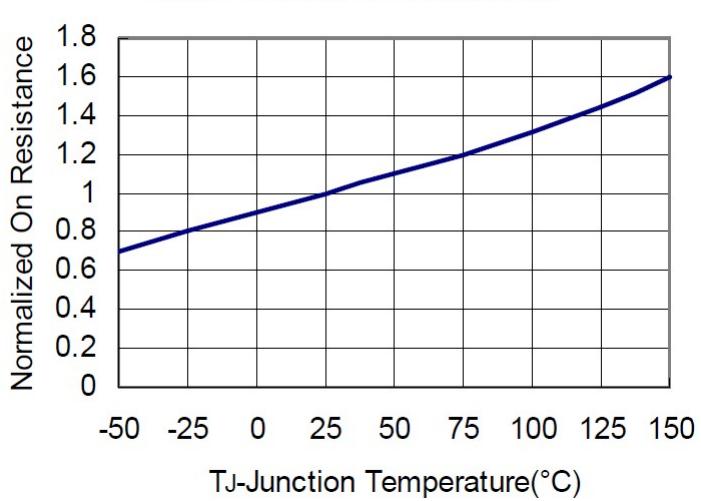
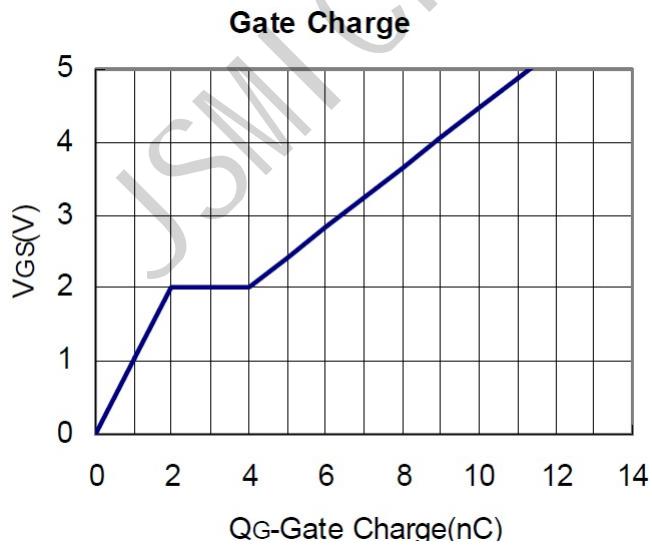
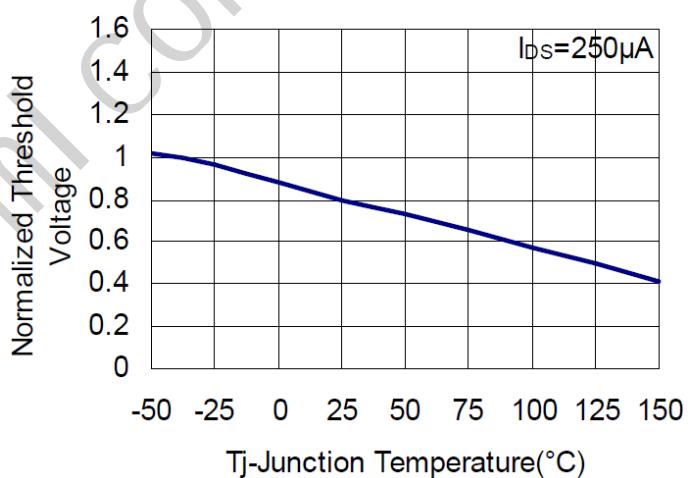
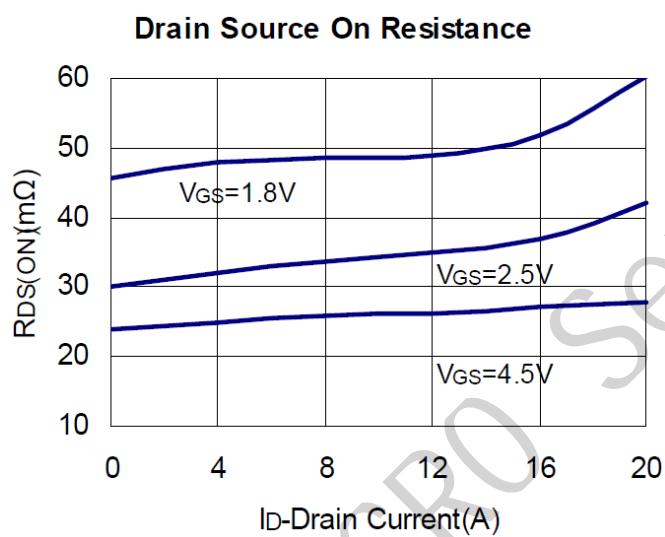
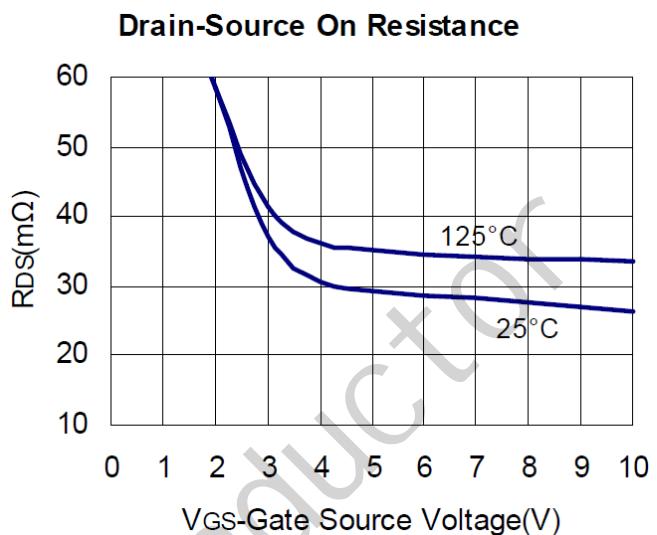
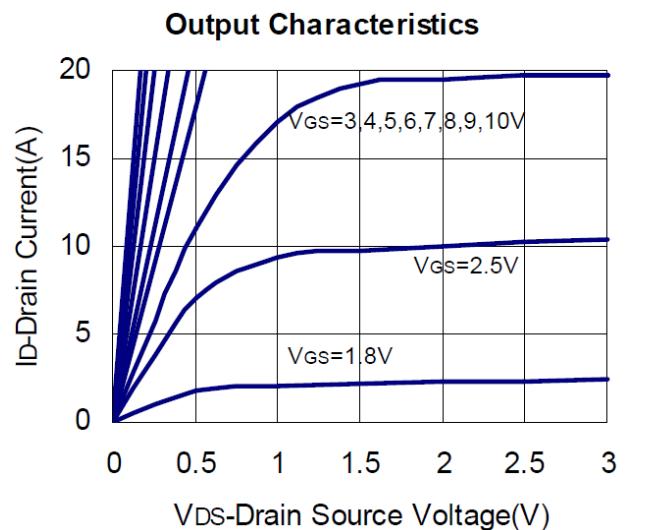
■ **ELECTRICAL CHARACTERISTICS**($T_A=25^\circ C$ Unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit	
Static Parameters							
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	20			V	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	0.5		1.0	V	
I_{GSS}	Gate Leakage Current	$V_{DS}=0V, V_{GS}=\pm 12V$			± 100	nA	
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=20V, V_{GS}=0$		1		uA	
		$V_{DS}=20V, V_{GS}=0$ $T_J=55^\circ C$		5			
$R_{DS(ON)}$	Drain-Source On-Resistance	$V_{GS}=4.5V, I_D=3.0A$	25	45		mΩ	
		$V_{GS}=2.5V, I_D=2.5A$	40	60			
		$V_{GS}=1.8V, I_D=2.0A$	65	90			
Source-Drain Diode							
V_{SD}	Diode Forward Voltage	$I_S=1.7A, V_{GS}=0V$		0.78	1.2	V	
Dynamic Parameters							
Q_g	Total Gate Charge	$V_{DS}=10V$ $V_{GS}=4.5V$ $I_D=5.0A$		11	13	nC	
Q_{gs}	Gate-Source Charge			1.45			
Q_{gd}	Gate-Drain Charge			2.3			
C_{iss}	Input Capacitance	$V_{DS}=10V$ $V_{GS}=0V$ $f=1MHz$		578		pF	
C_{oss}	Output Capacitance			116			
C_{rss}	Reverse Transfer Capacitance			96			
$T_{d(on)}$	Turn-On Time	$V_{DS}=10V$ $I_D=1.0A$ $V_{GEN}=4.5V$ $R_G=6\Omega$		14.5	25	nS	
T_r				42	62		
$T_{d(off)}$	Turn-Off Time			46	67		
T_f				34	43		

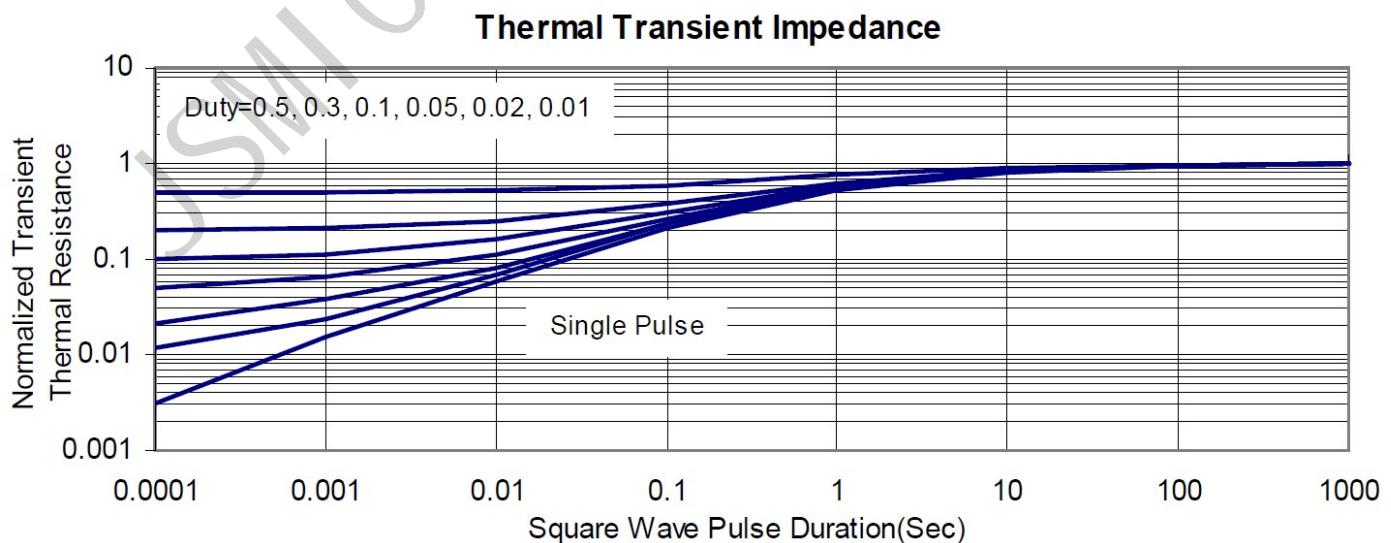
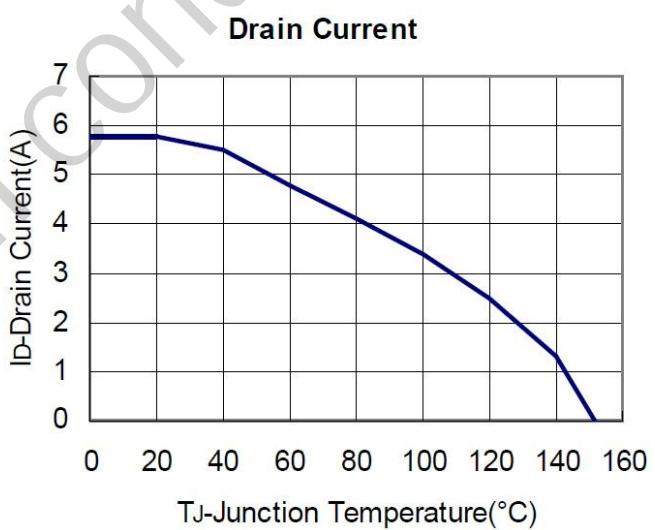
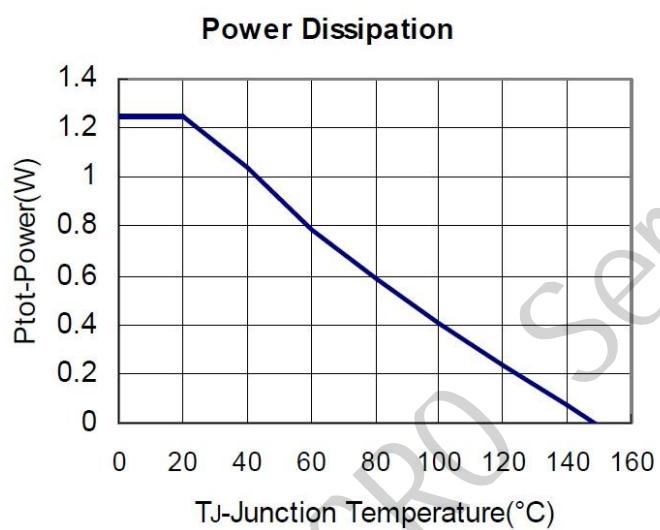
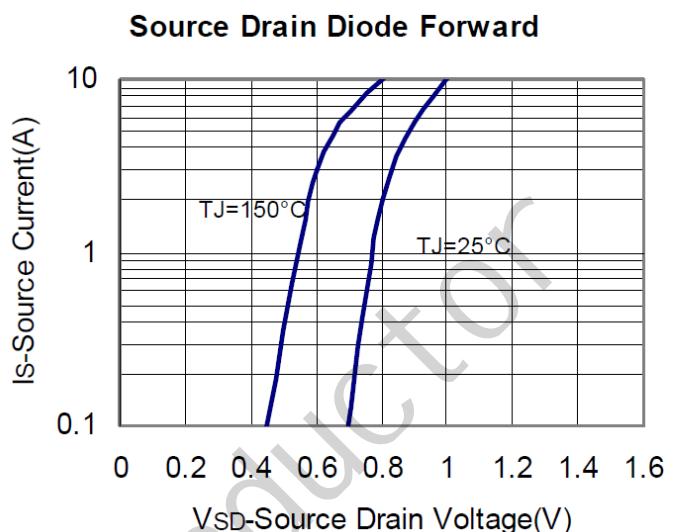
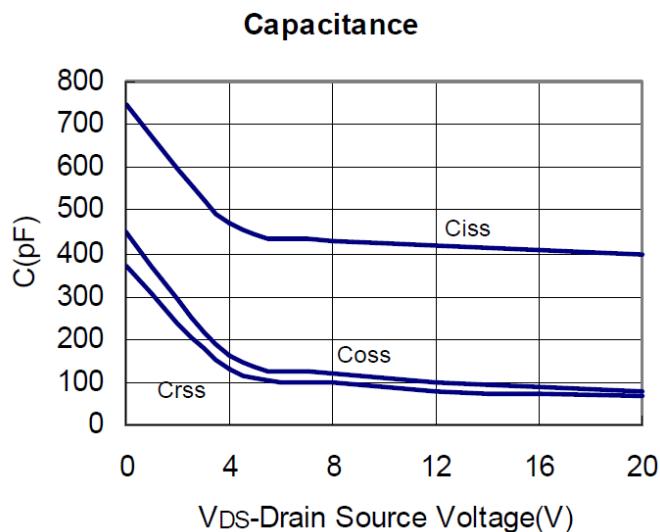
Note: 1. Pulse test: pulse width<=300uS, duty cycle<=2%

2. Static parameters are based on package level with recommended wire bonding

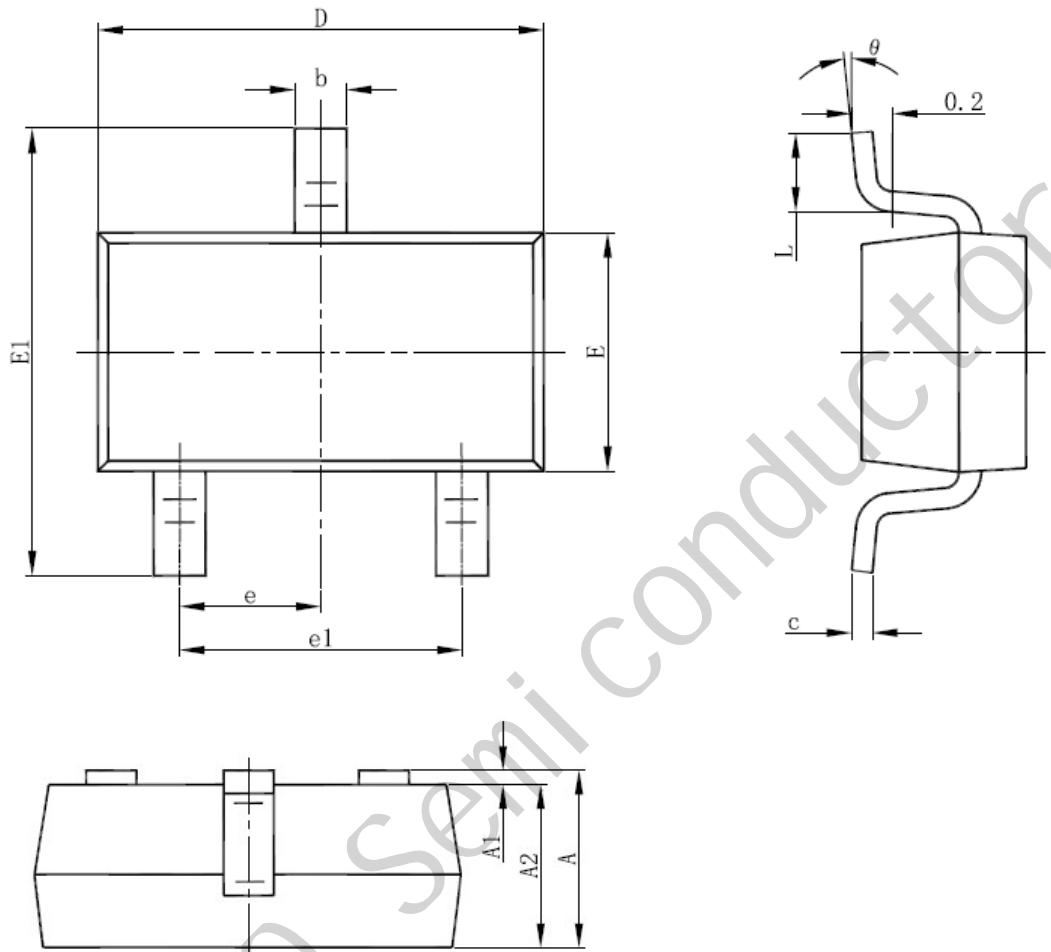
■ **TYPICAL CHARACTERISTICS (25°C Unless Note)**



■ **TYPICAL CHARACTERISTICS (continuous)**



■ SOT23-3L PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°