Design for a 16x9 Sequential Multiplier

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***Abstract*—Design provided for a sequential implementation of 16x9 magnitude multiplier, done on Verilog HDL.Main objective here is to reduce processing logic by time-sharing a single instance of processing logic to perform multiple processing operations (with different inputs) in different intervals of time (defined by different clock cycles) At the end of a clock cycle will need to store the result of processing done during the clock cycle – lest we lose them, because inputs to the processing logic will change at the start of the next clock cycle.**

***Index Terms*—Multiplier, Sequential, Memory, Control Unit, Accumulator, Adder, Verilog, Reset**

I. Circuit Design Details

The multiplication between (a) - Multiplicand (16 bit)and (b) - Multiplier (9 bit) is shown in fig(1). The method used here is shift and add method. An adder is used which is of the length 16 bits (equal to maximum of the lengths of (a) and (b)). Output of the adder is stored in a register bank, Accumulator(17 bit register - extra bit for carry). After each addition contents of the register bank is shifted right into another SIPO register bank(8 bit). The final (25 bit) output is the concatenated result of the outputs of the SIPO register(8 bit) and the Accumulator(17 bit).

A sequential circuit is a combinational circuit with memory. The output of the sequential circuit depends on present inputs and present state [past outputs]. The information stored in the sequential circuit represents the present state. The present state and present input will define the output of the next state.

The control table module is used to initiate all control signals. Fig.(2) describes the block diagram of the sequential multiplier, along with the control signals, which are sequenced using a sequencer block.

The block diagram explains the whole operation of the sequential multiplier. When RESET is high(active LOW reset operation), the partial product(PP) is generated using a logic block, which returns 0 if the LSB of (b), is 0, else returns (a). Then PP is transferred to the adder block which performs the addition of the accumulator([16:1]) and PP. The result is stored in the accumulator which then performs the right shift operation into the SIPO register for every positive edge of the clock. This process is continued for 12 pos-edges before obtaining the required product output.

Fig.(3) describes the changes in the 25 bit output(Prod) for the inputs,

(a) = in_Mx = 16'b1111111111111111

(b) = in_My = 9'b111111111

with every time step until finally it reaches the desired value on the 12 th positive clock edge. Thus,

Prod = 1fefe01 = 25'b1111111101111111000000001

II. Circuit Diagrams and Required Outputs

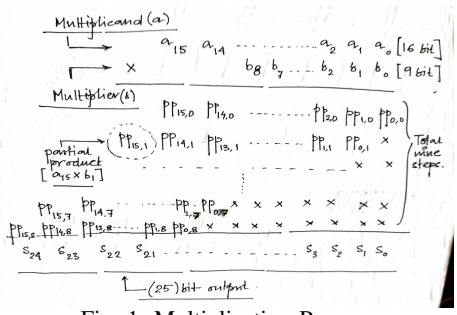

Fig. 1: Multiplication Process

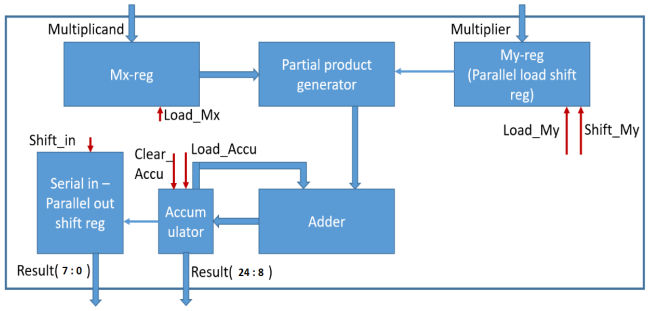

Fig. 2: Block diagram of 16x9 Sequential Multiplier

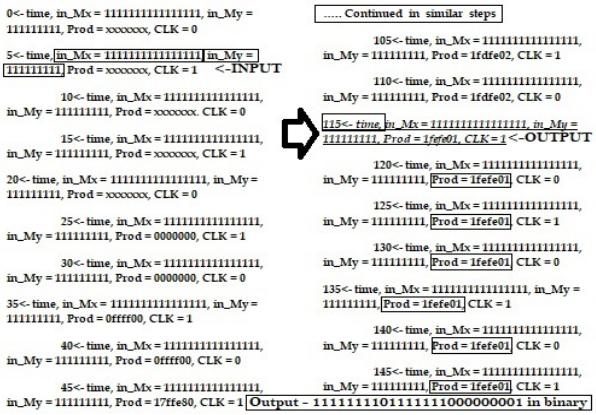

Fig. 3: Required 25 bit Output

References

[1] https://github.com/priyam4197/Sequential-multiplier-16x9
[2] https://digitalsystemdesign.in/sequential-multiplier/
[3] Neil Weste, Harris & Banerjee, CMOS VLSI Design: A Circuits and Systems Perspective, Edition, Pearson Education, Boston.