Design for an 8 bit Vedic Multiplier

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***Abstract*—Design provided for an 8 bit Vedic Multiplier circuit using the Vedic Mathematics (Urdhva Tiryagbhyam sutra) for generating the partial products. The partial product addition in Vedic multiplier is realized using carry-skip technique. An 8-bit multiplier is realized using four 4-bit multiplier and three ripple carry adders.**

***Index Terms*—Multiplier, Vedic, digital, 8bit, Adder**

I. Reference Circuit Details

The Vedic logic used is the "Urdhva Triyakbhyam Sutra". Urdhva – Triyakbhyam is the general formula applicable to all cases of multiplication of a large number by another large number. It means vertically and crosswise.

The method is explained for two, 2 bit numbers A and B where A = a1a0 and B = b1b0 as shown in Fig. 2. Firstly, the least significant bits are multiplied which gives the least significant bit of the final product (vertical). Then, the LSB of the multiplicand is multiplied with the next higher bit of the multiplier and added with, the product of LSB of multiplier and next higher bit of the multiplicand (crosswise). The sum gives second bit of the final product and the carry is added with the partial product obtained by multiplying the most significant bits to give the sum and carry. The sum is the third corresponding bit and carry becomes the fourth bit Of the final product.

The 2X2 Vedic multiplier module is implemented using four 2 - input AND gates two half-adders which is displayed in the block diagram in Fig. 2.

The 4x4 bit Vedic multiplier module is implemented using four 2x2 bit Vedic multiplier modules as discussed in Fig. 3.

Thus, following similar steps and using the fundamental of Vedic multiplication, taking four bits at a time and using 4 bit multiplier blocks we can perform the multiplication. The outputs of 4x4 bit multipliers are added accordingly to obtain the final product. Here total four 4-bit multipliers and three 8 bit Ripple-Carry Adders are required as shown in Fig. 4.

II. Reference Circuit Diagrams and Outputs

Fig. 1: Working of Bits

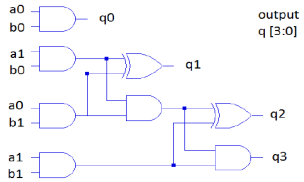

Fig. 2: Vedic 2x2 Multiplier Hardware Design

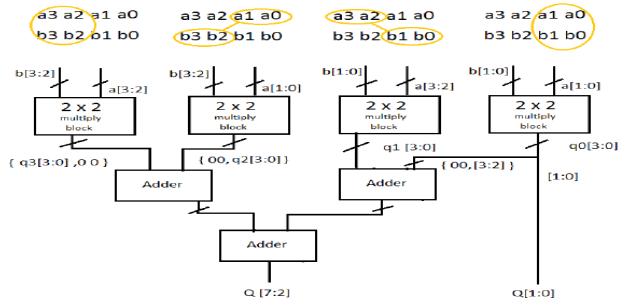

Fig. 3: Vedic 4x4 Multiplier Block Diagram

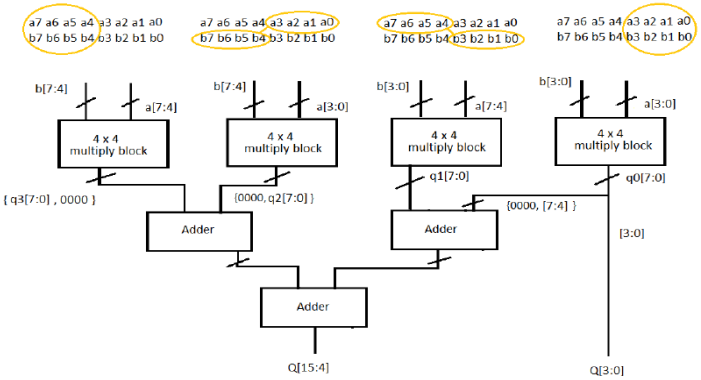

Fig. 4: 8-Bit Vedic Multiplier Block Diagram

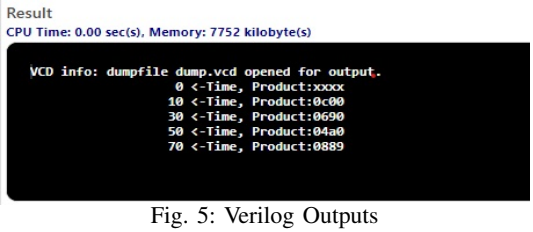

Fig. 5: Verilog Outputs

References

[1] Douglas A. Pucknell, Kamran Eshraghian, " Basic VLSI Design", PHI, Third Edition.
[2] Neil Weste, Harris & Banerjee, CMOS VLSI Design: A Circuits and Systems Perspective, Edition, Pearson Education, Boston.
[3] http://vlsinano.blogspot.com/2018/03/vedic-multiplier-verilog-code-and.html