Design and Implementation of Combinational Logic Based Electronic Buzzer Circuit using CMOS

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19 February 2022

***Abstract*—Design for a CMOS digital combinational logic based electronic buzzer circuit that selects the output based on the relative time of application of input. There are three independent digital input points, corresponding to which there are three outputs. The output corresponding to the first applied input becomes high from an initial low state and remains stable at that state, unaffected by any change in input signals from the other two input points. The output returns to its initial low state only when the first input signal is removed. The circuit is purely combinational as the outputs are independent of any clock signal.**

***Index Terms*—buzzer, digital, CMOS, combintional, logic**

I. Reference Circuit Details

The electronic buzzer circuit selects the output corresponding to the the input applied first. The other two inputs become don't cares, and do not affect the output until the first input signal becomes low again. The proposed circuit utilizes the properties of 'D-type Latch', also called transparent latch, without using the enable. The latch circuit composed of NOR gates and NOT gates, is slightly modified to meet the design requirements.

Fig. 3 represents the digital combinational logic design of the circuit using NOR and NOT gates. Fig. 1 and Fig. 2 represent the NOR and NOT gates using CMOS circuit which is comprised of two parts - the pull-up lattice composed of PMOS circuit and the pull-down lattice composed of NMOS circuit. PMOS circuit is connected to supply voltage VDD and NMOS circuit is connected to Ground terminal. Fig. 4 represents the various output waveforms. The inputs are taken as A, B and C with outputs as Q1, Q2 and Q3 corresponding to the respective inputs.

Q1 = (A'+QA+B+C)',
Q2 = (B'+QB+A+C)',
Q3 = (C'+QC+A+B)'

II. Reference Circuit Diagrams and Waveforms

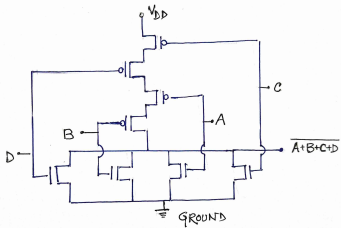

Fig. 1. CMOS 4 input NOR Gate.

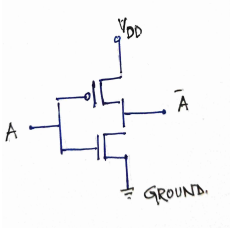

Fig. 2. CMOS 2 input NOT Gate

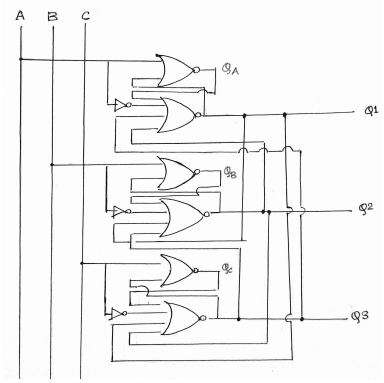

Fig. 3. Reference Combinational logic circuit design.

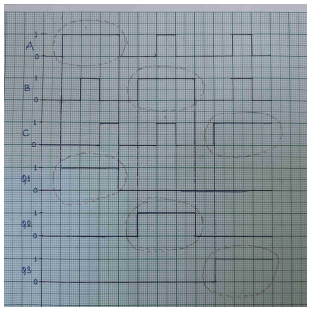

Fig. 4. Waveforms

References

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