Jitter Optimisation in a Generalised All-Digital Phase-Locked Loop Model

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***Abstract*—In this brief, we study jitter behavior in an event-driven self-sampled model of an All-Digital Phase-Locked Loop. We provide its steady-state analysis using simulations of a discrete-time model. We show that digital jitter, a function of two control parameters of the model, can be mapped onto a on-dimensional manifold and approximated via a simple function. The latter can be used to perform jitter optimisation under constraints for the control parameters. The verification is done through FPGA measurements and shows excellent agreement with the analytic approximation.**

***Index Terms*—All-digital phase-locked loop, digital jitter, synchronisation, control, piece-wise linear systems, event-driven systems.**

I. Introduction

PHASE-LOCKED loops (PLL) and their networks have a wide range of application in electronics and other fields, including frequency synthesis for wireless devices [1], DC motor drive [2], recovery of small signals [3], demodulation of tone signals for telecommunications and remote control [4], recovery of information [5], atomic force microscopy [4] and many others. In recent years, PLLs have become particularly important in the development of the Internet of Things (IoT), where these systems are used for communication. Due to a rapid development of this field and the introduction of several popular standards, studying such systems draw attention of many researchers, e.g., [6]–[10].

A PLL is also used as the source of clocking signals in complex Systems-on-a-Chips (SoCs). Modern SoCs require higher clocking frequencies and smaller propagation delays. A significant power consumption of such systems and increasing internal noise make their further application problematic. Currently, clocking in SoCs is implemented using All-Digital Phase-Locked Loops (ADPLL). Simpler implementation, easier adaptation to various applications and absence of amplitude noise made these systems a common design choice [11], [12].

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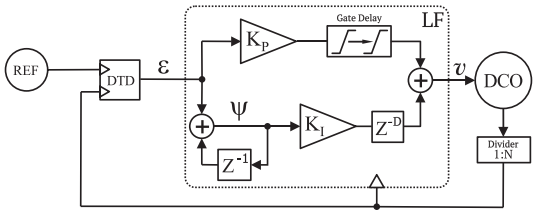


Fig. 1. An example of Type II second order ADPLL [20].

The self-sampled nature and even-driven dynamics of an ADPLL leads to a high degree of nonlinearity in it. Sometimes the method of describing functions can be applied for a class of switching systems, however, it can lead to erroneous conclusions [13] This, together with design dependent mathematical models, makes the analysis and optimisation of an ADPLL cumbersome. Nevertheless, for the case of the well-known ADPLL model presented in [14], a steady state analysis and optimisation can be performed [15]–[19]. The aim of this brief is to provide an insight into jitter dynamics in a more general ADPLL model.

This brief is organized as follows. In Section II, we present a discrete-time model of an even-driven self-sampled ADPLL. In Section III, we demonstrate the dynamics of the system in the phase plane using numerical simulations and investigate the jitter behavior of the system. In Section IV, we validate out theoretical predictions through a hardware model implemented on an FPGA. Finally, Section V summarises the study.

II. Statement of the Problem

The model of an ADPLL considered in this brief consists of the following blocks: Digital Time Detector (DTD), Loop Filter (LF) in the form of a Proportional-Integral Controller (PIC), Digitally Controlled Oscillator (DCO), and Frequency Divider (FD) (see Fig. 1). The DTD calculates the time intervals between rising edges of two input signals: the external reference signal and the divided signal arriving from the DCO. The corresponding error signal is processed by the PIC that tunes the frequency of the DCO. After passing through the FD, the signal is fed back to the DTD. Such a feedback minimises the phase error between the external reference signal and the divided signal. Although, the output clock is generated by the DCO, for the control loop the relevant output is the frequency-divided DCO signal. In this brief, we refer to the combination of DCO and FD as a local clock producing

the *local signal* as a meander of high and low voltage levels. The corresponding rising edges of the reference and local signals we define as the reference and local *events*.

An ADPLL is an asynchronous digital system. In such a system, the DTD changes its state at either reference or local events, whereas the controller updates its state only at a local event. The analytical description of such a behaviour is challenging, and there are only a few theoretical models known in the literature. One of the most known models is proposed in [14] and can be summarised as follows

$$\begin{cases} \tau_{k+1} = \tau_k - \mathrm{sgn}(\tau_{k-d}) - r\,\psi_{k-D}, \\ \psi_{k+1} = \psi_k + \mathrm{sgn}(\tau_{k+1}), \end{cases} \tag{1}$$

where $\tau_k \propto t_k^{\mathrm{R}} - t_k^{\mathrm{L}}$, the index k denotes k^{th} clocking cycle of both reference 'R' and local 'L' clock signals, t_k^{R} and t_k^{L} are corresponding time instances; $\varepsilon_k = \mathrm{sgn}(\tau_k)$ is the error signal at the DTD, $\mathrm{sgn}(\cdot)$ is the signum function, ψ_k is the integral error of the PIC. The parameter r is the ratio of the integral K_{i} and proportional K_{p} gains of the PIC, and D is the delay in the feedback loop. The index d distinguishes Type I ($d = D$) and Type II ($d = 0$) ADPLL as introduced in [14], [20].

The main assumption of the model (1) is its quasi-synchronous behaviour implying that the state of both the PIC and DTD changes within the same clocking cycle k of both the reference and local clocks. In the general case, such a one-cycle assumption may be violated due to conditional switching rules of the bang-bang detector described as a finite-state machine. To take this into account, one should improve the definition of the timing error through some integers p, q as $\varepsilon_k = \mathrm{sgn}(t_{k+p}^{\mathrm{R}} - t_{k+q}^{\mathrm{L}})$.

Let us consider the following examples of event sequences, where the numbers in brackets correspond to $[k, p, q]$, and the measurement intervals are highlighted by a figure bracket:

$$\underbrace{R_1L_1}_{[1\,0\,0]}\,\underbrace{R_2L_2}_{[2\,0\,0]}\,\underbrace{R_3L_3}_{[3\,0\,0]}\,\underbrace{L_4R_4}_{[4\,0\,0]}\,\underbrace{L_5R_5}_{[5\,0\,0]}, \tag{2a}$$

$$\underbrace{L_1R_1}_{[1\,0\,0]}\,\underbrace{L_2R_2}_{[2\,0\,0]}\,\underbrace{R_3R_4L_3}_{[3\,0\,0]}\,\underbrace{L_4R_5}_{[4\,1\,0]}, \tag{2b}$$

$$\underbrace{R_1L_1}_{[1\,0\,0]}\,\underbrace{L_2R_2}_{[2\,0\,0]}\,\underbrace{L_3L_4R_3}_{[3\,0\,0]}\,\underbrace{L_5R_4}_{[4\,0\,1]}. \tag{2c}$$

In the first sequence (2a), the error measurement is completed within a cycle of the same order k. Therefore, this sequence does not contradict the model (1) giving the error sequence $(---++)$. The second sequence (2b) has three reference events in a row ($R_2R_3R_4$) surrounded by two local time instances. Such a combination may occur when the local period T^{L} is at least twice bigger than the reference period T^{R}. As a result, the simple difference $t_k^{\mathrm{R}} - t_k^{\mathrm{L}}$ contradicts the detector's conditional switching rule, and a mismatch occurs. For the correct representation of the detector's error, the following time difference has to be used $t_5^{\mathrm{R}} - t_4^{\mathrm{L}} \mapsto \varepsilon = +1$ instead of $t_4^{\mathrm{R}} - t_4^{\mathrm{L}} \mapsto \varepsilon = -1$ which is the case for (1). The third sequence (2c) shows that the mismatch may occur even when the periods are relatively close, which is the case for two events of the same type in a row.

To resolve these issues, we introduced an event-driven ADPLL model in [21] which also takes into account the detector's quantisation function and intrinsic clock noises. This model was generalised to describe networks of ADPLLs and showed its consistency with hardware measurements [22], [23]. The model [21] reads:

$$\begin{cases} F_n^{\mathrm{L}} = F_{\mathrm{c}}^{\mathrm{L}} + \Delta F_{\mathrm{DCO}}(K_{\mathrm{p}}\varepsilon_n + K_{\mathrm{i}}\psi_n), \\ \eta_{n+1} = (\frac{1}{2F_n^{\mathrm{L}}\zeta_n^{\mathrm{L}}} + \eta_n)\theta^-(\eta_n) + (\eta_n - \frac{1}{2F_n^{\mathrm{R}}\zeta_n^{\mathrm{R}}})\theta^+(\eta_n), \\ \xi_{n+1} = (\frac{1}{2F_n^{\mathrm{L}}\zeta_n^{\mathrm{L}}} - \eta_n)\theta^-(\eta_n) + (\eta_n + \frac{1}{2F_n^{\mathrm{R}}\zeta_n^{\mathrm{R}}})\theta^+(\eta_n), \\ m_{n+1} = \frac{m_n}{2} + \mathrm{sgn}(\eta_n)(1 - \frac{m_n^2}{2}), \\ \tau_{n+1} = m_n\tau_n + m_{n+1}(\xi_{n+1} - |\eta_{n+1}|), \\ \varepsilon_{n+1} = Q_\tau(\tau_n, \tau_{\mathrm{TDC}}, N_{\mathrm{TDC}}), \\ \psi_{n+1} = \psi_n + \theta^-(\eta_n)\varepsilon_n, \\ t_{n+1} = t_n + \xi_n - |\eta_n|. \end{cases} \tag{3}$$

The variables and parameters of this model are as follows. The index n denotes the number of an event ('R' or 'L') in the chronological order, $F_n^{\mathrm{L,R}}$ are the frequencies of the local and reference clocks, η_n and ξ_n are the auxiliary variables aimed to describe the causality in the DTD. The DTD is described through m_n, τ_n. The sign of η_n indicates the leading clock: the local clock leads if $\eta_n < 0$, and the reference clock leads if $\eta_n > 0$ respectively. The proportional and integral errors are ε_n and ψ_n. Note that ψ_n updates only at the local event which is described by the Heaviside step function of negative argument $\theta^-(\eta_n) = \theta^+(-\eta_n)$. Log-normal random variables $\zeta_n^{\mathrm{L,R}} = \exp[\mathrm{N}(0, \sigma_{\mathrm{L,R}})]$ describe intrinsic thermal noise of the reference and local oscillators, where σ_{L} and σ_{R} are the corresponding standard deviations. However, flicker noise can be also taken into account if the corresponding random process is considered [24].

The parameters of the DCO are: F_{c} is the DCO central frequency, ΔF_{DCO} is the DCO gain, and K_{p} and K_{i} stand for the proportional and integral gain factors. The parameters τ_{TDC} and $2N_{\mathrm{TDC}}$ are the time resolution step and the total number of steps in the TDC, which is characterised by the quantisation functions Q_τ as

$$Q_\tau(\tau) = \mathrm{sgn}(\tau)\min(\lceil|\tau|/\tau_{\mathrm{TDC}}\rceil, N_{\mathrm{TDC}}). \tag{4}$$

Here $\lceil\cdot\rceil$ is the ceiling rounding function. Without the loss of generality, the initial conditions can be chosen as: $\tau_0 = 0$, $\varepsilon_0 = 0$, $\psi_0 = 0$ and $m_0 = 0$, with η_0 and ξ_0 depending on the initial phases of the local and reference signals. Delay $D = 1$ is implicitly included in the way how equations (3) are written down. Firstly, frequency (3.1) is updated (note the index n), and then the integral error ψ_{n+1} is updated.

The numerical simulation of model (3) is ultra fast due to its event-driven nature, and we use it for studying the dynamics and jitter behaviour of an ADPLL in the next sections.

III. Modelling Results

A. Phase Planes

In Fig. 2, numerical simulations of the model (3) are carried out for two values of the TDC resolution ($N_{\mathrm{TDC}} = 1$ and 7). When $N_{\mathrm{TDC}} = 1$, the implementation of the DTD is equivalent to the sgn−function detector. For simplicity, in this section we consider only quantisation noise and set $\sigma_{\mathrm{L,R}} = 0$. The parameters used to generate simulations are shown in the legends to the figures. We demonstrate the dynamics of the ADPLL in the phase plane spanned by the state variables $(\tau_n, F_n^{\mathrm{L}} - F^{\mathrm{R}})$ where the reference frequency is constant.

Figures 2(a) and (b) show the dynamics of the system for the case $N_{\mathrm{TDC}} = 1$ while Figs. 2(d) and (e) show the dynamics

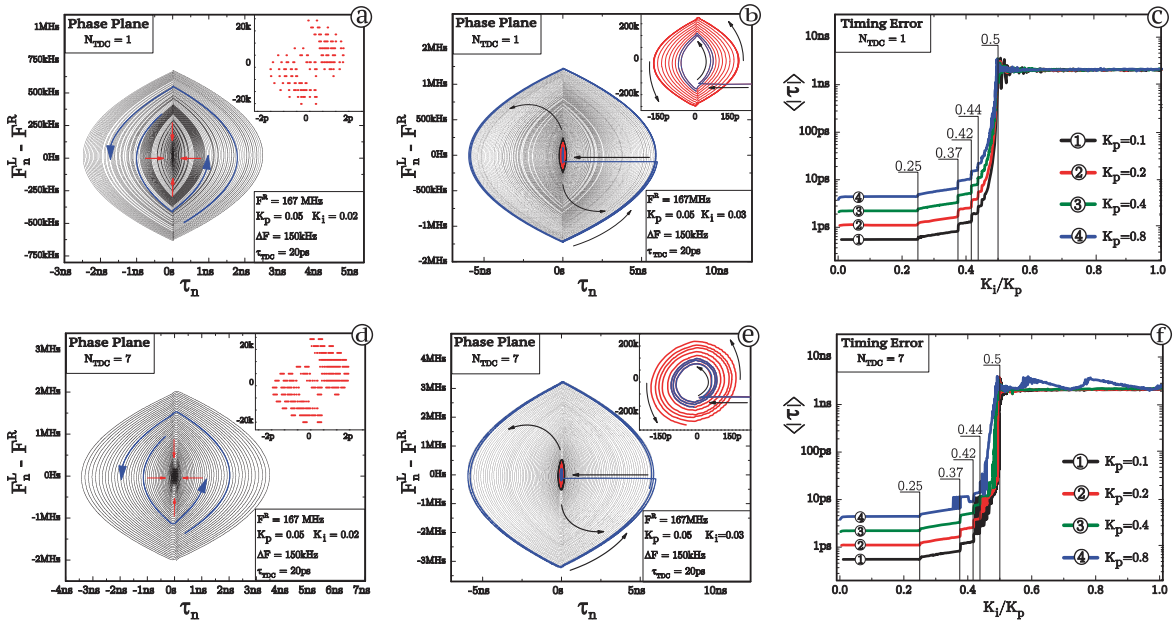


Fig. 2. Dynamics of the ADPLL for two cases of the detector resolution, $N_{\mathrm{TDC}} = 1$ (subfigures (a), (b) and (c)) and 7 (subfigures (d), (e) and (f)) depending on the set of control parameters K_{p} and K_{i}. Figures (a) and (d) show that the studied ADPLL is capable of tracking the reference signal and all the trajectories flow into an attractor while figures (b) and (e) show an unstable case. The magnitude of the timing error is presented in figures (c) and (f).

for $N_{\mathrm{TDC}} = 7$. One can see that in both cases the gains K_{p} and K_{i} affect the system significantly. For $K_{\mathrm{i}}/K_{\mathrm{p}} < 0.5$, the ADPLL operates in the phase tracking regime (Figs. 2(a) and (d)). For this case, the system is characterised by an attractor depicted in upper right corner of each figure. The width of the attractor represents the magnitude of the timing error, which is around $\tau_{\max} \approx 2$ ps. This value corresponds to $\approx 0.05\%$ of the average period. The attractors are similar for both cases because the magnitude of the error ε rarely exceeds 1. So, for the chosen parameters, in the phase tracking regime, 1-step and 7-steps DTDs behave similarly.

The dynamics in the phase plane become more complex if $K_{\mathrm{i}}/K_{\mathrm{p}} > 0.5$ (Figs. 2 (b) and (e)). When a point on a phase trajectory reaches the right (or left) edge of the attractor, it jumps into the vicinity of the attractor's center. After that, it starts to diverge until next drop down. The maximal timing error is $\tau_{\max} \approx 6$ ns that corresponds to the period of reference signal. Note that the corresponding PI control for analogue circuit is a second-order system which is stable for all positive K_{i} and K_{p}.

The difference between the phase plots presented above can be quantified using the averaged timing error $\langle|\tau|\rangle$ that describes the measure of the jitter produced by the ADPLL. It can be described by averaging the absolute value of the timing error τ over a long period of time:

$$\langle|\tau|\rangle = \lim_{t\to\infty} t^{-1} \int_0^t |\tau(t')|\, dt'. \tag{5}$$

The dependence of the average timing error $\langle|\tau|\rangle$ on the control parameters is shown in Figs. 2(c) and (f). It can be clearly seen that the timing error can be minimal if an appropriate ratio of $K_{\mathrm{p}}/K_{\mathrm{i}}$ is chosen. On the contrary, the timing error is very large when $K_{\mathrm{i}}/K_{\mathrm{p}} > 0.5$. There are a number of specific points where $\langle|\tau|\rangle$ as a function of $K_{\mathrm{i}}/K_{\mathrm{p}}$ experiences discontinuity jumps, and these points are the same for all K_{p}. The points likely appear as the result of cascade bifurcations. The analysis of bifurcations is out of scope of this brief, however, it could be an interesting subject of independent research.

B. Jitter Behaviour

In Figures 2(c) and (f), the values of K_{p} are chosen from the set $0.1 \cdot 2^n$ where $n = 0, 1, 2$ and 3 are selected intentionally. It can be seen that in a log scale the asymptotic behaviour of the timing error is proportional to $\sim K_{\mathrm{p}}$ as $K_{\mathrm{i}}/K_{\mathrm{p}} \to 0$. A closer look at the timing error $\langle|\tau|\rangle/K_{\mathrm{p}}$ versus $K_{\mathrm{i}}/K_{\mathrm{p}}$ reveals that it can be mapped approximately onto a single line $J(x)$

$$\langle|\tau|\rangle = K_{\mathrm{p}}\, J(K_{\mathrm{i}}/K_{\mathrm{p}}) \tag{6}$$

for all positive K_{i} and K_{p} under the condition that $K_{\mathrm{i}}/K_{\mathrm{p}} < 0.5$. This map is shown in Fig. 3(a) as a scatter plot, where each colour point represents the value of K_{p}. If the intrinsic DCO noise is added to the system (see Fig. 3(e) and (g)), the timing error still follows the trend of the proposed smooth line. However, it is less accurate for small gains K_{p}, and it is shown by the red dots, deviating somewhat from the curve.

By investigating the behaviour of function $< |\tau| >$ in the vicinity of $K_{\mathrm{i}}/K_{\mathrm{p}} = 0.5^{-}$ in a double-log scale, one can agree that the function $J(x)$ can be approximated as

$$J(x) = J_0 a^{km} (a^k - x^k)^{-m}, \tag{7}$$

where a, J_0, m and k are constants. In all cases, $a = 0.5$, and particular J_0, m and k are shown in the legends of the Fig. 3. This function gives a very good match with simulation results and can be used to describe both, approximate behaviour of ADPLL jitter and its lower bound as a function of control parameters.

The proposed approximation for jitter can used to minimise ADPLL jitter through optimisation of PI control parameters. In

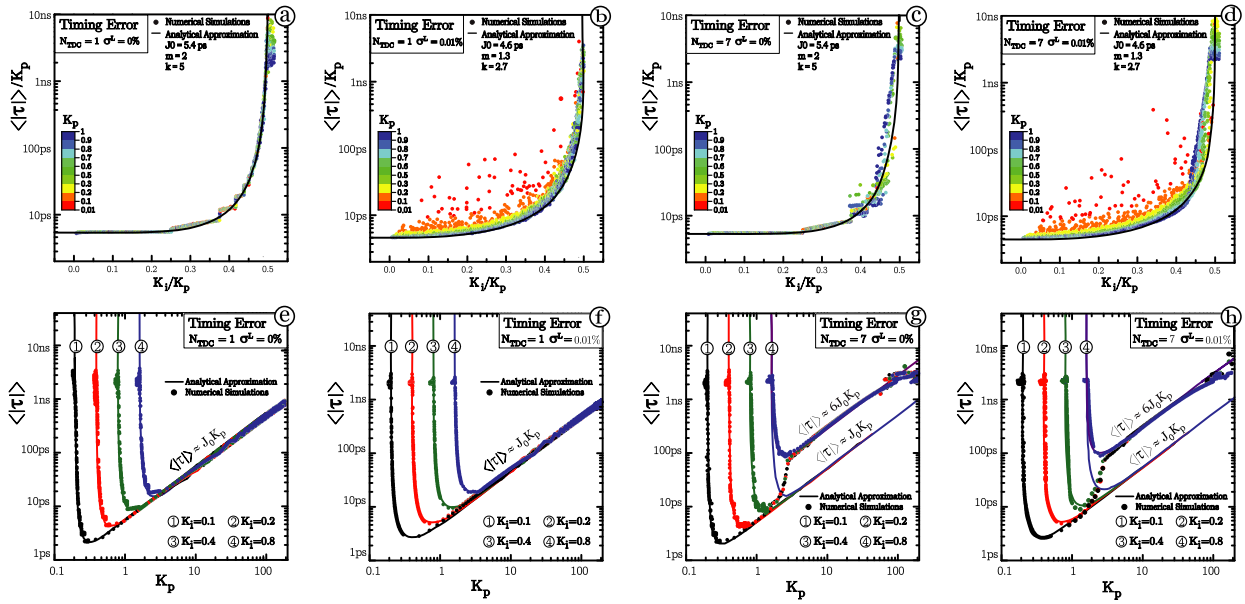


Fig. 3. Jitter behaviour of the ADPLL. Figures (a, e, c, g) correspond to the simulations with no noise in the reference signal or the DCO, whilst the simulations shown in figures (b, g, d, h) use weak DCO noise distributed according to the log-normal distribution with a zero mean and standard deviation of 0.01% of the period. The graphs for $N_{\mathrm{TDC}} = 1$ (figures (a), (b), (e) and (f)) and $N_{\mathrm{TDC}} = 7$ (figures (c), (d) ,(g) and (h)) show no significant difference implying no significant effect of the TDC resolution on the dynamics of the ADPLL.

Figs. 3(e-h) it is shown that for a given frequency acquisition rate (which is proportional to K_{i}) one can minimise the timing error (6) subject to K_{p}. By taking the derivative of (6) with respect to K_{p}, we get

$$K_{\mathrm{i}}/K_{\mathrm{p}}^{\mathrm{opt}} = a(1+mk)^{-\frac{1}{k}}. \tag{8}$$

A more general class of optimisation can also be considered through conditional extrema of (6) with given constraints on K_{i} and K_{p}.

The dependence of jitter on K_{p} is shown in the bottom row of Fig. 3 for different values of K_{i}. The dots correspond to the simulation results while the solid lines to the approximation introduced by expressions (6) and (7). It can be seen that for all the plots the dependence of $\langle|\tau|\rangle$ on K_{p} has a minimum at a specific $K_{\mathrm{p}}^{\mathrm{opt}}$. Its position changes linearly on K_{i} in accordance to the suggested approximation. The parameters J_0, m and k are shown in the legends. For a 7-step detector, the dependence becomes more complex due to the DTD quantisation function. However, when K_{p} becomes large, the averaged absolute value of the timing error approaches $\approx N_{\mathrm{TDC}} \cdot \tau_{\mathrm{TDC}}$, and the detector's behaviour resembles that of a one-step (sign-function) detector. Note that τ_{TDC} affects the jitter behaviour as well. When τ_{TDC} approaches zero, the quantised error is $\pm N_{\mathrm{TDC}}$. In the opposite case, when τ_{TDC} approaches infinity, the DTD acts like a signum-detector with $\varepsilon_n = \pm 1$.This is indirectly incorporated into the value K_p that determines jitter.

IV. FPGA Validation

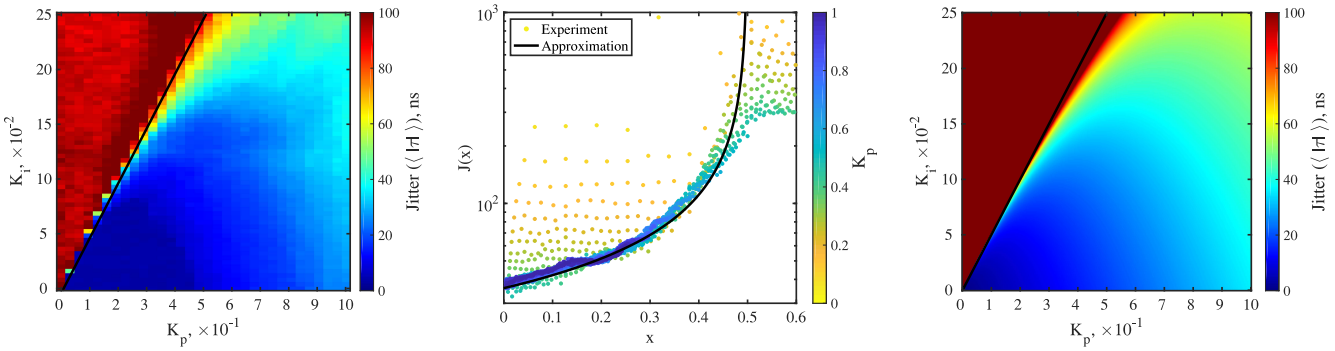
To validate our results, we have performed jitter measurements from an ADPLL model implemented on a Field-Programmable Gate Array (FPGA). This choice is motivated by better accessibility and controlability of all blocks of ADPLL. The methodology of ADPLL modelling on FPGA is described in detail in [23]. For this brief, we have designed and carried out experiments to verify the proposed jitter model. The parameters of the FPGA implementation are shown in Tab. I.

TABLE I
Parameters of the FPGA Implementation

Parameter	Value	Parameter	Value
DCO period range,	178–274 ns	ΔT_{DCO}	1.5 ns
Reference period,	200 ns	τ_{TDC}	1.0 ns
Clock noise, $\sigma_{\mathrm{L(R)}}/T_{\mathrm{L(R)}}$	0.1%	N_{DTD}	11

For the measurements, we use the plane of parameters $(K_{\mathrm{p}}, K_{\mathrm{i}})$ consisted of 32×64 points, where $K_{\mathrm{p}} = (0, 1 \ldots, 31)/32$ and $K_{\mathrm{i}} = (0, 1 \ldots, 63)/256$. The sweep through the plane of parameters is controlled by a MATLAB-to-FPGA programming interface. The output signal of the local clock is connected to an oscilloscope having a sampling time of 0.5 ns. The measurements from the oscilloscope are processed in MATLAB which returned the average timing error $\langle|\tau|\rangle$. For each measurement, the total number of sampling points is 4 MS, which covered around 10^4 periods of the reference signal.

The results of jitter's measurements are shown in Fig. 4(a). From the figure, one can see that jitter rapidly increases when K_{i} exceed $0.5K_{\mathrm{p}}$, as it was mentioned in Section III. When a jitter level with a constant K_{i} is considered, one can see that the dependence repeats patterns which are shown in the bottom row of Fig. 3. Namely, when K_{p} increases, jitter drops down, passes its minimum value, and increases again. By applying the reduction transform (6) and (7) with parameters $J_0 = 35$, $a = 0.5$, $k = 1$, $m = 0.7$, jitter from Fig. 4(a) was mapped approximately onto the line shown in Fig. 4(b). From the figure it is seen that the approximation is less accurate for small K_{p}, which was the case of ADPLL with relatively high intrinsic



(a) FPGA Measurement results (b) Map reduction (c) Approximation from the map reduction

Fig. 4. Jitter dependence on proportional K_p and integral K_i gains. The upper region from the black line $K_\mathrm{i} = 0.5K_\mathrm{p}$ in Figs. (a,c) corresponds to desynchronised regime.

noise shown in Figs. 3(b) and (d). Finally, Fig. 4(c) shows the reconstruction of jitter as a function of $(K_\mathrm{p}, K_\mathrm{i})$ from $J(x)$ described above, which is consistent with measurements from Fig. 4(a). A bias of approx. 15 % for all range of parameters can be due to the tolerances during the fitting of the $J(x)$ function. Nevertheless, the trend in the two maps are very close, and that allows one to perform a system optimisation.

V. Conclusion

In this brief we investigated the dynamics of an ADPLL described by model (3). This model is most general to describe the system in frequency acquisition, phase acquisition and phase tracking regimes. We showed that the structure of ADPLL's attractor dramatically depends on the set of control parameters. Namely, the attractor that corresponds to a synchronous regime rapidly collapses when $K_\mathrm{i} > K_\mathrm{p}/2$. To quantify the measure of synchronicity, we used the average timing error (jitter). We showed that the jitter, as a function of $K_\mathrm{p}, K_\mathrm{i}$, can be mapped onto a one dimensional line. This model would allow one to quickly find some initial estimate of the optimal parameters. A fine tuning can be performed by more accurate simulations in Cadence using the results of this model as the initial seed.

References

[1] M. Salarpour, F. Farzaneh, and R. B. Staszewski, "Synchronization-phase alignment of all-digital phase-locked loop chips for a 60-GHz MIMO transmitter and evaluation of phase noise effects," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 7, pp. 3187–3199, Jul. 2019.

[2] Y.-H. Yoon and J.-M. Kim, "Precision control of a sensorless PM BLDC motor using PLL control algorithm," *Elect. Eng.*, vol. 100, no. 2, pp. 1097–1111, 2018.

[3] H. A. Hamed, A. F. Abdou, E. H. E. Bayoumi, and E. E. El-Kholy, "A fast recovery technique for grid-connected converters after short dips using a hybrid structure PLL," *IEEE Trans. Ind. Electron.*, vol. 65, no. 4, pp. 3056–3068, Apr. 2018.

[4] P. Kourtessis and S. D. Walker, "A complete 8-GHz QPSK-MODEM featuring novel subcarrier and data synchronization for optical communications," *IEEE Trans. Commun.*, vol. 55, no. 5, pp. 987–995, May 2007.

[5] D. Abramovitch, "Phase-locked loops: A control centric tutorial," in *Proc. Amer. Control Conf. (IEEE Cat. No.CH37301)*, vol. 1. Anchorage, AK, USA, 2002, pp. 1–15.

[6] J. Masuch and M. Delgado-Restituto, *Ultra Low Power Transceiver for Wireless Body Area Networks*. Cham, Switzerland: Springer, 2013.

[7] H. Okuni *et al.*, "26.1 A 5.5mW ADPLL-based receiver with hybrid-loop interference rejection for BLE application in 65nm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, San Francisco, CA, USA, 2016, pp. 436–437.

[8] Y.-H. Liu, V. K. Purushothaman, C. Bachmann, and R. B. Staszewski, "Design and analysis of a DCO-based phase-tracking RF receiver for IoT applications," *IEEE J. Solid-State Circuits*, vol. 54, no. 3, pp. 785–795, Mar. 2019.

[9] R. B. Staszewski and P. T. Balsara, *All-Digital Frequency Synthesizer in Deep-Submicron CMOS*. Hoboken, NJ, USA: Wiley, 2006.

[10] M. Ding *et al.*, "A 0.8 V 0.8 mm^2 bluetooth 5/BLE digital-intensive transceiver with a 2.3mW phase-tracking RX utilizing a hybrid loop filter for interference resilience in 40nm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, San Francisco, CA, USA, 2018, pp. 446–448.

[11] R. E. Best, *Phase Locked Loops: Design, Simulation, and Applications*. New York, NY, USA: McGraw-Hill Professional, 2007.

[12] F. Brandonisio and M. P. Kennedy, *Noise-Shaping All-Digital Phase-Locked Loops*. Cham, Switzerland: Springer, 2013.

[13] S. Engelberg, "Limitations of the describing function for limit cycle prediction," *IEEE Trans. Autom. Control*, vol. 47, no. 11, pp. 1887–1890, Nov. 2002.

[14] N. Da Dalt, "A design-oriented study of the nonlinear dynamics of digital bang-bang PLLs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 1, pp. 21–31, Jan. 2005.

[15] S. Tertinek and O. Feely, "Investigation of first-order digital bang-bang phase-locked loops with reference clock jitter," in *Proc. NORCHIP*, Tallinn, Estonia, 2008, pp. 217–222.

[16] G. Marucci, S. Levantino, P. Maffezzoni, and C. Samori, "Minimum-jitter design of bang-bang PLLs in the presence of 1/f^2 and 1/f^3 DCO noise," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, Beijing, China, 2013, pp. 173–176.

[17] G. Marucci, S. Levantino, P. Maffezzoni, and C. Samori, "Exploiting stochastic resonance to enhance the performance of digital bang-bang PLLs," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 60, no. 10, pp. 632–636, Oct. 2013.

[18] G. Marucci, S. Levantino, P. Maffezzoni, and C. Samori, "Analysis and design of low-jitter digital bang-bang phase-locked loops," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 1, pp. 26–36, Jan. 2014.

[19] L. Avallone, M. P. Kennedy, S. Karman, C. Samori, and S. Levantino, "Jitter minimization in digital PLLs with mid-rise TDCs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 3, pp. 743–752, Mar. 2020.

[20] N. D. Dalt, "Markov chains-based derivation of the phase detector gain in bang-bang PLLs," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 11, pp. 1195–1199, Nov. 2006.

[21] E. Koskin, E. Blokhina, C. Shan, E. Zianbetov, O. Feely, and D. Galayko, "Discrete-time modelling and experimental validation of an all-digital PLL for clock-generating networks," in *Proc. 14th IEEE Int. New Circuits Syst. Conf. (NEWCAS)*, Vancouver, BC, Canada, Jun. 2016, pp. 1–4.

[22] E. Koskin, E. Blokhina, C. Shan, E. Zianbetov, O. Feely, and D. Galayko, "Generation of a clocking signal in synchronized all-digital PLL networks," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 65, no. 6, pp. 809–813, Jun. 2018.

[23] E. Koskin, P. Bisiaux, D. Galayko, and E. Blokhina, "All-digital phase-locked loop arrays: Investigation of synchronisation and jitter performance through FPGA prototyping," in *Proc. 17th IEEE Int. New Circuits Syst. Conf. (NEWCAS)*, Munich, Germany, 2019. pp. 1–4.

[24] B. Kaulakys and T. Meškauskas, "Modeling 1/f noise," *Phys. Rev. E, Stat. Phys. Plasmas Fluids Relat. Interdiscip. Top.*, vol. 58, no. 6, p. 7013, 1998.