RIPPLE CARRY ADDER

Bachelor of Technology
Computer Science and Engineering

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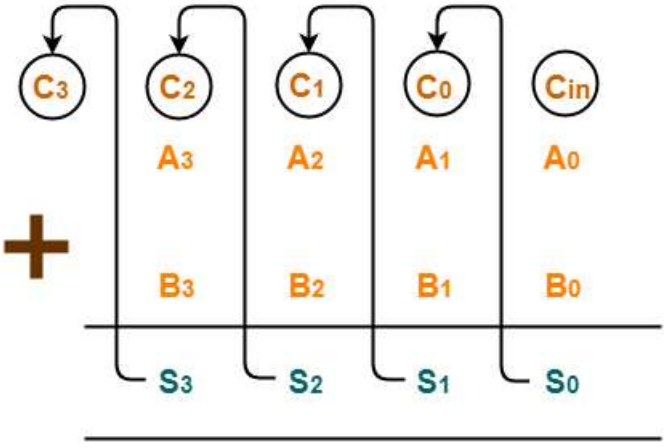
1. Introduction

Ripple Carry Adder is a combinational logic circuit. It is used for the purpose of adding two n-bit binary numbers. It requires n full adders in its circuit for adding two n-bit binary numbers. It is also known as n-bit parallel adder.

2. Body

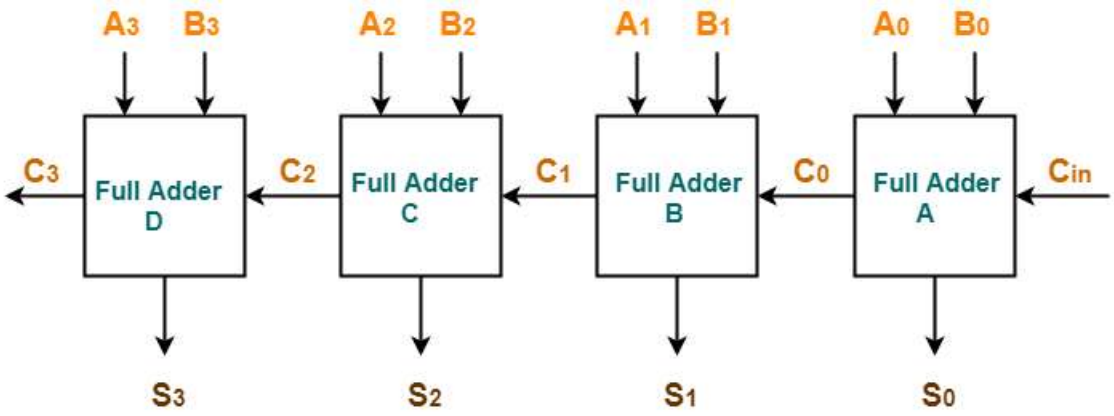
4 bit ripple carry adder

4-bit ripple carry adder is used for the purpose of adding two 4-bit binary numbers. In Mathematics, any two 4-bit binary numbers A3A2A1A0 and B3B2B1B0 are added as shown below-



Adding two 4-bit Numbers

Using ripple carry adder, this addition is carried out as shown by the following logic diagram-



4-bit Ripple Carry Adder

Ripple Carry Adder works in different stages.

- **Each full adder takes the carry-in as input and produces carry-out and sum bit as output.**
- **The carry-out produced by a full adder serves as carry-in for its adjacent most significant full adder.**
- **When carry-in becomes available to the full adder, it activates the full adder.**
- **After full adder becomes activated, it comes into operation.**

Working Of 4-bit Ripple Carry Adder-

Let-

- **The two 4-bit numbers are 0101 (A3A2A1A0) and 1010 (B3B2B1B0).**
- **These numbers are to be added using a 4-bit ripple carry adder.**

4-bit Ripple Carry Adder carries out the addition as explained in the following stages-

Stage-01:

- **When Cinis fed as input to the full Adder A, it activates the full adder A.**
- **Then at full adder A, A0= 1, B0= 0, Cin= 0.**

Full adder A computes the sum bit and carry bit as-

Calculation of S0–

$S0 = A0 \oplus B0 \oplus Cin$

$S0 = 1 \oplus 0 \oplus 0$

S0= 1

Calculation of C0–

C0= A0B0⊕ B0Cin⊕ CinA0

C0= 1.0 ⊕ 0.0 ⊕ 0.1

C0= 0 ⊕ 0 ⊕ 0

C0= 0

Stage-02:

- **When C0s fed as input to the full adder B, it activates the full adder B.**
- **Then at full adder B, A1= 0, B1= 1, C0= 0.**

Full adder B computes the sum bit and carry bit as-

Calculation of S1–

S1= A1⊕ B1⊕ C0

S1= 0 ⊕ 1 ⊕ 0

S1= 1

Calculation of C1–

C1= A1B1⊕ B1C0⊕ C0A1

C1= 0.1 ⊕ 1.0 ⊕ 0.0

C1= 0 ⊕ 0 ⊕ 0

C1= 0

Stage-03:

- **When C1is fed as input to the full adder C, it activates the full adder C.**
- **Then at full adder C, A2= 1, B2= 0, C1= 0.**

Full adder C computes the sum bit and carry bit as-

Calculation of S2–

S2= A2⊕ B2⊕ C1

S2= 1 ⊕ 0 ⊕ 0

S2= 1

Calculation of C2–

C2= A2B2⊕ B2C1⊕ C1A2

C2= 1.0 ⊕ 0.0 ⊕ 0.1

C2= 0 ⊕ 0 ⊕ 0

C2= 0

Stage-04:

- **When C2 is fed as input to the full adder D, it activates the full adder D.**
- **Then at full adder D, A3= 0, B3= 1, C2= 0.**

Full adder D computes the sum bit and carry bit as-

Calculation of S3–

S3= A3⊕ B3⊕ C2

S3= 0 ⊕ 1 ⊕ 0

S3= 1

Calculation of C3–

C3= A3B3⊕ B3C2⊕ C2A3

C3= 0.1 ⊕ 1.0 ⊕ 0.0

C3= 0 ⊕ 0 ⊕ 0

C3= 0

Thus finally,

- **Output Sum = S3S2S1S0= 1111**
- **Output Carry = C3= 0**

Why Ripple Carry Adder is Called So?

In Ripple Carry Adder,

- **The carry out produced by each full adder serves as carry-in for its adjacent most significant full adder.**
- **Each carry bit ripples or waves into the next stage.**
- **That's why, it is called as "Ripple Carry Adder".**

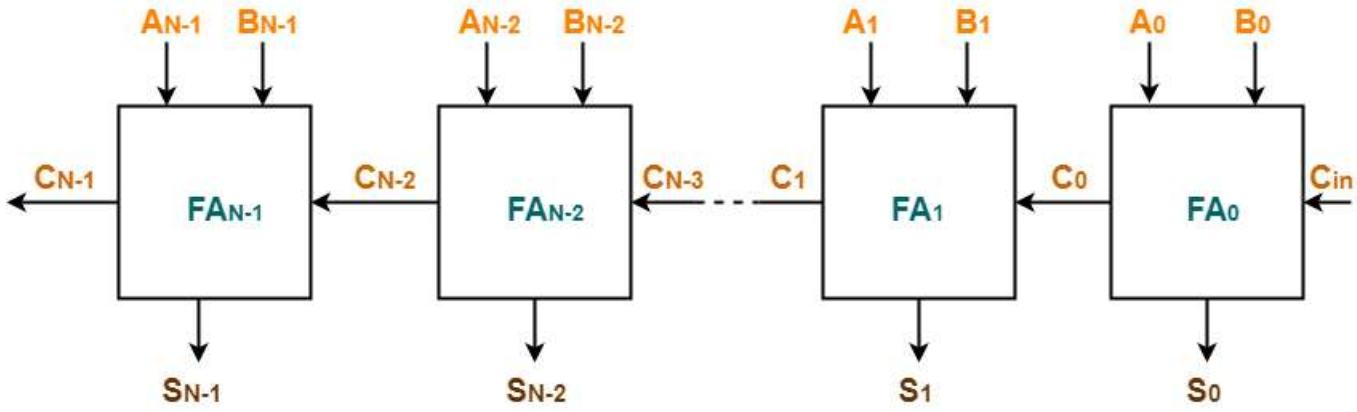
Disadvantages of Ripple Carry Adder-

- **Ripple Carry Adder does not allow to use all the full adders simultaneously.**
- **Each full adder has to necessarily wait until the carry bit becomes available from its adjacent full adder.**
- **This increases the propagation time.**
- **Due to this reason, ripple carry adder becomes extremely slow.**
- **This is considered to be the biggest disadvantage of using ripple carry adder.**

To overcome this disadvantage, Carry Look Ahead Adder comes into play.

Delay in Ripple Carry Adder-

Consider a N-bit Ripple Carry Adder as shown-



N-bit Ripple Carry Adder

The following kinds of problems may be asked based on delay calculation in Ripple Carry Adder.

Type-01 Problem:

- **You will be given the carry propagation delay and sum propagation delay of each full adder.**
- **You will be asked to calculate the worst case delay of the ripple carry adder.**

Solution-

In Ripple Carry Adder,

- **A full adder becomes active only when its carry in is made available by its adjacent less significant full adder.**
- **When carry in becomes available to the full adder, it starts its operation.**

- **It produces the corresponding output sum bit and carry bit.**

If you are asked to calculate the time after which the output sum bit or carry bit becomes available from any particular full adder, then it is calculated as-

Time After Which Carry Bit CxBecomes Available-

Required time

= Total number of full adders till full adder producing Cx X Carry propagation delay of full adder

Time After Which Sum Bit Sx Becomes Available-

Required time

= Time taken for its carry in to become available + Sum propagation delay of full adder

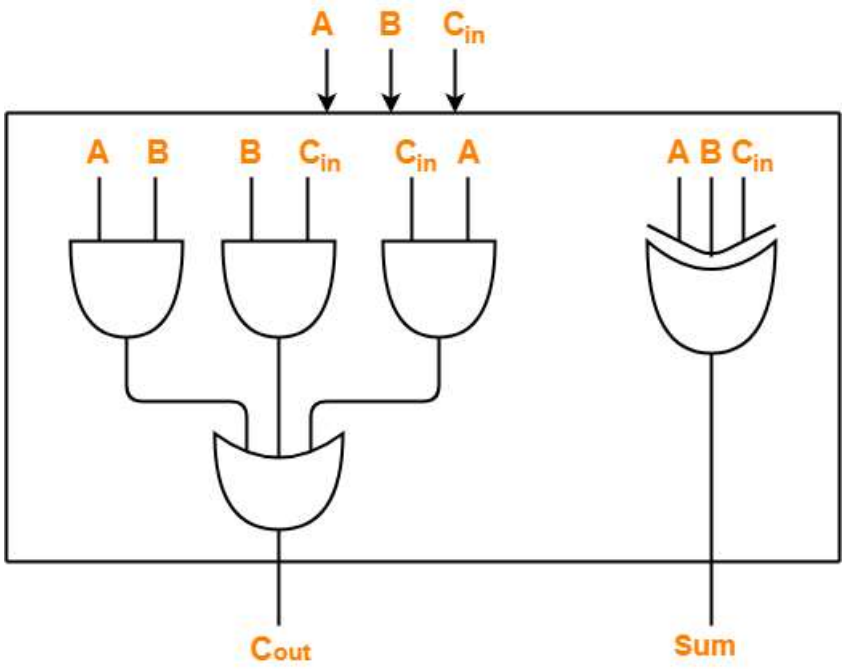
= { Total number of full adders before full adder producing Sx X Carry propagation delay of full adder } + Sum propagation delay of full adder

We will calculate worst case delay for the last full adder

Type-02 Problem:

- **You will be given the propagation delay of some basic logic gates.**
- **You will be told how the full adder has been implemented.**
- **Then, you will be asked to calculate the worst case delay of Ripple Carry Adder.**

Suppose each full adder in the given ripple carry adder has been implemented as-



Full Adder Implementation

Solution-

- **The computation has to be done in the same manner as in Type-01 problem.**
- **It's just that in Type-02 problem, one step is increased.**
- **We have to first calculate the carry propagation delay and sum propagation delay in terms of logic gates.**
- **Then, our problem will reduce to Type-01 problem.**

Let-

- **Propagation delay of AND gate = Tpd(AND)**
- **Propagation delay of OR gate = Tpd(OR)**
- **Propagation delay of XOR gate = Tpd(XOR)**

Calculating Carry Propagation Delay-

- **We calculate the carry propagation delay of full adder using its carry generator logic circuit.**
- **It has 2 levels in the given implementation.**
- **At first level, three AND gates operate.**
- **All the three AND gates operate in parallel.**
- **So, we consider the propagation delay due to only one AND gate.**

- **At second level, OR gate operates.**

Now,

Carry propagation delay of full adder

= Time taken by it to generate the output carry bit

= Propagation delay of AND gate + Propagation delay of OR gate

= Tpd(AND) + Tpd(OR)

Calculating Sum Propagation Delay-

- **We calculate the sum propagation delay of full adder using its sum generator logic circuit.**
- **It has only 1 level at which XOR gate operates in the given implementation.**

Now,

Sum propagation delay of full adder

= Time taken by it to generate the output sum bit

= Propagation delay of XOR gate

= Tpd(XOR)

Now,

- **We have got the carry propagation delay and sum propagation delay of full adders.**
- **Our problem reduces to Type-01 problem.**
- **We use the same formulas as we have learnt in Type-01 problem to make the required calculations.**

3. Conclusion

Ripple carry adder is a combinational logic circuit used for the purpose of adding two n-bit binary numbers. 4-bit ripple carry adder is used for adding two 4-bit binary numbers. N-bit ripple carry adder is used for adding two N-bit binary numbers. Carry propagation delay of a full adder is the time taken by it to produce the output carry bit. Sum propagation delay of a full adder is the time taken by it to produce the output sum bit. Worst case delay of a ripple carry adder is the time after which the output sum bit and carry bit becomes available from the last full adder.

4. References

The information in this report has been taken from the following:

Book-

DIGITAL DESIGN BY MORRIS MANO

Link-

https://www.gatevidyalay.com/