EXPT NO. : 7

AIM:

Design of a 'Carry-Look- Ahead' Adder circuit

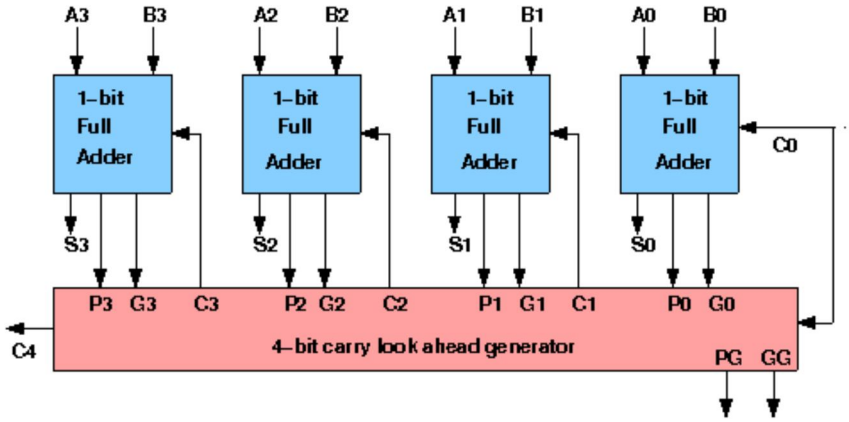
APPARATUS REQUIRED:

Sl. No.	COMPONENT	SPECIFICATION	QTY.
1.	X-OR GATE	IC 7486	1
2.	AND GATE	IC 7408	1
3.	OR GATE	IC 7432	1
4.	BREAD BOARD	-	1
5.	PATCH CORDS	-	-
6.	POWER SUPPLY WITH LOGIC PROBE	-	1

THEORY:

To reduce the computation time, there are faster ways to add two binary numbers by using carry look ahead adders. They work by creating two signals P and G known to be **Carry Propagator** and **Carry Generator**. The carry propagator is propagated to the next level whereas the carry generator is used to generate the output carry, regardless of input carry.

The block diagram of a 4-bit Carry Look Ahead Adder is shown here below –



The number of gate levels for the carry propagation can be found from the circuit of full adder. The signal from input carry C_{in} to output carry C_{out} requires an AND gate and an OR gate, which constitutes two gate levels. So if there are four full adders in the parallel adder, the output carry C_5 would have 2 X 4 = 8 gate levels from C_1 to C_5. For an n-bit parallel adder, there are 2n gate levels to propagate through.The corresponding boolean expressions are given here to construct a carry look ahead adder. In the carry look ahead circuit we need to generate the two signals carry propagator (P) and carry generator (G),

$$P_i = A_i \oplus B_i$$

$$G_i = A_i \cdot B_i$$

The output sum and carry can be expressed as

$$Sum_i = P_i \oplus C_i$$

$$C_{i+1} = G_i + (P_i \cdot C_i)$$

Having these we could design the circuit. We can now write the Boolean function for the carry output of each stage and substitute for each Ci its value from the previous equations:

$$C_1 = G_0 + P_0 \cdot C_0$$

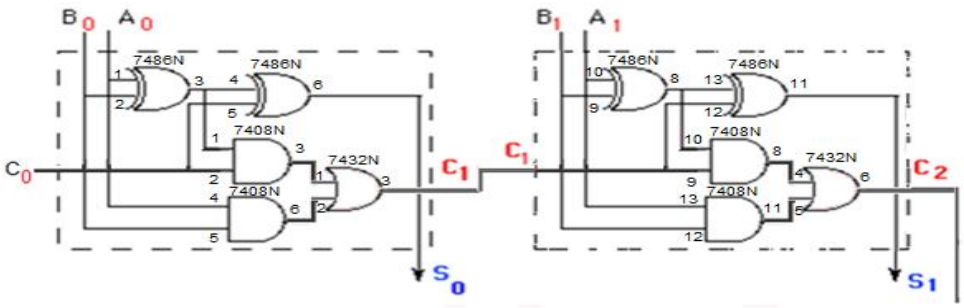
$$C_2 = G_1 + P_1 \cdot C_1 = G_1 + P_1 \cdot G_0 + P_1 \cdot P_0 \cdot C_0$$

$$C_3 = G_2 + P_2 \cdot C_2 = G_2\, P_2 \cdot G_1 + P_2 \cdot P_1 \cdot G_0 + P_2 \cdot P_1 \cdot P_0 \cdot C_0$$

$$C_4 = G_3 + P_3 \cdot C_3 = G_3\, P_3 \cdot G_2\, P_3 \cdot P_2 \cdot G_1 + P_3 \cdot P_2 \cdot P_1 \cdot G_0 + P_3 \cdot P_2 \cdot P_1 \cdot P_0 \cdot C_0$$

CARRY LOOK AHEAD ADDER LOGIC DIAGRAM:

2 Bit CLA:



TRUTH TABLE:

INPUT					OUTPUT		
A_0	B_0	C_0	A_1	B_1	S_0	S_1	C_2
0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	1
0	0	0	1	1	0	1	0
0	1	0	1	1	1	1	0
0	0	1	0	0	1	0	0
0	1	1	0	0	0	1	0
0	1	1	1	1	0	1	1
1	1	1	1	1	1	1	1

PROCEDURE:

(i) Connections are given as per circuit diagram.

(ii) Logical inputs are given as per circuit diagram.

(iii) Observe the output and verify the truth table.

OBSERVATION TABLE:

INPUT					OUTPUT		
A_0	**B_0**	**C_0**	**A_1**	**B_1**	**S_0**	**S_1**	**C_2**