EXPT NO: 11

AIM:

To use a multiplexer unit to design a composite ALU

APPARATUS REQUIRED:

SL.NO	COMPONENT	SPECIFICATIONS	QTY
1	MULTIPLEXER(8:1)	IC 74151	1
2	AND GATE	IC 7408	1
3	OR GATE	IC 7432	1
4	NOT GATE	IC 7404	1
6	BREAD BOARD	-	1
7	PATCH CORDS	-	-
8	POWER SUPPLY WITH LOGIC PROBE	-	1

THEORY:

Arithmetic logic unit is that part of the computer which performs the different logic operations and arithmetic operations like addition, subtraction, multiplication and division. It is the high speed digital circuit that solves calculations and does comparisons.

Functions of ALU:

- Almost all the actions are done by it. It gets its data from a certain computer memory called Processor Register. After the data gets processed, its results get stored in output registers of the ALU
- The arithmetic logic unit can perform integer arithmetic operations like addition, subtraction etc.
- It can also perform bitwise logical operations like AND, OR, XOR etc.

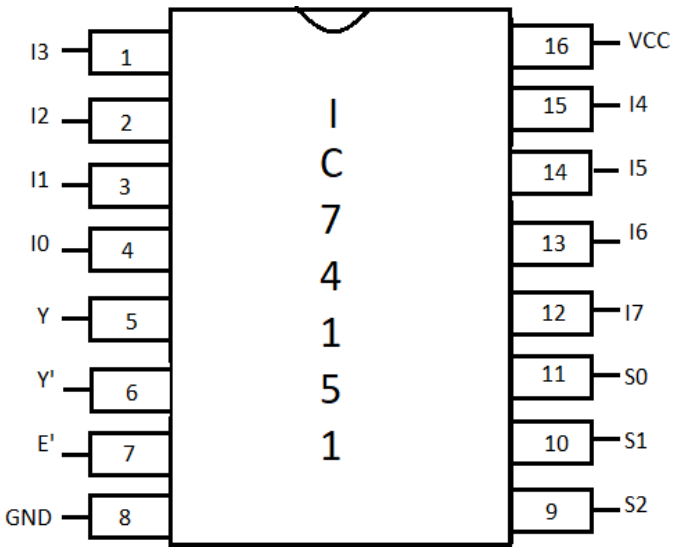
- The arithmetic logic unit performs bit shifting operations like

rotating or shifting a certain word to either the left or the right by a given number of bits. These can also be represented as divisions by 2 and also multiplications by 2. These are the simple operations carried out by the ALU. An ALU can be designed by using 8x1 multiplexer. By the three functions select inputs S0, S1, S2 distinct arithmetic or logical operations can be performed. In the following table 8x1 multiplexer selects different logic functions and their inverse at its outputs Y and Y' respectively

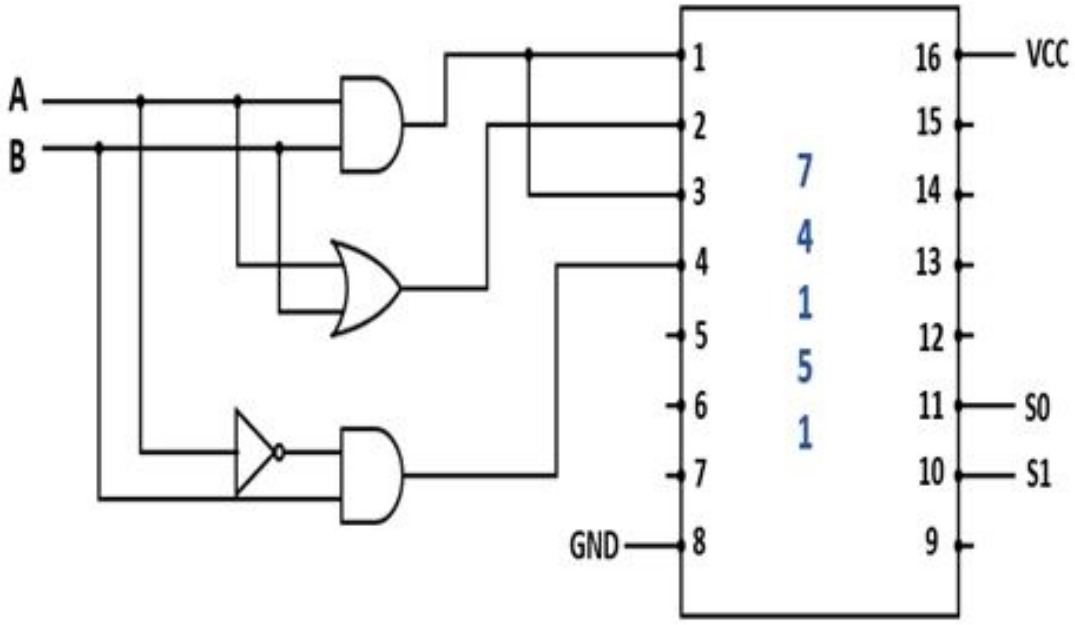
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
4, 3, 2, 1, 15, 14, 13, 12	I_0 to I_7	multiplexer inputs
5	Y	multiplexer output
6	$\overline{Y}$	complementary multiplexer output
7	$\overline{E}$	enable input (active LOW)
8	GND	ground (0 V)
11, 10, 9	S_0, S_1, S_2	select inputs
16	V_{CC}	positive supply voltage

IC74151 PIN DAIGRAM:



8 INPUT MULTIPLEXER



Truth Table:

E'	S0	S1	A	B	Y	Y'	
0	0	0	0	0	0	1	AND
0	0	0	0	1	0	1	
0	0	0	1	0	0	1	
0	0	0	1	1	1	0	
0	0	1	0	0	0	1	OR
0	0	1	0	1	1	0	
0	0	1	1	0	1	0	
0	0	1	1	1	1	0	
0	1	0	0	0	0	1	CARRY
0	1	0	0	1	0	1	
0	1	0	1	0	0	1	
0	1	0	1	1	1	0	
0	1	1	0	0	0	1	BORROW
0	1	1	0	1	1	0	
0	1	1	1	0	0	1	
0	1	1	1	1	0	1	

PROCEDURE:

1. Connections are given as per circuit diagram.
2. Logical inputs are given as per circuit diagram.
3. Observe the output and verify the truth table.

OBSERVATION TABLE:

E'	S0	S1	S2	A	B	Y	Y'