

COMPUTER ORGANIZATION LAB (PCC- CS 392)

EXPT NO. : 4

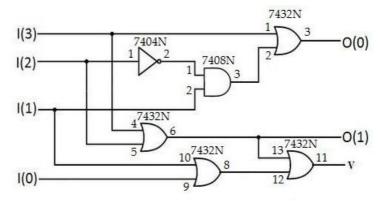
DESIGN AND IMPLEMENTATION OF ENCODER AND DECODER

AIM: To design and implement encoder and decoder using logic gates.

APPARATUS REQUIRED:

SI. No.	COMPONENT	SPECIFICATION	QTY.
1.	OR GATE	IC 7432	1
2.	NOT GATE	IC 7404	1
3.	AND GATE	IC 7408	1
4.	BREAD BOARD	-	1
5.	PATCH CORDS	-	-
6.	POWER SUPPLY WITH LOGIC PROBE	-	1

ENCODER: An encoder is a digital circuit that performs inverse operation of a decoder. An encoder has 2^n input lines and n output lines. In encoder the output lines generates the binary code corresponding to the input value. In octal to binary encoder it has eight inputs, one for each octal digit and three output that generate the corresponding binary code. In encoder it is assumed that only one input has a value of one at any given time otherwise the circuit is meaningless. It has an ambiguity that when all inputs are zero the outputs are zero. The zero outputs can also be generated when $I_0 = 1$.



LOGIC DIAGRAM FOR ENCODER:

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TRUTH TABLE:

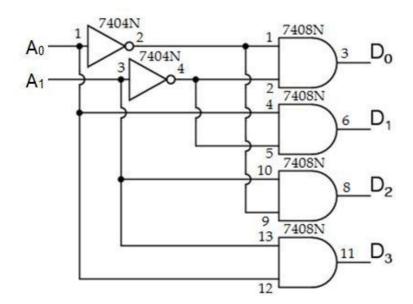
lo	I ₁	l ₂	l ₃	O ₁	O ₀	V
0	0	0	1	0	0	1
0	0	1	0	0	1	1
0	1	0	0	1	0	1
1	0	0	0	1	1	1

OBSERVATION TABLE:

I ₀	I ₁	l ₂	l ₃	O ₁	O ₀	V

DECODER: A decoder is a multiple input multiple output logic circuit which converts coded input into coded output where input and output codes are different. The input code generally has fewer bits than the output code. Each input code word produces a different output code word i.e. there is one to one mapping can be expressed in truth table. In the block diagram of decoder circuit the encoded information is present as n input producing 2^n possible outputs. 2^n output values are from 0 through out $2^n - 1$.

LOGIC DIAGRAM FOR DECODER:



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COMPUTER ORGANIZATION LAB MANUAL (CS 393)

TRUTH TABLE:

OUTPUT					
A ₁	A ₀	D ₀	D ₁	D ₂	D_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

PROCEDURE:

- (i) Connections are given as per circuit diagram.
- (ii) Logical inputs are given as per circuit diagram.
- (iii) Observe the output and verify the truth table.

OBSERVATION TABLE:

A ₁	A ₀	D ₀	D ₁	D_2	D ₃

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