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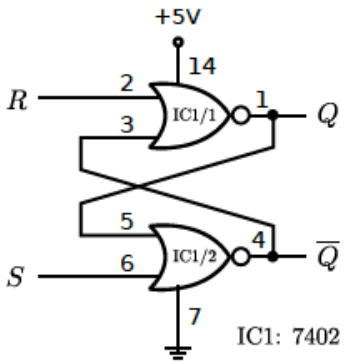
Name: ..... Student ID: .....

Laboratory 10

Flip-Flops

1. S-R Flip-Flop:

1.1 Connect a logic circuit as shown in the following figure. The input should be connected to the logic switches and the output should be connected to logic monitor.



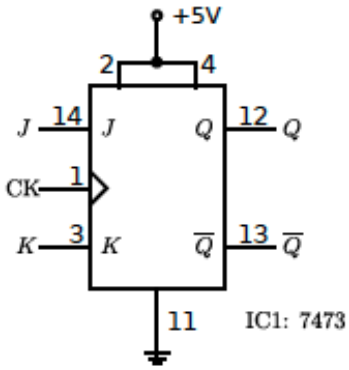
1.2 Supply the logic to the input S and R as shown in the following figure. Record the results.

S	R	Q	Q'	State
0	0	0 (Q)	1 ($\overline{Q}$)	Unchange
0	1	0	1	Reset
1	0	1	0	Set
1	1	0	0	Unused

Instructor's signature

2. J-K Flip-Flop, T Flip-Flop, D Flip-Flop:

2.1 Connect the circuit as shown in the following figure. The CK input should be connected to output 1 of a debounce switch.



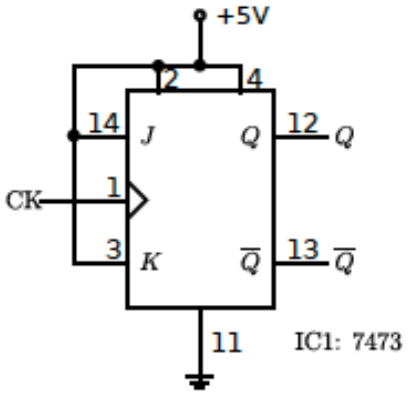
2.2 CK=1 refers to the state where the debounce switch is not pressed and CK=0 refers to the state where the debounce switch is pressed and the pulse is supplied to pin CK.

2.3 Record the results in the following table.

Input			Output		
J	K	CK	Q	Q'	State
0	0	0	0 (Q)	1 ($\overline{Q}$)	Unchanged
0	0	1	0 (Q)	1 ($\overline{Q}$)	Unchanged
0	1	0	0 (Q)	1 ($\overline{Q}$)	Unchanged
0	1	1	0	1	Reset
1	0	0	0 (Q)	1 ($\overline{Q}$)	Unchanged
1	0	1	1	0	Set
1	1	0	1 (Q)	0 ($\overline{Q}$)	Unchanged
1	1	1	0 ($\overline{Q}$)	1 (Q)	Toggled

Instructor's signature

2.4 Connect the circuit as shown in the following figure.



2.5 Supply a pulse using a debounce switch as shown in the following table.

2.6 Observe and record the status of Q and Q'

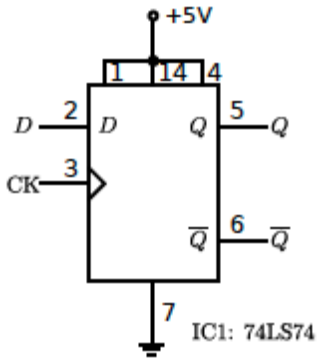
CK	Q	Q'
1	1 ($\overline{Q}$)	0 (Q)
0	1 (Q)	0 ($\overline{Q}$)
1	0 ($\overline{Q}$)	1 (Q)
0	0 (Q)	1 ($\overline{Q}$)

2.7 Name the type of this flip-flop

Toggle Flip Flop

Instructor's signature

2.7 Connect the circuit as shown in the following figure.



2.8 Connect pin CK to the output 1 of the debounce switch. Connect pin D to the logic switch and the output Q and Q' to the logic monitor.

2.9 CK=0 refers to the state where the debounce switch is not pressed. CK=1 refers to the state where the debounce switch is pressed **one time** to supply the pulse to CK. Record the results in the following table.

D	CK	Q	Q'
0	0	0 (Q_0)	1 ($\overline{Q_0}$)
1	0	0 (Q_0)	1 ($\overline{Q_0}$)
1	1	1	0
0	0	0	1
0	1	0	1

Instructor's signature

3. **Assignments:**

3.1 Construct a logic circuit which can add two 2-bits binary numbers according to the following conditions:

a) Receive the first 2-bits binary number by using SW7 and SW6 where SW7 is the MSB.
b) To get the next input, press debounce switch to supply the rising edge for the CLK signal
c) Get the second 2-bits number by using the SW7 and SW6 again.
d) Show the results using logic monitors. Use D7 and D6 to display the sum and D5 to display the carry out.

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3.2 Given an IC 7474, dual D-type positive-edge-triggered flip-flops with preset and clear. Show the procedure and a logic circuit to obtain a **J-K flip-flop** using this given IC and additional necessary gates.

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3.3 Given an IC 7474, dual D-type positive-edge-triggered flip-flops with preset and clear. Show the procedure and a logic circuit to obtain a **S-R flip-flop** using this given IC and additional necessary gates.

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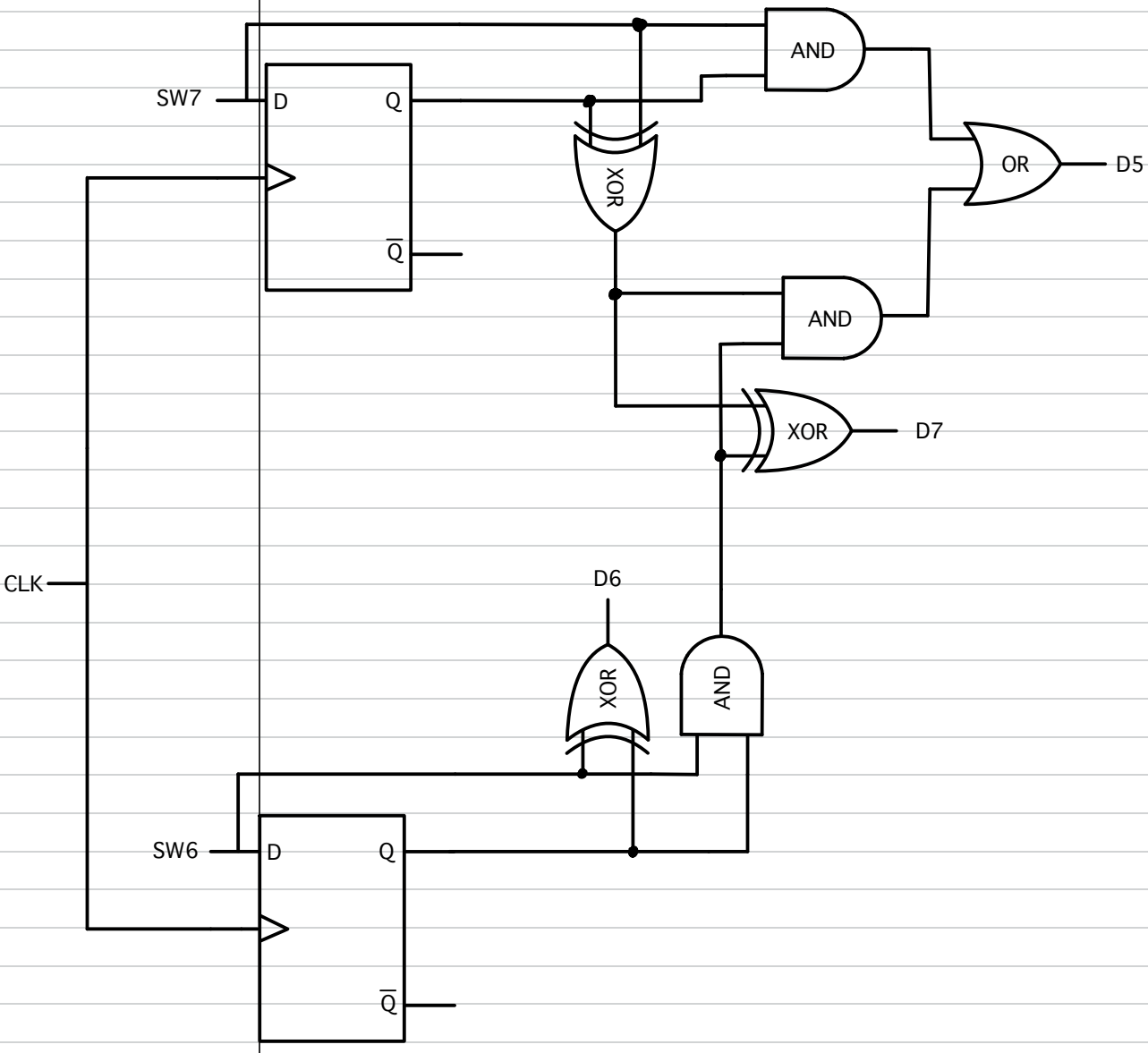

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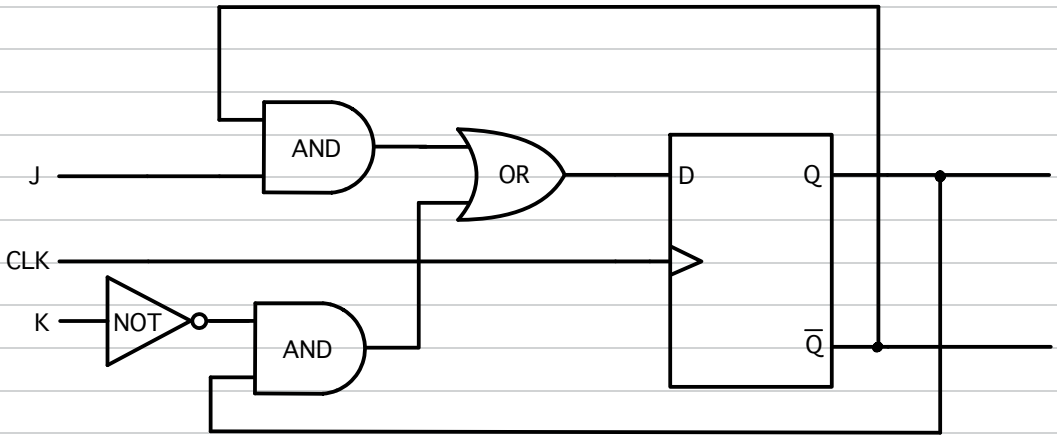

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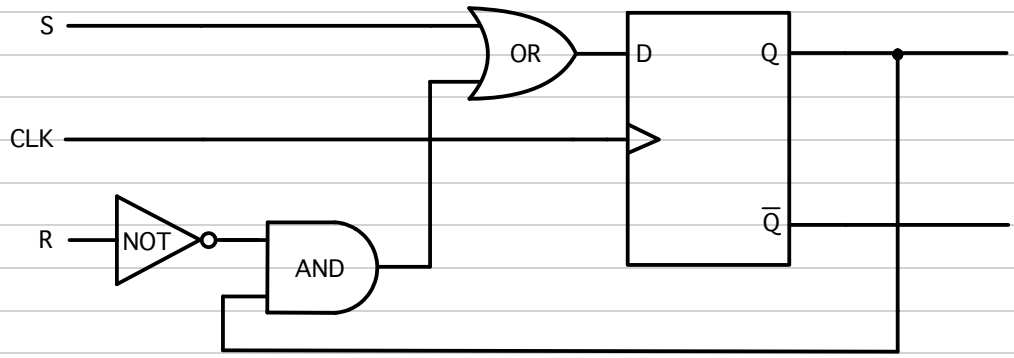

Logic Diagram of frequently used gates