# 11
# Fundamentals of Sequential Circuits

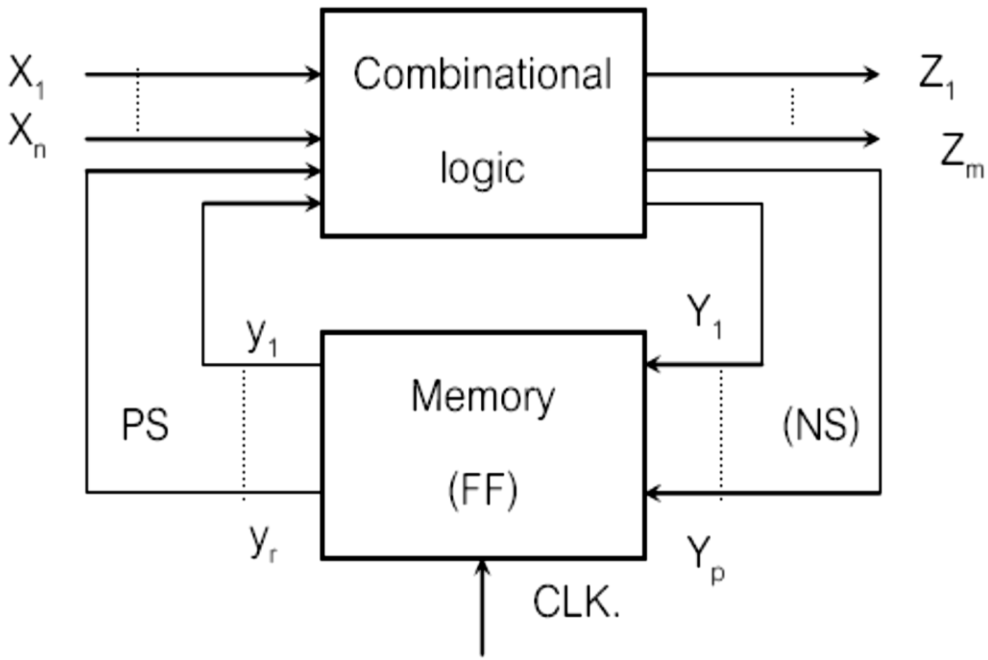
# Sequential Circuits

In digital systems in general, usually consisting of

- Combinational Logic Circuits and
- Sequential Circuits:
  - the ability to remember the Present State, and
  - To produce the Next State e.g. operation of elevator,
  - which requires inputs from both the control panels in every floor and the position of the elevator.

Therefore, the Sequential Circuits need to have a unit of memory (flip-flops) in conjunction with the combinational logic circuit.

# Sequential Circuits: Block Diagram




Where

$x_1,\ldots, x_n$ are input variables;

$z_1,\ldots, z_m$ are output variables;

$y_1,\ldots, y_r$ are present states;

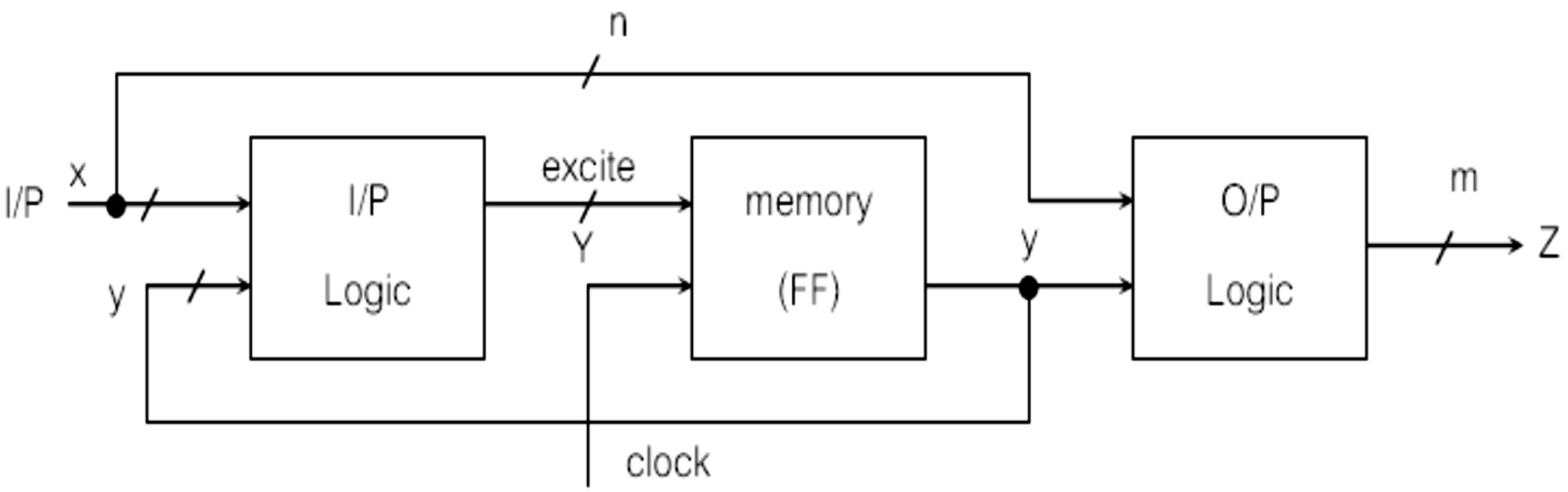
$Y_1,\ldots, Y_p$ are next states

Then we may the relationships of

- The logical output: $z_i = f_i\,(x_1,\ldots, x_n, y_1,\ldots, y_r)$
- The flipflop state: $Y_i = g_i\,(x_1,\ldots, x_n, y_1,\ldots, y_r)$

# Sequential Circuits: Block Diagram

We may re-write the Block Diagram to a simple form :



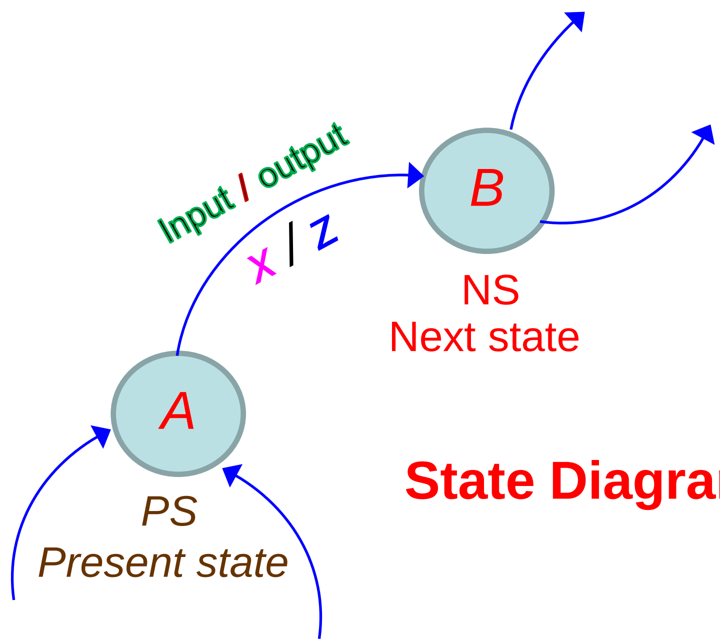
# Sequential Circuits: State Table and State Diagram

**State Table**:
Table that shows both the logical outputs ($z_i$) together with the next states ($Y_i$) when applying the logical inputs ($x_i$) and the present states ($y_i$) of the flipflops.

**State Diagram:**
Diagram that shows states as a circles with the arrow in as the logical input. The outward arrow show the output in the direction to the Next state.

| Input / *PS* | *x* |
|---|---|
| | |
| *y* | *Y* / *z* |
| | Next state / Output |
| | |

**State Table**

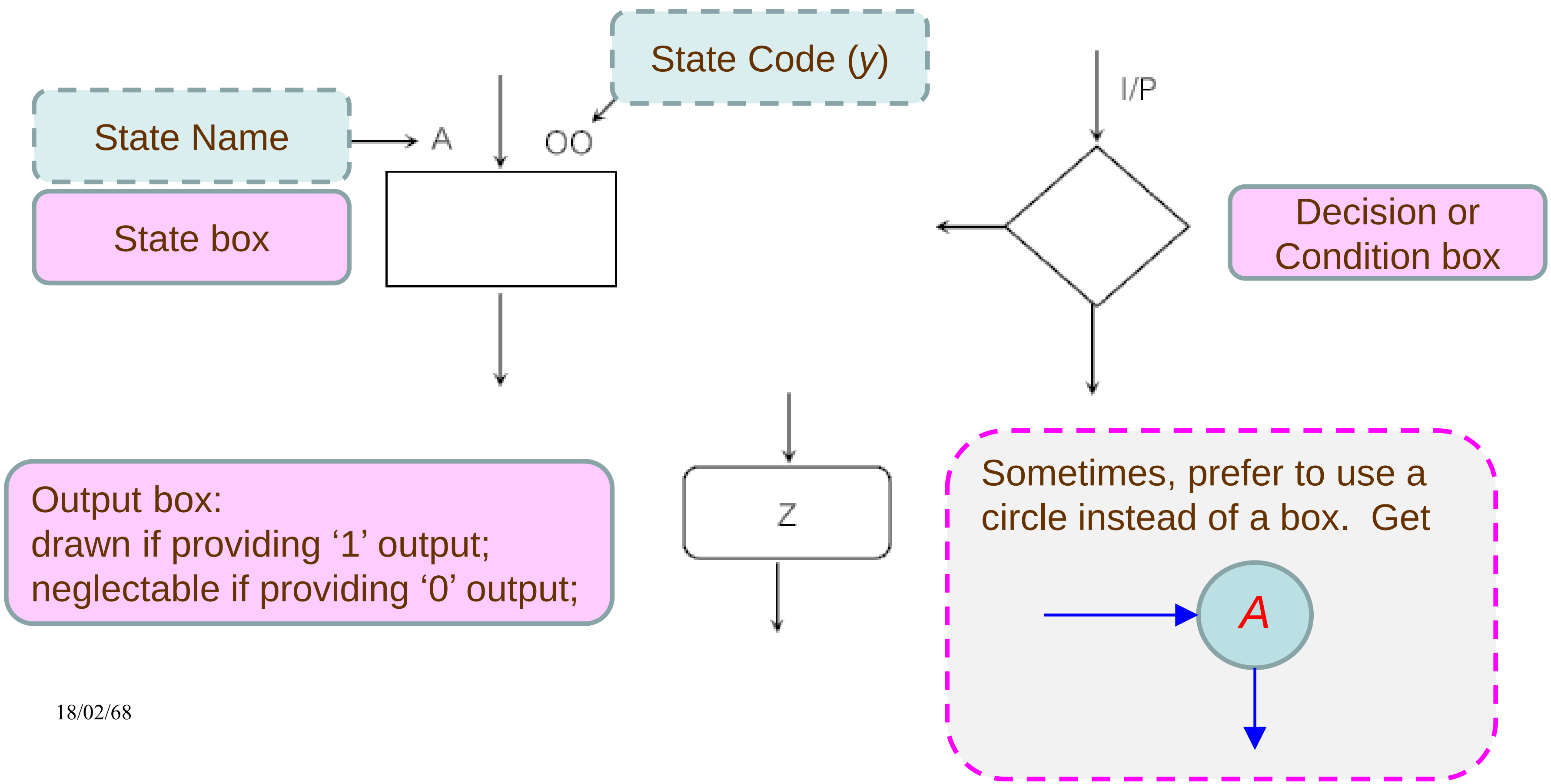



**State Diagram**

# Algorithmic State Machine Chart (ASM Chart)

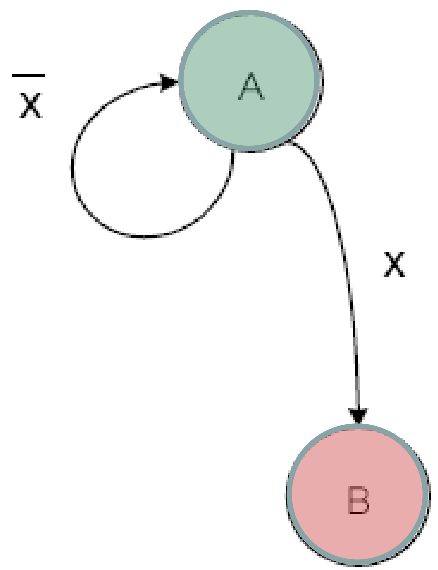
## Algorithmic State Machine Chart (ASM Chart)

ASM Chart is a flow-chart that describes the sequential operation of the circuit.  The ASM chart has 3 basic symbols as shown:

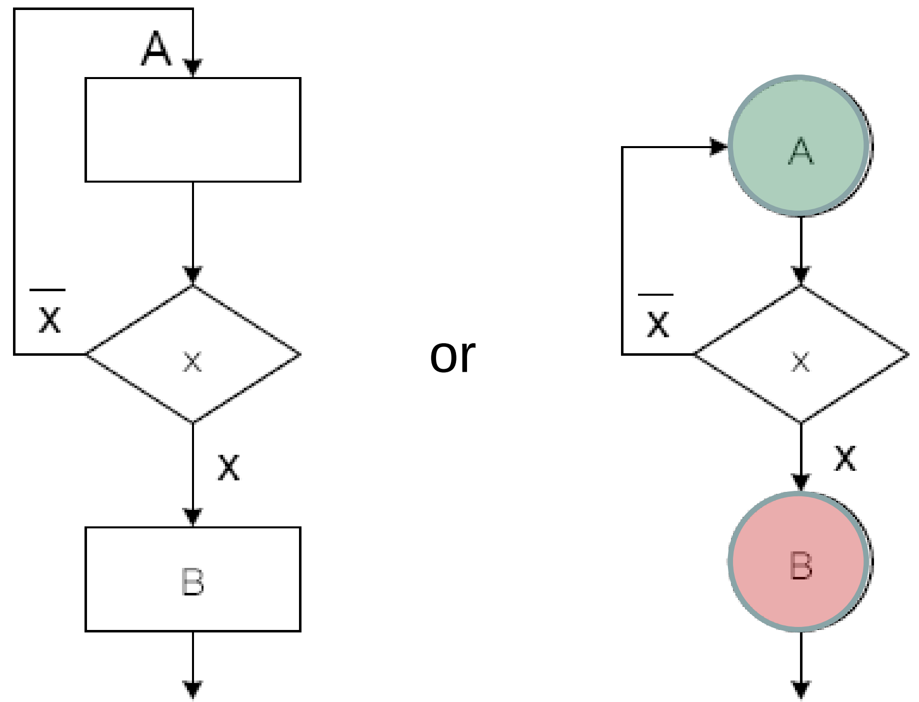


# State Diagram v.s. ASM Chart

## Example: Writing State Diagram compared with ASM Chart




State Diagram




ASM Chart

# The Mealy and Moore Model

## The Mealy and Moore Model

The Sequential circuits can be described into two forms:

Mealy Model: has logical output as a function of both P.S. and logical inputs;

Moore Model: has logical output as a function of P.S. ONLY.

Both have the N.S. as a function of both P.S. and logical inputs.

**Mealy:**

Z = Output data = Z(x, y)

Y = Next state = Y(x, y)

**Moore:**

Z = Output data = Z(y)

Y = Next state = Y(x, y)

x = Input data  Z = Input data

y = Present State (PS)  Y = Next State (NS)

# The Sequential Circuit: Mealy Model

**Example:** The state table below is in the forma of Mealy. Find

A) The state diagram

B) The ASM Chart

C) The characteristics of z (the order of z) when input x is as follows X: 011011 and the initial state is at state A.

| PS \ x | 0 | 1 |
|---|---|---|
| A | B/1 | C/0 |
| B | B/0 | A/1 |
| C | A/0 | C/0 |
| | | |

**Mealy:**

Y = Next state = Y(x, y)

Z = Output data = Z(x, y)

# The Sequential Circuit: Mealy Model

Solution: A) The state diagram

Consider the state table, find that the output *z* depends on both input *x* and the present state *y*.

- $x$ = 0, 1
- $y$ = A, B and C for the codes 00, 01 and 10.
- $Y$ has the number of state the same as $y$
- $z$ = 0, 1

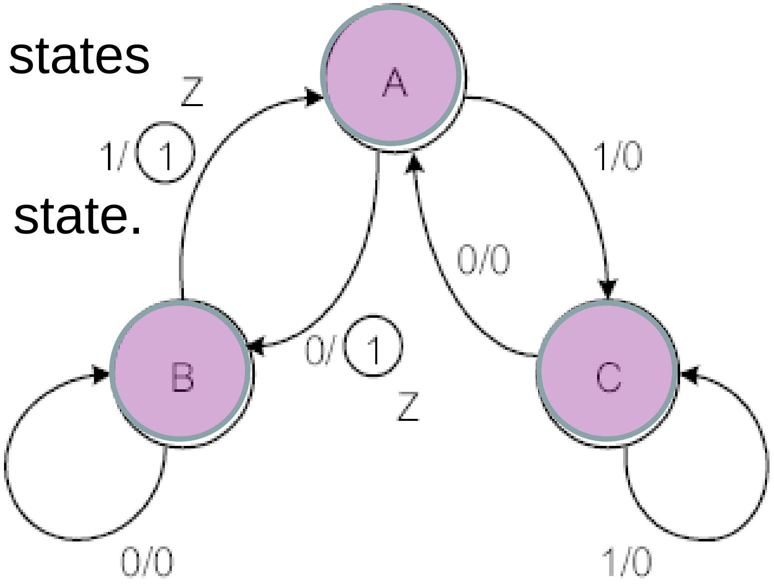
How to draw the **state diagram**

I. Write circles representing the existing states A, B, and C.

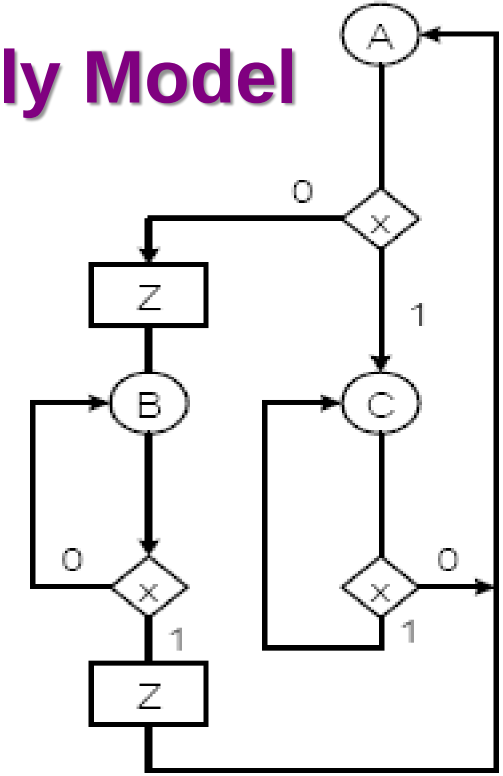
I. Draw a line from P.S. to N.S. for every state.

II. Add input/output on that line.

III. Do this for all states in the table.



# The Sequential Circuit: Mealy Model




## B) ASM Chart

- Just follow the state table;
- Start from state A;
- with the excite of x = 0 and x =1;
- Carry on for the other states until reaching to the last state.

## C) The characteristics of *z*

- Start from the first input 0 and initial state A;
- Find the next output and state from the state diagram
- Keep doing this until the last input.

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Time: | 1 | 2 | 3 | 4 | 5 | 6 | |
| Input *x*: | 0 | 1 | 1 | 0 | 1 | 1 | (6 bit) |
| Present state *y*: | A | B | A | C | A | C | |
| Next state *Y*: | B | A | C | A | C | C | |
| Output *z*: | 1 | 1 | 0 | 0 | 0 | 0 | |

# The Sequential Circuit: Moore Model

**Example:** The state table below is in the forma of Moore. Find

A) The state diagram

B) The ASM Chart

C) The characteristics of z (the order of z) when input x is as follows X: 100110 and the initial state is at state A.

| PS \ x | 0 | 1 | z |
|---|---|---|---|
| A | C | B | 0 |
| B | B | C | 1 |
| C | B | A | 0 |
| | | | |

Moore:

Y = Next state = Y(x, y)

Z = Output data = Z(y)

# The Sequential Circuit: Moore Model

Solution: A) The state diagram
Consider the state table:

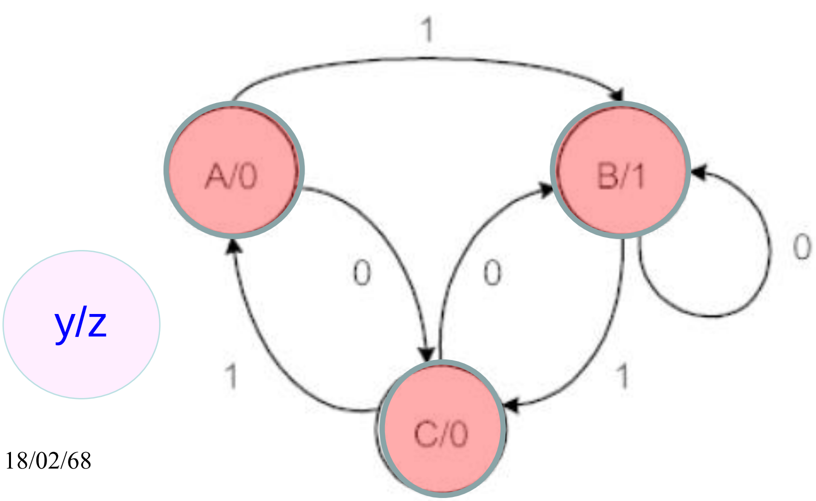
How to draw the **state diagram**

I. Write circles representing the existing states A, B, and C.

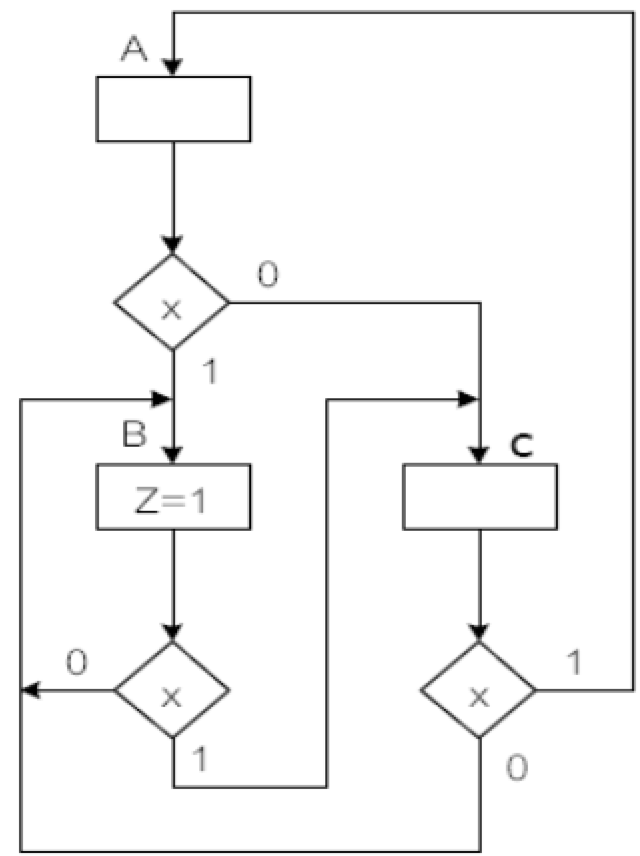
II. Also write the output just behind the state name (separating by slash).

III. Draw a line from P.S. to N.S.

IV. Do this for all states in the table.




B) ASM Chart



# The Sequential Circuit: Moore Model

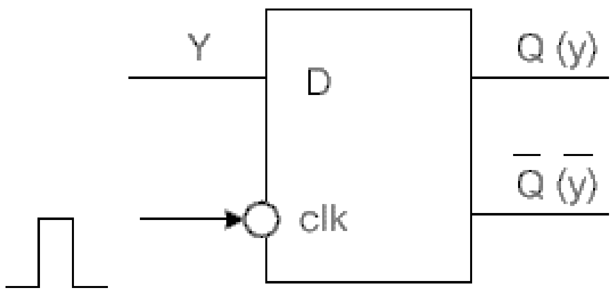
C) The characteristics of *z*

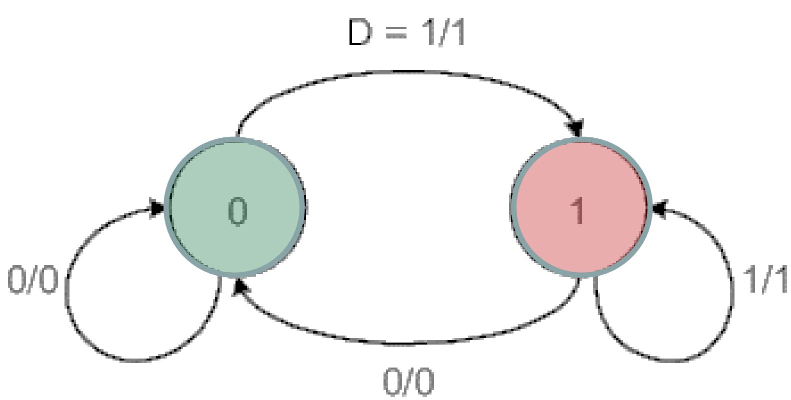
- Start from the first input 1 and initial state A;
- Find the next output and state from the state diagram
- Keep doing this until the last input.

| | | | | | | |
|---|---|---|---|---|---|---|
| Time: | 1 | 2 | 3 | 4 | 5 | 6 |
| Input *x*: | 1 | 0 | 0 | 1 | 1 | 0 |
| Present state *y*: | A | B | B | B | C | A |
| Next state *Y*: | B | B | B | C | A | C |
| Output *z*: | 1 | 1 | 1 | 0 | 0 | 0 |

# Excitation Table, State Diagram & State Equations of FlipFlops

## D FlipFlop




## State Diagram

## Excitation Table

| Input | Output Q (clk = 1) | | |
|---|---|---|---|
| D | PS (y) | NS (Y) | |
| 0 | 0 | 0 | Reset |
| 0 | 1 | 0 | |
| 1 | 0 | 1 | Set |
| 1 | 1 | 1 | |

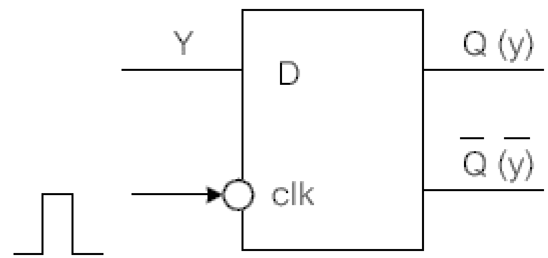
## State Equation

# State Equation for D FlipFlop

Change the state table to Karnaugh Map, get

| PS y \ D | 0 | 1 |
|---|---|---|
| 0 | 0 | 1 |
| 1 | 0 | 1 |

NS (Y)

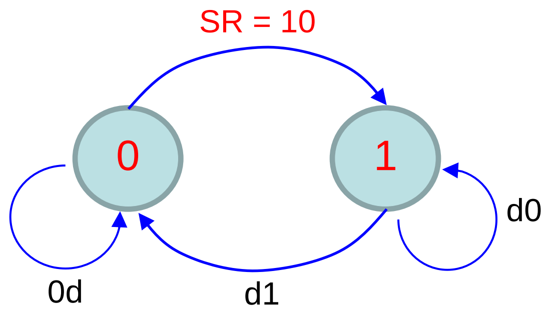



The relationship of NS (Y): $Y = D$

The relationship from the state table is called **State Equation.**

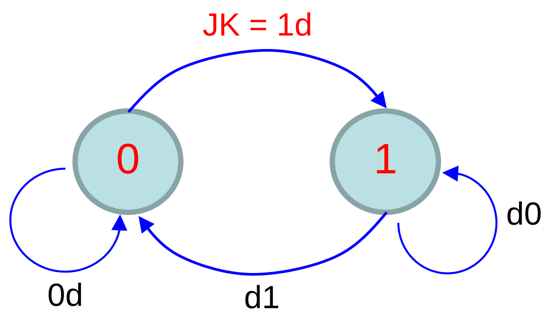
Likewise, When considering the excitation table of Flip-Flops: RS, JK and T will get the relationship of NS (Y) as follows.

# State Equations for RS-, JK-, T- FlipFlops



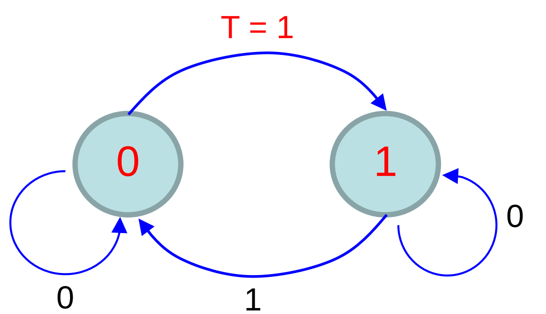

## SR Flipflop

$$Y = S + \bar{R}\, y$$




## JK Flipflop

$$Y = J\,\bar{y} + \bar{K}\, y$$




## T Flipflop

$$Y = T\,\bar{y} + \bar{T}\, y$$

# State Equations for RS-, JK-, T- FlipFlops

| ***S-R*** <br> ***y*** | **00** | **01** | **11** | **10** |
|---|---|---|---|---|
| 0 | | | | |
| 1 | | | | |

| ***J-K*** <br> ***y*** | **00** | **01** | **11** | **10** |
|---|---|---|---|---|
| 0 | | | | |
| 1 | | | | |

| ***T*** <br> ***y*** | **0** | **1** |
|---|---|---|
| 0 | | |
| 1 | | |

# The Sequential Circuit: Analysis

**Analyzing A Synchronous Sequential Circuit**

I. Find the logical equation of the *Y*(NS) and *z*(output);

II. Write excitation table for *Y*(NS) and for *z*(output) in the form of *y* v.s *x*;

III. Combine *Y* and *z* by writing in the form of *Y/z* ,

called this as transition table ;

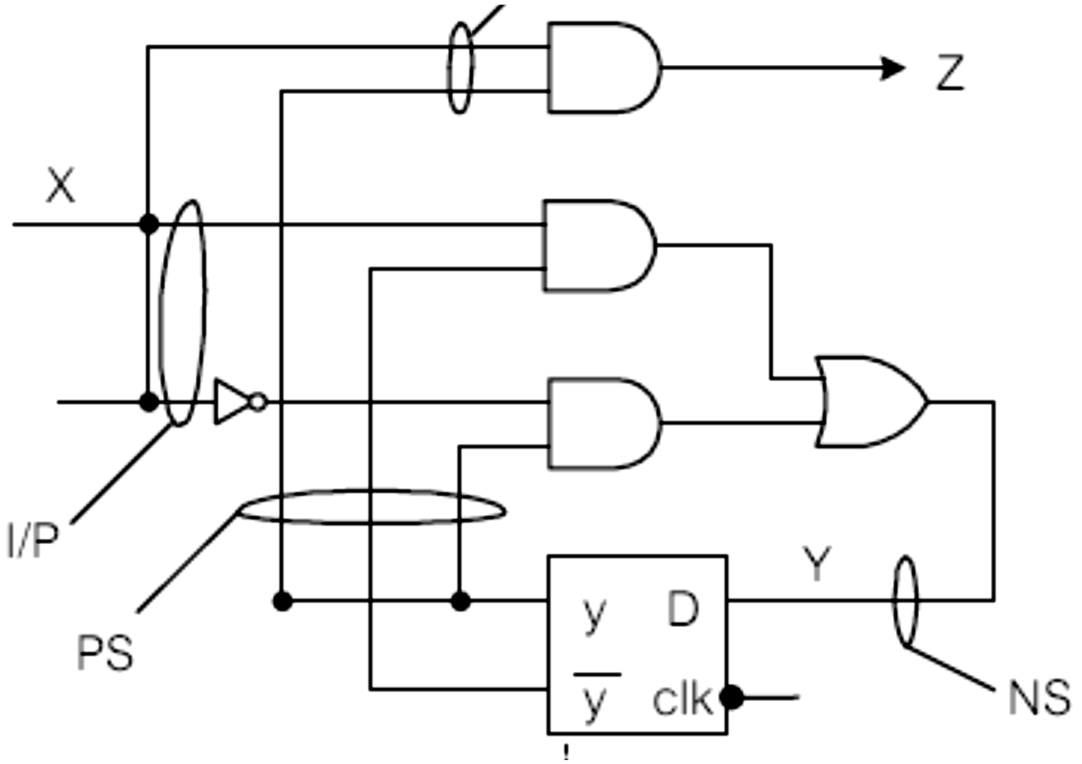
I. Assign the name or symbol for the state *y* or *Y*, to obtain the state table.

II. From the state table, draw the state diagram for use in consideration of

the outputs of the circuit, which may be presented as the timing diagram.

# The Sequential Circuit: Analysis

**Example:** Find the state table, state diagram and timing diagram for the circuit below, when the input $x$ = 011010 and initial state = A.



# The Sequential Circuit: Analysis

**Solution:** From the circuit, we have the input *x,* the output *z* and state of the flipflop *y* and *Y*.

I. Write the logical equation applied to the D Flip-flops:

$$D = Y$$

$$Y = x\bar{y} + \bar{x}y$$

And $$z = xy$$

II. Bring *Y* and *z* put into the K-Maps get the excitation tables:

| y \ x | 0 | 1 |
|---|---|---|
| 0 | 0 | 1 |
| 1 | 1 | 0 |

Y (N/S)

| y \ x | 0 | 1 |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 0 | 1 |

Z

# The Sequential Circuit: Analysis

III. Combine the K-Maps of *Y* and *z*, and get transition table (*Y/z*)

| y \ x | 0 | 1 |
|---|---|---|
| 0 | 0/0 | 1/0 |
| 1 | 1/0 | 0/1 |

Y /Z

=>

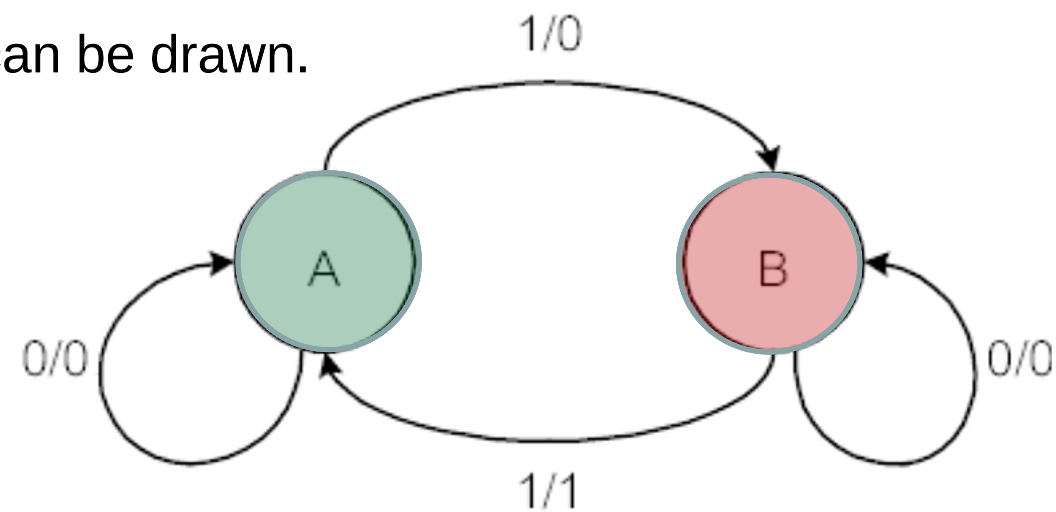
State table

| PS \ x | 0 | 1 |
|---|---|---|
| A | A/0 | B/0 |
| B | B/0 | A/1 |

NS/Z

IV. Assign the name of present state: A = [*y*] = [0] and B = [*y*] = [1]. Then obtain the state table (NS/*z*)

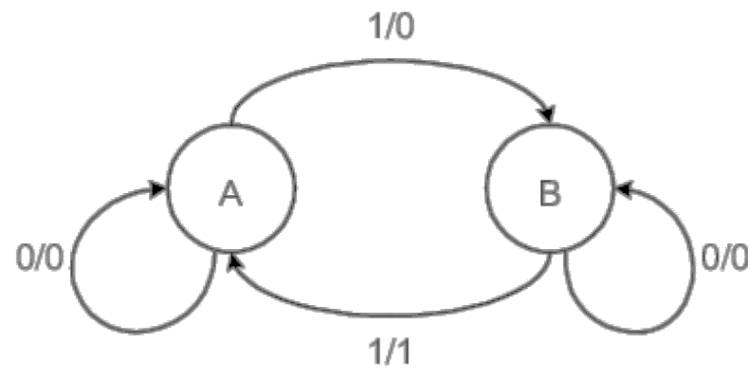
V. Then the state diagram can be drawn.



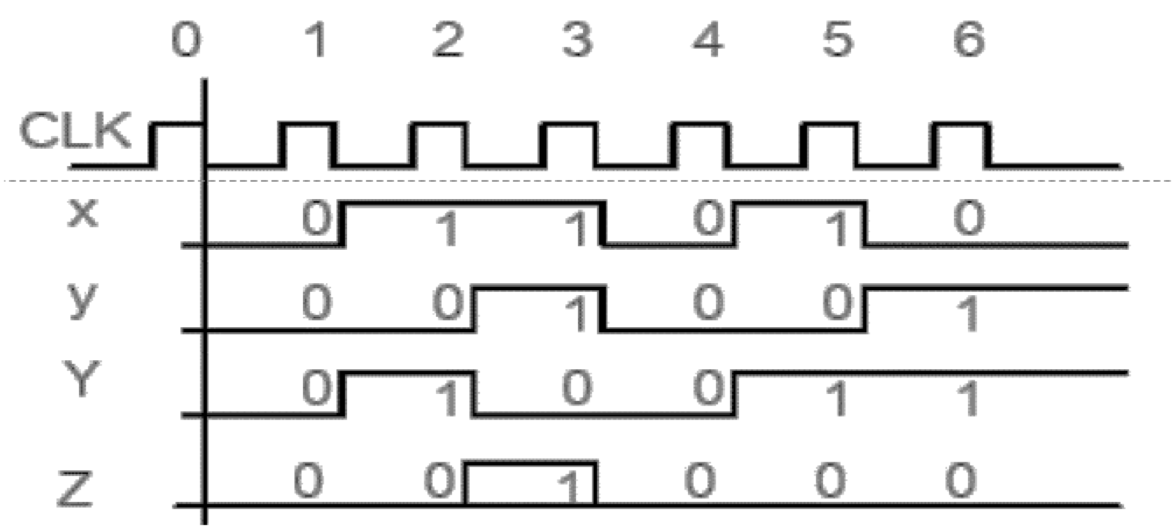
# The Sequential Circuit: Analysis

V. From the obtained state diagram, when the input x = 011010 and initial state A:

x = 0 1 1 0 1 0
y = A A B A A B
Y = A B A A B B
z = 0 0 1 0 0 0

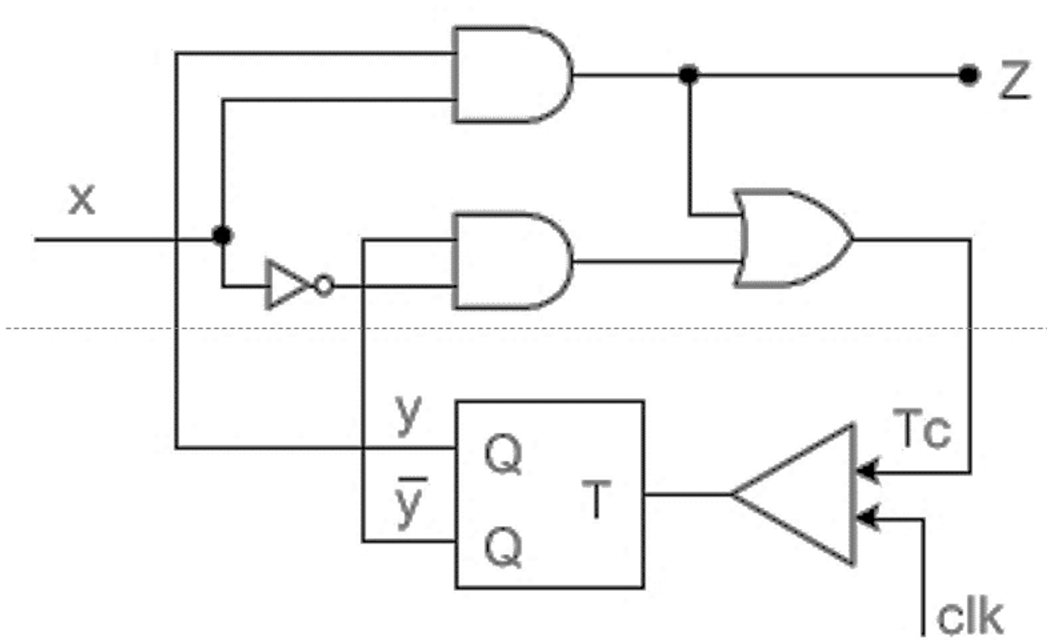



And get the timing diagram:



# The Sequential Circuit: Analysis

**Example:** Find the state table, state diagram and timing diagram for the circuit below, when the input $x$ = 01101000 and initial state A.




**Solution:**

I. Write the logical equation applied to the T Flip-flops triggered at T:

$$T_C = xy + \bar{x}\bar{y} = \overline{x \oplus y}$$

And $z = xy$

# The Sequential Circuit: Analysis

II. Bring *Y* and *z* put into the K-Maps:

| y \ x | 0 | 1 |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 0 | 1 |

Z

| y \ x | 0 | 1 |
|---|---|---|
| 0 | 1 | 0 |
| 1 | 0 | 1 |

TC

III. Combine the K-Maps of *Y* and *z*, and get transition table (*Y/z*)

| y \ x | 0 | 1 |
|---|---|---|
| 0 | 1 | 0 |
| 1 | 1 | 0 |

Y (N/S)

| y \ x | 0 | 1 |
|---|---|---|
| 0 | 1/0 | 0/0 |
| 1 | 1/0 | 0/1 |

Y/Z

Consider *Y*(NS) from $T_C$ and *y*

IV. Assign the name of present state: A = [*y*] = [0] and B = [*y*] = [1].

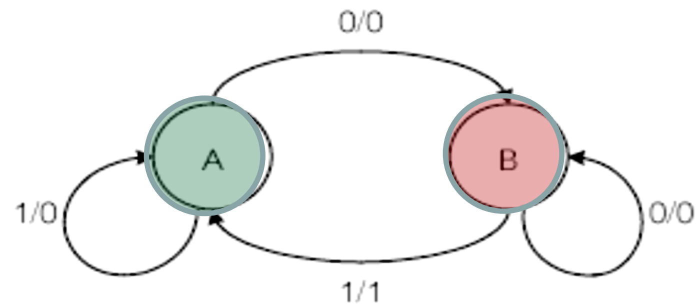
Then obtain the state table (NS/*z*)

V. Then the state diagram can be drawn.

| y \ x | 0 | 1 |
|---|---|---|
| A | B/0 | A/0 |
| B | B/0 | A/1 |

NS/Z

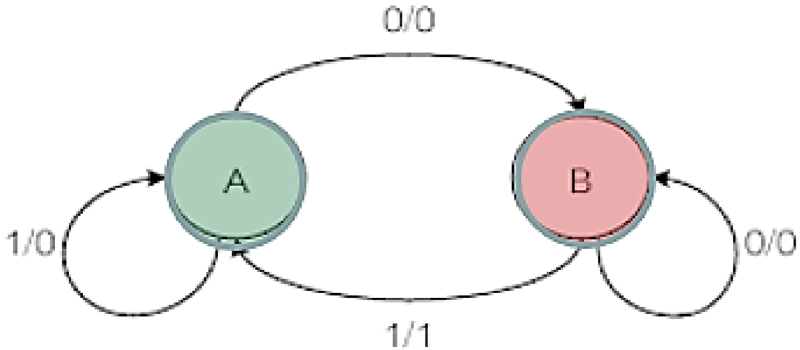
=>



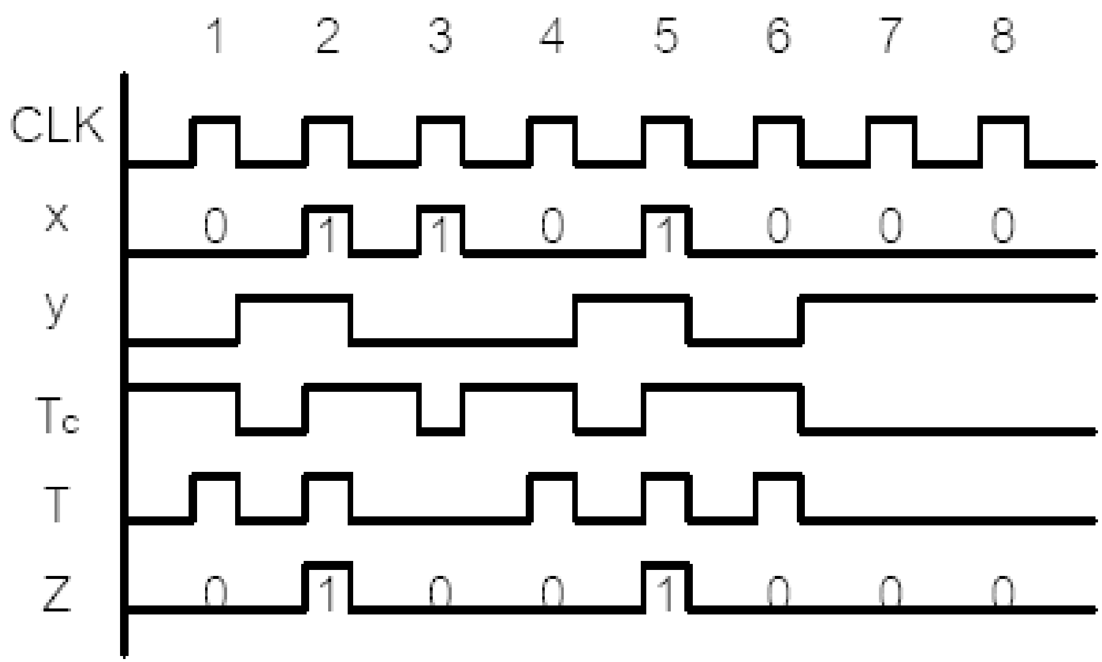
# The Sequential Circuit: Analysis

V. From the obtained state diagram, when the input x = 01101000 and initial state A:

x = 0 1 1 0 1 0 0 0
y = A B A A B A B B
Y = B A A B A B B B
z = 0 1 0 0 1 0 0 0

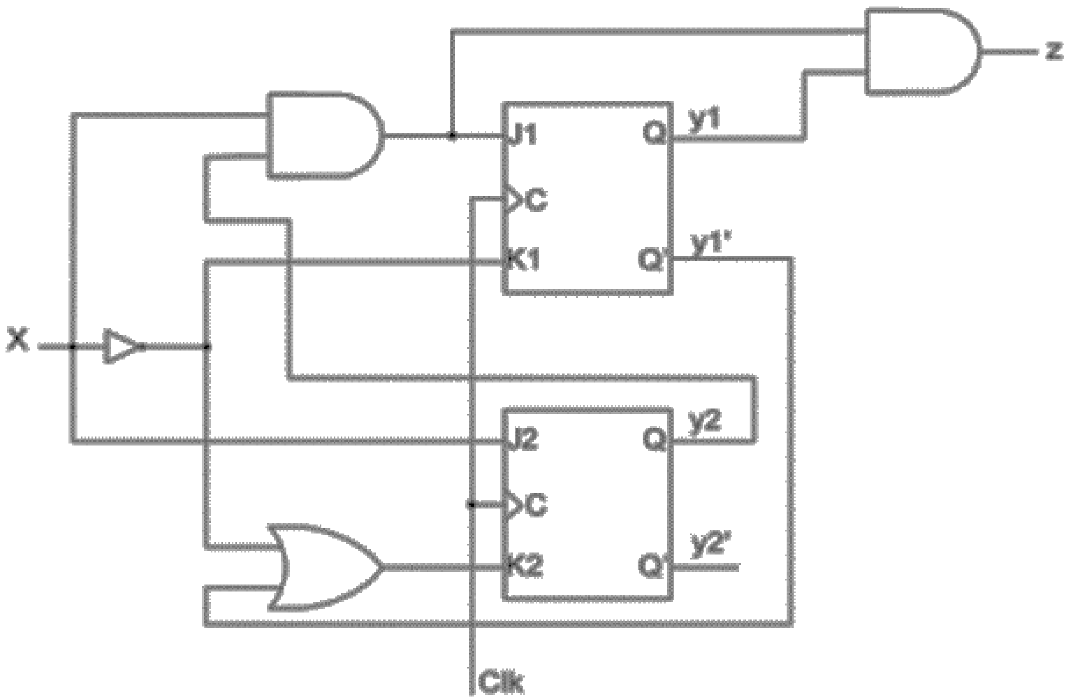



And get the timing diagram:



# The Sequential Circuit: Analysis

**Example:** Find the state table, state diagram and timing diagram for the circuit below for the input *x* = 00111100 and initial state = 10.




Since there are TWO Flip-flops, which produce $y_1$ *and* $y_2$ or ($Y_1$ *and* $Y_2$) then they can produce 4 states of 00, 01, 10 and 11.

# The Sequential Circuit: Analysis

**Solution:**

I. Write the logical equation applied to the JK Flip-flops :

$$z = xy_1y_2$$

$$J_1 = xy_2\,, \qquad K_1 = \overline{x}$$

And $\quad J_2 = x, \qquad K_2 = \overline{x} + \overline{y}_1$

II. Bring *Y* and *z* put into the K-Maps:

| $y_1y_2$ \ x | 0 | 1 |
|---|---|---|
| 00 | 0 | 0 |
| 01 | 0 | 0 |
| 11 | 0 | 1 |
| 10 | 0 | 0 |

Z

| $y_1y_2$ \ x | 0 | 1 |
|---|---|---|
| 00 | 0 | 0 |
| 01 | 0 | 1 |
| 11 | 0 | 1 |
| 10 | 0 | 0 |

$J_1$

| $y_1y_2$ \ x | 0 | 1 |
|---|---|---|
| 00 | 1 | 0 |
| 01 | 1 | 0 |
| 11 | 1 | 1 0 |
| 10 | 1 | 0 |

$K_1$

# The Sequential Circuit: Analysis

$J_2 = x$, $K_2 = \overline{x} + \overline{y_1}$

| x → | 0 | 1 |
|---|---|---|
| 00 | 0 | 1 |
| 01 | 0 | 1 |
| 11 | 0 | 1 |
| 10 | 0 | 1 |

| y₁y₂ \ x | 0 | 1 |
|---|---|---|
| 00 | 1 | 1 |
| 01 | 1 | 1 |
| 11 | 1 | 0 |
| 10 | 1 | 0 |

| $y_1y_2$ \ x | 0 | | 1 | |
|---|---|---|---|---|
| 00 | 01 | 01 | 00 | 11 |
| 01 | 01 | 01 | 10 | 11 |
| 11 | 01 | 01 | 10 | 10 |
| 10 | 01 | 01 | 00 | 10 |
| | $J_1k_1$ | $J_2k_2$ | $J_1k_1$ | $J_2k_2$ |

| PS \ x | 0 | 1 |
|---|---|---|
| 00 | 00 | 01 |
| 01 | 00 | 10 |
| 11 | 00 | 11 |
| 10 | 00 | 11 |

$Y_1Y_2$

## III. Combine the K-Maps of *Y* and *z*, and get transition table (*Y/z*)

| PS \ x | 0 | 1 |
|---|---|---|
| 00 | 00 | 01 |
| 01 | 00 | 10 |
| 11 | 00 | 11 |
| 10 | 00 | 11 |

$Y_1 Y_2$

| PS \ x | 0 | 1 |
|---|---|---|
| 00 | 00/0 | 01/0 |
| 01 | 00/0 | 10/0 |
| 11 | 00/0 | 11/1 |
| 10 | 00/0 | 11/0 |

Y1 Y2 /Z

| $y_1y_2$ \ x | 0 | 1 |
|---|---|---|
| 00 | 0 | 0 |
| 01 | 0 | 0 |
| 11 | 0 | 1 |
| 10 | 0 | 0 |

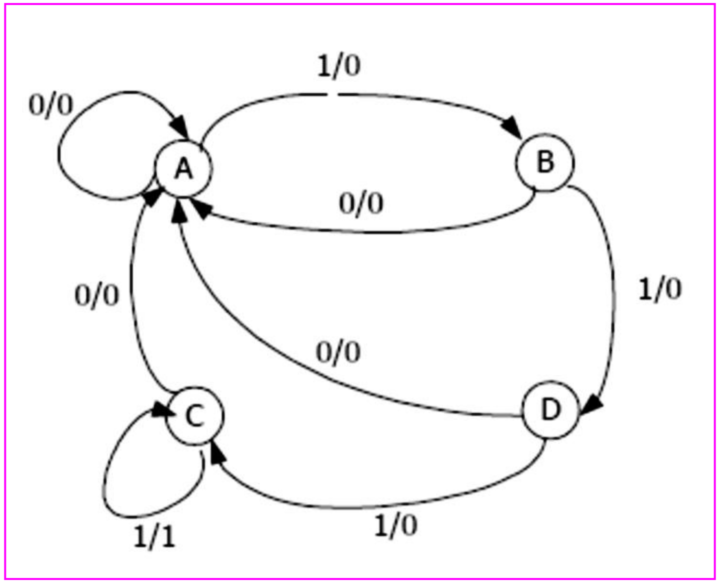
Z

IV. Assign the name of present state: A = [$y_1$ $y_2$] = [00], B = [01], C = [11] and D = [10]. Then obtain the state table (NS/*z*).

| PS \ x | 0 | 1 |
|---|---|---|
| A | A/0 | B/0 |
| B | A/0 | D/0 |
| C | A/0 | C/1 |
| D | A/0 | C/0 |

$Y_1 Y_2$

V. Then the state diagram can be drawn



V. From the obtained state diagram, when the input x = 00111100 and initial state 10:

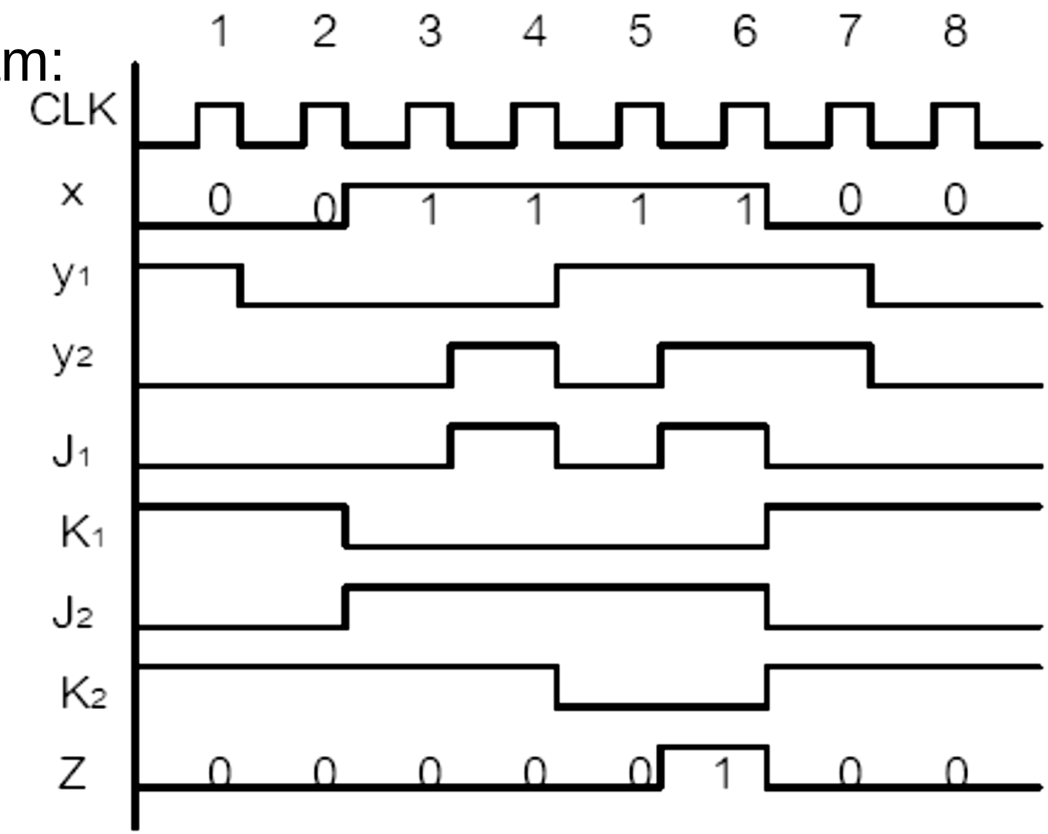
x = 0  0 1  1  1  1 0  0

y = D  A A  B D C C A

Y = A  A B D C C A  A

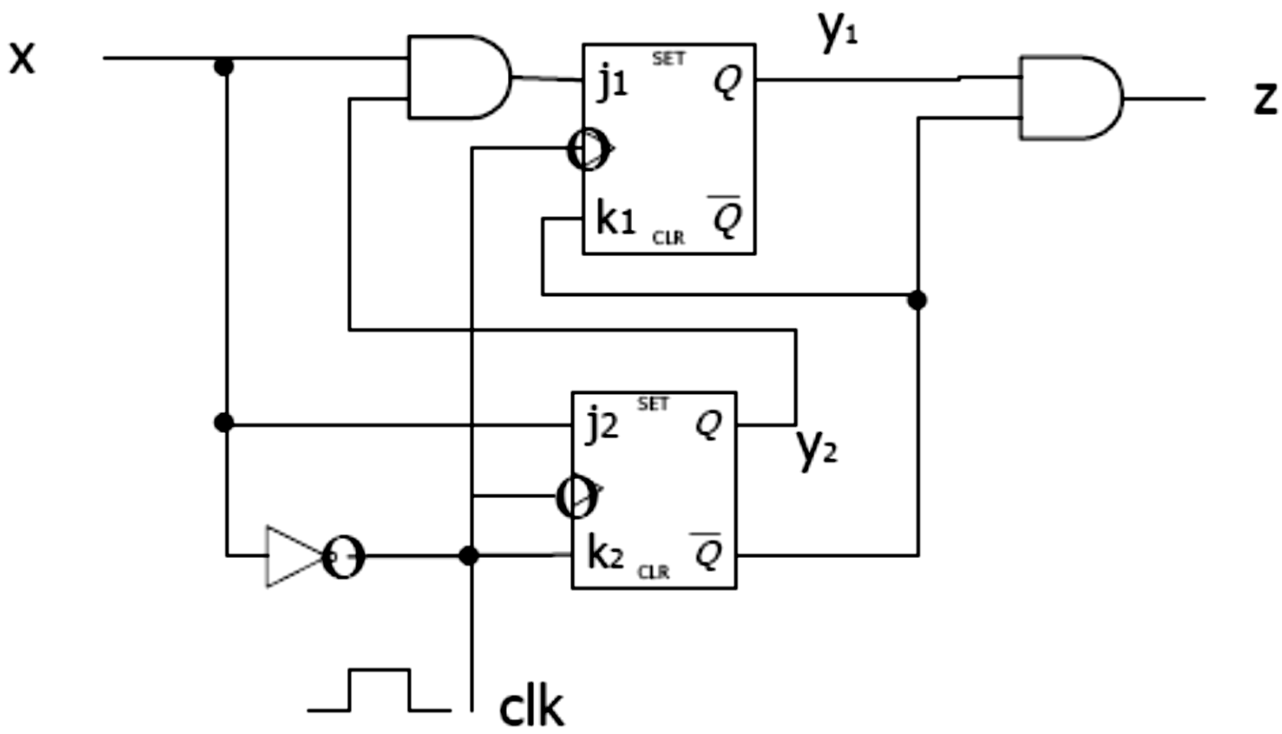
z = 0  0  0 0  0  1 0 0

And get the timing diagram:



# The Sequential Circuit: Analysis

**Example:** From the circuit, find the state table, state diagram and timing diagram for the input *x* = 1101110101 and initial state = 00.




Since there are TWO Flip-flops, which produce $y_1$ *and* $y_2$ or ($Y_1$ *and* $Y_2$) then they can produce 4 states of 00, 01, 10 and 11.

# The Sequential Circuit: Analysis

**Solution:**

I. Write the logical equation applied to the T Flip-flops triggered at T:

$$z = y_1 \overline{y}_2$$ (➔ Moore Model)

$$J_1 = x\, y_2\,, \qquad K_1 = \overline{y}_2$$

And $$J_2 = x, \qquad K_2 = \overline{x}$$

II. Bring $Y$ and $z$ put into the K-Maps:

III. Combine the K-Maps of $Y$ and $z$, and get transition table ($Y/z$)

(For short-cut, we may use the state equations, instead.)

$$Y_1 = J_1\overline{y}_1 + \overline{K}_1 y_1 = x\, y_2 \overline{y}_1 + y_2 y_1 = y_2(x\,\overline{y}_1 + y_1) = y_2(x + y_1)$$

$$Y_2 = J_2\overline{y}_2 + \overline{K}_2 y_2 = x\,\overline{y}_2 + x\, y_2 = x$$

and get transition table ($Y/z$)

| $y_1y_2$ \ x | 0 | 1 | z |
|---|---|---|---|
| 00 | 00 | 01 | 0 |
| 01 | 00 | 11 | 0 |
| 11 | 10 | 11 | 0 |
| 10 | 00 | 01 | 1 |

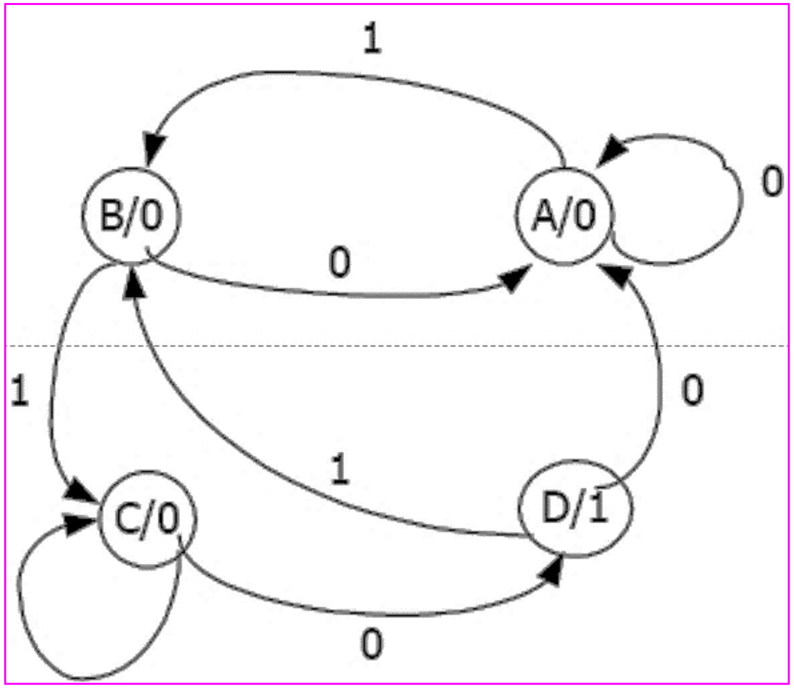
# The Sequential Circuit: Analysis

IV. Assign the name of present state: A = [$y_1$ $y_2$] = [00], B = [01], C = [11] and D = [10]. Then obtain the state table (NS/$z$).

| PS \ x | 0 | 1 | z |
|---|---|---|---|
| A | A | B | 0 |
| B | A | C | 0 |
| C | D | C | 0 |
| D | A | B | 1 |

$Y_1 Y_2$

V. Then the state diagram can be drawn



V. Then find the output for the input x = 110111101… and initial state of 00:

| *t* | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| *x* | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| *y* | *A* | *B* | *C* | *D* | *B* | *C* | *C* | *C* | *D* | *B* | *A* | *A* | *B* |
| *Y* | *B* | *C* | *D* | *B* | *C* | *C* | *C* | *D* | *B* | *A* | *A* | *B* | *A* |
| *Z* | 0 | 0 | **1** | 0 | 0 | 0 | 0 | **1** | 0 | 0 | 0 | 0 | 0 |
| | | | | | | | | | | | | | |