Name: ..... Student ID: .....

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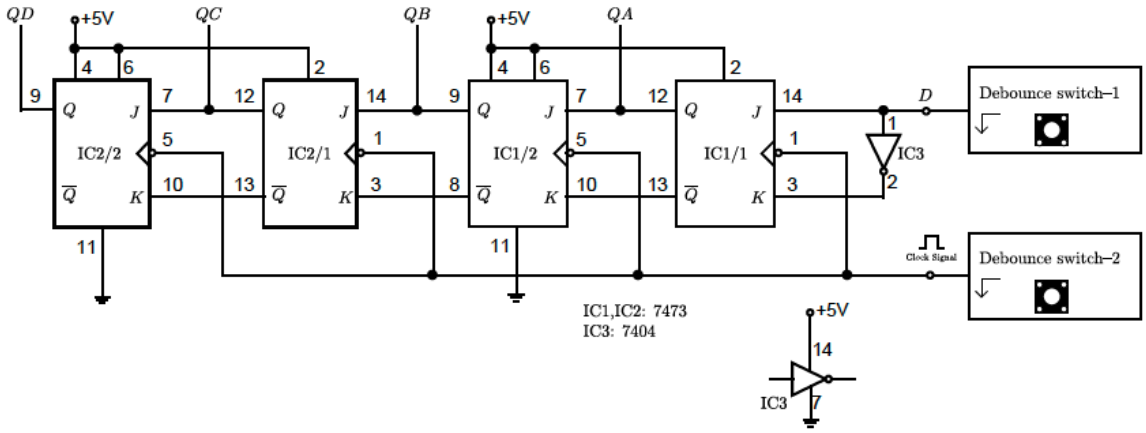
Laboratory 11

Shift Registers

1. Connect a logic circuit as shown in the following figure.



2. Connect output *QA-QD* to the logic monitor, input *D* to the falling edge output of the debounce switch 1 and pin CLK to the falling edge output of the debounce switch 2.
3. Supply the logic as shown in the following table. A clock pulse can be generated and applied to the circuit by pressing the debounce switch 2 once. Observe and record the results.

D	CLK Pulse No.	QA	QB	QC	QD	Remarks
0	1					Press and hold debounce SW 1
0	2					Press and hold debounce SW 1
0	3					Press and hold debounce SW 1
0	4					Press and hold debounce SW 1
1	5					Release de-bounce SW 1
0	6					Press and hold debounce SW 1
0	7					Press and hold debounce SW 1

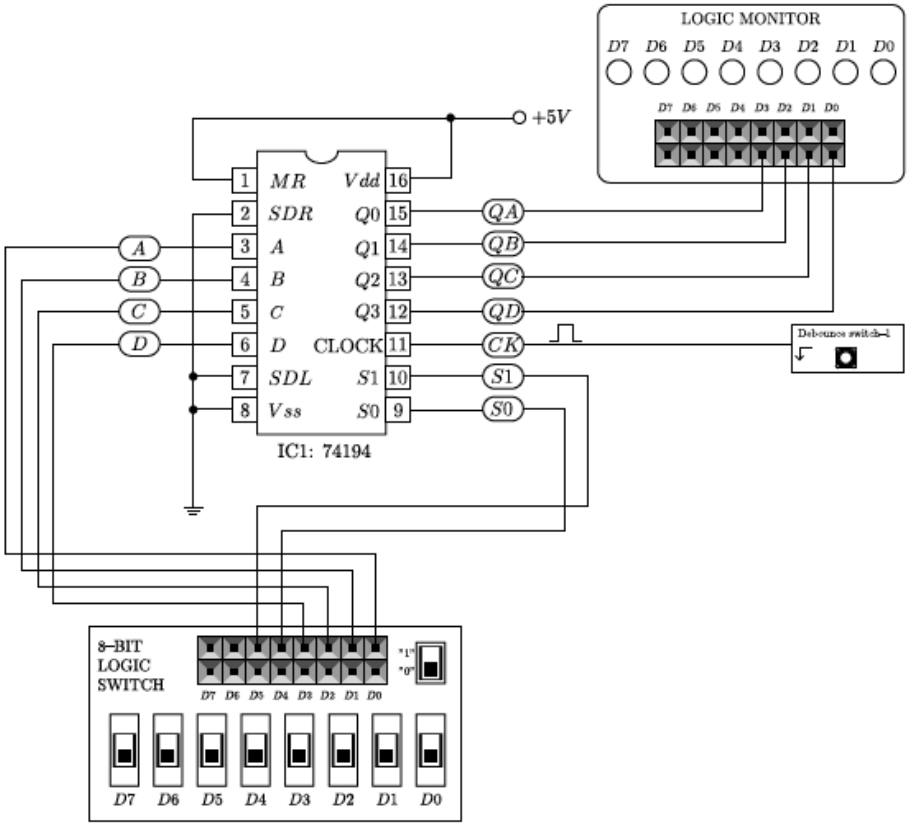
D	CLK Pulse No.	QA	QB	QC	QD	Remarks
0	8					Press and hold debounce SW 1
0	9					Press and hold debounce SW 1
0	10					Press and hold debounce SW 1

Instructor's signature

4. What can be concluded from the previous experiment?

Instructor's signature

5. Connect the circuit as shown in the following figure



The operation mode of IC 74194 is given as in the following table.

Mode	S1	S0
Parallel data input	1	1
Data latching	0	0
Left shift register	1	0
Right shift register	0	1

6. Connect pin S1, S0 and DCBA to the logic switches. Connect pin CK to the debounce switch 1 and connect output QD-QA to the logic monitor.
7. Supply the input DCBA to be 0011
8. Supply the pulses to pin CK as shown in the following table. A clock pulse can be generated and applied to the circuit by pressing the debounce switch 1 once. Observe and record the results for QD-QA

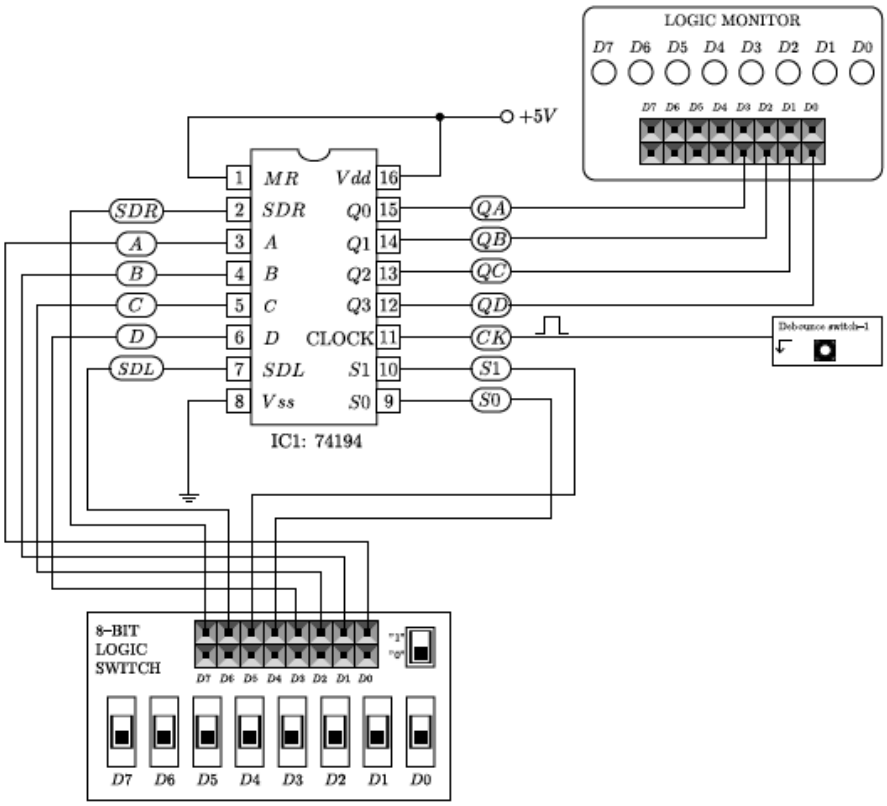
S1	S0	CK pulse No.	QA	QB	QC	QD	Mode
1	1	1					
0	1	2					
0	1	3					
1	0	4					
1	0	5					

Instructor's signature

9. What can be concluded from the previous experiment?

Instructor's signature

10. Connect the circuit as shown in the following figure. Note that SDL and SDR pins are now connected to the logic switches.



11. Supply the logic signal 0000 to the input DCBA.
12. Supply the pulses to pin CK as shown in the following table. A clock pulse can be generated and applied to the circuit by pressing the debounce switch 1 once. Observe and record the results for QD-QA

S1	S0	SDL	SDR	CK pulse No.	QA	QB	QC	QD	Mode
0	1	0	1	1					
0	1	0	1	2					
0	1	0	0	3					
0	1	0	0	4					
0	1	0	0	5					
0	1	0	0	6					
1	0	1	0	7					
1	0	1	0	8					
1	0	0	0	9					
1	0	0	0	10					
1	0	0	0	11					
1	0	0	0	12					

Instructor's signature

13. What can be concluded from the previous experiment?

Instructor's signature

14. **Assignments:**

14.1 Implements the circuit that accepts the serial input. The 4-bit binary output of this circuit should be connected to LED D3 to D0 which D3 is MSB. The LED D4 should active "HIGH" when the output LED D3 to D0 can be divided by 7 otherwise it should active "LOW". If the 4-bit binary output is "1111", D5 should active "HIGH" and D3 to D0 should be cleared.

Instructor's signature

Logic Diagram of frequently used gates