Name: Theepakorn Phayonrat Student ID: 6701132

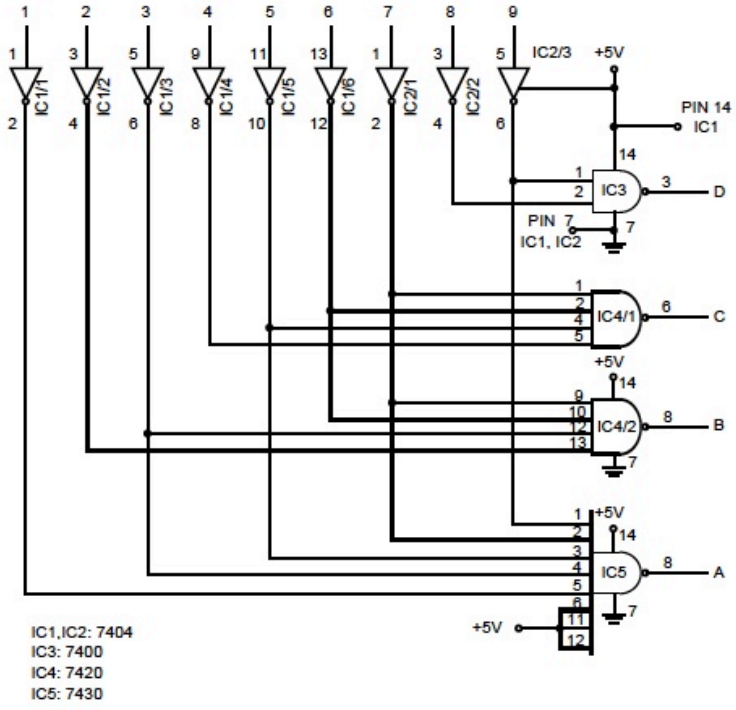
Name: ..... Student ID: .....

Laboratory 8

Encoder and Decoder

1. Encoder:

1.1 Connect a logic circuit as shown in the following figure. Input 1-7 shall be connected to logic switches, which are normally set to 0. Inputs 8-9 shall be connected to a **rising edge** of debounce switch 1 and 2 respectively. All the outputs shall be connected to a logic monitor.



1.2 Set the inputs as shown in the following table. In case the data from input 1-7 are chosen, simply supply logic 1 to the circuit. However, if the data from input 8-9 are chosen, the corresponding debounce switch must be held until the results is recorded.

1.3 Record the results in the table.

1.4 Disconnect the output from the logic monitor and reconnect them to HEX decoder on the board. Redo the experiments as in 1.2 and record the result in the table.

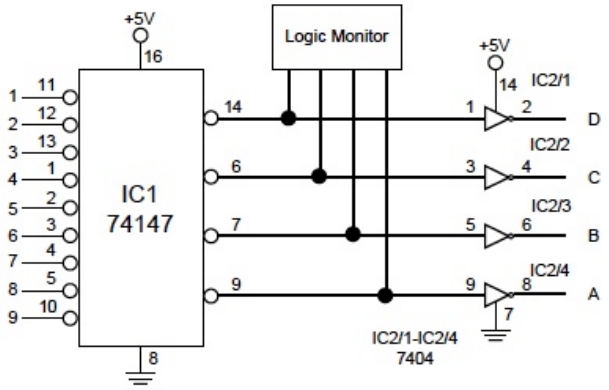
Input									Output				7-Segments
1	2	3	4	5	6	7	8	9	D	C	B	A	LED
0	0	0	0	0	0	0	0	0	0	0	0	0	
1	0	0	0	0	0	0	0	0	0	0	0	1	
0	1	0	0	0	0	0	0	0	0	0	1	0	
0	0	1	0	0	0	0	0	0	0	0	1	1	
0	0	0	1	0	0	0	0	0	0	1	0	0	
0	0	0	0	1	0	0	0	0	0	1	0	1	
0	0	0	0	0	1	0	0	0	0	1	1	0	
0	0	0	0	0	0	1	0	0	0	1	1	1	
0	0	0	0	0	0	0	1	0	1	0	0	0	
0	0	0	0	0	0	0	0	1	1	0	0	1	

1.5 Draw conclusions from the preceding experiment

We were building BCD to binary encoder.

Instructor's signature

1.6 Connect the circuit as shown in the following figure. Note that input 8 and 9 should be connected to the **falling edge** debounce switch 1 and 2 respectively. IC2 is omitted in this experiment and the outputs of IC1 are connected directly to the logic monitor and later to HEX decoder.



1.7 Connect the inputs as shown in the following table and record the corresponding results.

Input									Output				7-Segments
1	2	3	4	5	6	7	8	9	D	C	B	A	LED
1	1	1	1	1	1	1	1	1	1	1	1	1	
1	1	1	1	1	1	1	1	0	0	1	1	0	
1	1	1	1	1	1	1	0	1	0	1	1	1	
1	1	1	1	1	1	0	1	1	1	0	0	0	
1	1	1	1	1	0	1	1	1	1	0	0	1	
1	1	1	1	0	1	1	1	1	1	0	1	0	
1	1	1	0	1	1	1	1	1	1	0	1	1	
1	1	0	1	1	1	1	1	1	1	1	0	0	
1	0	1	1	1	1	1	1	1	1	1	0	1	
0	1	1	1	1	1	1	1	1	1	1	1	0	

1.8 Compare the experiment results of 1.6-1.7 with the results obtained from 1.1-1.4

If we consider the first case of 2nd experiment to be at last case,
we can conclude that the 2nd experiment was the 1st experiment with shift range from 0-9 to 6-F#

Instructor's signature

1.9 Connect IC2 to the outputs of IC1. Its outputs are then connected to the logic monitor and later to HEX decoder.

1.10 Connect the inputs as shown in the following table and record the corresponding results.

Input									Output				7-Segments
1	2	3	4	5	6	7	8	9	D	C	B	A	LED
1	1	1	1	1	1	1	1	1	0	0	0	0	
1	1	1	1	1	1	1	1	0	1	0	0	1	
1	1	1	1	1	1	1	0	1	1	0	0	0	
1	1	1	1	1	1	0	1	1	0	1	1	1	
1	1	1	1	1	0	1	1	1	0	1	1	0	
1	1	1	1	0	1	1	1	1	0	1	0	1	
1	1	1	0	1	1	1	1	1	0	1	0	0	
1	1	0	1	1	1	1	1	1	0	0	1	1	
1	0	1	1	1	1	1	1	1	0	0	1	0	
0	1	1	1	1	1	1	1	1	0	0	0	1	

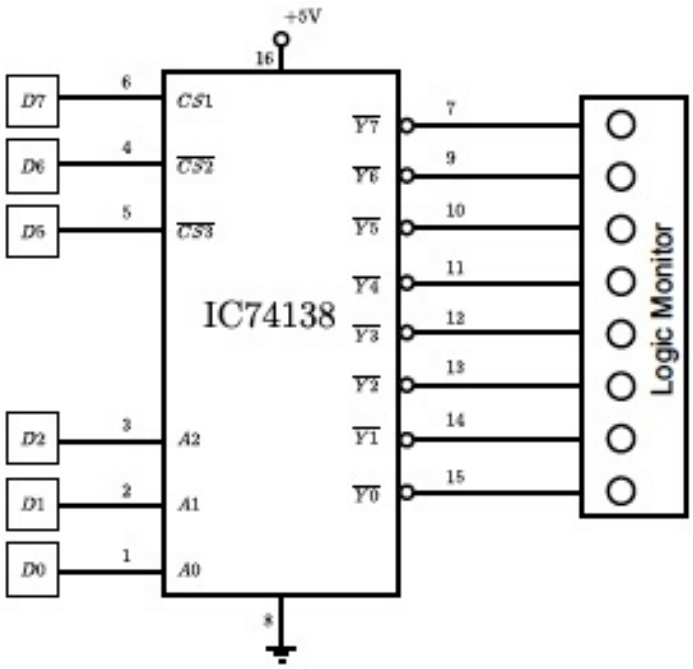
1.11 Compare the experiment results of 1.9-1.10 with the results obtained from 1.1-1.4

We get the same result.

Instructor's signature

2. Decoder:

2.1 Connect the circuit as shown in the following figure.



2.2 Supply the voltage while setting all inputs to 0.

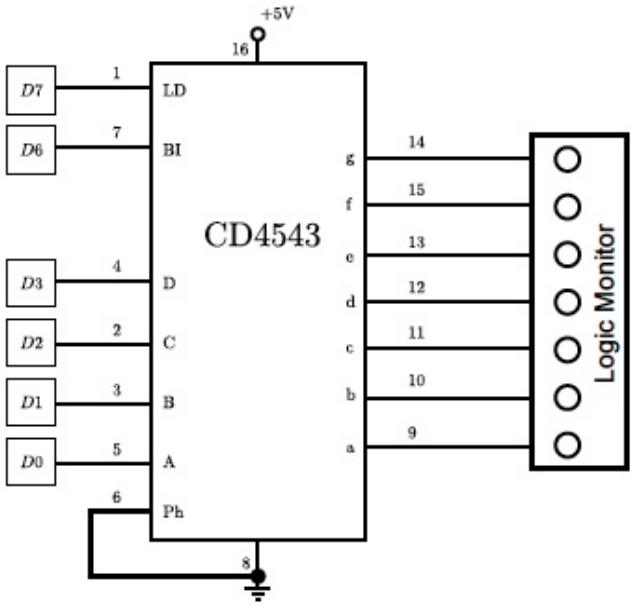
2.3 Change the inputs according to the following table. Observe the status of logic monitor and record the results.

Input						Output							
CS1	CS2'	CS3'	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
0	0	1	X	X	X	1	1	1	1	1	1	1	1
0	1	0	X	X	X	1	1	1	1	1	1	1	1
0	0	0	X	X	X	1	1	1	1	1	1	1	1
1	0	1	X	X	X	1	1	1	1	1	1	1	1
1	1	1	X	X	X	1	1	1	1	1	1	1	1
0	1	1	X	X	X	1	1	1	1	1	1	1	1
1	0	0	0	0	0	0	1	1	1	1	1	1	1
1	0	0	0	0	1	1	0	1	1	1	1	1	1
1	0	0	0	1	0	1	1	0	1	1	1	1	1
1	0	0	0	1	1	1	1	1	0	1	1	1	1
1	0	0	1	0	0	1	1	1	1	0	1	1	1
1	0	0	1	0	1	1	1	1	1	1	0	1	1
1	0	0	1	1	0	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0

Remarks: X can be logic 0 or 1.

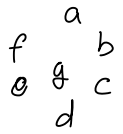
Instructor's signature

2.4 Connect the circuit as shown in the following figure. The input, D,C,B,A, LD and BI shall be connected to the logic switches while the outputs shall be connected to the logic monitor.



2.5 Supply voltage to the circuit and change inputs as shown in the following table.

2.6 Observe the status of the logic monitor and record the results

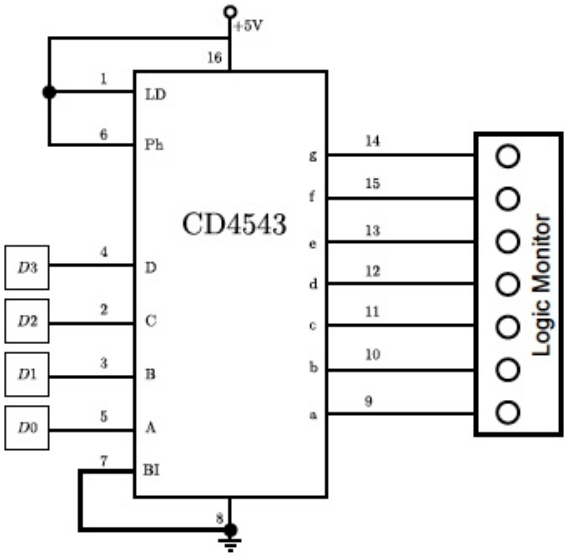


Input						Output							
LD	BI	D	C	B	A	*a*	*b*	*c*	*d*	*e*	*f*	*g*	Display
X	1	X	X	X	X								
1	0	0	0	0	0								
1	0	0	0	0	1								
1	0	0	0	1	0								
1	0	0	0	1	1								
1	0	0	1	0	0								
1	0	0	1	0	1								
1	0	0	1	1	0								
1	0	0	1	1	1								
1	0	1	0	0	0								
1	0	1	0	0	1								
1	0	1	0	1	0								
1	0	1	0	1	1								
1	0	1	1	0	0								
1	0	1	1	0	1								
1	0	1	1	1	0								
1	0	1	1	1	1								
1	0	0	1	1	0								
0	0	0	1	1	1								
0	0	0	0	1	1								

Remarks: X can be logic 0 or 1.

Instructor's signature

2.7 Connect the circuit as shown in the following figure. The input D, C, B, A, LD and BI shall be connected to logic switches while the output shall be connected to the logic monitor.



2.8 Supply the voltage to the circuit and change the inputs as shown in the following table

2.9 Observe the status of logic monitor and record the results.

Inputs				Outputs								
D	C	B	A	*a*	*b*	*c*	*d*	*e*	*f*	*g*	Display	Inverse of Display
0	0	0	0									
0	0	0	1									
0	0	1	0									
0	0	1	1									
0	1	0	0									
0	1	0	1									
0	1	1	0									
0	1	1	1									
1	0	0	0									

Inputs				Outputs								
1	0	0	1									
D	C	B	A	*a*	*b*	*c*	*d*	*e*	*f*	*g*	Display	Inverse of Display
1	0	1	0									
1	0	1	1									
1	1	0	0									
1	1	0	1									
1	1	1	0									
1	1	1	1									

Instructor's signature

3. Assignments

3.1 Design a circuit, which receives decimal number 0-9 as its inputs, encodes them to BCD, change to base 6 and decodes them. The output shall be display on 7-segments as follows.

Decimal Inputs	7-Segments Outputs
0	00
1	01
2	02
3	03
4	04
5	05
6	10
7	11
8	12
9	13

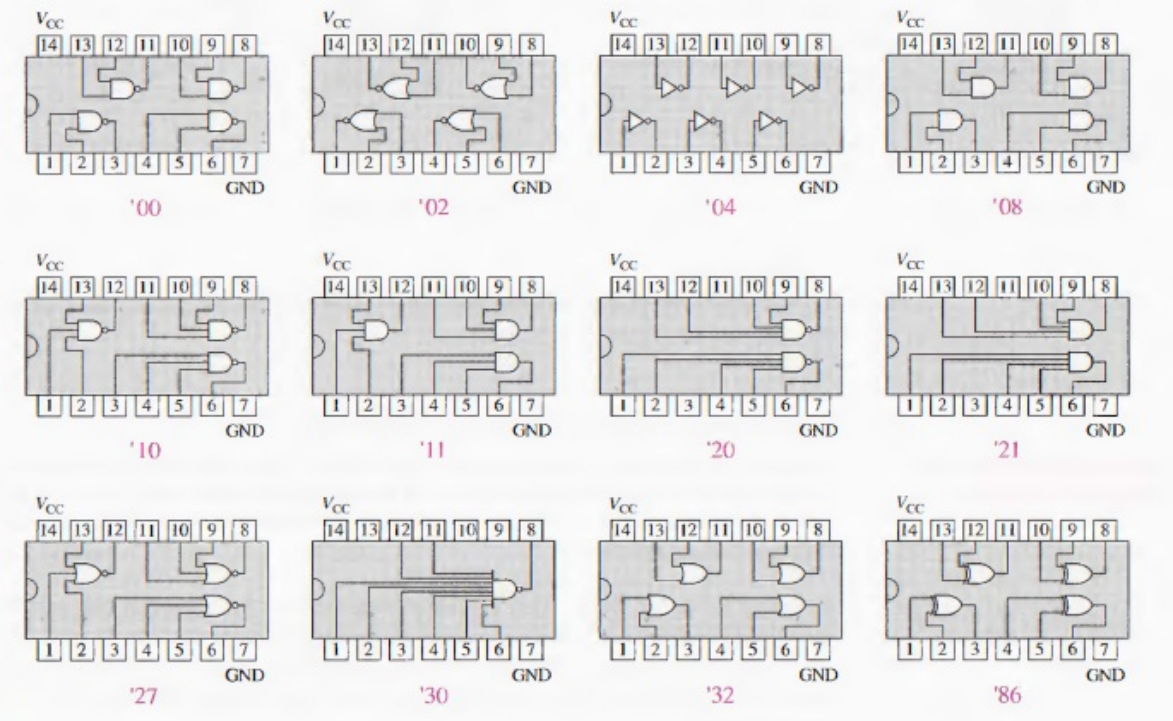
Instructor's signature

3.2 Use a decoder IC 74138 and some other necessary gates to express the following function

$$f(a,b,c) = \Sigma m(0,2,5,7)$$

Instructor's signature

Logic Diagram of frequently used gates



Theepakorn Phanyarat 6701352

3.1 Design a circuit, which receives decimal number 0-9 as its inputs, encodes them to BCD, change to base 6 and decodes them. The output shall be display on 7-segments as follows.

Decimal Inputs	7-Segments Outputs
0	00
1	01
2	02
3	03
4	04
5	05
6	10
7	11
8	12
9	13

Dec	A	B	C	D	O_3	O_2	O_1	O_0
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	0	0	0	1	0
3	0	0	1	1	0	0	1	1
4	0	1	0	0	0	1	0	0
5	0	1	0	1	0	1	0	1
6	0	1	1	0	1	0	0	0
7	0	1	1	1	1	0	0	1
8	1	0	0	0	1	0	1	0
9	1	0	0	1	1	0	1	1

$O_0 = D$

AB \ CD	00	01	11	10
00	0	1	1	0
01	0	1	1	0
11	x	x	x	x
10	0	1	x	x

$O_1 = A + \bar{B}C$

AB \ CD	00	01	11	10
00	0	0	1	1
01	0	0	0	0
11	x	x	x	x
10	1	1	x	x

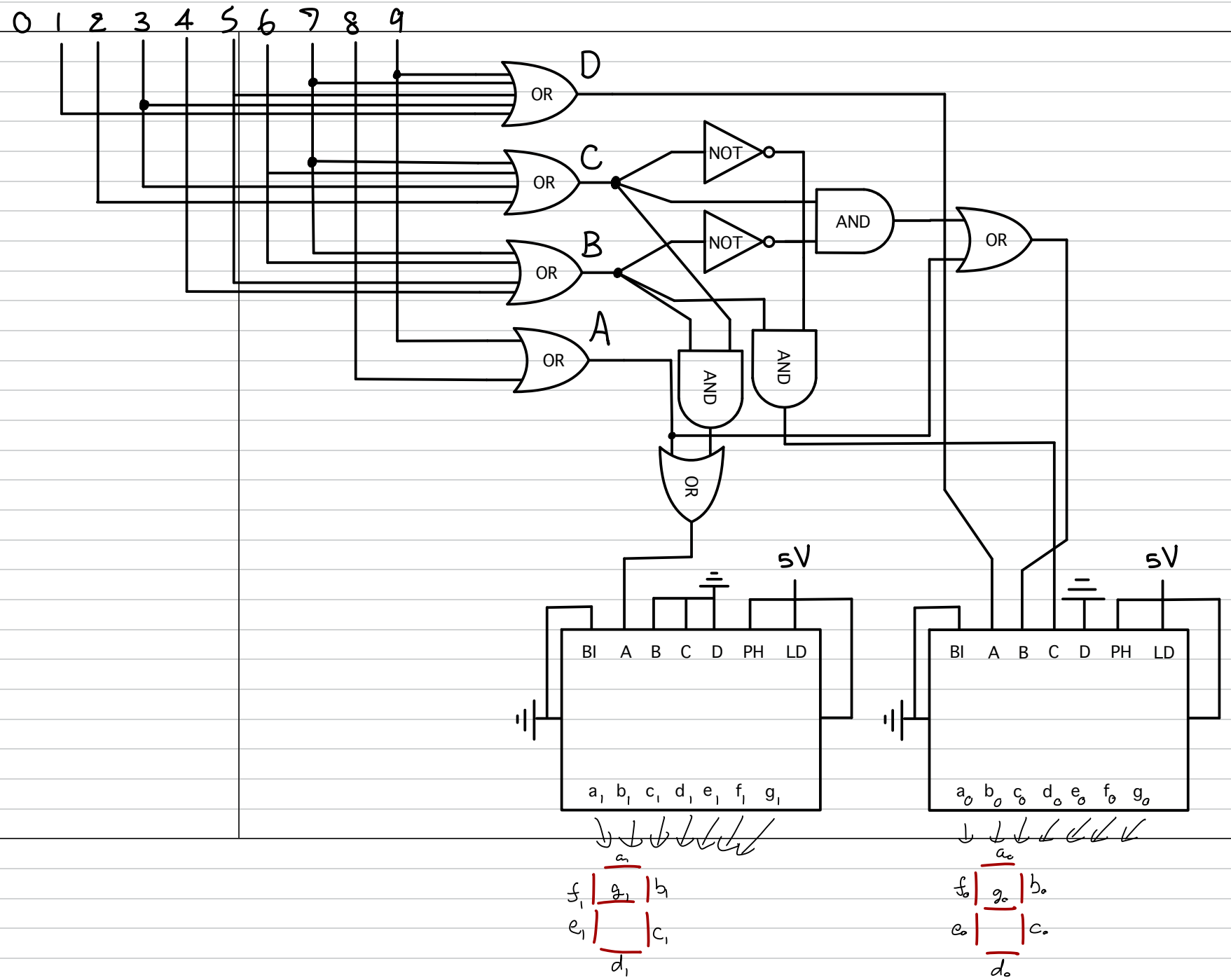
$O_2 = B\bar{C}$

AB \ CD	00	01	11	10
00	0	0	0	0
01	1	1	0	0
11	x	x	x	x
10	0	0	x	x

$O_3 = A + BC$

AB \ CD	00	01	11	10
00	0	0	0	0
01	0	0	1	1
11	x	x	x	x
10	1	1	x	x

Theepakorn Phayomhat 6701352



Theepakorn Phayomhat 6511352

3.2 Use a decoder IC 74138 and some other necessary gates to express the following function

$$f(a,b,c) = \Sigma m(0,2,5,7)$$