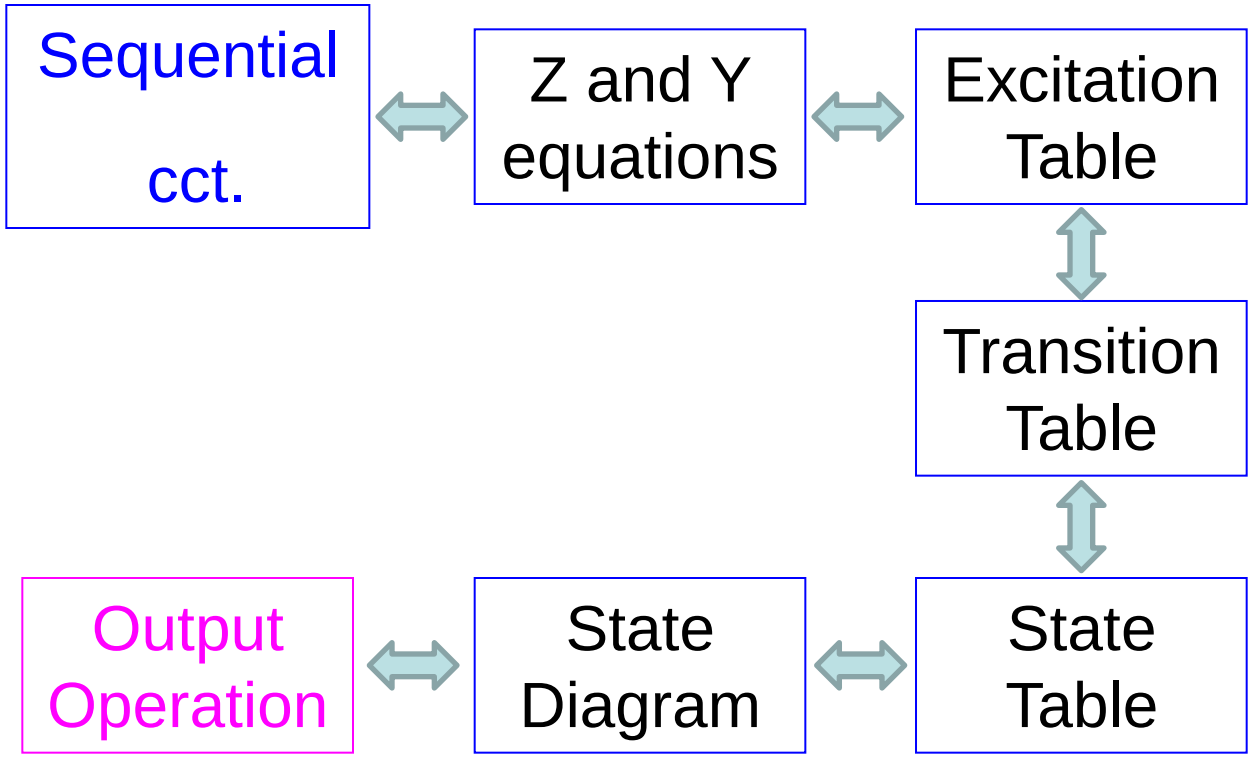
12

Synchronous Sequential Circuit Design

Circuit Analysis ➔



Circuit Design ➔

Synchronous Sequential Circuit Design

Design Principles : follows these steps

1) Find the state diagram and state table from the given assignments;

2) Assign the appropriate codes for the state names,

such as A = 00, B = 01, C = 11 and D = 10.

3) Write the transition table and excitation map of the desired flip-flops,

4) Write the k-map between the inputs of logical inputs and present states (PS) for individual outputs of next states (NS) and logical outputs.

5) Write the logic equations from the k-map and create the corresponding circuit.

Synchronous Sequential Circuit Design: Example

Example For the given state table, design a synchronous sequential cct.
Using A) D flipflop
B) JK flipflop

PS \ X	0	1
A	A/0	B/0
B	A/0	C/1
C	B/0	D/0
D	C/1	D/0

NS/Z

A) Using **D flip-flops**:

1) From the given state table,

2) Since there are 4 states, we need 2 D flip-flops.

We can assign the state variable codes y_1y_2,

by setting A = 00, B = 01, C = 11 and D = 10.

Y_1Y_2 \ X	0	1
00	00 / 0	01 / 0
01	00 / 0	11 / 1
11	01 / 0	10 / 0
10	11 / 1	10 / 0

Y_1Y_2 / Z

3) Write the transition table,

Synchronous Sequential Circuit Design: Example

Since using D flip-flops, whose state equation is D = Y;

So $D_1 = Y_1$ and $D_2 = Y_2$

Then get excitation maps of both D flip-flops.

Y_1Y_2 \ X	0	1
00	00 / 0	01 / 0
01	00 / 0	11 / 1
11	01 / 0	10 / 0
10	11 / 1	10 / 0

Y_1Y_2 / Z

Y_1Y_2 \ X	0	1
00	00 / 0	01 / 0
01	00 / 0	11 / 1
11	01 / 0	10 / 0
10	11 / 1	10 / 0

Y_1Y_2 / Z

Y_1Y_2 \ X	0	1
00	00 / 0	01 / 0
01	00 / 0	11 / 1
11	01 / 0	10 / 0
10	11 / 1	10 / 0

Y_1Y_2 / Z

Synchronous Sequential Circuit Design: Example

4) Write the k-map between the inputs of logical inputs and PS for individual outputs of next states (NS) and logical outputs.

Y_1Y_2 \ X	0	1
00	00 / 0	01 / 0
01	00 / 0	11 / 1
11	01 / 0	10 / 0
10	11 / 1	10 / 0

Y_1Y_2 / Z

Y_1Y_2 \ X	0	1
00	00 / 0	01 / 0
01	00 / 0	11 / 1
11	01 / 0	10 / 0
10	11 / 1	10 / 0

Y_1Y_2 / Z

Y_1Y_2 \ X	0	1
00	00 / 0	01 / 0
01	00 / 0	11 / 1
11	01 / 0	10 / 0
10	11 / 1	10 / 0

Y_1Y_2 / Z

y_1y_2 \ X	0	1
00	0	0
01	0	1
11	0	1
10	1	1

D_1

y_1y_2 \ X	0	1
00	0	1
01	0	1
11	1	0
10	1	0

D_2

\ X	0	1
00	0	0
01	0	1
11	0	0
10	1	0

$D_1 = y_1\overline{y}_2 + x\,y_2$

$D_2 = \overline{x}\,y_1 + x\,\overline{y}_1 = x \oplus y_1$

$Z = x\,\overline{y}_1 y_2 + \overline{x}\,y_1\overline{y}_2$

Synchronous Sequential Circuit Design: Example

5) Write the logic equations

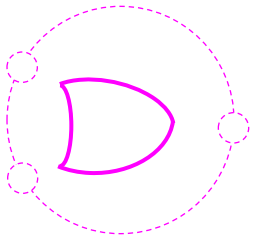
from the k-map

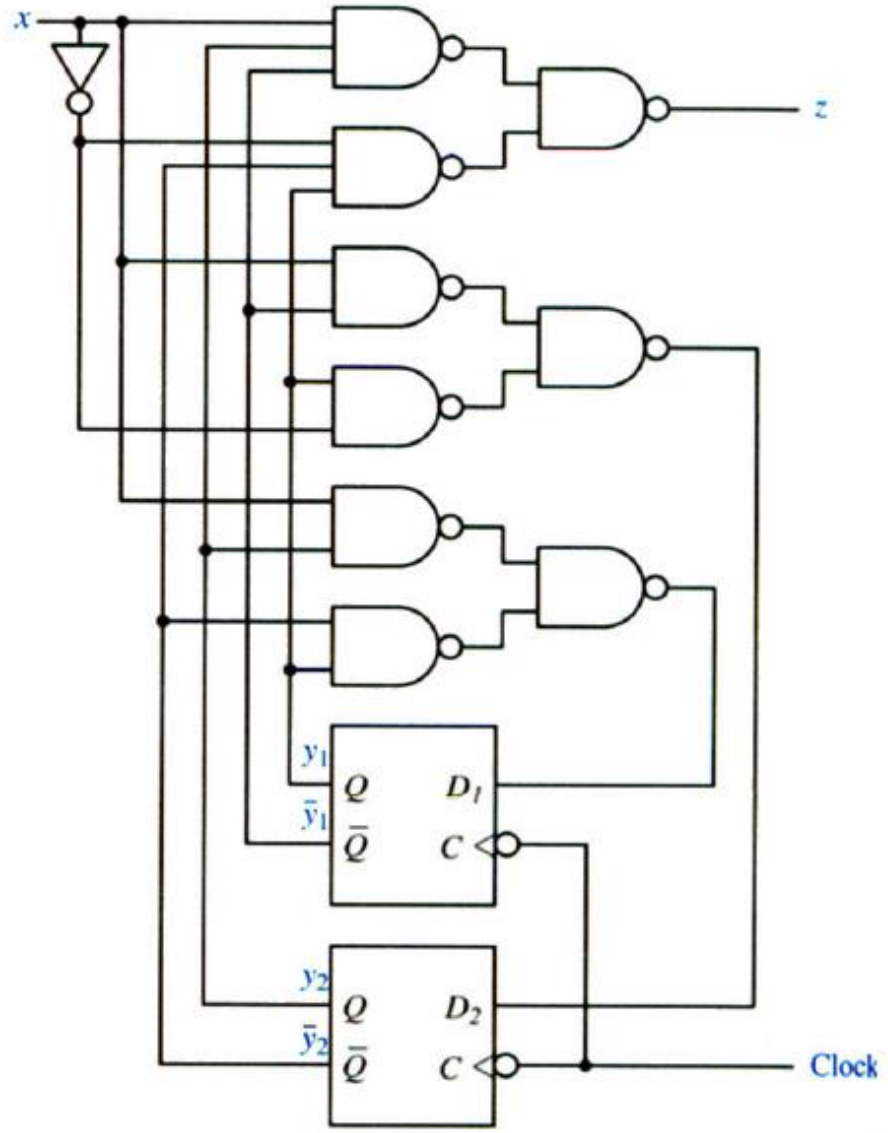
and draw the corresponding circuit.

$$Z = x\bar{y}_1 y_2 + \bar{x} y_1 \bar{y}_2$$

$$D_1 = y_1 \bar{y}_2 + x y_2$$

$$D_2 = \bar{x} y_1 + x \bar{y}_1 = x \oplus y_1$$





Synchronous Sequential Circuit Design: Example

A) Using **JK flip-flops**:

1) From the given state table,

2) Since there are 4 states, we need 2 JK flip-flops.

We can assign the state variable codes y_1y_2,

by setting A = 00, B = 01, C = 11 and D = 10.

3) Write the transition table,

PS \ X	0	1
A	A/0	B/0
B	A/0	C/1
C	B/0	D/0
D	C/1	D/0

NS/Z

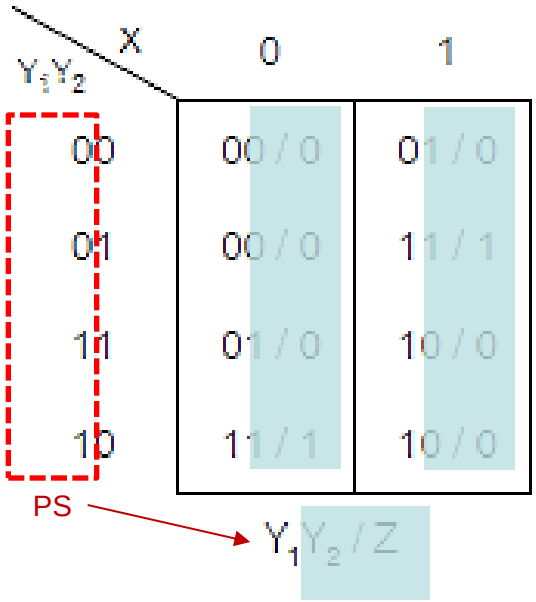
Y_1Y_2 \ X	0	1
00	00 / 0	01 / 0
01	00 / 0	11 / 1
11	01 / 0	10 / 0
10	11 / 1	10 / 0

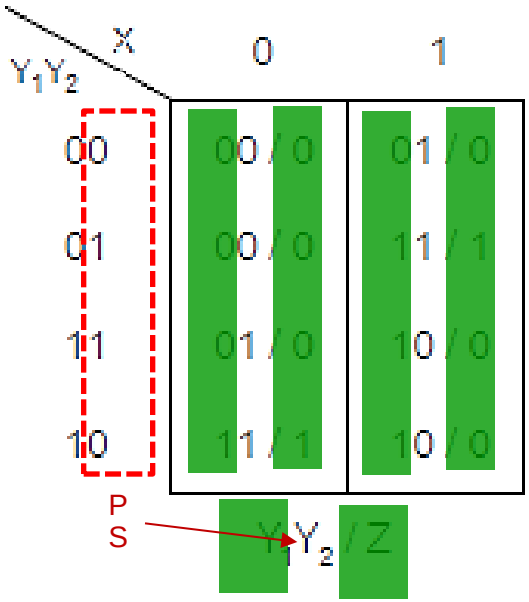
Y_1Y_2 / Z

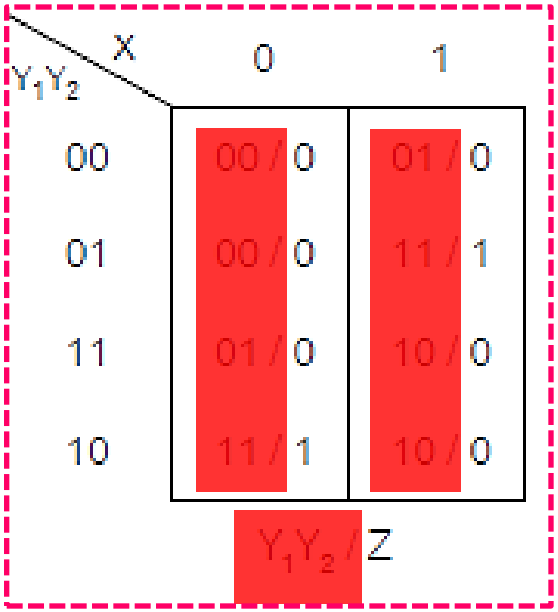
Synchronous Sequential Circuit Design: Example

Then get excitation maps of both JK flip-flops.

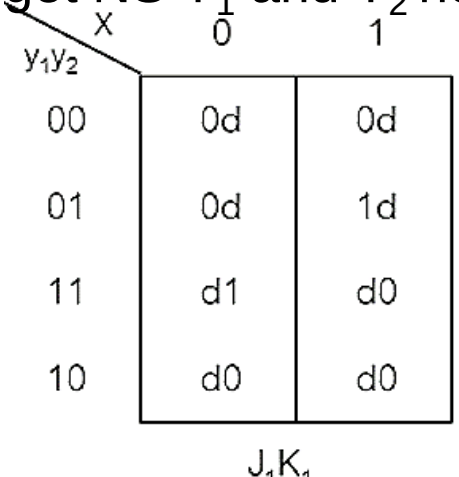
The same as D FF

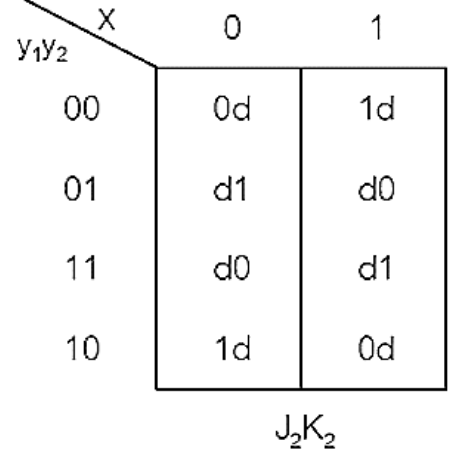


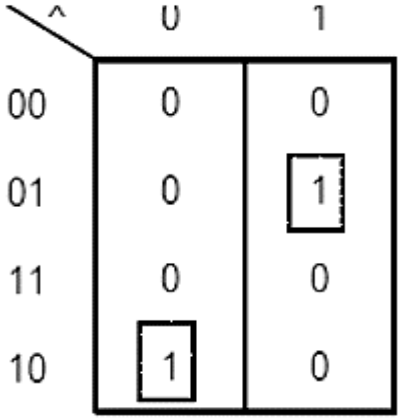




To get NS Y_1 and Y_2 need to apply at JK inputs by $[J_1K_1] = Y_1$ and $[J_2K_2] = Y_2$.

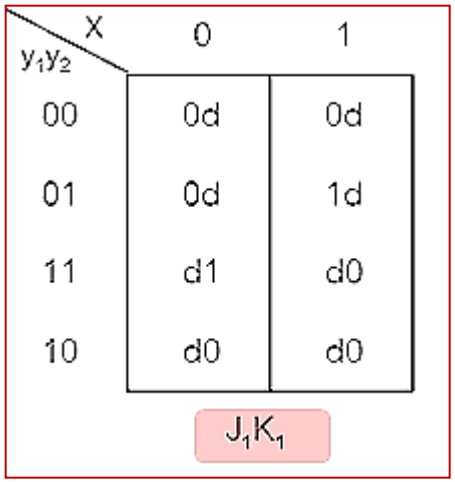






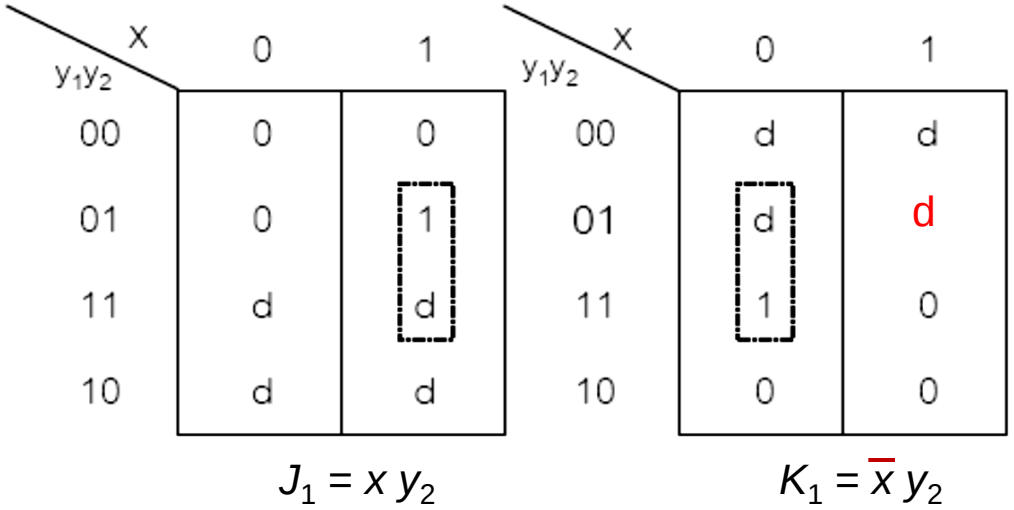
Synchronous Sequential Circuit Design: Example

4) Write the k-map between the inputs of logical inputs and PS for individual outputs of next states (NS) and logical outputs.



y_1y_2 \ X	0	1
00	0d	0d
01	0d	1d
11	d1	d0
10	d0	d0

J_1K_1

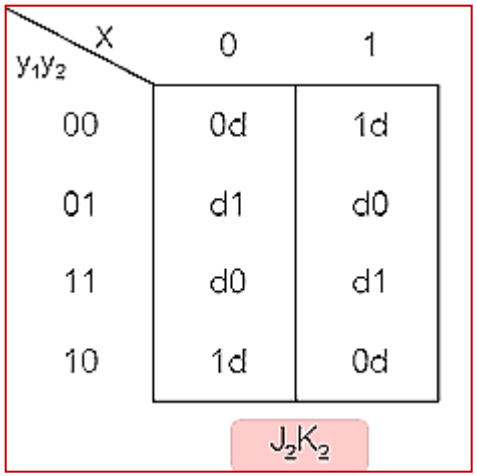


y_1y_2 \ X	0	1
00	0	0
01	0	1
11	d	d
10	d	d

$J_1 = x\, y_2$

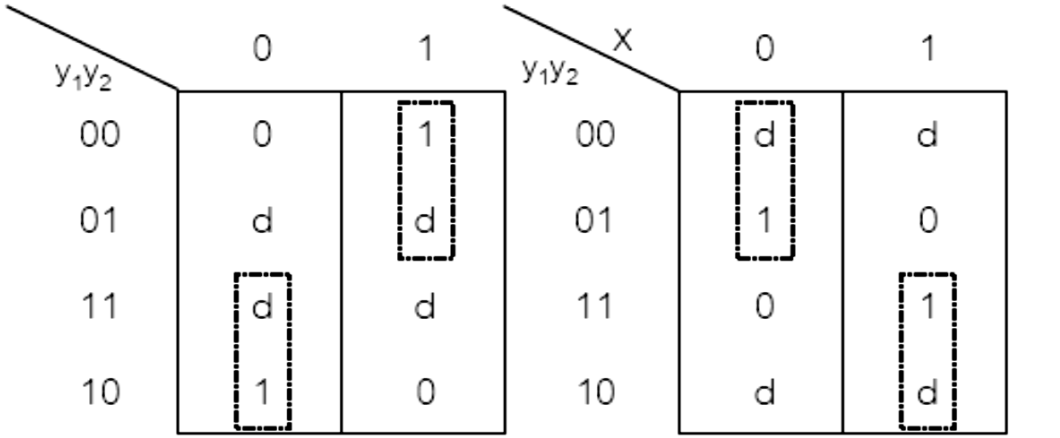
y_1y_2 \ X	0	1
00	d	d
01	d	d
11	1	0
10	0	0

$K_1 = \overline{x}\, y_2$



y_1y_2 \ X	0	1
00	0d	1d
01	d1	d0
11	d0	d1
10	1d	0d

J_2K_2



y_1y_2 \ X	0	1
00	0	1
01	d	d
11	d	d
10	1	0

$J_2 = x\, \overline{y}_1 + \overline{x}\, y_1$

$J_2 = x \oplus y_1$

y_1y_2 \ X	0	1
00	d	d
01	1	0
11	0	1
10	d	d

$K_2 = x\, y_1 + \overline{x}\, \overline{y}_1$

$K_2 = \overline{x \oplus y_1}$

Synchronous Sequential Circuit Design: Example

5) Write the logic equations

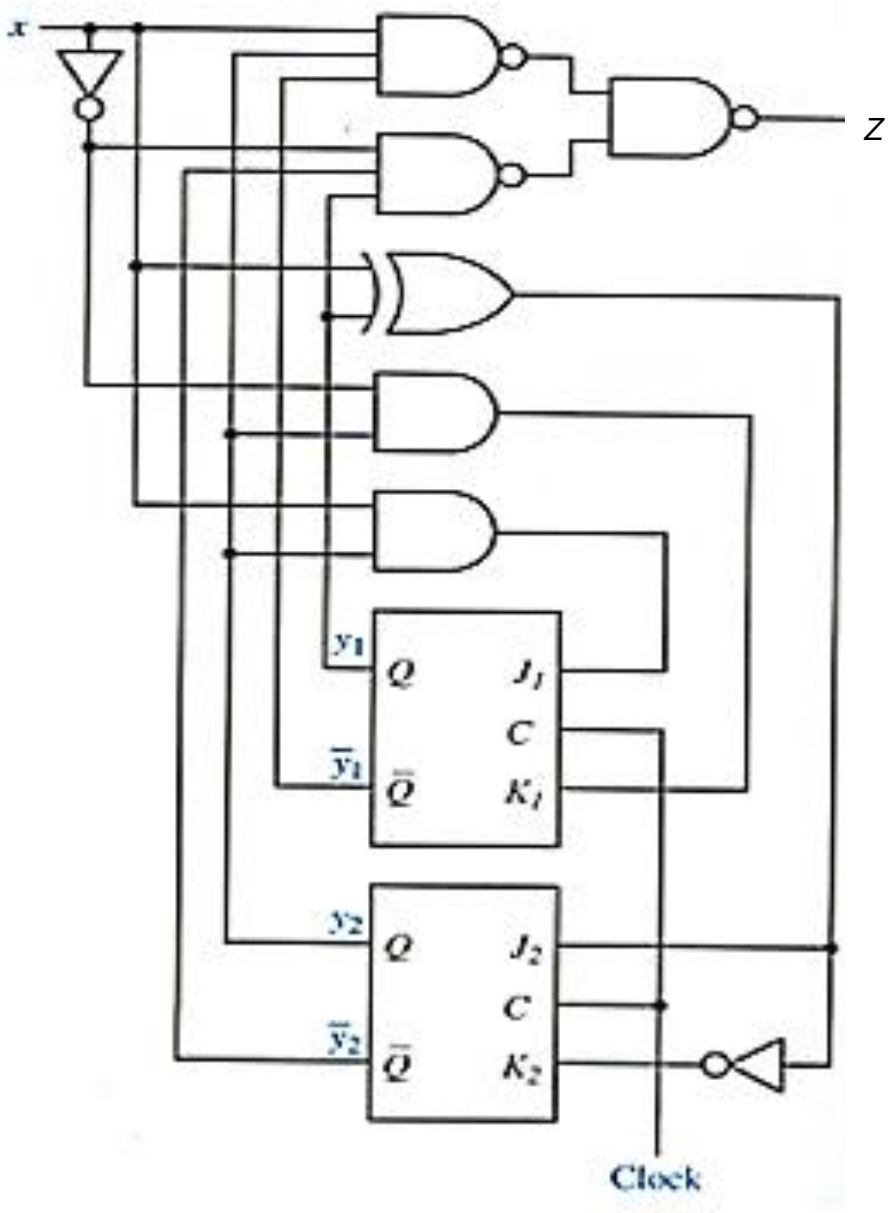
from the k-map

and draw the corresponding circuit.

$$Z = x\bar{y}_1 y_2 + \bar{x} y_1 \bar{y}_2$$

$J_1 = x\, y_2$ $\qquad$ $K_1 = \bar{x}\, y_2$

$J_2 = x \oplus y_1$ $\qquad$ $K_2 = \overline{x \oplus y_1}$

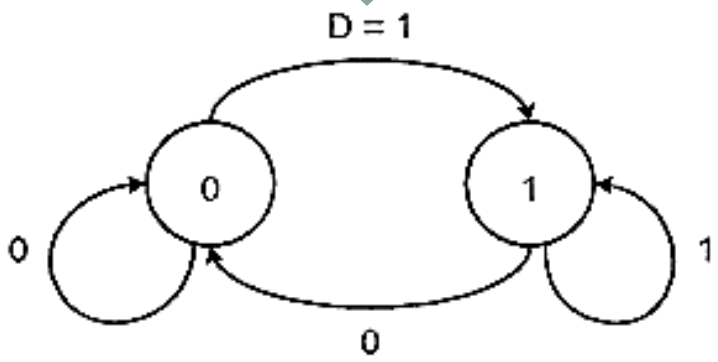


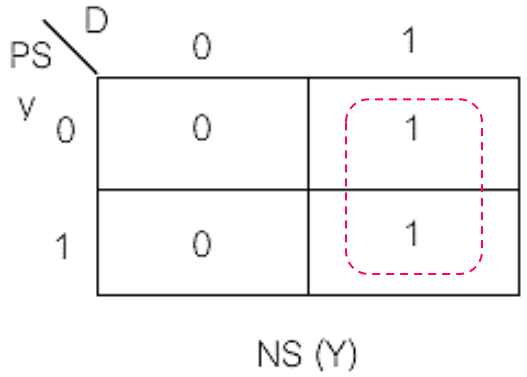
Flip-Flop Excitation Tables

Flip-flop input table

- In the previous example, we find that the excitation equations for the circuit with D FF is easier than that with JK FF.
- This is because D FF has the state equation, NS: Y = D
- The state equation can be derived from state diagram, excitation table and minimizing it in K-Map (transition table) as shown below:

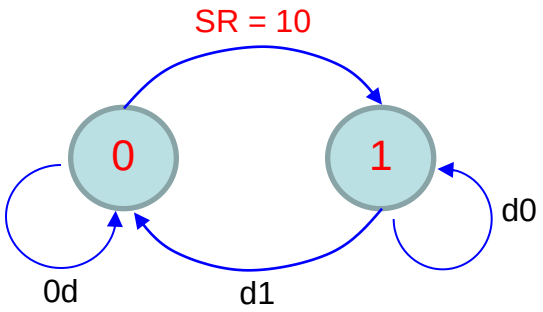
State Transitions $Q(t)$	$Q(t+\epsilon)$	Required Inputs $D(t)$
0	0	0
0	1	1
1	0	0
1	1	1





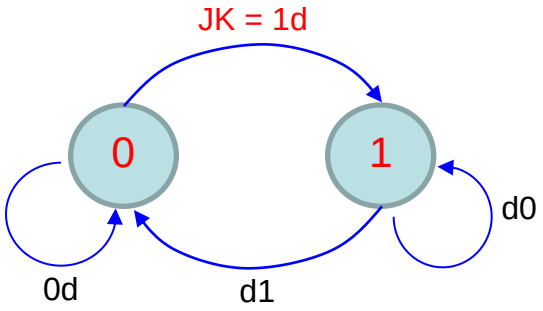
D Flip-flop: Y = D

Flip-Flop Excitation Tables



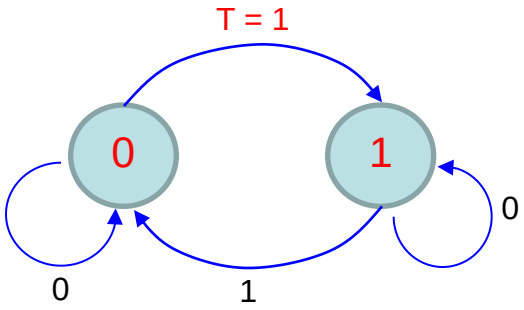
SR Flipflop

$Y = S + \overline{R}\, y$



JK Flipflop

$Y = J\,\overline{y} + \overline{K}\, y$



T Flipflop

$Y = T\,\overline{y} + \overline{T}\, y$

Synchronous Sequential Circuit Design: Example

Example From the State table below, design the Synchronous Sequential circuit using **a) D flip-flop** and **b) JK flip-flop**.

Step I: Assign the state codes:

- Let A = 000, B = 001, C = 010, D = 011 and E = 100
- And set the rest unused states (101, 110, 111) as Don't Care = ddd/d.

Step II: Change the state name to state codes, then get the transition table;

Input Variables: y_1, y_2, y_3 และ x

$y_1y_2y_3$	PS	X = 0	X = 1
000	A	B / 0	E / 0
001	B	A / 1	C / 1
010	C	B / 0	C / 0
011	D	C / 0	E / 0
100	E	D / 1	A / 0

NS/Z

	$y_1y_2y_3$	X = 0	X = 1
A	000	001 / 0	100 / 0
B	001	000 / 1	010 / 1
C	010	001 / 0	010/0
D	011	010 / 0	100 / 0
E	100	011/1	000 / 0
d	101	ddd / d	ddd / d
d	110	ddd / d	ddd / d
d	111	ddd / d	ddd / d

$Y_1Y_2Y_3$ / Z

Output Variables: Y_1, Y_2, Y_3 และ Z

Circuit Design: Example for D Flip-Flop.

Step III: Write individual outputs in the transition table in separated K-Maps:

$y_1y_2y_3$	x = 0	x = 1
A 000	001 / 0	100 / 0
B 001	000 / 1	010 / 1
C 010	001 / 0	010 / 0
D 011	010 / 0	100 / 0
E 100	011 / 1	000 / 0
d 101	ddd / d	ddd / d
d 110	ddd / d	ddd / d
d 111	ddd / d	ddd / d

$Y_1Y_2\,Y_3 / Z$

D_2

y_3x / y_1y_2	00	01	11	10
00				
01				
11				
10				

D_3

y_3x / y_1y_2	00	01	11	10
00				
01				
11				
10				

Z

y_3x / y_1y_2	00	01	11	10
00				
01				
11				
10				

y_3x / y_1y_2	00	01	11	10
00	0	1	0	0
01	0	0	1	0
11	d	d	d	d
10	0	0	d	d

$$D_1 = x\,\bar{y}_1\,\bar{y}_2\,\bar{y}_3 + x\,y_2\,y_3$$

Circuit Design: Example for JK Flip-Flop.

Step III: Write individual outputs in the transition table in separated K-Maps:

	$y_1y_2y_3$	X = 0	X = 1
A	000	001 / 0	100 / 0
B	001	000 / 1	010 / 1
C	010	001 / 0	010 / 0
D	011	010 / 0	100 / 0
E	100	011 / 1	000 / 0
d	101	ddd / d	ddd / d
d	110	ddd / d	ddd / d
d	111	ddd / d	ddd / d

$Y_1Y_2\,Y_3 / Z$

J_1K_1

y_1y_2 \ y_3X	00	01	11	10
00	0d	1d	0d	0d
01	0d	0d	1d	0d
11	dd	dd	dd	dd
10	d1	d1	dd	dd

J_2K_2

y_1y_2 \ y_3X	00	01	11	10
00				
01				
11				
10				

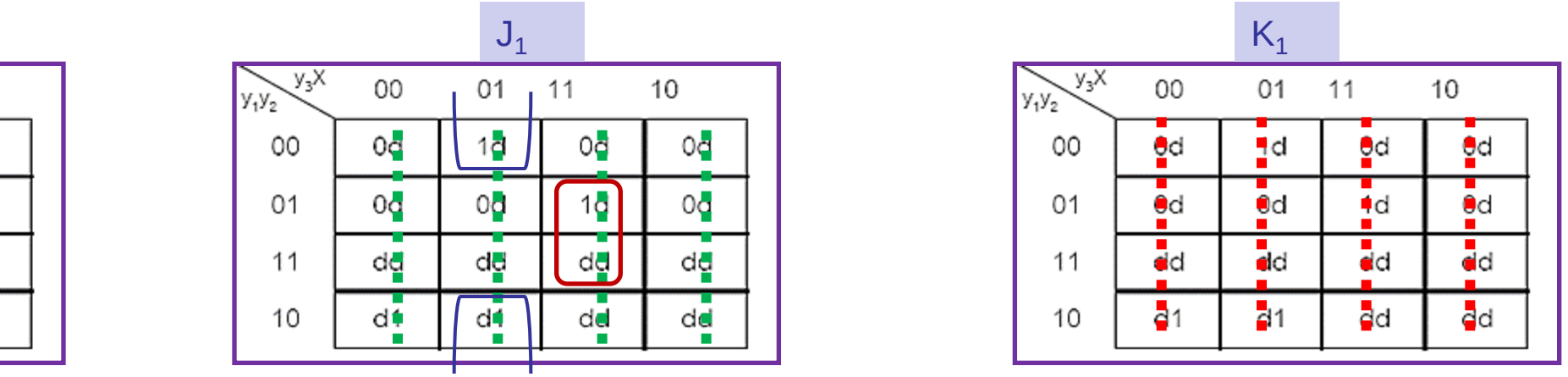
J_3K_3

y_1y_2 \ y_3X	00	01	11	10
00				
01				
11				
10				

y_1y_2 \ y_3X	00	01	11	10
00	0	0	1	1
01	0	0	0	0
11	d	d	d	d
10	1	0	d	d

$Y_1 = D_1$

Synchronous Sequential Circuit Design: Example



Then we get these equations:

$$J_1 = (y_2 \odot y_3)x \qquad K_1 = 1$$

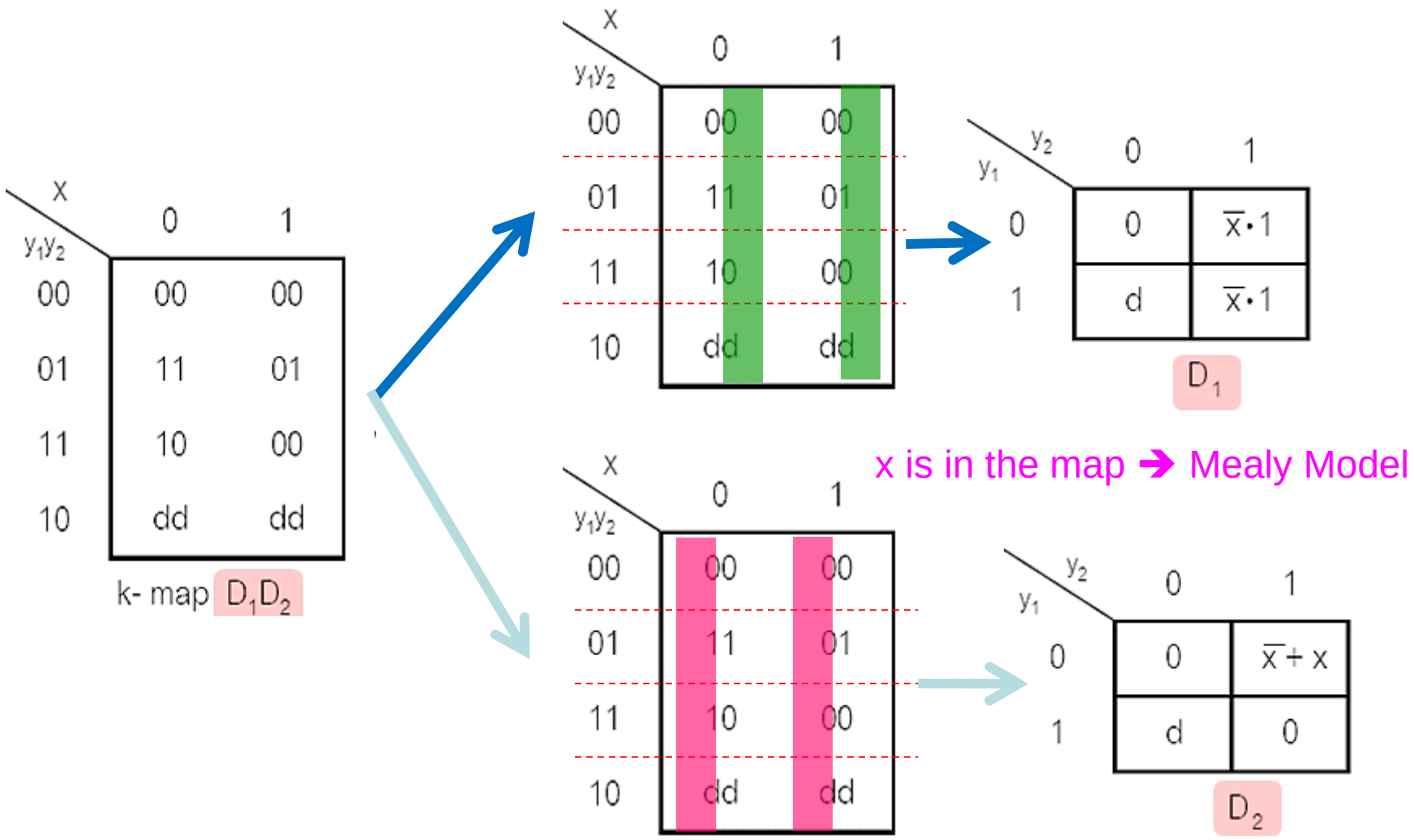
$$J_2 = y_3x + y_1\overline{y}_3x \qquad K_2 = (y_3 \odot x)$$

$$J_3 = \overline{x} \qquad K_3 = 1$$

$$Z = \overline{y}_2 y_3 + y_1\overline{x} + y_2\overline{y}_3x$$

Equation Reduction By Variable Entry Map (VEM)

Example: We can reduce the equation in a system with **two** D Flip-Flops, as follows:



Equation Reduction By Variable Entry Map (VEM)

Example: We can reduce the equation by VEM in a system with **three** D Flip-Flops, as follows:

y_3x / y_1y_2	00	01	11	10
00	0	1	0	0
01	0	0	1	0
11	d	d	d	d
10	0	0	d	d

Y_1 of First D FF

y_1y_2 \ y_3	0	1
00	x	0
01	0	x
11	d	d
10	0	d

Y_1 of First D FF

x is in the map ➔ Mealy Model

K-Map Transform From D FF to JK FF

Converting a K-map table of D flipflop to a k-map of JK flipflop

- For a transition table, finding a K-map for D flip-flop is easier than that of JK flip-flop;
- Firstly, we prefer to design with D flip-flop to produce the excitation table;
- Then transform it to that of the JK flip-flop (the most popular);
- Finally, we get the logic equation for that circuit.

Principles from state equation of D flipflop: $Y = D$

and the equation of JK flipflop: $Y = J\bar{y} + \bar{K}y$

Then get the relationship: $D = J\bar{y} + \bar{K}y$

So, we can separate the excitation Maps for J and K as :

Map J : $D = J\bar{y}$

For y = 0 ➔ $J = Y = D$

For y = 1 ➔ $J = d$

Map K : $D = \bar{K}y$

For y = 0 ➔ $K = d$

For y = 1 ➔ $K = \bar{Y} = \bar{D}$

K-Map Transform From D FF to JK FF

Example From the first example, transform the K-map of individual outputs D FF/JK FF to those of the JK FF.

Solution From the results of D FF

y_1y_2 \ x	0	1
00	0	0
01	0	1
11	0	1
10	1	1

Map J : $D = J\bar{y}$

$y = 0 \rightarrow J = Y = D$

$y = 1 \rightarrow J = d$

Map K : $D = \bar{K}y$

$y = 0 \rightarrow K = d$

$y = 1 \rightarrow K = \bar{Y} = \bar{D}$

y_1y_2 \ x	0	1
00	0	0
01	0	1
11	0	1
10	1	1

$J_1 = y_2\, x$

y_1y_2 \ x	0	1
00	0	0
01	0	1
11	0	1
10	1	1

$\bar{K}_1 = y_2\, x$

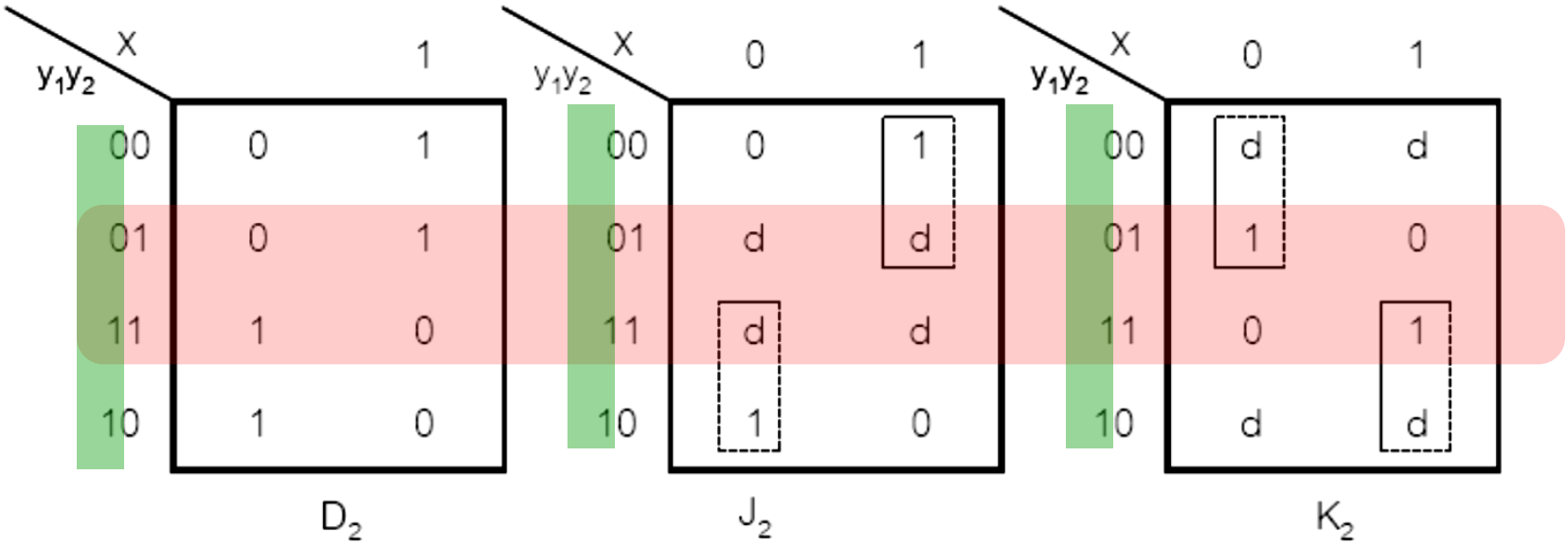
d	d
d	d

1	0
0	0

$K_1 = y_2\, x$

d	d
d	d

K-Map Transform From D FF to JK FF



$$\therefore J_2 = y_1\overline{x} + \overline{y}_1 x = x \oplus y_1 \qquad \therefore K_2 = \overline{y}_1\overline{x} + y_1 x = x \odot y_1$$

We get the same solution as done in the first example, but much easier.

Map J : D = J $\overline{y}$

y = 0 ➔ J =Y = D

y = 1 ➔ J = d

Map K : D = $\overline{K}$ y

y = 0 ➔ K = d

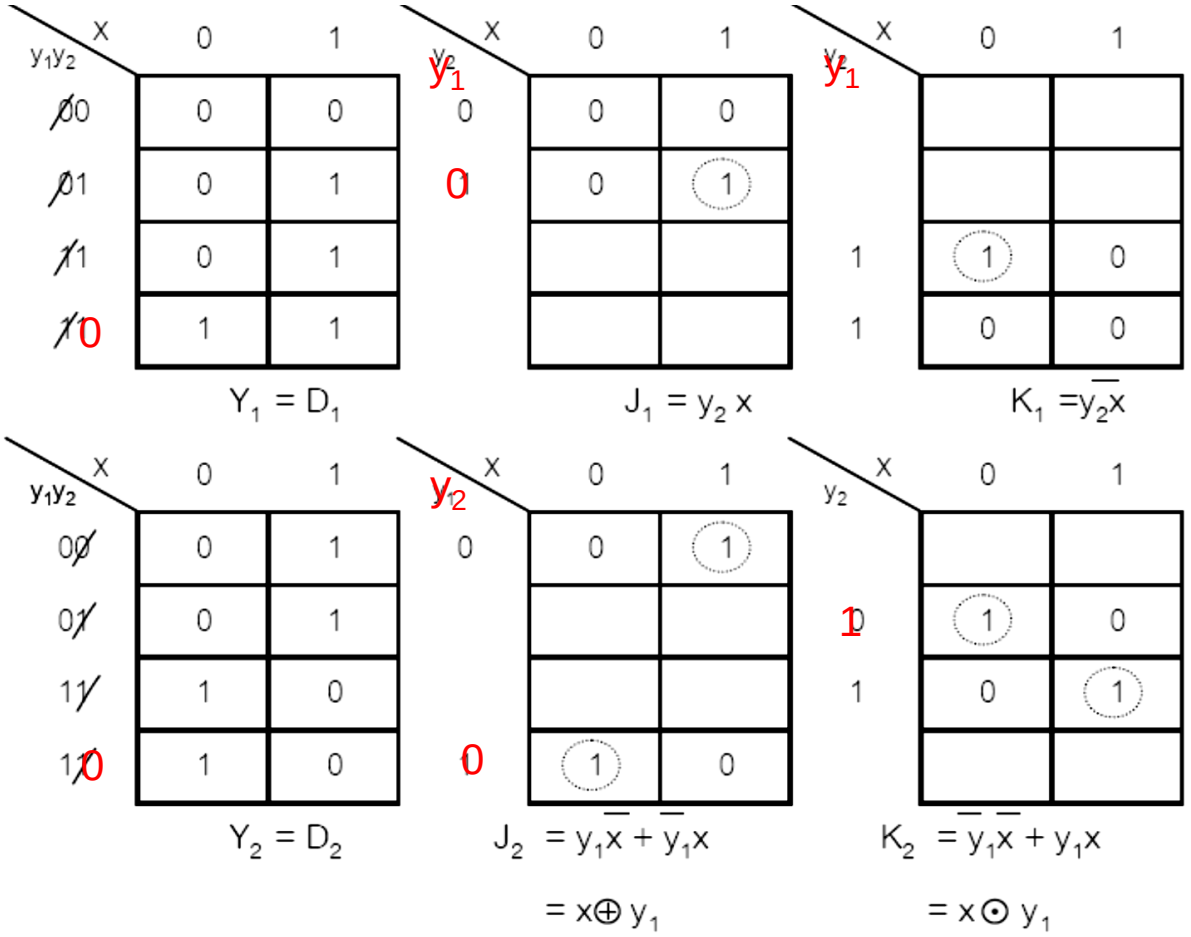
y = 1 ➔ K = $\overline{Y}$ = $\overline{D}$

K-Map Transform From D FF to JK FF

Example Redo the problem by Short-out method: Ignore the don't care cases,

- consider the case of $y = 0$ for the J Map and
- the case of $y = 1$ for the K Map.

Solution



Map J : D = J $\bar{y}$

y = 0 ➔ J =Y = D

y = 1 ➔ J = d

Map K : D = $\bar{K}$ y

y = 0 ➔ K = d

y = 1 ➔ K = $\bar{Y}$ = $\bar{D}$

Synchronous Sequential Circuit Design: Example

Example Find the state diagram and state tables of the synchronous sequential circuit that detects bit stream of 0110 in the pattern of

a) non-overlapping and b) overlapping in the stream.

Solution

a) Non-overlapping: If x = 0110110110
The circuit will produce z = 0001000001

We can draw the state diagram to detect 0110 by assigning 4 states:

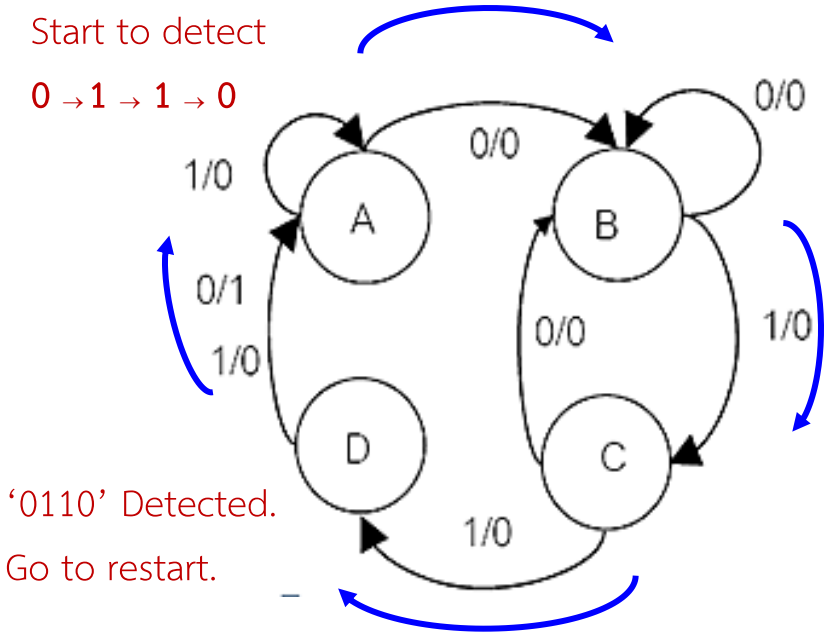
A = State to detect '0'

B = State to detect '01'

C = State to detect '011'

D = State to detect '0110'

Then go to A



Synchronous Sequential Circuit Design: Example

b) Overlapping: If x = 0110110110
The circuit will produce z = 0001001001

We can draw the state diagram to detect 0110 by assigning 4 states:

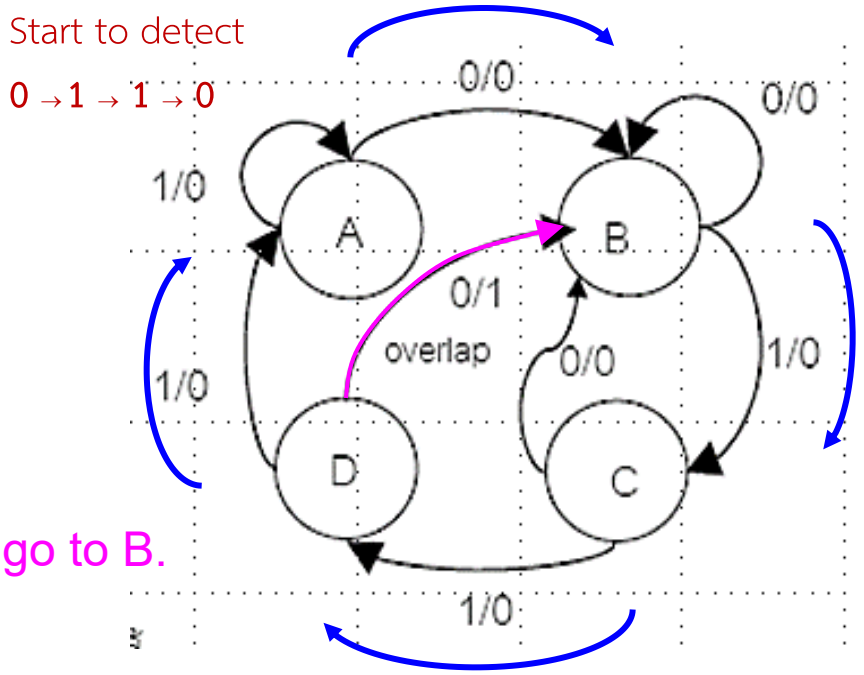
So, we need 4 states:

A = State to detect ‘0’

B = State to detect ‘01’

C = State to detect ‘011’

D = State to detect ‘0110’



Since it has detected ‘0’ Then go to B.

Synchronous Sequential Circuit Design: Example

The state tables of both circuit can be produced from their state diagrams obtained.

PS \ X	0	1
A	B/0	A/0
B	B/0	C/0
C	B/0	D/0
D	A/1	A/0

NS/Z

Non-overlapping

PS \ X	0	1
A	B/0	A/0
B	B/0	C/0
C	B/0	D/0
D	B/1	A/0

NS/Z

Overlapping

- We could assign the state codes for the individual state names.
- e.g., from the assignment table above: A = 00, B = 01, C = 11 and D = 10
- Then we can also make their transition tables,
- excitation tables and the sequential circuits.

Synchronous Sequential Circuit Design: Example

Example Find the state diagram and state tables of the synchronous sequential circuit that detects bit stream of 1001 in the pattern of

a) non-overlapping and b) overlapping in the bit stream.

Answer

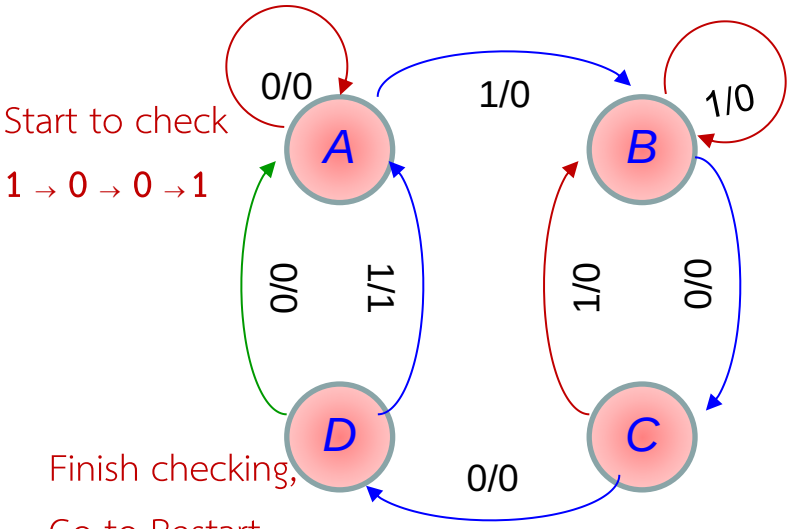
PS \ X	0	1
A	A/0	B/0
B	C/0	B/0
C	D/0	B/0
D	A/0	A/1

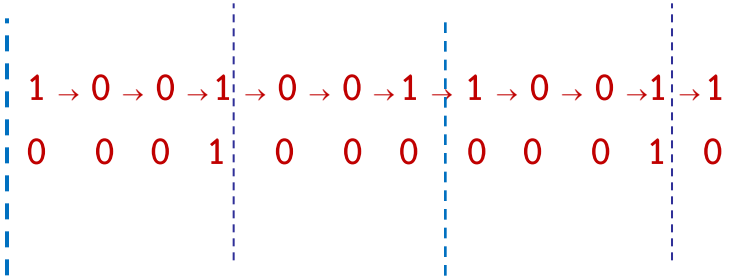
Non-overlapping

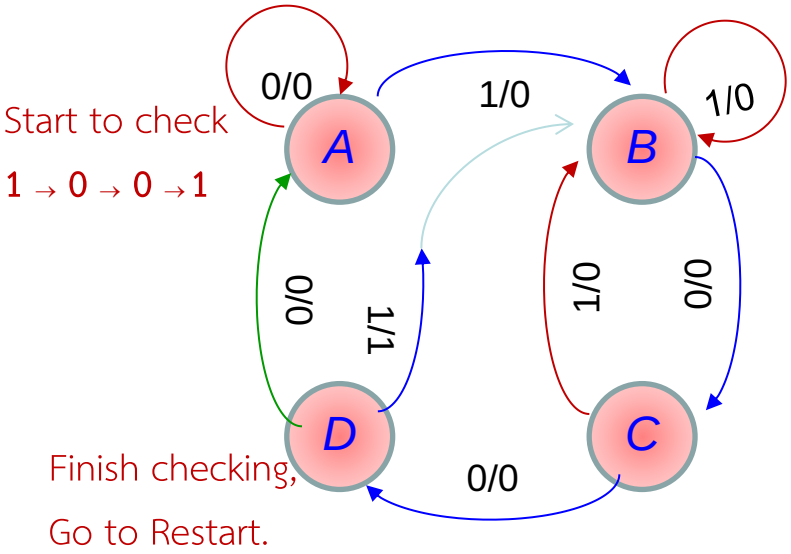
PS \ X	0	1
A	A/0	B/0
B	C/0	B/0
C	D/0	B/0
D	A/0	B/1

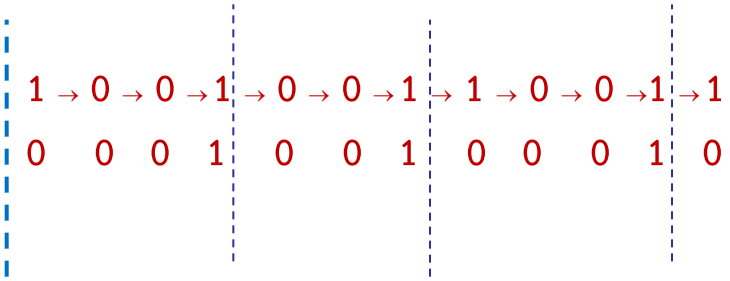
Overlapping

Solution


Start to check
1 → 0 → 0 → 1
A
B
C
D
0/0
1/0
1/0
0/1
1/0
0/0
0/0
Finish checking,
Go to Restart.


1 → 0 → 0 → 1 → 0 → 0 → 1 → 1 → 0 → 0 → 1 → 1
0 0 0 1 0 0 0 0 0 0 1 0


Start to check
1 → 0 → 0 → 1
A
B
C
D
0/0
1/0
1/0
0/1
1/0
0/0
0/0
Finish checking,
Go to Restart.


1 → 0 → 0 → 1 → 0 → 0 → 1 → 1 → 0 → 0 → 1 → 1
0 0 0 1 0 0 1 0 0 0 1 0