Name: ....Theepakorn...Phayomrat.................... Student ID: ......67011352..............................

Name: .... Student ID: ....

Laboratory 11

Shift Registers

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1. Connect a logic circuit as shown in the following figure.

IC3   IC2.   Ic1

104   93   73

IC1,IC2: 7473
IC3: 7404
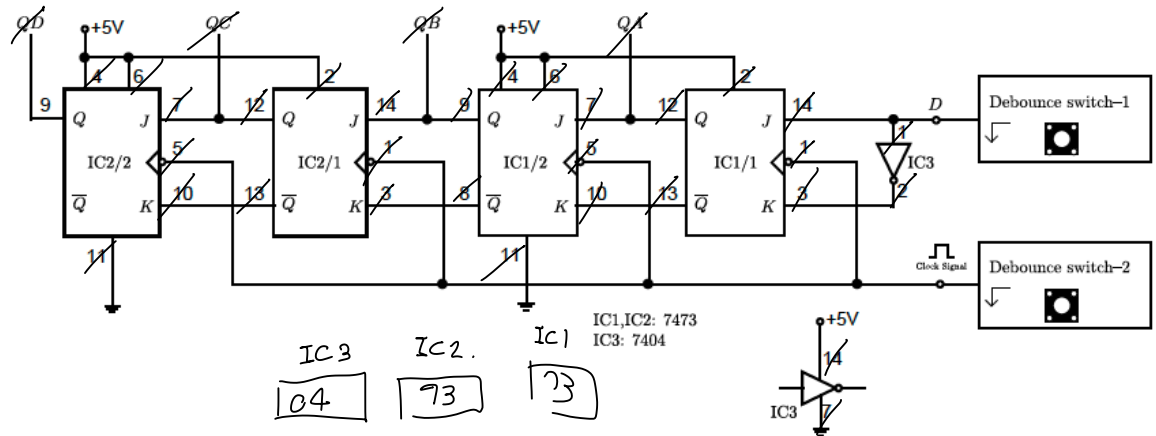
2. Connect output *QA-QD* to the logic monitor, input *D* to the falling edge output of the de-bounce switch 1 and pin CLK to the falling edge output of the debounce switch 2.
3. Supply the logic as shown in the following table. A clock pulse can be generated and applied to the circuit by pressing the debounce switch 2 once. Observe and record the results.

D	CLK Pulse No.	QA	QB	QC	QD	Remarks
0	1	O	1	1	/	Press and hold debounce SW 1
0	2	O	C	1	)	Press and hold debounce SW 1
0	3	C	C	O	)	Press and hold debounce SW 1
0	4	O	C	σ	C	Press and hold debounce SW 1
1	5	1	C	C	○	Release de-bounce SW 1
0	6	O	1	○	O	Press and hold debounce SW 1
0	7	C	C	1	C	Press and hold debounce SW 1

___

| D	CLK Pulse No.	QA	QB	QC	QD	Remarks
0	8	0	0	0	1	Press and hold debounce SW 1
0	9	0	0	0	0	Press and hold debounce SW 1
0	10	0	0	0	0	Press and hold debounce SW 1

Instructor's signature

4. What can be concluded from the previous experiment?

If the clock is (SW2) is pressed, number shift right
If the D sw (SW1) is release, number 1 is generated.

If not, it generate 0.

Instructor's signature

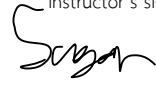
5. Connect the circuit as shown in the following figure
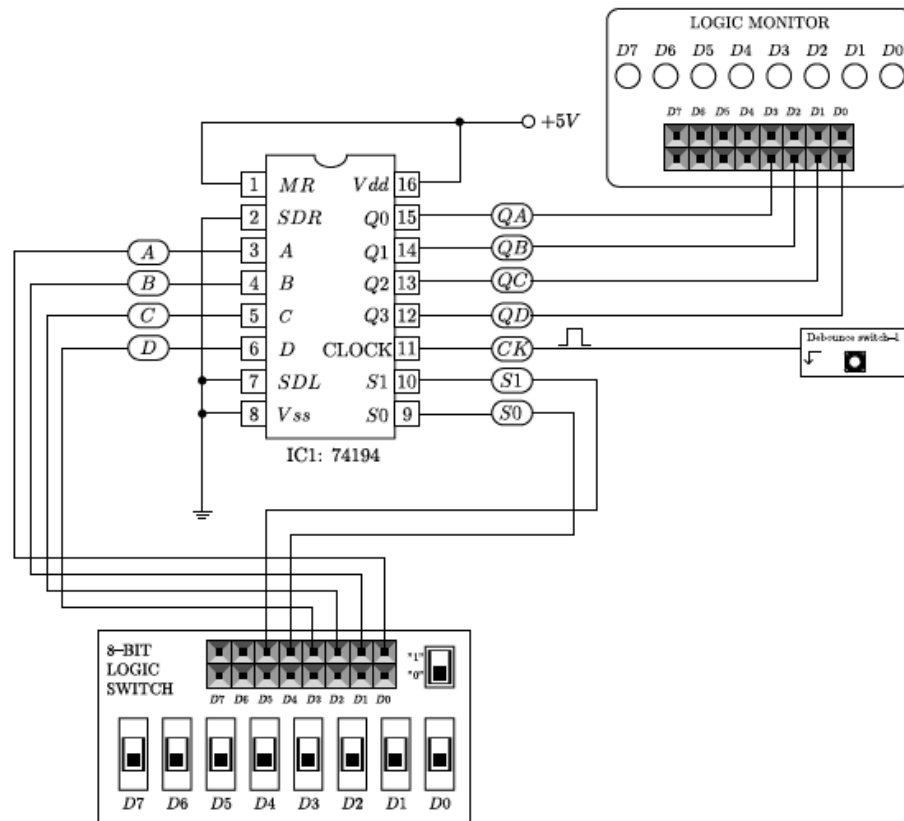
The operation mode of IC 74194 is given as in the following table.

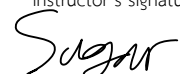| Mode	S1	S0
Parallel data input	1	1
Data latching	0	0
Left shift register	1	0
Right shift register	0	1

6. Connect pin S1, S0 and DCBA to the logic switches. Connect pin CK to the debounce switch 1 and connect output QD-QA to the logic monitor.
7. Supply the input DCBA to be 0011
8. Supply the pulses to pin CK as shown in the following table. A clock pulse can be generated and applied to the circuit by pressing the debounce switch 1 once. Observe and record the results for QD-QA

| S1	S0	CK pulse No.	QA	QB	QC	QD	Mode
1	1	1	1	1	0	0	Parallel Data Input
0	1	2	0	1	1	0	Right Shift Register
0	1	3	0	0	1	1	Right Shift Register
1	0	4	0	1	1	0	Left Shift Register
1	0	5	1	1	0	0	Left Shift Register

Instructor's signature

9. What can be concluded from the previous experiment?

S   S₀

0   0   Do nothing

0   1   Shift all output to the right by 1 position.

1   0   Shift all output to the left by 1 position

1   1   Add 1 into slots being turned on in D₀-D₃ ✗

Instructor's signature

10. Connect the circuit as shown in the following figure. Note that SDL and SDR pins are now connected to the logic switches.
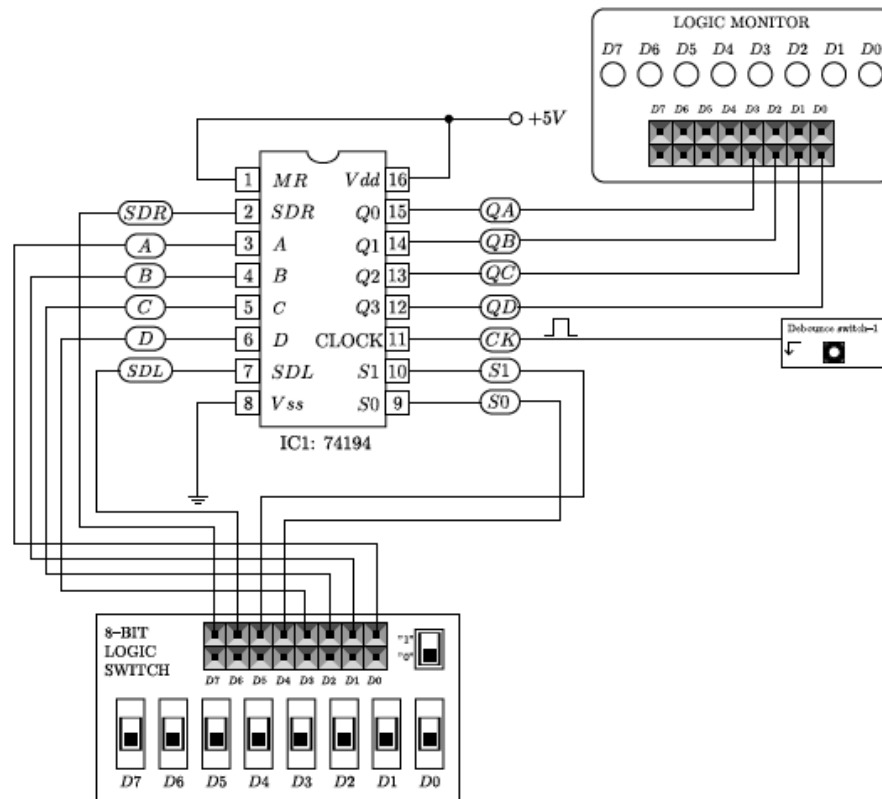
11. Supply the logic signal 0000 to the input DCBA.
12. Supply the pulses to pin CK as shown in the following table. A clock pulse can be generated and applied to the circuit by pressing the debounce switch 1 once. Observe and record the results for QD-QA

S1 D_5	S0 D_4	(SDL) D_6	(SDR) D_7	CK pulse No.	QA	QB	QC	QD	Mode
0	1	0	1	1	1	0	0	0	Shift R
0	1	0	1	2	1	1	0	0	Shift R
0	1	0	0	3	0	1	1	0	Shift R
0	1	0	0	4	0	0	1	1	Shift R
0	1	0	0	5	0	0	0	1	Shift R
0	1	0	0	6	0	0	0	0	Shift R
1	0	1	0	7	0	0	0	1	Shift L
1	0	1	0	8	0	0	1	1	Shift L
1	0	0	0	9	0	1	1	0	Shift L
1	0	0	0	10	1	1	0	0	Shift L
1	0	0	0	11	1	0	0	0	Shift L
1	0	0	0	12	0	0	0	0	Shift L

Instructor's signature

Me mue

13. What can be concluded from the previous experiment?

SDL   SDR

0   0   If we shift, it will not generate 1 from both L and R.

0   1   If we shift R, it will generate 1 from L

1   0   If we shift L, it will generate 1 from R

1   1   If we shift R or L, it will generate from both side
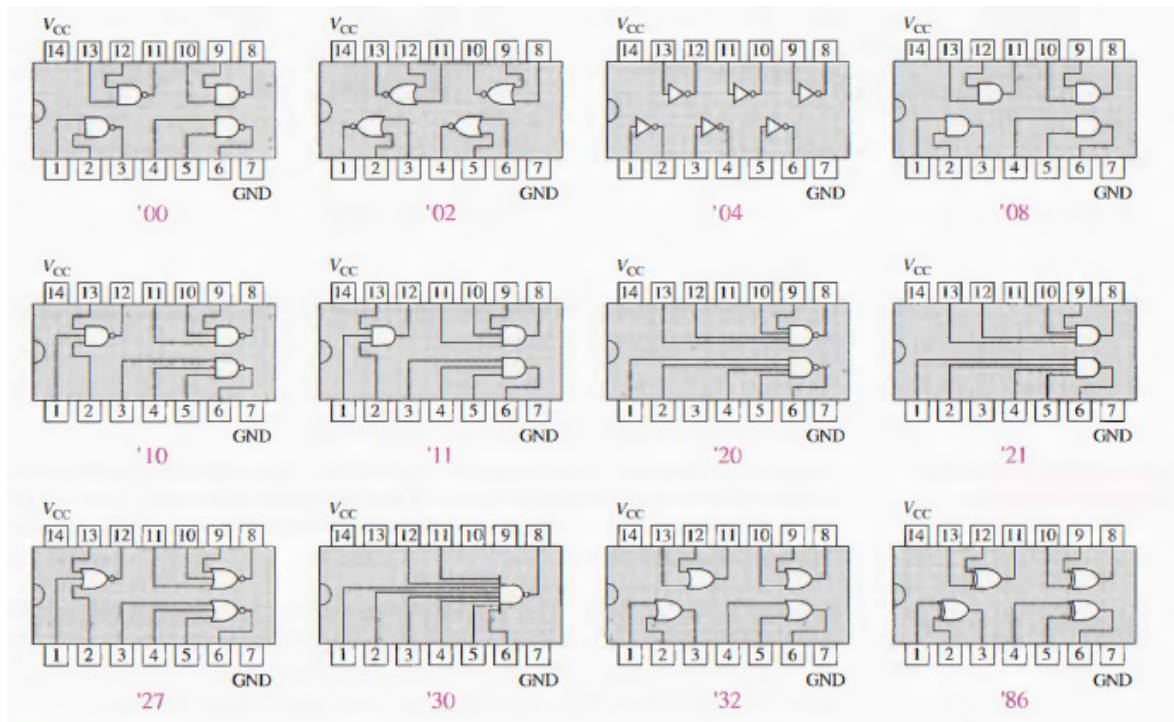   but we cannot see both of 1 from 2 sides at the same time

Instructor's signature

14. **Assignments:**

    14.1 Implements the circuit that accepts the serial input. The 4-bit binary output of this circuit should be connected to LED D3 to D0 which D3 is MSB. The LED D4 should active "HIGH" when the output LED D3 to D0 can be divided by 7 otherwise it should active "LOW". If the 4-bit binary output is "1111", D5 should active "HIGH" and D3 to D0 should be cleared.

Instructor's signature

Logic Diagram of frequently used gates

'00   '02   '04   '08

'10   '11   '20   '21

'27   '30   '32   '86

Theepakorn Phayonrat   67011352

14.1 Implements the circuit that accepts the serial input. The 4-bit binary output of this circuit
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     cleared.

CLK

Input

D   Q   D   Q   D   Q   D   Q

Q̄   Q̄   Q̄   Q̄

A   B   C   D

Check   Check
↓ for ↘   ↓ for
111₂   1111₂

AND   AND   AND   AND — D2

                              AND — D1

                     NOT

OR   AND — D0

D5

                              AND — D3

D4