

T 965

N 82

## Programmable Array Logic (PAL®) High Speed PAL Series 20 AP

### General Description

The PAL family utilizes National Semiconductor's Schottky TTL process and bipolar PROM fusible-link technology to provide user-programmable logic to replace conventional SSI/MSI gates and flip-flops. Typical chip count reduction gained by using PALs is greater than 4:1.

The family lets the systems engineer customize his chip by opening fusible links to configure AND and OR gates to perform his desired logic functions. Complex interconnections that previously required time-consuming layout are thus transferred from PC board to silicon where they can be easily modified during prototype checkout or production.

The PAL transfer function is the familiar sum of products with a single array of fusible links. Unlike the PROM, the PAL is a programmable AND array driving a fixed OR array. (The PROM is a fixed AND array driving a programmable OR array). In addition, the PAL family offers these options:

- Variable input/output in ratio
- Programmable TRI-STATE® outputs
- Registers and feedback

Unused inputs are tied directly to V<sub>CC</sub> or GND. Product terms with all fuses blown assume the logical high state, and product terms connected to both true and complement of any single input assume the logical low state. Registers consist of D-type flip-flops that are loaded on the low-to-high transition of the clock. The registers power up with high (V<sub>OH</sub>) at the output pin, regardless of the polarity fuse. PAL logic diagrams are shown with all fuses blown, enabling the designer use of the diagrams as coding sheets.

The entire PAL family is programmed on inexpensive conventional PROM programmers with appropriate personality and socket adapter cards. Once the PAL is programmed and verified, two additional fuses may be blown to defeat

verification. This feature gives the user a proprietary circuit which is very difficult to copy.

### Functional Description

The PAL Series 20AP represents an enhancement of existing PAL architectures which provides greater design flexibility and improved testability. Several new features have been incorporated into the family, including programmable output polarity, power-up reset, and register preload.

The programmable output polarity feature allows the user to program individual outputs either active high or active low. This feature eliminates any possible need for inversion of signals outside the device.

The registered members of the Series 20AP have been designed to reset during system power-up. Upon application of power, all registers are initialized to a logic 0 state, setting all outputs to a logic 1.

The testability of the registered devices has been increased through the use of the preload feature. During testing, registers can be loaded with any arbitrary state value, thereby allowing full logical verification.

### Features

- Programmable output polarity
- Power up reset for all registers
- Preload feature during testing
- Programmable replacement for TTL logic
- Simplifies prototyping and board layout
- Skinny DIP packages
- Reliable tungsten fuses
- 25 ns max. propagation delay

### Ordering Information

Part Number	Description
PAL16P8A	OCTAL 16 Input AND-OR Gate Array 016660
PAL16RP8A	OCTAL 16 Input Registered AND-OR Gate Array 010984
PAL16RP6A	HEX 16 Input Registered AND-OR Gate Array 010985
PAL16RP4A	QUAD 16 Input Registered AND-OR Gate Array 010986

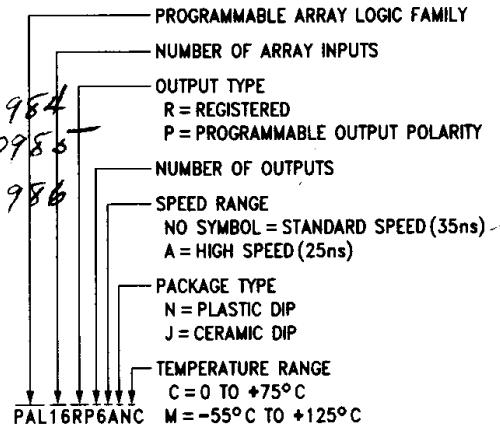
#### PAL Part Numbers

The PAL part number reveals the logic operation the part performs. The example shown, the PAL16RP6ANC, is a device that accommodates 16 input terms and generates 6 register output terms. It is contained in a 20-pin plastic dual-in-line package and meets commercial temperature range specifications.

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TL/L/8504-1

## Absolute Maximum Ratings

	Operating	Programming
Supply Voltage, V <sub>CC</sub>	7V	12V
Input Voltage	5.5V	12V***
Off-State Output Voltage	5.5V	12V
Storage Temperature	-65°C to +150°C	

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

## Recommended Operating Conditions

Symbol	Parameter	Military			Commercial			Units
		Min	Typ	Max	Min	Typ	Max	
V <sub>CC</sub>	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
t <sub>w</sub>	Width of Clock	Low	25	14	20	14		ns
		High	15	6	10	6		
t <sub>su</sub>	Setup Time from Input or Feedback to Clock	16RP8A	Polarity Fuse Intact	30	15	25	15	ns
		16RP6A	Polarity Fuse Blown	35	20	30	20	ns
t <sub>h</sub>	Hold Time	0	-10		0	-10		ns
T <sub>A</sub>	Operating Free-Air Temperature	-55			0		75	°C
T <sub>C</sub>	Operating Case Temperature			125				°C

## Electrical Characteristics Over Recommended Operating Temperature Range

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
V <sub>IH</sub> *	High Level Input Voltage			2			V
V <sub>IL</sub> *	Low Level Input Voltage					0.8	V
V <sub>IC</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min., I <sub>I</sub> = -18 mA			-0.8	-1.5	V
V <sub>OH</sub>	High Level Output Voltage	V <sub>CC</sub> = Min.	I <sub>OH</sub> = -2 mA MIL	2.4	2.8		V
		V <sub>IL</sub> = 0.8V	I <sub>OH</sub> = -3.2 mA COM				
V <sub>OL</sub>	Low Level Output Voltage	V <sub>CC</sub> = Min.	I <sub>OL</sub> = 12 mA MIL		0.3	0.5	V
		V <sub>IL</sub> = 0.8V	I <sub>OL</sub> = 24 mA COM				
I <sub>OZH</sub>	Off-State Output Current †	V <sub>CC</sub> = Max.	V <sub>O</sub> = 2.4V			100	µA
		V <sub>IL</sub> = 0.8V	V <sub>O</sub> = 0.4V			-100	µA
I <sub>I</sub>	Maximum Input Current	V <sub>CC</sub> = Max., V <sub>I</sub> = 5.5V				1	mA
I <sub>IH</sub>	High Level Input Current†	V <sub>CC</sub> = Max., V <sub>I</sub> = 2.4V				25	µA
I <sub>IL</sub>	Low Level Input Current †	V <sub>CC</sub> = Max., V <sub>I</sub> = 0.4V			-0.04	-0.25	mA
I <sub>os</sub>	Output Short-Circuit Current**	V <sub>CC</sub> = 5V, V <sub>O</sub> = 0V		-30	-70	-130	mA
I <sub>cc</sub>	Supply Current	V <sub>CC</sub> = Max.			140	180	mA

† I/O pin leakage is the worst case of I<sub>OZX</sub> or I<sub>IX</sub> e.g. I<sub>IL</sub> and I<sub>OZH</sub>.

\* These are absolute voltages with respect to pin 10 on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

\*\* Only one output shorted at a time.

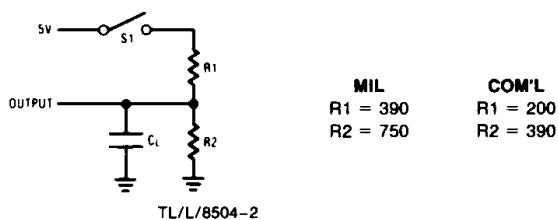
\*\*\* Pins 1 and 11 may be raised to 20V max.

## Switching Characteristics

Over Recommended Ranges of Temperature and  $V_{CC}$   
 Military:  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}^*$ ,  $V_{CC} = 5V \pm 10\%$ . Commercial:  $T_A = 0^\circ\text{C}$  to  $75^\circ\text{C}$ ,  $V_{CC} = 5V \pm 5\%$

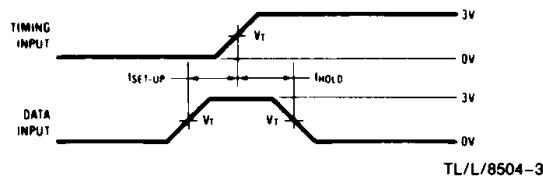
Symbol	Parameter	Test Conditions	Military			Commercial			Units
			Min	Typ	Max	Min	Typ	Max	
$t_{PD}$	16P8A, 16RP6A, 16RP4A	$R_1 = 200\Omega$ $R_2 = 390\Omega$		15	30		15	25	ns
	Input or Feedback to Output		20	35		20	30		
	Polarity Fuse Blown								
	$t_{CLK}$		10	20		10	15		
	$t_{PZX}$		10	25		10	20		
	$t_{PXZ}$		11	25		11	20		
	Input to Output Enable		10	30		10	25		
	Input to Output Disable		13	30		13	25		
	$f_{MAX}$		20	40		28.5	40		MHz
	Maximum Frequency		18.5	33		25	33		

## AC Test Load

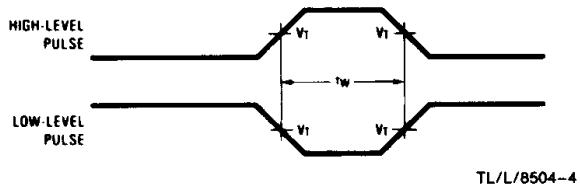


## Test Waveforms

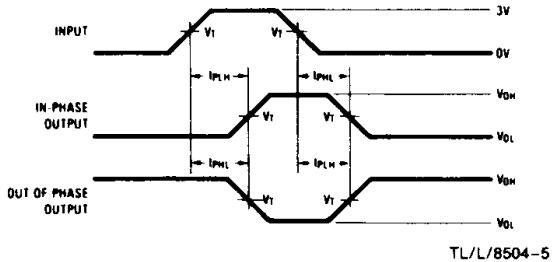
### Setup and Hold



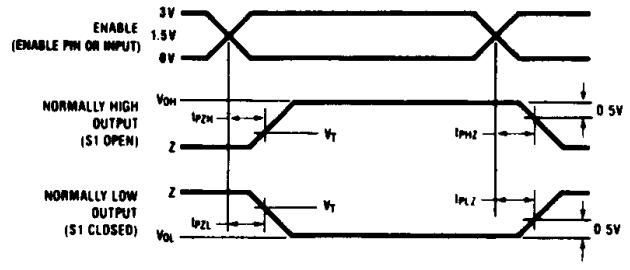
### Pulse Width



### Propagation Delay



### Enable and Disable



### Notes:

$C_L$  includes probe and jig capacitance.

$V_T = 1.5V$ .

In the example above, the phase relationships between inputs and outputs have been chosen arbitrarily.

All input pulses are supplied by generators having the following characteristics: PRR = 1 MHz,  $Z_{OUT} = 50\Omega$ ,  $t_r \leq 5$  ns,  $t_f \leq 5$  ns.

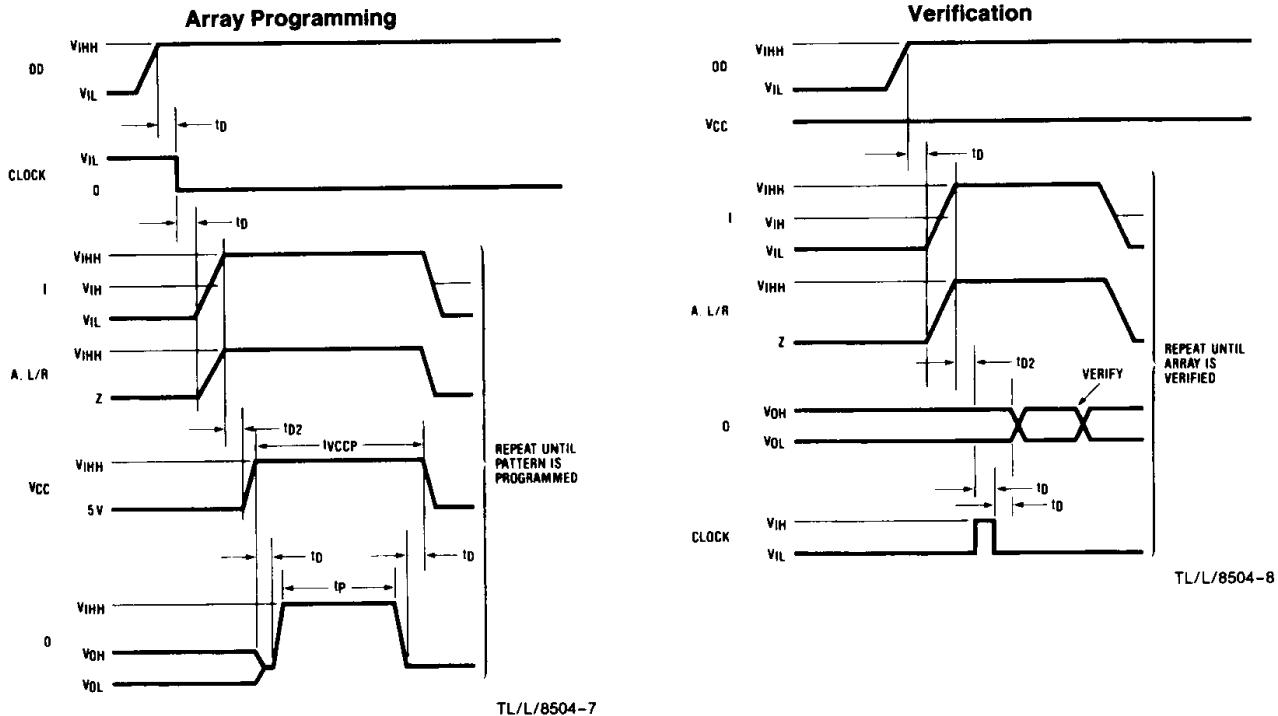
$t_{PD}$  is tested with switch  $S_1$  closed and  $C_L = 50$  pF.

For TRI-STATE outputs, output enable times are tested with  $C_L = 50$  pF to the 1.5V level;  $S_1$  is open for high-impedance to HIGH tests and closed for high-impedance to LOW tests. Output disable times are tested with  $C_L = 5$  pF. HIGH to high-impedance tests are made to an output voltage of  $V_{OH} - 0.5V$  with  $S_1$  open. LOW to high-impedance tests are made to the  $V_{OL} + 0.5V$  level with  $S_1$  closed.

## Programming Parameters

Symbol	Parameter	Min	Typ	Max	Units
$V_{IH}$	Program Level Input Voltage	11.5	11.75	12	V
$I_{IH}$	Output Program Pulse			50	mA
	OD, L/R			50	
	All Other Inputs			15	
$I_{CCH}$	Program Supply Current			900	mA
$t_{VCCP}$	Pulse Width of $V_{CC}$ @ $V_{IH}$			60	$\mu s$
$t_p$	Program Pulse Width	10	20	50	$\mu s$
$t_D$	Delay Time	100			ns
$t_{D2}$	Delay Time after L/R Pin	10			$\mu s$
	$V_{CCP}$ Duty Cycle			20	%
$V_P$	Output Polarity and Security Fuse Programming Voltage	19.5	20	20.5	V
$I_{P1}$	Security Fuse Programming Supply Current			400	mA
$I_{P2}$	Output Polarity Programming Supply Current			200	mA
$t_{PP}$	Output Polarity and Security Fuse Programming Pulse Width	10	40	70	$\mu s$
	Output Polarity and Security Fuse Programming Duty Cycle			50	%
$t_{RP}$	Rise Time of Output Programming and Address Pulses	1	1.5	10	V/ $\mu s$
	Rise Time of Security Fuse Programming Pulses	1	1.5	10	
$V_{CCPP}$	$V_{CC}$ Value During Security Fuse Programming	5.25	6	6.25	V
	$V_{CC}$ Value for First Verify	4.75	5	5.25	
	$V_{CC}$ Value for High $V_{CC}$ Verify	5.4	5.5	5.6	
	$V_{CC}$ Value for Low $V_{CC}$ Verify	4.4	4.5	4.6	
$V_{CCOP}$	$V_{CC}$ Value During Output Polarity Programming	5.25	5.5	5.75	V

## Programming Waveforms



### Notes:

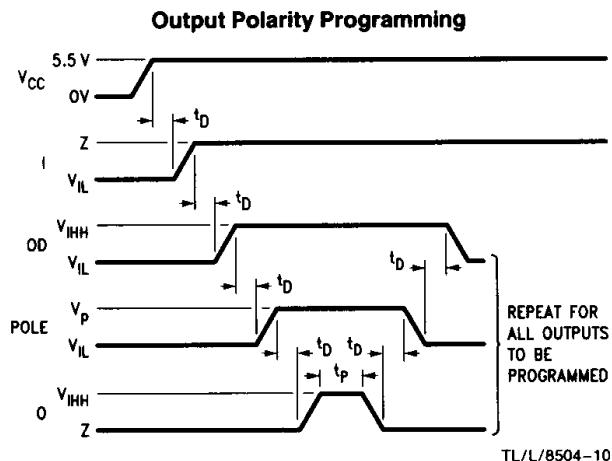
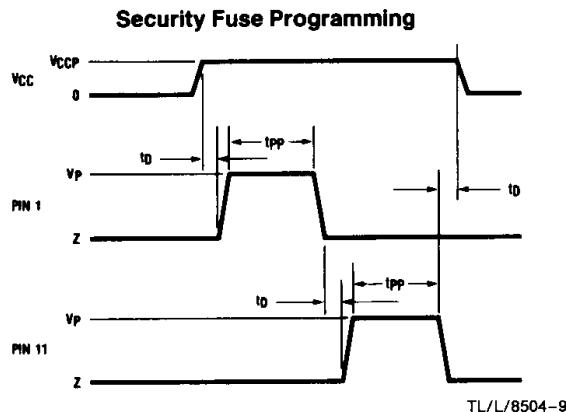
$V_{CC}$  (Low Voltage Verify) = 4.5V

$V_{CC}$  (High Voltage Verify) = 5.5V

$V_{CC}$  (First Verify) = 5V

A Delay ( $t_{D2}$ ) must always precede the Positive Clock Transition. (e.g. see step 1.2.3.3 for underblow condition)

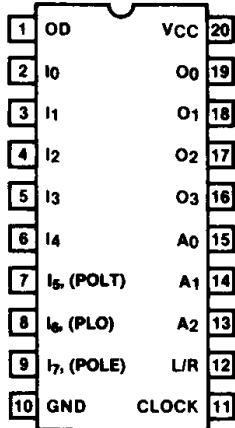
## Programming Waveforms (Continued)



## Programmer Development Systems

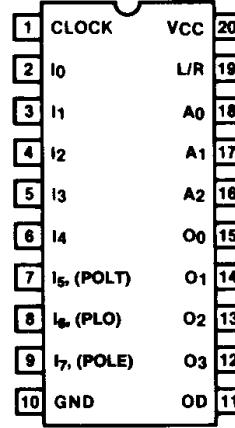
Vendor	PAL 20AP	PAL 20s (ALL)	PAL 24s (STD)	PAL 24s (FAST)
Data I/O	—LogicPak	—LogicPak (Rev-010) —1427 Card Set	—LogicPak (Rev-010)	—LogicPak (Rev-010)
Structured Design	—SD 1000	—SD 20/24 —SD1000	—SD 20/24 —SD1000	—SD 20/24 —SD1000
STAG	—ZL 30	—PM202 (Rev 3) —PM2200	—PM202 (Rev 3) —PM2200	—PM202 (Rev 3) —PM2200
DIGELEC		—UP803 (FAM51) or (FAM52)	—UP803 (FAM51) or (FAM52)	—UP803 (FAM51) or (FAM52)
KONTRON		—MPP80S MOD 21		

## Connection Diagrams



TL/L/8504-11

**FIGURE 1. Pin Identification**



TL/L/8504-12

# Programming/Verifying Procedure\*

Note: For programming purposes many PAL pins have double functions. As long as Pin 1 is at  $V_{IHH}$ , Pin 11 is at ground, and Pin 12 is either at  $V_{IHH}$  or Z (as defined in Table I)—Pins 16, 17, 18, and 19 are outputs. The other pin functions are:  $I_0$  (Pin 2) through  $I_7$  (Pin 9) plus Pin 12 address the proper row; A0 (Pin 15), A1 (Pin 14), and A2 (Pin 13) address the proper product lines.

When Pin 11 is at  $V_{IHH}$ , Pin 1 is at ground, and Pin 19 is either at  $V_{IHH}$  or Z—Pins 12, 13, 14, and 15 are outputs. The other pin functions are:  $I_0$  (Pin 2) through  $I_7$  (Pin 9) plus Pin 19 address the proper row; A0 (now Pin 18), A1 (now Pin 17), and A2 (now Pin 16) address the proper product lines.

\*NSC programming spec. Rev. 1

## Pre-Verification

### Step 1.1 Pre-verification-Security-Fuses

Step 1.1.1 Raise Pin 2 to  $V_p$ .

Step 1.1.2 Place a 2k resistor to ground on Pin 1 and measure voltage across it.

—Reject part if measured voltage is less than 1.5V.

Step 1.1.3 Place a 2k resistor to ground on Pin 11 and measure voltage across it.

—Reject part if measured voltage is less than 1.5V.

### Step 1.2 Pre-verification-Array

Step 1.2.1 Raise  $V_{CC}$  to 5.0V.

Step 1.2.2 Raise output disable, OD, to  $V_{IHH}$ .

Step 1.2.3 Select an input line by specifying inputs and L/R as shown in Table I.

Step 1.2.4 Select a product line by specifying A0, A1, and A2 one-of-eight select as shown in Table II.

Step 1.2.5 Pulse the CLOCK pin and verify (with CLOCK at  $V_{IL}$ ) that the output pin, O is TTL high.

—For TTL high, continue procedure.

—For TTL low, stop procedure and reject part.

### Step 1.3 Pre-verification—Programmable Polarity Fuses (METHOD 1)

Step 1.3.1 Raise  $V_{CC}$  to 5.0V.

Step 1.3.2 Raise Pin 3 to  $V_p$ .

Step 1.3.3 Raise Pin 4 to  $V_p$ .

Step 1.3.4 Pulse the CLOCK pin and test (with CLOCK at  $V_{IL}$ ) the state of the output pin, O.

—For unblown polarity fuse the output will be at logic 0.

—For blown polarity fuse the output will be at logic 1.

### Step 1.4 Pre-verification—Programmable Polarity Fuses (METHOD 2)

Step 1.4.1 Raise  $V_{CC}$  to 5.0V.

Step 1.4.2 For any input condition determine the state of each output.

Step 1.4.3 Raise Pin 7 to  $V_p$ .

Step 1.4.4 Compare the output states now with their states at Step 1.4.2.

—If the state of the output has changed, then the output polarity fuse is unblown.

—If the state of the output is unchanged, then the output polarity fuse is blown.

### Step 1.5 Pre-verification—Programmable Polarity Fuses (METHOD 3)

Step 1.5.1 Raise  $V_{CC}$  to 5.0V.

Step 1.5.2 Raise all inputs to  $V_{IHH}$ .

Step 1.5.3 Raise Pin 11 to  $V_{IHH}$ .

Step 1.5.4 Pulse the CLOCK pin and verify (with CLOCK at  $V_{IL}$ ) the state of the output pin.

—If output is at logic 0, then the output polarity fuse is unblown.

—If output is at logic 1, then the output polarity fuse is blown.

## Programming Algorithm

### Step 2.1 Raise Output Disable pin, OD, to $V_{IHH}$ .

### Step 2.2 Programming pass. For all fuses to be blown:

Step 2.2.1 Lower CLOCK pin to ground.

Step 2.2.2 Select an input line by specifying inputs and L/R as shown in Table I.

Step 2.2.3 Select a product line by specifying A0, A1, and A2 one-of-eight select as shown in Table II.

Step 2.2.4 Raise  $V_{CC}$  to  $V_{IHH}$ .

Step 2.2.5 Program the fuse by pulsing the output pins of the selected product group one at a time to  $V_{IHH}$  (as shown in the Programming Waveforms).

Step 2.2.6 Lower  $V_{CC}$  to 5V.

Step 2.2.7 Repeat this procedure from Step 2.2.2 until pattern is complete.

### Step 2.3 First verification pass. For all fuse locations:

Step 2.3.1 Select an input line by specifying inputs and L/R as shown in Table I.

Step 2.3.2 Select a product line by specifying A0, A1, and A2 one-of-eight select as shown in Table II.

Step 2.3.3 Pulse the CLOCK pin and verify (with CLOCK at  $V_{IL}$ ) that the output pin, O, is in the correct state.

—For verified output state, continue procedure.

—For overflow condition, stop procedure and reject part.

—For underflow condition, reexecute steps 2.2.4 through 2.2.6 and 2.2.3. If successful, continue procedure. After three attempts to blow fuse without success, reject part.

Step 2.3.4 Repeat this procedure from step 2.3.1 until the entire array is exercised.

## Programming Algorithm (Continued)

Step 2.4 High Voltage Verify. For all fuse locations:

Step 2.4.1 Raise  $V_{CC}$  to 5.5V.

Step 2.4.2 Select an input line by specifying inputs and L/R as shown in Table I.

Step 2.4.3 Select a product line by specifying A0, A1, and A2 one-of-eight select as shown in Table II.

Step 2.4.4 Pulse the CLOCK pin and verify (with CLOCK at  $V_{IL}$ ) that the output pin, O, is in the correct state.

—For verified output state, continue procedure.

—For invalid output state, stop procedure and reject part.

Step 2.4.5 Repeat this procedure from step 2.4.2 until the entire array is exercised.

Step 2.5 Low Voltage Verify. For all fuse locations:

Step 2.5.1 Lower  $V_{CC}$  to 4.5V.

Step 2.5.2 Select an input line by specifying inputs and L/R as shown in Table I.

Step 2.5.3 Select a product line by specifying A0, A1, and A2 one-of-eight select as shown in Table II.

## Voltage Legend

L = Low level input voltage,  $V_{IL}$

H = High level input voltage,  $V_{IH}$

TABLE I. Input Line Select

Input Line Number	Pin Identification								
	I <sub>7</sub>	I <sub>6</sub>	I <sub>5</sub>	I <sub>4</sub>	I <sub>3</sub>	I <sub>2</sub>	I <sub>1</sub>	I <sub>0</sub>	L/R
0	HH	HH	HH	HH	HH	HH	HH	L	Z
1	HH	HH	HH	HH	HH	HH	HH	H	Z
2	HH	HH	HH	HH	HH	HH	HH	L	HH
3	HH	HH	HH	HH	HH	HH	HH	H	HH
4	HH	HH	HH	HH	HH	HH	L	HH	Z
5	HH	HH	HH	HH	HH	HH	H	HH	Z
6	HH	HH	HH	HH	HH	HH	L	HH	HH
7	HH	HH	HH	HH	HH	HH	H	HH	HH
8	HH	HH	HH	HH	HH	L	HH	HH	Z
9	HH	HH	HH	HH	HH	H	HH	HH	Z
10	HH	HH	HH	HH	HH	L	HH	HH	HH
11	HH	HH	HH	HH	HH	H	HH	HH	HH
12	HH	HH	HH	HH	L	HH	HH	HH	Z
13	HH	HH	HH	H	HH	HH	HH	HH	Z
14	HH	HH	HH	L	HH	HH	HH	HH	HH
15	HH	HH	HH	H	HH	HH	HH	HH	HH
16	HH	HH	H	L	HH	HH	HH	HH	Z
17	HH	HH	H	H	HH	HH	HH	HH	Z
18	HH	HH	H	L	HH	HH	HH	HH	HH
19	HH	HH	H	H	HH	HH	HH	HH	HH
20	HH	HH	L	HH	HH	HH	HH	HH	Z
21	HH	HH	H	HH	HH	HH	HH	HH	Z
22	HH	HH	L	HH	HH	HH	HH	HH	HH
23	HH	HH	H	HH	HH	HH	HH	HH	HH
24	HH	L	HH	HH	HH	HH	HH	HH	Z
25	HH	H	HH	HH	HH	HH	HH	HH	Z
26	HH	L	HH	HH	HH	HH	HH	HH	HH
27	HH	H	HH	HH	HH	HH	HH	HH	HH
28	L	HH	Z						
29	H	HH	Z						
30	L	HH	HH						
31	H	HH	HH						

Step 2.5.4 Pulse the CLOCK pin and verify (with CLOCK at  $V_{IL}$ ) that the output pin, O, is in the correct state.

—For verified output state, continue procedure.

—For invalid output state, continue procedure and reject part.

Step 2.5.5 Repeat this procedure from 2.5.2 until entire array is exercised.

## Programming the Security Fuses

Step 3.1 Verify per Step 2.4 and Step 2.5.

Step 3.2 Raise  $V_{CC}$  to 6V.

Step 3.3 Program the first fuse by pulsing Pin 1 to V<sub>P</sub>. (From 1 to 5 pulses is acceptable.)

Step 3.4 Program the second fuse by pulsing Pin 11 to V<sub>P</sub>. (1 to 5 pulses is acceptable.)

Step 3.5 Verify per Step 1.1: — A device is "secured" if it verifies as blank per step 1.1.

HH = High level program voltage,  $V_{IH}$

Z = 10 kΩ to 5V

TABLE II. Input Line Select

Product Line Number	Pin Identification							
	O <sub>3</sub>	O <sub>2</sub>	O <sub>1</sub>	O <sub>0</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	
0, 32	Z	Z	Z	HH	Z	Z	Z	
1, 33	Z	Z	Z	HH	Z	Z	HH	
2, 34	Z	Z	Z	HH	Z	HH	Z	
3, 35	Z	Z	Z	HH	Z	HH	HH	
4, 36	Z	Z	Z	HH	HH	Z	Z	
5, 37	Z	Z	Z	HH	HH	Z	HH	
6, 38	Z	Z	Z	HH	HH	HH	HH	
7, 39	Z	Z	Z	HH	HH	HH	HH	
8, 40	Z	Z	HH	Z	Z	Z	Z	
9, 41	Z	Z	HH	Z	Z	Z	HH	
10, 42	Z	Z	HH	Z	Z	HH	Z	
11, 43	Z	Z	HH	Z	Z	HH	HH	
12, 44	Z	Z	HH	Z	HH	Z	Z	
13, 45	Z	Z	HH	Z	HH	Z	HH	
14, 46	Z	Z	HH	Z	HH	Z	HH	
15, 47	Z	Z	HH	Z	HH	Z	HH	
16, 48	Z	HH	Z	Z	Z	Z	Z	
17, 49	Z	HH	Z	Z	Z	Z	HH	
18, 50	Z	HH	Z	Z	Z	Z	HH	
19, 51	Z	HH	Z	Z	Z	Z	HH	
20, 52	Z	HH	Z	Z	HH	Z	Z	
21, 53	Z	HH	Z	Z	HH	Z	HH	
22, 54	Z	HH	Z	Z	HH	Z	HH	
23, 55	Z	HH	Z	Z	HH	Z	HH	
24, 56	HH	Z	Z	Z	Z	Z	Z	
25, 57	HH	Z	Z	Z	Z	Z	HH	
26, 58	HH	Z	Z	Z	Z	Z	HH	
27, 59	HH	Z	Z	Z	Z	Z	HH	
28, 60	HH	Z	Z	Z	Z	HH	Z	
29, 61	HH	Z	Z	Z	Z	HH	Z	
30, 62	HH	Z	Z	Z	Z	H	HH	
31, 63	HH	Z	Z	Z	Z	HH	HH	

## Programming the Output Polarity Fuses

Initial Programming Pass.

Step 4.1 Raise V<sub>CC</sub> to 5.5V.

Step 4.2 Set all inputs and output pins to Z.

Step 4.3 Raise output disable, OD, to V<sub>IHH</sub> to disable the selected outputs.

Step 4.4 Raise Polarity Enable, Pin 9 (POLE) to V<sub>P</sub>.

Step 4.5 Program the fuse by pulsing the desired output to V<sub>IHH</sub>.

Step 4.6 Lower Pin 9 (POLE) to V<sub>IH</sub>.

Step 4.7 Lower OD to V<sub>IL</sub>.

Step 4.8 Repeat this procedure from Step 4.3 to Step 4.7 until all desired outputs are programmed.

is as follows:

1 Raise V<sub>CC</sub> to 4.5V.

2 Disable output registers by setting Pin 11 to V<sub>IH</sub>.

3 Apply V<sub>IL</sub>/V<sub>IH</sub> to all output registers.

4 Pulse Pin 8 to V<sub>P</sub>. Then back to 0 V.

5 Remove V<sub>IL</sub>/V<sub>IH</sub> from all output registers.

6 Lower Pin 11 to V<sub>IL</sub> to enable the output registers.

7 Verify for V<sub>OL</sub>/V<sub>OH</sub> at all output registers.

## National Mask Logic (NML)

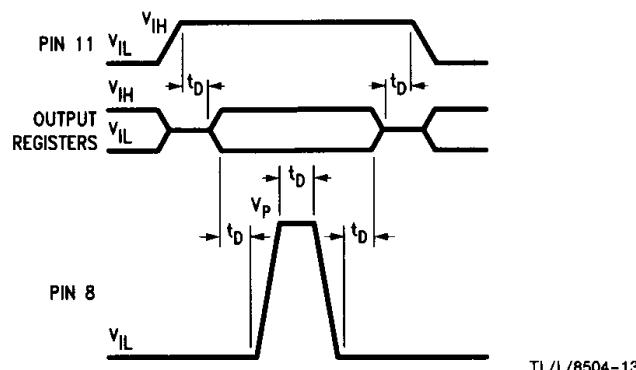
If a large number of PALs of the same pattern are to be used, it may be economical to consider mask-programming the PAL to avoid programming costs. These mask-programmed devices will meet or exceed all of the performance specifications of the fuse-programmed devices they replace. These specifications are listed previously in this data sheet.

To generate a NML PAL, National requires a set of logic equations written in PALASM™ format, plus test vectors which the user generates as acceptance criteria for the finished product.

## Output Register PRELOAD

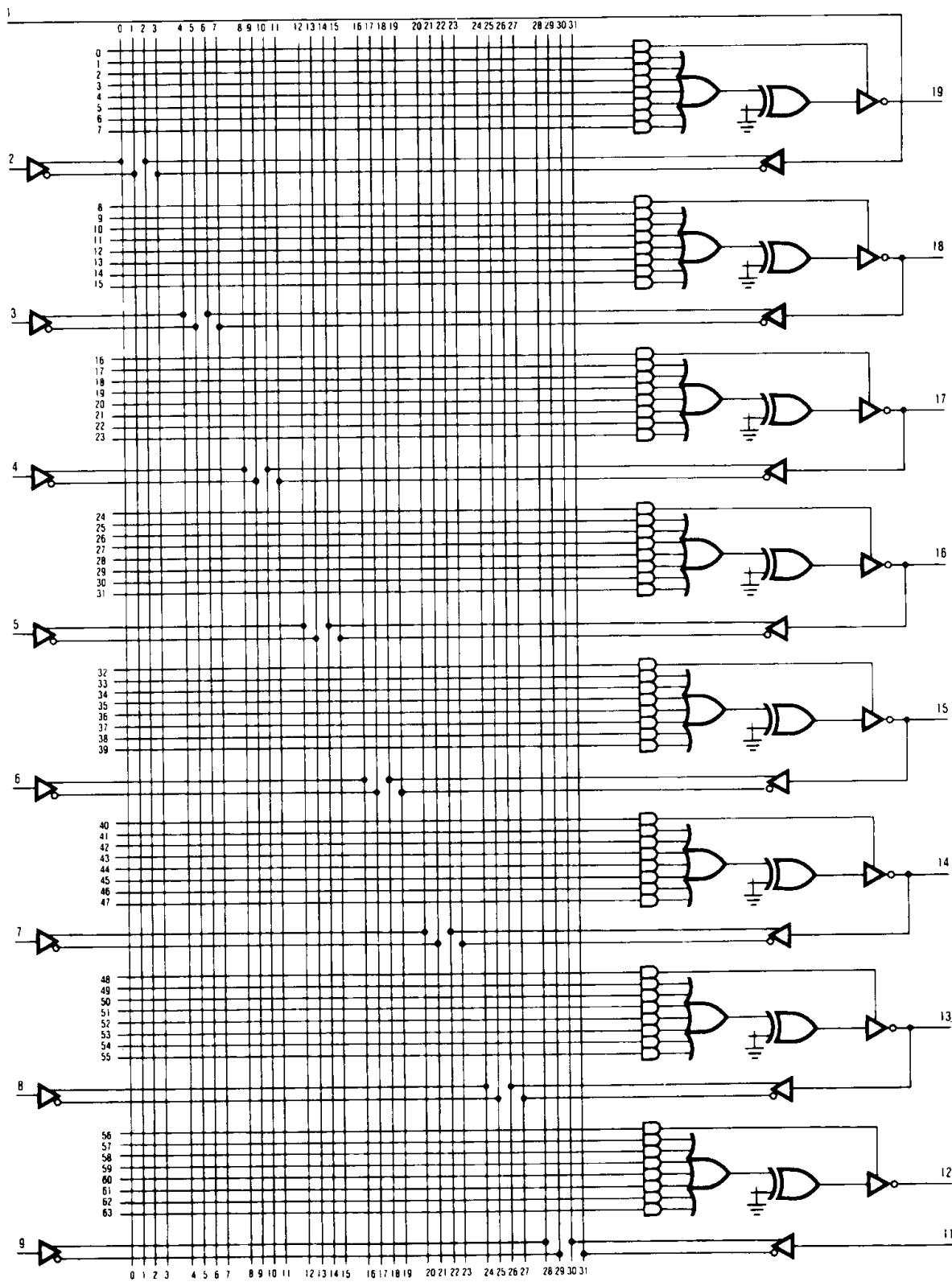
The PRELOAD function allows the register to be loaded from data placed on the output pins. This feature aids functional testing which would otherwise require a state sequencer for test coverage. The procedure for PRELOAD

## Programming Waveform



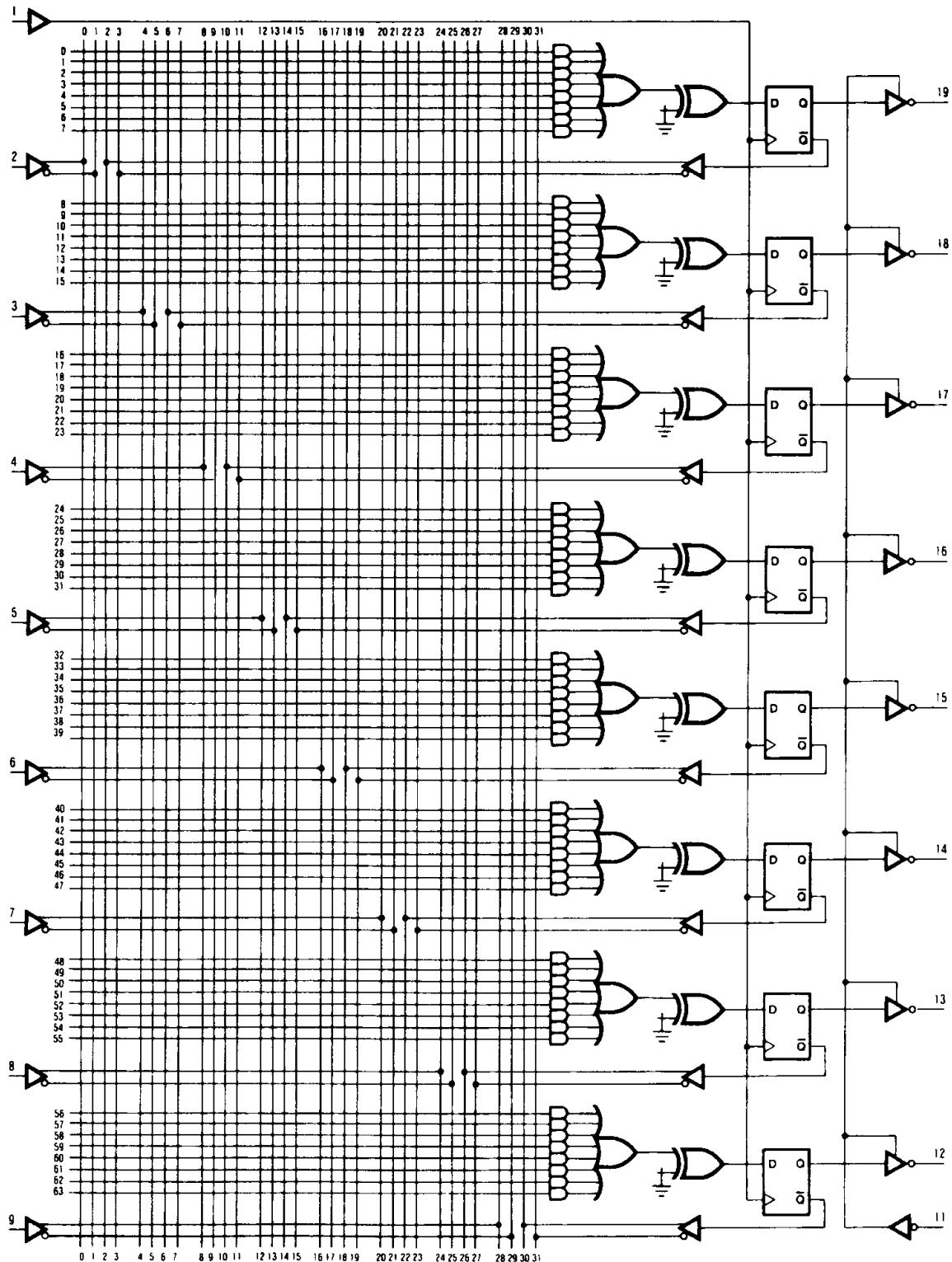
TL/L/8504-13

## Logic Diagram PAL16P8A



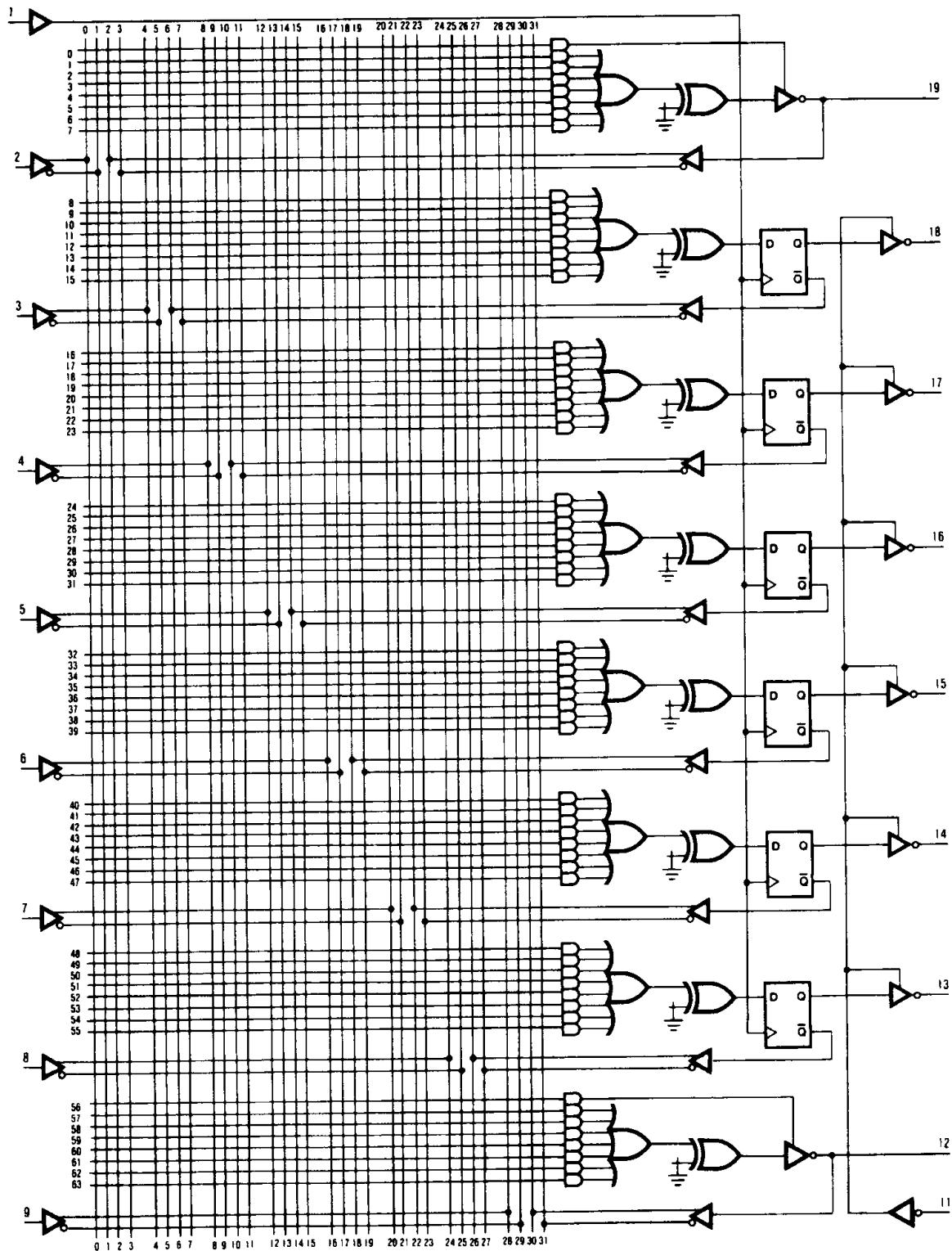
TL/L/8504-15

## Logic Diagram PAL16RP8A



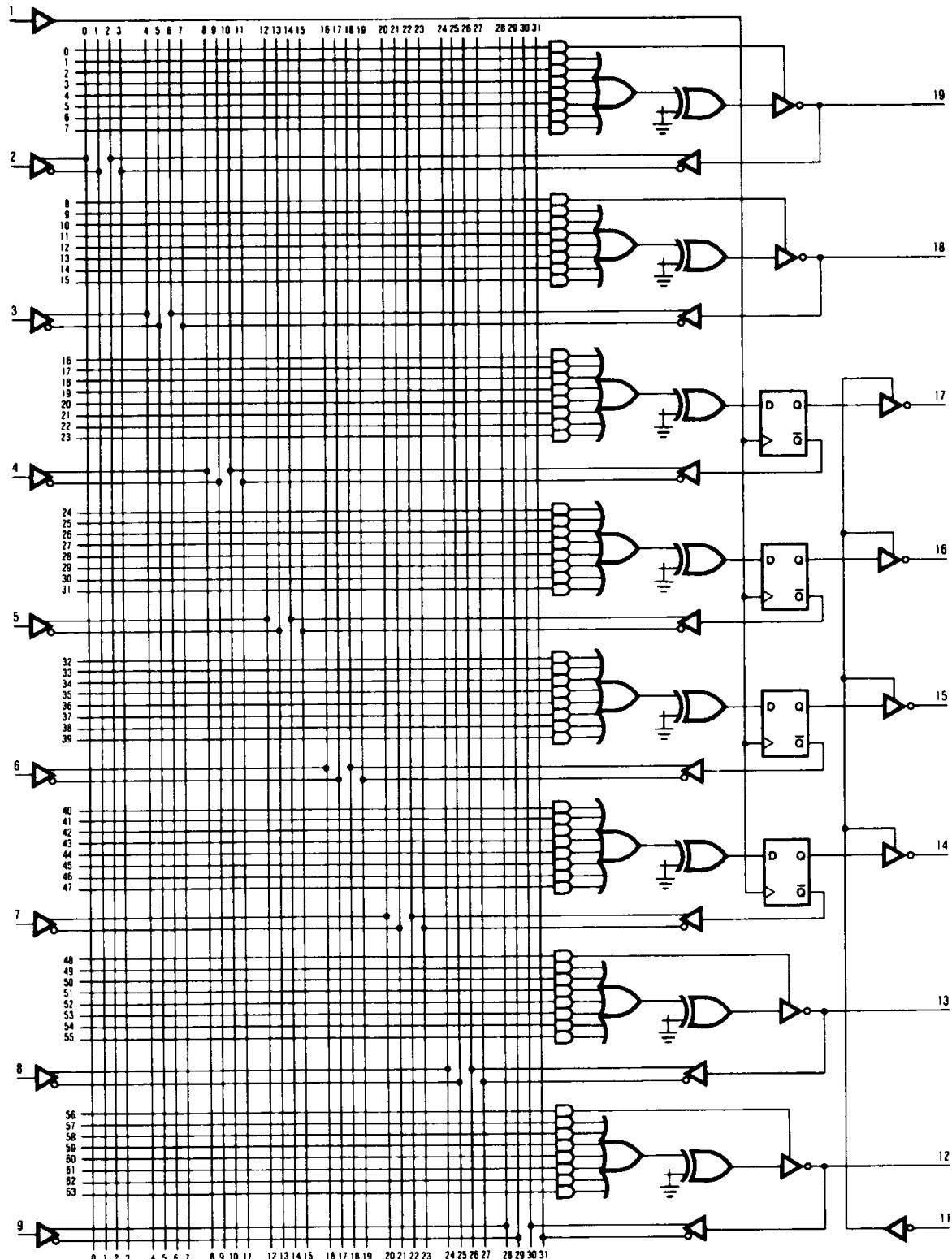
TL/L/8504-14

## Logic Diagram PAL16RP6A



TL/L/8504-16

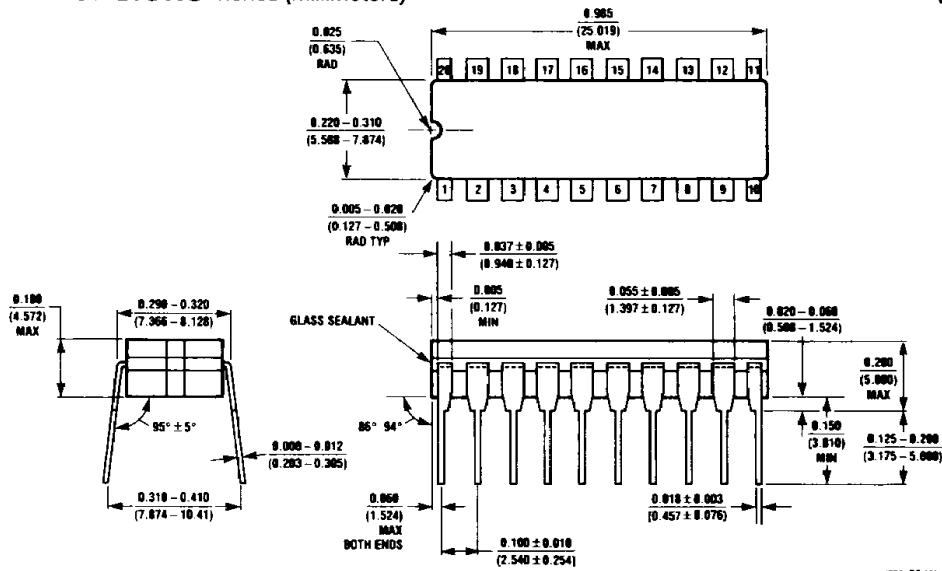
## Logic Diagram PAL16RP4A



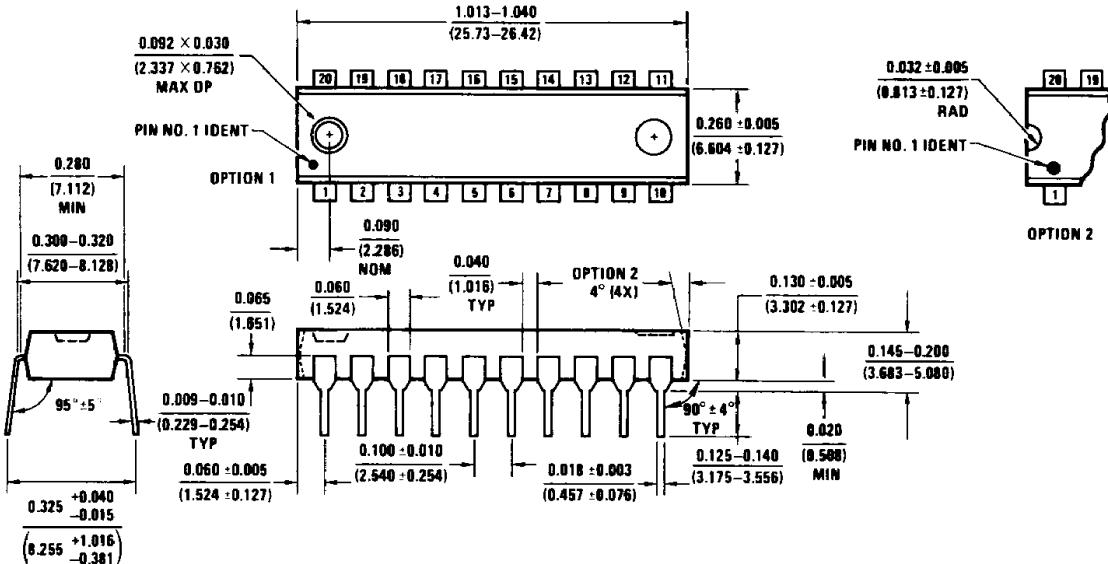
TL/L/8504-17

**Physical Dimensions** inches (millimeters)

Lit # 114405



J20A (REV M)

**20-Lead Dual-In-Line Package (J)  
NS Package J20A**


N20A (REV F)

**20-Lead Dual-In-Line Package (N)  
NS Package N20A**
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