# IC testing pushes zero defects in autos

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As the amount of electronic content in automobiles continues to increase, tighter control over the IC parts going into modern autos is needed so that defect per million (DPM) rates are driven down, field returns and warranty issues related to electronic components are minimized, and liability is decreased.

The Automotive Electronics Council AEC-Q001 specification recommends a general method for using part average testing (PAT) to remove abnormal parts from populations and thus improve the quality and reliability of parts from a supplier. PAT is a methodology that prescribes finding test results that fall outside six sigma from the population mean for a given wafer, lot or group of parts being tested. Any test result outside the six-sigma limit for a given device is considered an outlier and removed from the population–parts that fail the PAT limits are not shipped to the customer.

There is intense pressure to improve reliability and bring the defect rate down, especially now that many important safety functions such as braking, traction control, and dynamic and active stability control are governed by semiconductors. While dedicated to improving the quality of shipped parts, suppliers are also trying to minimize the impact of applying these specifications to their yields. Since manufacturing costs continue to drop and test costs remain relatively flat, the margins on devices shrink as test cost becomes a greater component of manufacturing cost. Major yield hits simply cannot be tolerated–suppliers must thoroughly evaluate their test process to find candidate tests and iteratively refine the candidate list until they zero in on a good target.

Without sophisticated analysis and simulation tools, suppliers will be applying these specifications without a good understanding of what it means to their supply chain–or applying them blindly and missing critical tests, resulting in shipping at the same DPM rates with the guarantee that the devices were tested using a specification like PAT. In such a case, the guarantee is meaningless and reliability suffers.

Some suppliers seem to think that performing PAT at wafer probe is good enough, but studies show countless issues with that approach. Using PAT at wafer probe is the first quality gate, but the rest of the downstream manufacturing process adds potential variability from a myriad of sources–variability that causes more PAT outliers at package test. If suppliers truly want to ship the highest quality parts, they will need to perform PAT at both probe and final test, and their customers should drive this approach. One look at the data conclusively supports that PAT must be performed at both quality gates.

One method in the PAT process is to analyze recent data from several lots to establish static PAT limits for each test of interest. These limits are calculated as the Robust Mean ± Six Sigma and are normally incorporated into the test program as the upper specification limit (USL) and the lower specification limit (LSL). Static PAT limits must be reviewed and updated at least every six months.

The preferred method is to calculate dynamic PAT limits for each lot or wafer. The dynamic PAT limits are normally tighter than the static PAT limits and weed out any outliers not in the normal distribution. The important distinction is that dynamic PAT limits are calculated on a wafer or lot basis, thus the limits are continuously changing based on the performance of the material for that wafer or lot. Dynamic PAT limits are calculated as the Mean ± (n * Sigma) or Median ± (N * Robust Sigma) and cannot be less than the LSL or greater than the USL specified in the test program.

Calculated dynamic PAT limits are designated as the lower PAT limit (LPL) and the upper PAT limit (UPL) in **Figure 1**. Any values outside the dynamic PAT limits but within the LSL and USL are

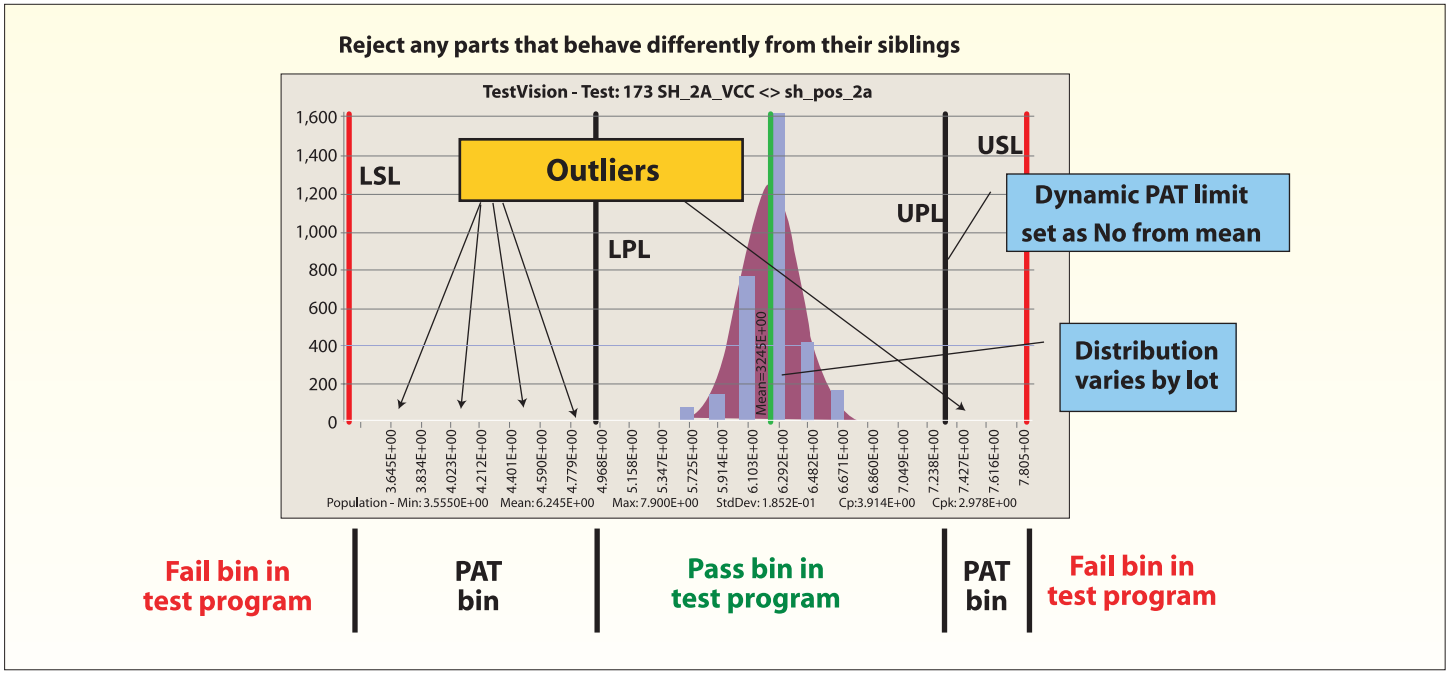


Figure 1: Any values outside the dynamic PAT limits but within the LSL and USL are considered outliers, which are usually designated as failures.

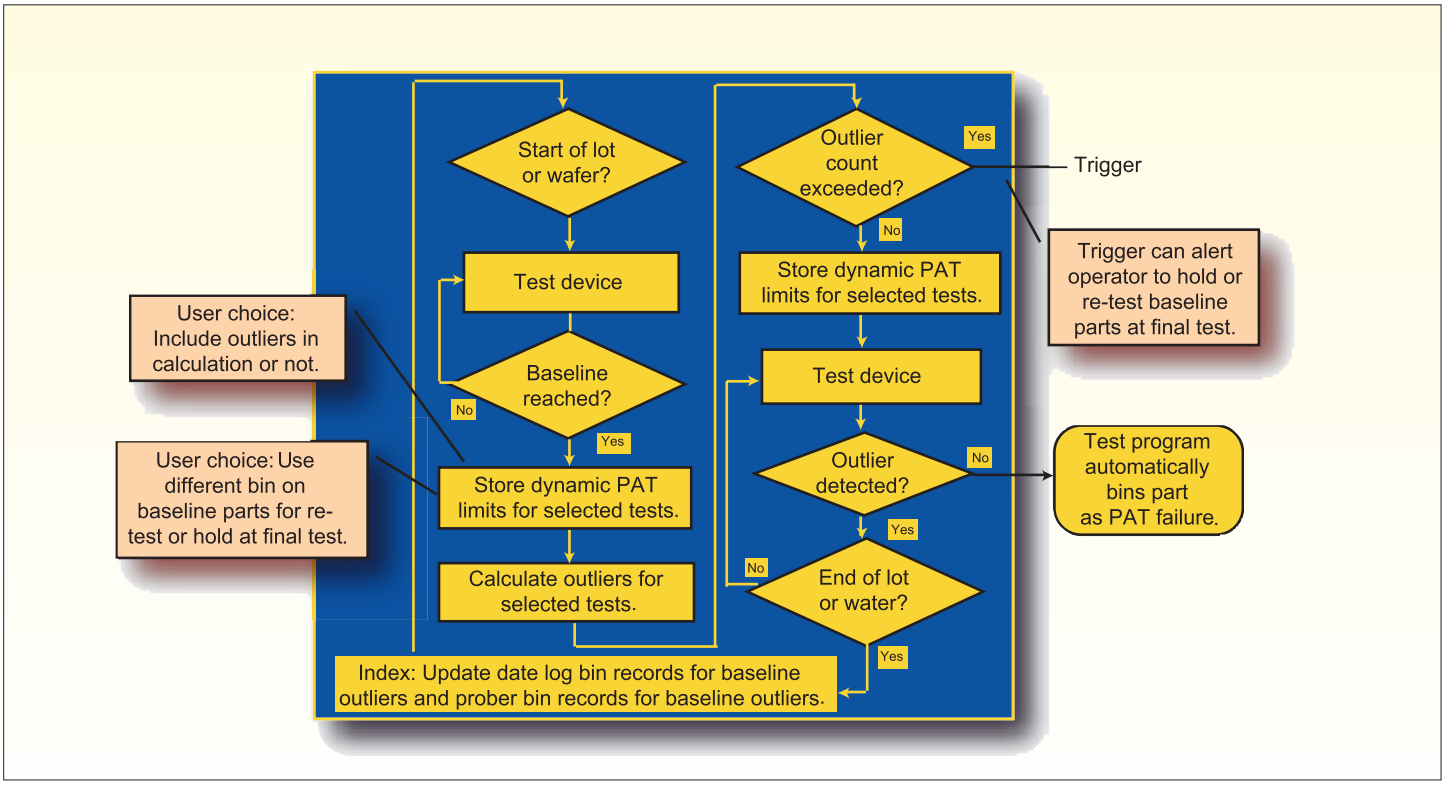


Figure 2: Some tests may simply not be 'stable' enough to be measured against the PAT standard.

considered outliers. These outliers are usually designated as failures and are binned out to a special outlier software or hardware bin. Keeping track of the calculated PAT limits for a given wafer or lot and the number of outliers detected per test is important for traceability at a later date.

## Real-time implementation

There are two main and very different schools of thought when it comes to implementing PAT in production–real-time PAT and statistical post processing (SPP). Suppliers must ask themselves if they want to institutionalize two different approaches for probe and final test or if a single solution for PAT makes more sense.

Real-time PAT relies on calculating dynamic PAT limits and making binning decisions in real-time as parts are tested, without affecting test time. This requires a dynamic real-time engine that can handle complicated data streams for monitoring and sampling. Likewise, this process requires a robust statistical engine capable of taking test data and performing the necessary calculations to generate new limits, passing the new limits and binning information into the test program–all the while, monitoring the entire process to ensure stability and control. Real-time processing works for both probe and final test and handles baseline outliers as required by suppliers.

Statistical post-processing produces the same end result, processing statistics from device test and making binning decisions after a lot has been completed. However, because binning decisions are made after a lot has been processed, post-processing can only be used for wafer probe since the test and binning results must be tied to a specific device so that it can be re-binned. At package test, there is no way to connect test and binning results to a particular device because there is no tracking mechanism or serialization once parts have been packaged. SPP also requires 100 percent data logging of test results so that decisions can be made, increasing IT infrastructure needs and slowing test times. Since results are post-processed, SPP handles baseline outliers as part of the general population of devices in a lot.

Both methods allow for powerful algorithms to be run against the test and binning results, like regional PAT and other failure patterns. One example of regional PAT is the proverbial "good guy in a bad neighborhood" where one good (passing) die on a wafer is surrounded by multiple failing die. In an effort to reduce the DPM for automotive devices, most suppliers want to pitch this "good guy in the bad neighborhood" because studies show that it is highly likely that this passing device will fail prematurely.

Consider a power management device made for automotive use. We have pulled historical test data into an analysis tool and dug deeply into the device's parametric data to discover which tests are good candidates for PAT. Some tests are better than others, more suited to PAT, or more critical to the functioning of a device. If all tests for a device are selected, the yield hit will be quite unacceptable.

The problem with some tests is that they are simply not "stable" enough to be measured against the PAT standard. The source of variability may be inherent in the device itself, may come from the test process (i.e. an instrument in a piece of ATE incapable of producing granular measurement), or may have been introduced during the packaging process. These tests are simply not in statistical control and cannot be measured.

A baseline is used to establish dynamic PAT limits on a given wafer or lot. For example, on a wafer containing 1,000 die, a baseline of 100 representative die would be an appropriate statistical sample of that wafer.

Once the baseline is reached, several important tasks are performed before dynamic PAT limits can be applied in the real-time environment. A normalcy check is performed for each of the selected tests. If the data is normally distributed the standard deviation is calculated using the "normal" method, but if the data is not normally distributed the standard deviation is calculated using the "robust" method.

## Forward to implementation

The dynamic PAT limits for each selected test must be calculated and stored in memory for use on subsequent tests. The original LSL and USL are unchanged and used to detect test failures according to the original test program pass/fail binning. Calculations to identify outliers in the baseline for the selected tests are performed. At

probe test, the x-y coordinates are saved for processing at end of wafer. At package test, the baseline devices are binned to a "baseline" bin. If outliers are detected in the baseline, these devices can then be identified for re-test.

After the baseline is reached, each selected test is checked against the dynamic PAT limits and binned accordingly in real-time for each device. Devices that fail the PAT limits drop into a unique "outlier" software or hardware bin, which identifies them as PAT outlier devices post-test.

The best part of a real-time system is the potential for real-time process feedback while devices are being tested, triggering actions and alerting personnel to issues immediately. For example, a trigger may be actuated if the total number of outliers in the baseline exceeds a user-entered threshold and alerts the test operator that the baseline binned parts at package test should be retested.

In a real-time environment, outliers in the statistical baseline must be post processed after the lot has been run. In the SPP environment, this is not an issue, since the entire population of data is processed at the same time, after the lot has finished. Handling of outliers in baseline devices is important, even if the actual number of outliers is usually small.

While both PAT solutions offer advantages, the fastest road to meeting reliability requirements without disturbing the test process is via real-time, active quality management that is based on sound statistical methodologies.