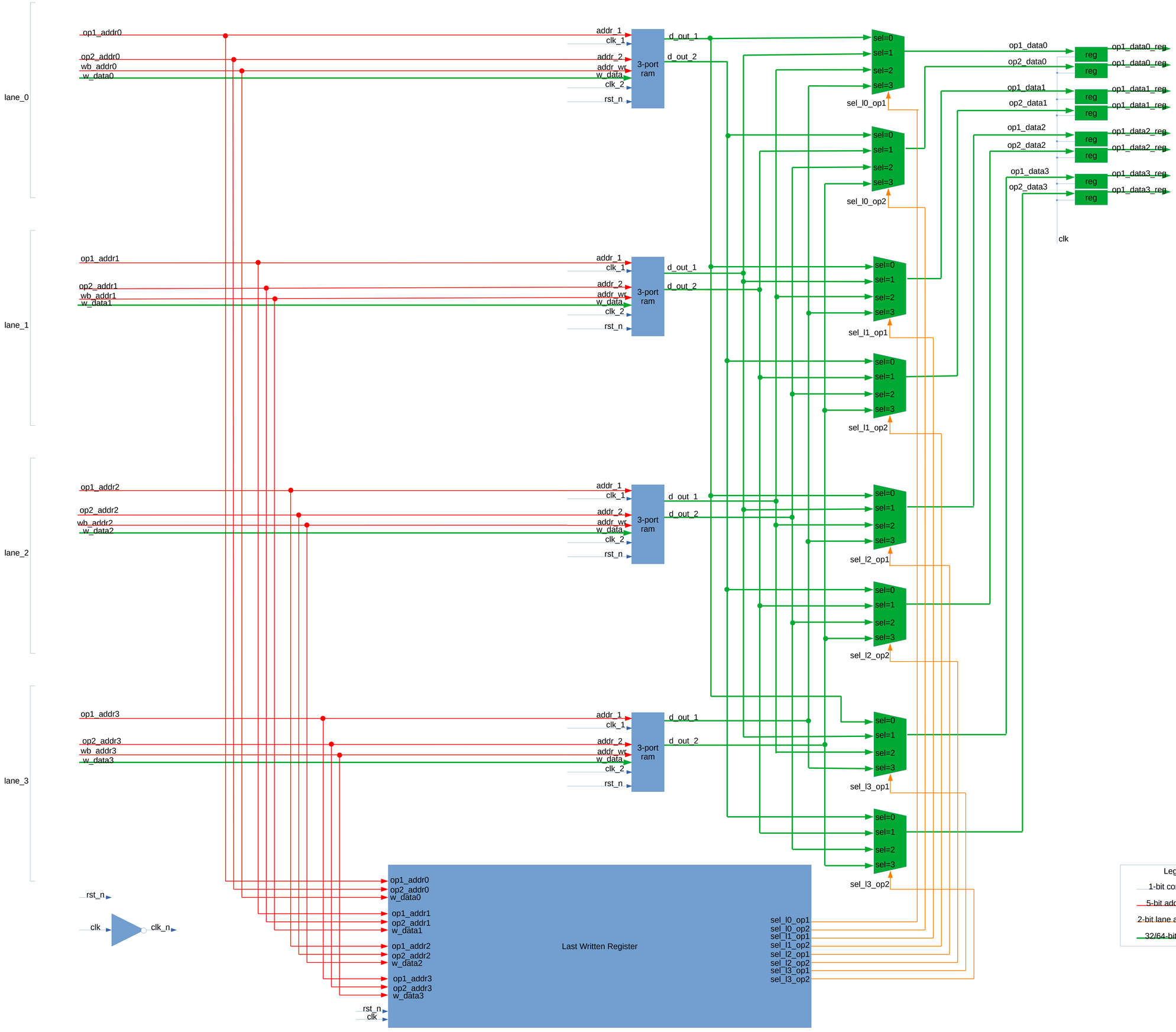
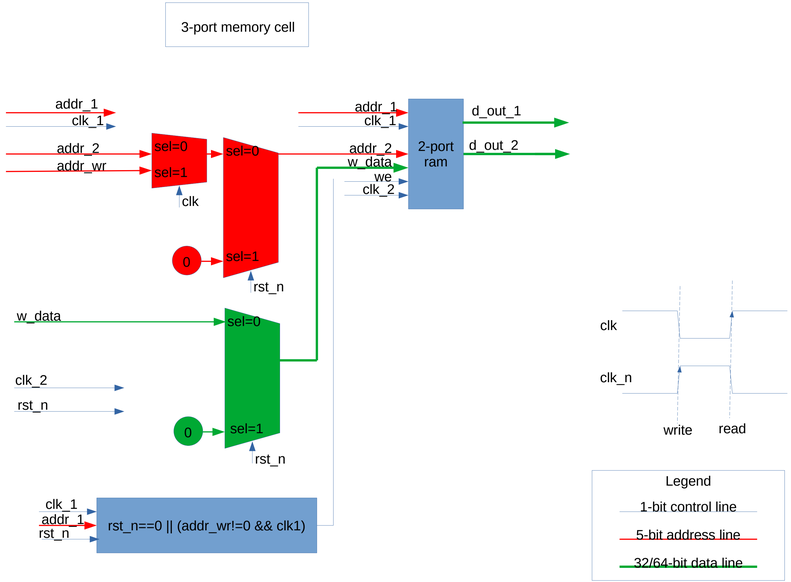

lane_0
lane_1
lane_2
lane_3
op1_addr0
op2_addr0
wb_addr0
w_data0
op1_addr1
op2_addr1
wb_addr1
w_data1
op1_addr2
op2_addr2
wb_addr2
w_data2
op1_addr3
op2_addr3
wb_addr3
w_data3
addr_1
clk_1
addr_2
addr_wr
w_data
clk_2
rst_n
3-port ram
d_out_1
d_out_2
sel=0
sel=1
sel=2
sel=3
sel_l0_op1
sel_l0_op2
sel_l1_op1
sel_l1_op2
sel_l2_op1
sel_l2_op2
sel_l3_op1
sel_l3_op2
op1_data0
op2_data0
op1_data1
op2_data1
op1_data2
op2_data2
op1_data3
op2_data3
reg
op1_data0_reg
op1_data1_reg
op1_data2_reg
op1_data3_reg
clk
rst_n
clk
clk_n
Last Written Register
sel_l0_op1
sel_l0_op2
sel_l1_op1
sel_l1_op2
sel_l2_op1
sel_l2_op2
sel_l3_op1
sel_l3_op2
Legend
1-bit control line
5-bit address line
2-bit lane address line
32/64-bit data line


3-port memory cell
addr_1
clk_1
addr_2
addr_wr
sel=0
sel=1
clk
sel=0
sel=1
0
rst_n
addr_1
clk_1
addr_2
w_data
we
clk_2
2-port
ram
d_out_1
d_out_2
w_data
sel=0
clk_2
rst_n
0
sel=1
rst_n
clk_1
addr_1
rst_n
rst_n==0 || (addr_wr!=0 && clk1)
clk
clk_n
write
read
Legend
1-bit control line
5-bit address line
32/64-bit data line

Last Written Register

op1_addr0
op2_addr0
w_data0
op1_addr1
op2_addr1
w_data1
op1_addr2
op2_addr2
w_data2
op1_addr3
op2_addr3
w_data3
rst_n
clk

sel_l0_op1
sel_l0_op2
sel_l1_op1
sel_l1_op2
sel_l2_op1
sel_l2_op2
sel_l3_op1
sel_l3_op2

This module has no diagram, it is implemented directly in Verilog.

R1[2]
R2[2]
R3[2]
R4[2]
R5[2]
R6[2]
R7[2]
R8[2]
R9[2]
R10[2]
R11[2]
R12[2]
R13[2]
R14[2]
R15[2]
R16[2]

Legend
1-bit control line
5-bit address line
2-bit lane address line
32/64-bit data line