***Advanced System on Chip Course***

**QUIZ 7**

**Issue 1.0**

# MODULE 7: AXI4-Lite GPIO peripheral and DDR Memory Controller

**Question 1:**

Which of the following tasks is typically performed by a GPIO peripheral?

1. It provides interface between the system bus and an LCD screen.
2. It is used to generate parallel communication interfaces.
3. It provides additional storage space for data and control signals.
4. None of the above.

**Question 2:**

Why are GIPO peripherals widely used in systems on chips?

1. Because they facilitate the interaction between the system and the environment, especially in embedded applications.
2. Because they facilitate the integration of IP cores from different vendors in order to achieve a required functionality.
3. Because they provide high-speed transceivers for high-bandwidth data I/O.
4. Because they improve the performance of the system by enhancing its storage capacity.

**Question 3:**

Typically, what are the configurable properties of a GPIO?

1. Pin enable, clock frequency, select connected peripheral.
2. Pin enable, clock frequency, depth of shift register.
3. Pin enable, data direction, select connected peripheral.
4. None of the above.

**Question 4:**

Which of the following statements is NOT correct?

1. Volatile memory typically needs longer access time compared to non-volatile memories.
2. Non-volatile memory is typically used for permanent data storage.
3. Volatile memory generally has a smaller storage capacity compared to non-volatile memory.
4. Non-volatile memory is generally more expensive than volatile memory.

**Question 5:**

Which of the following characteristics of an SoC are affected by the size of its on-chip memory?

1. Performance.
2. Power consumption.
3. Storage capability.
4. All of the above.

**Question 6:**

What is the minimum number of bits needed to represent an address in memory that has a storage capacity of 1kB?

1. 16 bits.
2. 10 bits.
3. 9 bits.
4. 8 bits.

**Question 7:**

Which of the following statements is NOT correct?

1. The bitline amplifier is typically a part of memory read/write interface circuitry.
2. The bitline amplifier amplifies the low voltage binary data signals at the output of the memory to recognizable logic levels that can be interpreted properly by logic outside the memory.
3. The bitline amplifier is controlled by the address decoder.
4. The design of bitline amplifier requires analog circuitry.

**Question 8:**

Choose one memory type that can retain data even when disconnected from the power supply:

1. DDR.
2. DRAM.
3. Flash.
4. SRAM.

**Question 9:**

Which of the following is an advantage of DRAM over SRAM?

1. Unlike DRAM, a SRAM requires constant electrical support.
2. A DRAM cell requires fewer transistors than a SRAM cell.
3. A DRAM cell is capable of storing multiple bits compared to the single bit storage capacity of a SRAM cell.
4. A DRAM cell does not need to be constantly refreshed, unlike a SRAM cell.

**Question 10:**

Which of the following statement(s) is correct?

1. The purpose of having 2 bit lines (bit and bit’) in a SRAM memory cell is to improve its response speed.
2. The purpose of having 2 bit lines (bit and bit’) in a SRAM memory cell is to increase its storage capacity.
3. The purpose of having 2 bit lines (bit and bit’) in a SRAM memory cell is to reduce its power consumption.
4. The purpose of having 2 bit lines (bit and bit’) in a SRAM memory cell is to is to improve its noise margin.

**Question 11:**

Which of the following statements is an INCORRECT description of memory controllers?

1. A memory controller manages read and write operations to the memory block.
2. Some memory controllers can be connected to different memory devices at the same time.
3. A memory controller sometimes provides electrical support for some types of memory (e.g. DRAM).
4. The temporary buffers in memory controllers increase the storage capacity of the memory.

**Question 12:**

How many transistors a typical SRAM cell has?

1. Nine.
2. One.
3. Six.
4. Four.

**Question 13:**

In DDR (Double Data Rate) SDRAM:

1. Synchronous data transfer speed-up is achieved by writing and reading at the same time.
2. Synchronous data transfer speed-up is achieved by transferring data on both rising and falling edges of the clock signal.
3. Data transfer speed-up is achieved by writing and reading asynchronously.
4. None of the above.

**Question 14:**

Regarding ROM (read-only Memory):

1. Is non-volatile memory that only permits sequential address read operations.
2. Is non-volatile memory that permits random-access read operations.
3. Is volatile memory that only permits sequential address read operations.
4. Is volatile memory that permits random-access read operations.

**Question 15:**

Using the AXI low-power interface:

1. Only peripherals which require powerdown sequences can be controlled.
2. Only peripherals which do not require powerdown sequences can be controlled.
3. Both types of peripherals, those which require powerdown sequences and those which do not, can be controlled.
4. None of the above.

**Answers**

Q1)1

Q2)1

Q3)3

Q4)1

Q5)4

Q6)2

Q7) 3

Q8) 3

Q9)2

Q10)4

Q11)4

Q12)3

Q13)2

Q14)2

Q15)3