Physical Layer Simulation of IEEE 802.11ad

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https://github.com/armaank/IEEE802.11ad

Abstract—We simulate a portion of the physical (PHY) layer of the IEEE 802.11ad standard for directional, multi-gigabit (DMG) wireless communication. The standard specifies a single carrier (SC)-PHY layer, that specifies various required modulation and coding schemes (MCS), as well as a frame structure. We demonstrate a functional link over an additive white Gaussian noise (AWGN) channel and present bit-error-rate (BER) curves for each of the data rates in the DMG SC-PHY specification.

Index Terms—IEEE802.11ad, WiGIG, wireless link simulations, Low-Density Parity Check Codes

I. INTRODUCTION

EEE 802.11ad was added to the 802.11 standard in 2012 as one of the first wireless standards to support multi-gigabit communications. The system achieves such high datarates by operating at the 60GHz band, with a 2GHz bandwidth, sacrificing range for tremendous throughput. Early applications of the standard include SoCs designed for virtual reality. The specification requires four different MCSs, however the core architecture of the DMG SC-PHY is illustrated below:

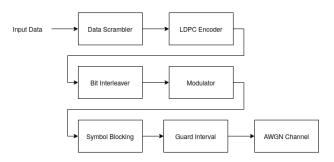


Figure 1. Transmitter block diagram for the DMG SC-PHY specification in IEEE 802.11ad

II. SYSTEM ARCHITECTURE

A single frame consists of a short-training field (STF), a channel estimation field (CEF), a header and the data field.

A. Frame Structure

The STF consists of 16 repetitions of Golay sequences, $Ga_{128}(n)$ of length 128, followed by a single repetition of $-Ga_{128}(n)$. The CEF is used for channel estimation, as well as indication of which modulation is going to be used for the packet. The CEF is composed of a concatenation of two sequences Golay sequences, $Gu_{512}(n)$ and $Gv_{512}(n)$, where the last 128 samples of $Gu_{512}(n)$ and $Gv_{512}(n)$ are equal to

the last 128 samples used in the STF. They are followed by a 128 samples sequence $Gv_{128}(n)$ equal to the first 128 samples of both $Gv_{512}(n)$ and $Gu_{512}(n)$. The CEF is pictured below in Fig. 2

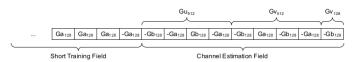


Figure 2. Channel estimation field for SC

The header is fixed in length and comprised of twelve fields. The data field is is made up of the message bits, split up into blocks.

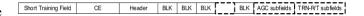


Figure 3. Frame structure for IEEE802.11ad

The AGC and TRN-R/T subfields are used for power and synchronization. We don't implement these fields, as they are optional according to the specification.

B. Data Scrambler

The header and data fields following the scrambler initialization field are scrambled by XORing each bit in turn with a length 127 periodic sequence generated by the polynomial $S(x) = x^7 + x^4 + 1$. This is realized using a linear feedback shift register (LFSR) structure. The seed value is set randomly and added unscrambled as the seven bits of the header field for the receiver.

C. Encoding

The data are encoded by a systematic LDPC encoder. The LDPC is a block code. Each block of information bits $(b_1,b_2,...,b_k)$ is concatenated with a block of parity bits $(p_1,p_2,...,p_{n-k})$ to create a codeword $c=(b_1,b_2,...,b_k,p_1,p_2,....,p_{n-k})$ such that $Hc^T=0$, where H is the (n-k)xn party check matrix. The block size n is $L_{CW}=672$ bits. The code rate, R, is equal to k/n.

Regarding the data, the LDPC encoding scheme depends on the repetition rate. If the repetition rate is 1, The output stream of the scrambler is broken into blocks of $L_{CWD}=L_{CW}\times R$ bits. To each data word, $n-k=L_{CW}-R\times L_{CW}$

MCS Indecx	Modulation	N_{cbps}	Repetiton	Code Rate	Data Rate (Mbps)
1	$\pi/2$ BPSK	1	2	1/2	385
2	$\pi/2$ BPSK	1	1	1/2	770
3	$\pi/2$ BPSK	1	1	5/8	962.5
4	$\pi/2$ BPSK	1	1	3/4	1155
5	$\pi/2$ BPSK	1	1	13/16	1251.25
6	$\pi/2$ QPSK	4	1	1/2	1540
7	$\pi/2$ QPSK	4	1	5/8	1925
8	$\pi/2$ QPSK	4	1	3/4	2310
9	$\pi/2$ QPSK	4	1	13/16	2502.5

parity bits are added to create a codeword c^m (the mth word), such that $Hc^{m^T}=0$. If the repetition rate is 2, then the data bits in each code word are concatenated with $L_{cw}/4$ zeros. The LDPC codeword c is created by generating the parity bits such that $Hc^T=0$, where H is the parity matrix for rate 1/2 LDPC code. Finally, we replace bits $L_{cw}/4+1$ through 336 of the codeword c with bits from the sequence XORed by a PN sequence that is generated from the LFSR used for data scrambling as defined. The LFSR is initialized to the all ones vector and reinitialized to the same vector after every codeword. Regardless of repetition rate, the coded bits then are concatenated together and padded.

The header is encoded separately from the data bits. The input header bits are scrambled, starting at the eight bit. The LDPC codeword c is generated by concatenating the header with the appropriate amount of zeros, such that $Hc^T=0$, where H is the parity check matrix for a rate 3/4 code. The header is then split up into two sequences, one of which is XORed with a PN sequence from the LFSR, initialized to the all ones vector. The two sequences are then concatenated together to form the encoded header bits. For each of the different code rates, the standard specifies a different parity check matrix H.

D. Modulation, Blocking and Guard Intervals

The STF, CEF is modulated as $\pi/2$ BPSK. The data field is modulated in ordinance with the specific modulation and coding scheme. Depending on the symbol mapping, a guard interval made of a 64 bit Golay sequence is inserted into the data field. For example, for $\pi/2$ BPSK, the number of coded bits per block (N_{cbpb}) is 448. Fig. 4 illustrates the insertion of the guard intervals for this case.



Figure 4. Block transmission for pi/2 BPSK

The two code words in the header field are blocked, an a 64 bit Golay sequence is placed between the two. The header

is then modulated as $\pi/2$ BPSK.

III. MODULATION AND CODING SCHEMES

We simulated the modulation and coding schemes, presented in Table I. For a transmitter or receiver to comply to the standard, only MCSs 1-4 must be implemented, all others are beyond the scope of what is required in the specification.

MCS 1 is typically designated for a control channel, whereas all other MCSs are used for high bit-rate data transmission.

IV. SIMULATIONS AND RESULTS

We simulated each of the specified MCSs over an AWGN channel to compute bit error rate curves. The standard was designed for high data rate communications, and uses extensive error correction, so simulating takes an extensive amount of computational time. In particular, we were unable to simulate more than one point on the BER curve for MCS 1, due to the repetition coding.

We simulated the transmission of ten frames, each consisting of 1000 data octets, corresponding to 8000 data bits per frame. For each frame, we computed the bit error rate over a range of signal-to-noise ratios for an AWGN channel. We scaled the channel noise accordingly to the modulation order and code rate. We then averaged the bit error rates over the ten packets to compute curves.

V. CONCLUSION

We successfully studied, implemented and simulated the DMG SC-PHY layer of the IEEE802.11ad standard. We were able to see how the combination of LDPC codes, various sequence types and various modulation schemes worked in tandem allow for high, multi-gigabit data rates in a wireless system.

REFERENCES