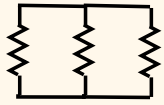
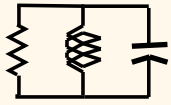
Hierarchy Level

Level 0



Resistor

Level 1

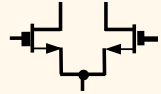


RLC

Level 2

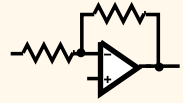
Small Signal

Level 3



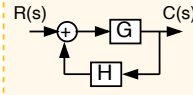
Transistor

Level 4



Block

Level 5



System

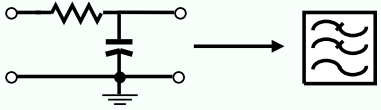
Task Category

Perception

Schematic component identification

System block identification

Circuit function classification



Analysis

Noise & Jitter

$$V_{n,rms} = \sqrt{4kTRB}; \sigma_t \approx \sigma_v / SR$$

Power & Energy

$$P_{avg} = V_{rms} \times I_{rms} \times cos(\pi)$$

Frequency Response

$$|H(j\omega)| = 1/\sqrt{1 + (\omega/\omega c)^2)}$$

Transient Response

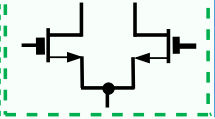
Transfer Function

⋮

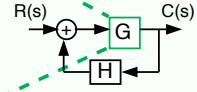
Design

Hierarchical design

Schematic-level design



Block-level design



Open-end design

Design a feedback CMOS op-amp with 1×/10×/100× gains, unity-gain stable (PM≥60°) into 10 kΩ‖50–250 pF, meeting A_0≥100 dB, GBW≥5 MHz, noise≤3 μV_{rms} (0.1–10 kHz).

Sources

Existing Online Resource

IEEE arXiv Google

Hierarchical Synthetic Generation Pipelines