Organization of Digital Computers Lab
EECS 112L

Lab 5: Synthesis

Armand Ahadi-Sarkani
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Objective

The objective of this lab is to perform synthesis on our pipelined processor in order to measure time, power, and area for it, using timing constraints to get the implementation to meet those constraints. We will also perform synthesis on a sample counter program.

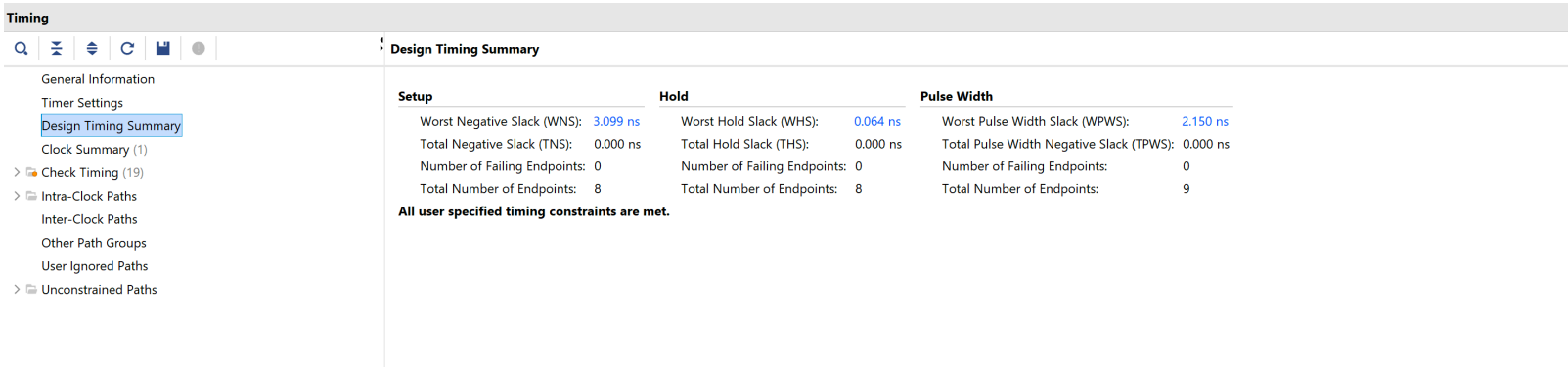
Procedure

1. The procedure for synthesis was performed on the sample counter program, using the default FPGA device.
2. Timing constraints were set for the synthesis, with a clock being set to 200 MHz, a period of 5 ns, a rise at 0 ns and fall at 2.5 ns.
3. A utilization report was created for this project.
4. A power report was created for this project, using standard parameters.
5. A schematic was generated for this project.
6. This procedure was repeated for the MIPS pipelined processor we created in Lab 4.

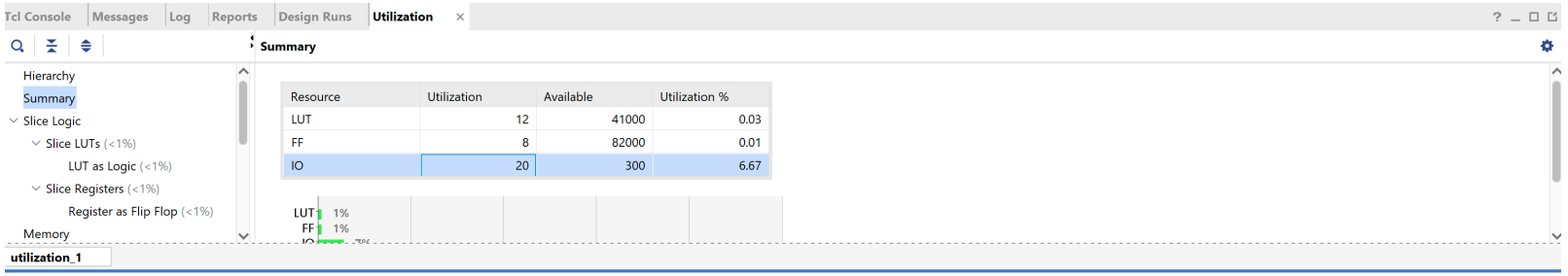
Simulation Results

Counter:

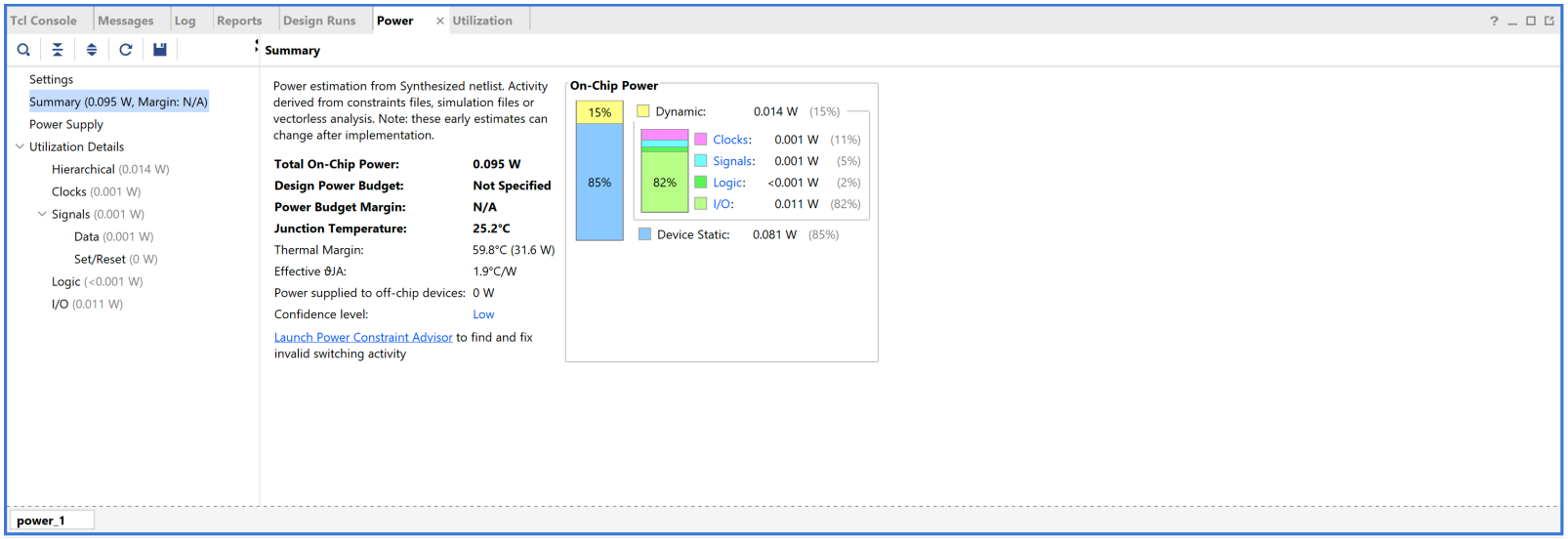
1. A screenshot of the Report Timing Summary is shown below, clearly the timing was met by the Vivado synthesis tool:



2. A screenshot of the Report Utilization is shown below. According to this report, 12 LUT, 8 FF, and 20 IO are used by this design. The number of counters is 300/20 = 15 counters, because that has the least amount of resources.

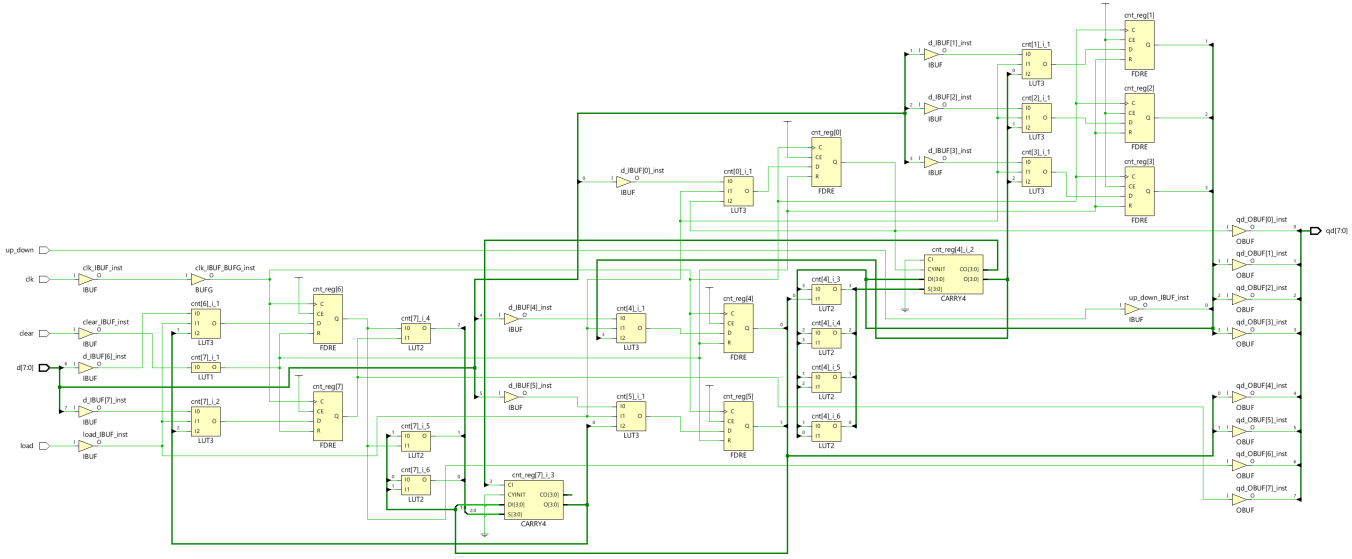


3. A screenshot of Report Power is shown below. Static power is greater than dynamic power in this case, because it is independent of the design, and in this case the design is very small and optimized such that the dynamic power used by the design is much lower than the static power that is inherently used for the FPGA. This design is clearly not using all of the capability of the FPGA.



4. I/O is the greatest source of dynamic power dissipation because of the capacitance of the I/O ports is much higher than the capacitance of the input wires in this very simple design, thus I/O capacitance makes up the largest percentage of the dynamic power dissipation.

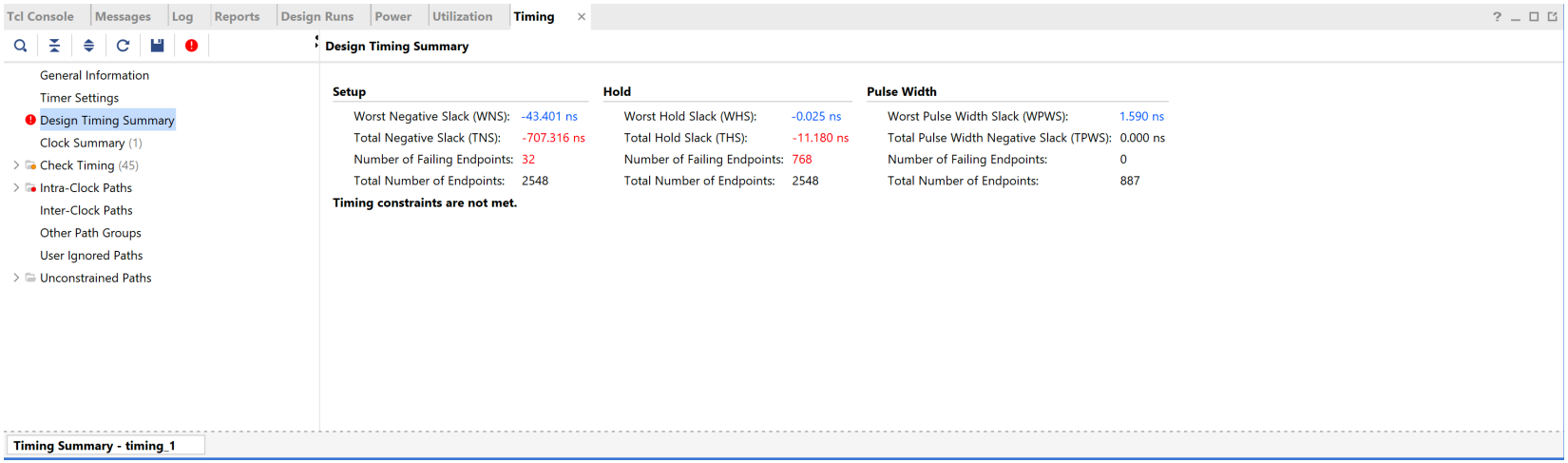
5. The schematic was found with synthesis and is shown below:



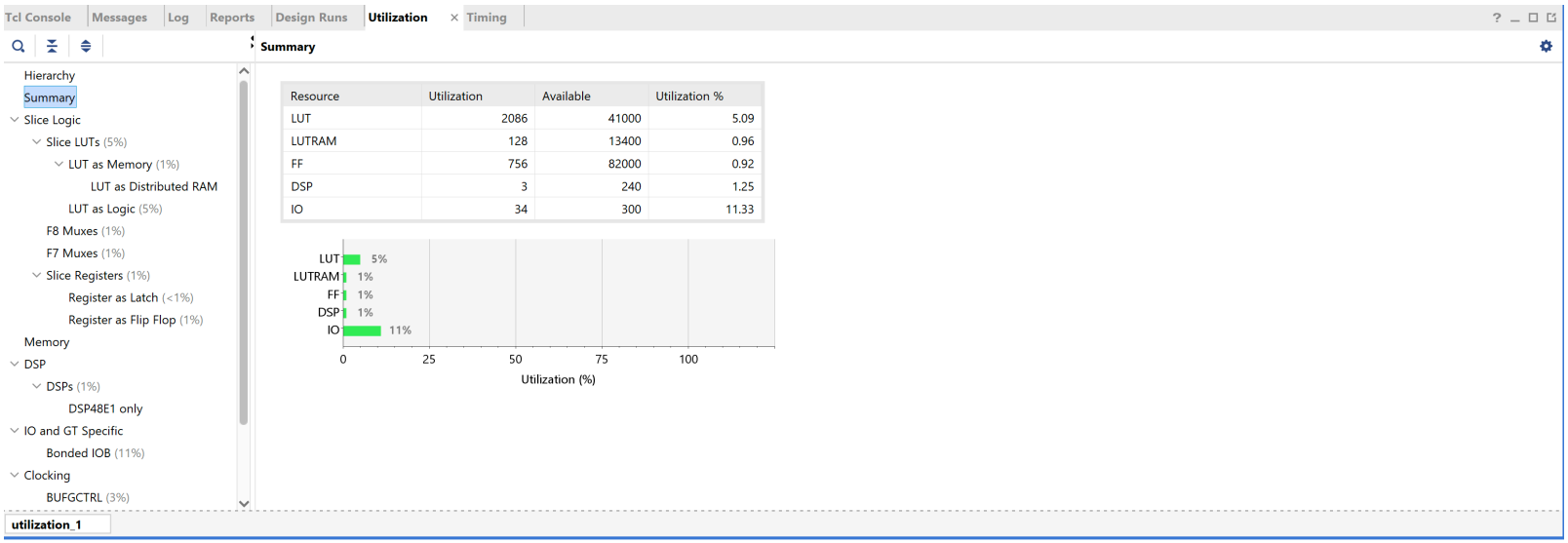
6. In the schematic, FDRE is just a type of D flip-flop that has a clock enable and a synchronous reset. LUT is a lookup table, in our case we are using LUT3, a 3-bit lookup table with dual output. CARRY4 is a fast carry logic unit with look ahead. IBUF is an I/O component that stands for input buffer. OBUF, on the other hand, is an output buffer.

MIPS Pipelined Processor:

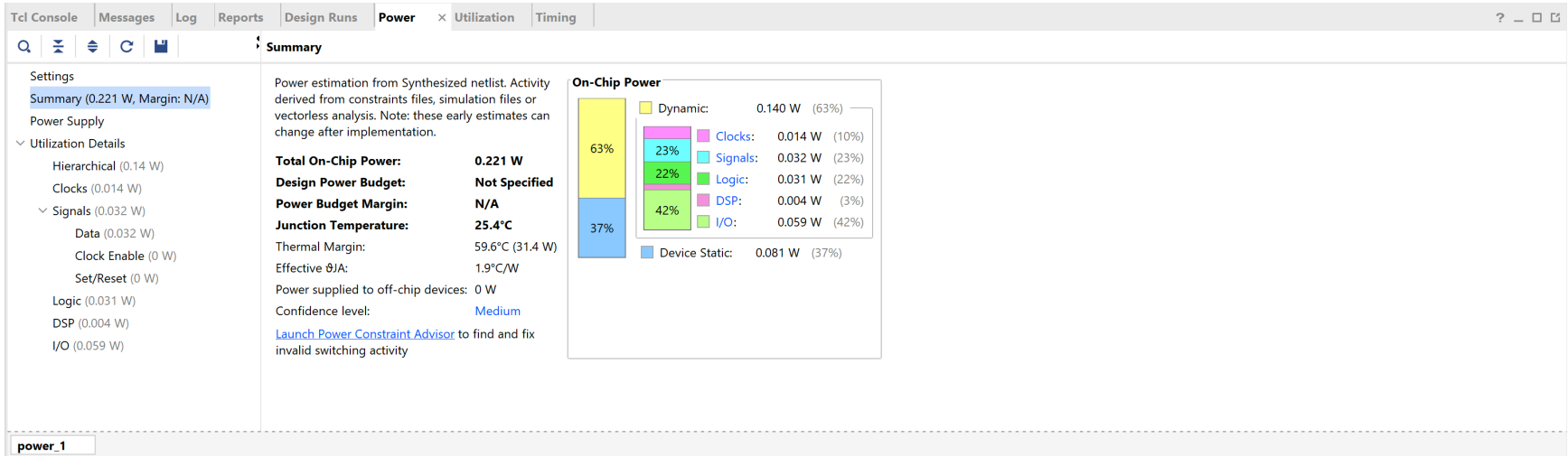
1. A screenshot of the Report Timing Summary is shown below, and the timing was not met because of the 5 ns constraint. Increasing it to 50 ns yields better results.



2. A screenshot of the Report Utilization is shown below:



3. A screenshot of the Report Power is shown below:



4. A screenshot of the schematic is shown on the next page.

Schematic

43 Cells 34 I/O Ports 847 Nets