

Organization of Digital Computers Lab

EECS 112L

Lab 5: Synthesis

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Objective

The objective of this lab is to perform synthesis on our pipelined processor in order to measure time, power, and area for it, using timing constraints to get the implementation to meet those constraints. We will also perform synthesis on a sample counter program.

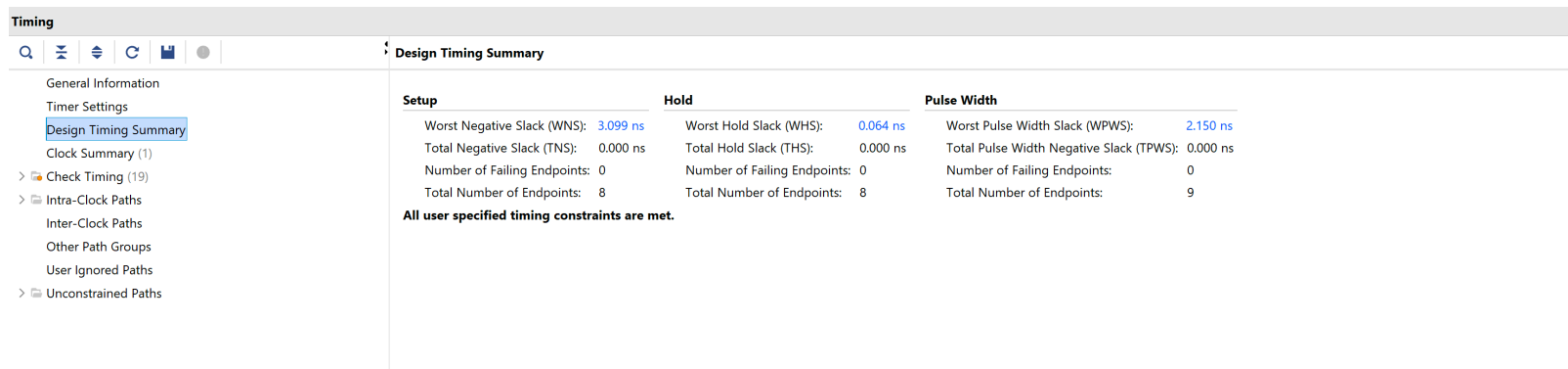
Procedure

1. The procedure for synthesis was performed on the sample counter program, using the default FPGA device.
2. Timing constraints were set for the synthesis, with a clock being set to 200 MHz, a period of 5 ns, a rise at 0 ns and fall at 2.5 ns.
3. A utilization report was created for this project.
4. A power report was created for this project, using standard parameters.
5. A schematic was generated for this project.
6. This procedure was repeated for the MIPS pipelined processor we created in Lab 4.

Simulation Results

Counter:

1. A screenshot of the Report Timing Summary is shown below, clearly the timing was met by the Vivado synthesis tool:

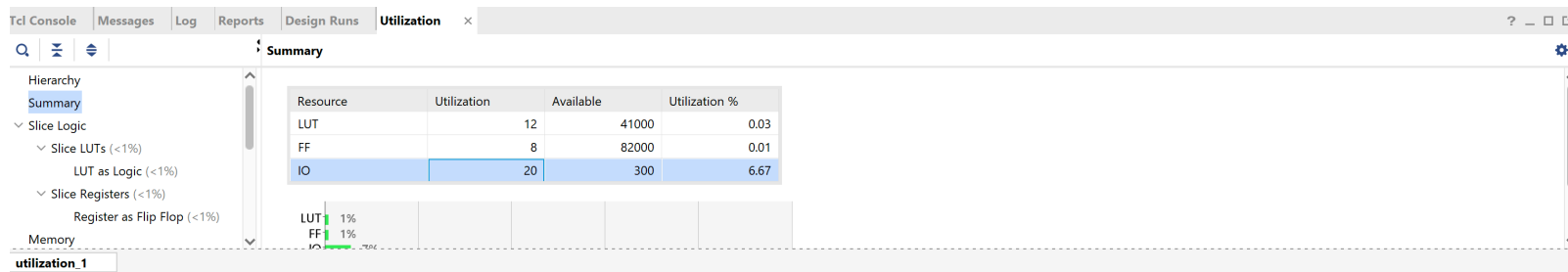


The screenshot shows the 'Design Timing Summary' window in Vivado. The left sidebar lists various timing reports, with 'Design Timing Summary' selected. The main area displays a table with three columns: Setup, Hold, and Pulse Width. The table contains summary statistics for Worst Negative Slack (WNS), Total Negative Slack (TNS), Number of Failing Endpoints, Worst Hold Slack (WHS), Total Hold Slack (THS), Worst Pulse Width Slack (WPWS), Total Pulse Width Negative Slack (TPWS), and Total Number of Endpoints. All values indicate that the timing constraints were met.

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 3.099 ns	Worst Hold Slack (WHS): 0.064 ns	Worst Pulse Width Slack (WPWS): 2.150 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 8	Total Number of Endpoints: 8	Total Number of Endpoints: 9

All user specified timing constraints are met.

2. A screenshot of the Report Utilization is shown below. According to this report, 12 LUT, 8 FF, and 20 IO are used by this design. The number of counters is $300/20 = 15$ counters, because that has the least amount of resources.

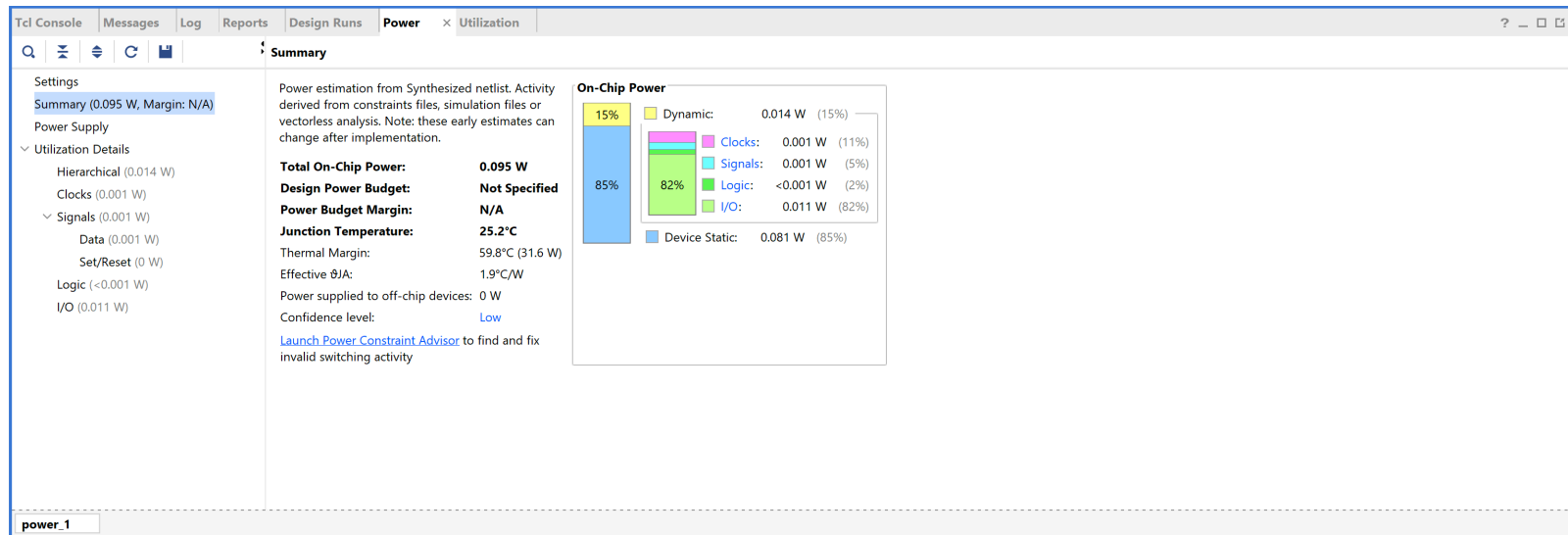


The screenshot shows the 'Report Utilization' window in Vivado. The left sidebar lists various utilization reports, with 'Summary' selected. The main area displays a table with four columns: Resource, Utilization, Available, and Utilization %. The table shows the utilization of LUTs, FFs, and IOs. The IO row is highlighted in blue.

Resource	Utilization	Available	Utilization %
LUT	12	41000	0.03
FF	8	82000	0.01
IO	20	300	6.67

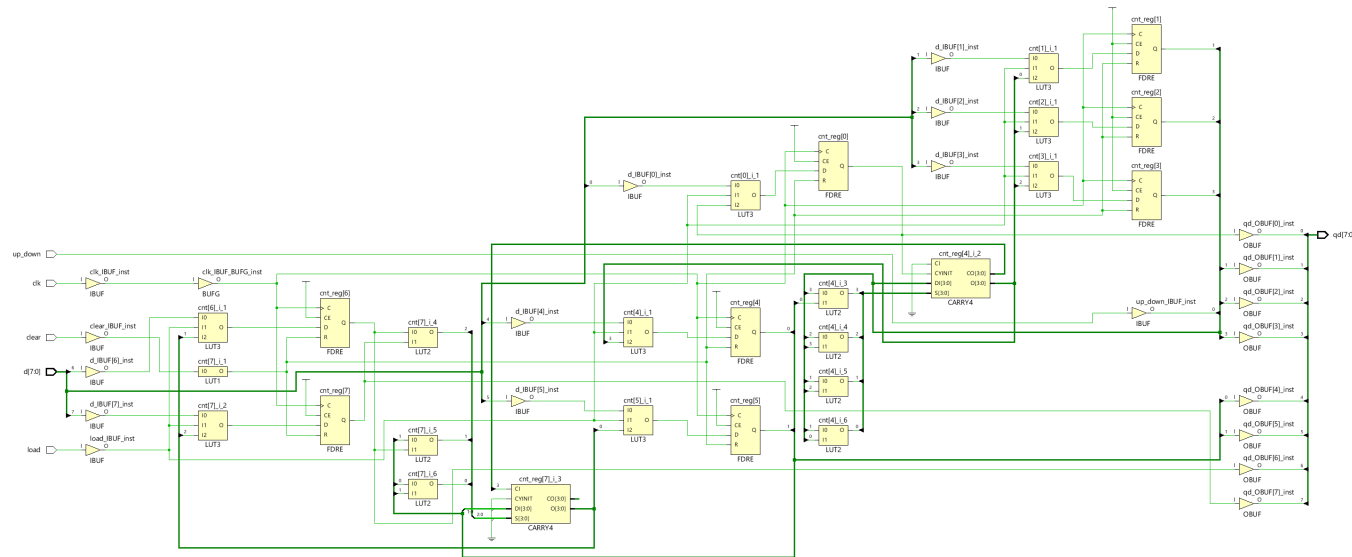
Below the table, there are small progress bars for LUT (1%), FF (1%), and IO (7%).

3. A screenshot of Report Power is shown below. Static power is greater than dynamic power in this case, because it is independent of the design, and in this case the design is very small and optimized such that the dynamic power used by the design is much lower than the static power that is inherently used for the FPGA. This design is clearly not using all of the capability of the FPGA.



4. I/O is the greatest source of dynamic power dissipation because of the capacitance of the I/O ports is much higher than the capacitance of the input wires in this very simple design, thus I/O capacitance makes up the largest percentage of the dynamic power dissipation.

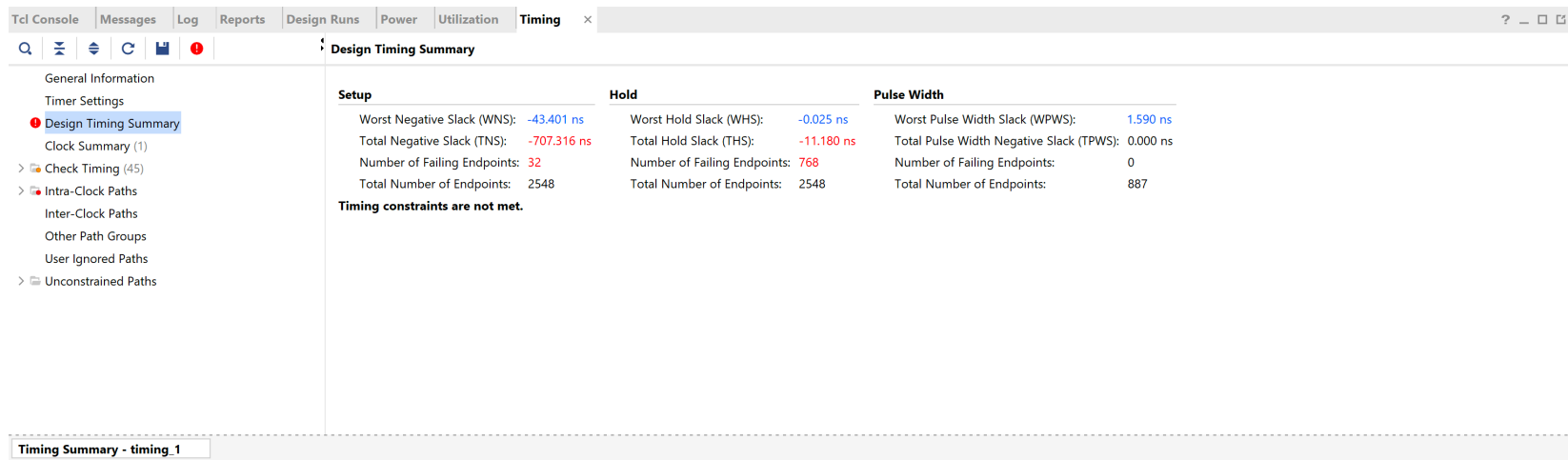
5. The schematic was found with synthesis and is shown below:



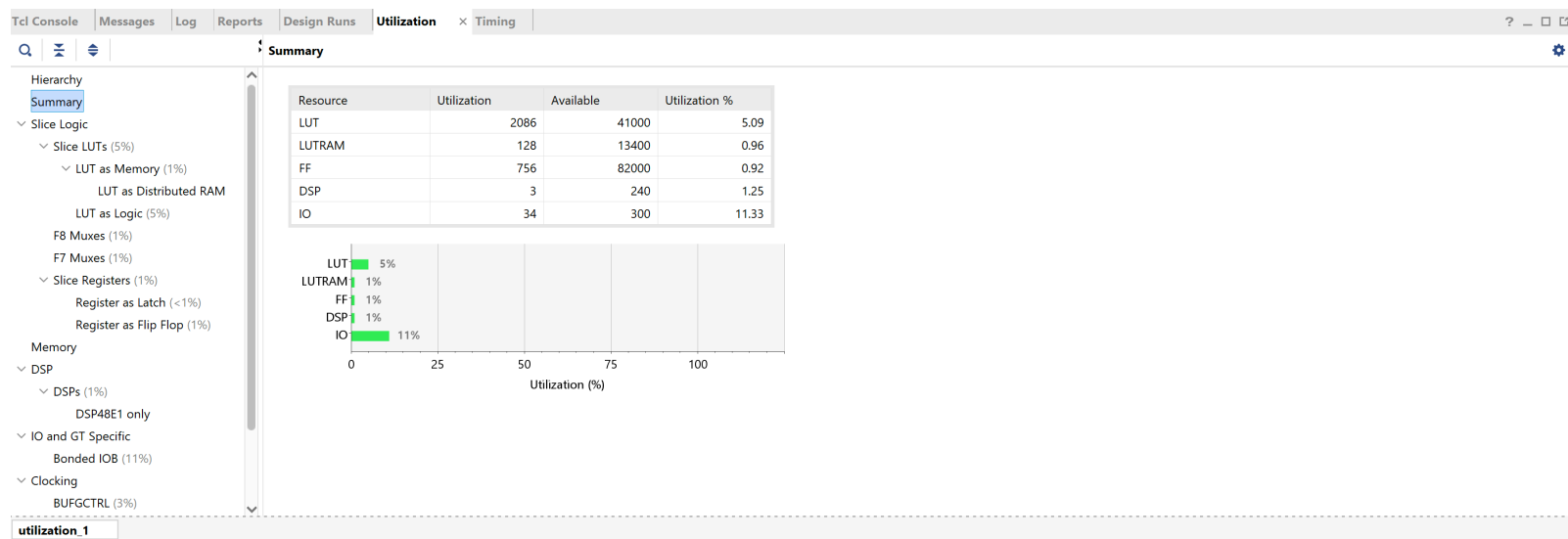
6. In the schematic, FDRE is just a type of D flip-flop that has a clock enable and a synchronous reset. LUT is a lookup table, in our case we are using LUT3, a 3-bit lookup table with dual output. CARRY4 is a fast carry logic unit with look ahead. IBUF is an I/O component that stands for input buffer. OBUF, on the other hand, is an output buffer.

MIPS Pipelined Processor:

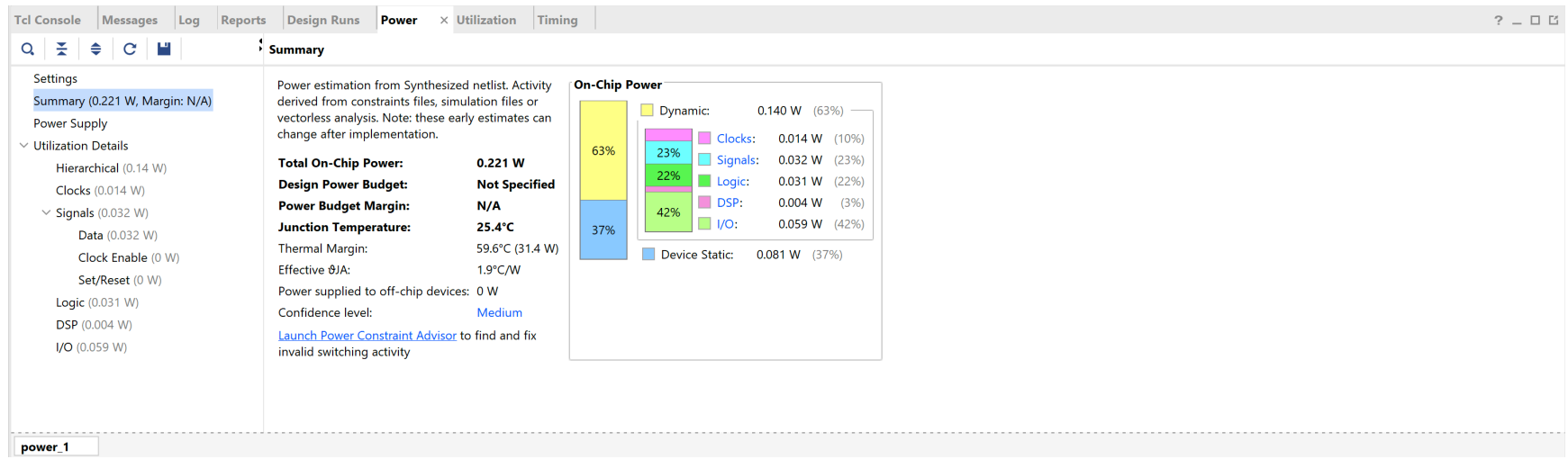
1. A screenshot of the Report Timing Summary is shown below, and the timing was not met because of the 5 ns constraint. Increasing it to 50 ns yields better results.



2. A screenshot of the Report Utilization is shown below:



3. A screenshot of the Report Power is shown below:



4. A screenshot of the schematic is shown on the next page.

Schematic

43 Cells 34 I/O Ports 847 Nets

