Bilkent University

Computer Science

CS224

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Design Report

Lab6

Section: 2

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Part 1)

1)

No.	Cache Size KB	N way cache	Word Size in bits	Block size(no. of words)	No. Of sets	Tag size in bits	Index size(Set No.) in bits	Word block offset size in bits[1]	Byte offset size in bits[2]	Block Replacement Policy Needed(Yes/No)
1	8	1	8	8	2^{10}	19	10	3	0	No
2	8	2	16	8	2^{8}	20	8	3	1	Yes
3	8	4	16	4	2^{8}	21	8	2	1	Yes
4	8	Full	16	4	2^{0}	29	0	2	1	Yes
9	32	1	16	2	2^{13}	17	13	1	1	No
10	32	2	16	2	2^{12}	18	12	1	1	Yes
11	32	4	8	8	2^{10}	19	10	3	0	Yes
12	32	Full	8	8	2^{0}	29	0	3	0	Yes

2)

a)

Instruction	Iteration No.				
	1	2	3	4	5
lw $t1 0xA4($0)	Compulsory	Hit	Hit	Hit	Hit
lw $t2 0xA8($0)	Hit	Hit	Hit	Hit	Hit
lw $t3 0xAC($0)	Hit	Hit	Hit	Hit	Hit

b)

MIPS memory = 4GB = 2^{32} bits

Instruction length = $\text{Log}_2(2^{32})$ = 32 bits

Cache is a direct map since N = 1

Number of blocks = 8/4 = 2

Since it is a direct map and number of blocks are 2, number of sets = 2

Index size = $\text{Log}_2(2^{1})$ = 1 bit

Block size = 4 = 2^2

Block offset = $Log_2(2^2)$ = 2 bits

1 word = 32 bits = 2^2 bytes

Byte offset = $Log_2(2^2)$ = 2 bits

Tag size = 32 – 1 – 2 – 2 = 27 bits

- Set size = 1(valid) + 27(tag) + (4 x 32(word)) = 156 bits
- Cache size = 2 x 156 = 312 bits

c) Hardware for the specified cache

- **1 32 bit 4:1 MUX** to choose words within the block
- **1 Comparator** to check if tag bit is the searched tag bit
- **1 AND Gate** to check valid bit and the result of the comparator

3)

a)

Instruction	Iteration No.				
	1	2	3	4	5
lw $t1 0xA4($0)	Compulsory	Capacity	Capacity	Capacity	Capacity
lw $t2 0xA8($0)	Compulsory	Capacity	Capacity	Capacity	Capacity
lw $t3 0xAC($0)	Capacity	Capacity	Capacity	Capacity	Capacity

b)

MIPS memory = 4GB = 2^{32} bits

Instruction length = $Log_2(2^{32})$ = 32 bits

Cache is 2 way associative, since N = 2

number of sets = 1, since it is a 2 way associative cache and the capacity is 2 words

number of blocks in each way = (2(capacity)/1(block size))/2(N) = 1

Since there is 1 set and 1 block in each way, index size= 0 bit, block offset = 0 bit

1 word = 32 bits = 2^2 bytes

Byte offset = $Log_2(2^2)$ = 2 bits

Tag size = 32 – 0 – 0 – 2 = 30 bits

- Set size = 2(N=2) x (1(valid) + 30(tag) + 32(word)) = 126 bits
- Cache size = set size = 126 bits

c) Hardware for the specified cache

- **1 32 bit 2:1 MUX** to choose the way
- **2 Comparator** to check if tag bit is the searched tag bit
- **2 AND Gate 1 OR Gate** to check valid bit and the result of the comparator in order to determine the hit