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Timeline you have created for the retiring instructions of `perf-test-dep-ldst.asm`.

| CYCLE | INSTRUCTION RETIRED | REASON |
|---|---|---|
| 1 | NOP | |
| 2 | NOP | |
| 3 | NOP | |
| 4 | NOP | |
| 5 | lbi r0, 0 | Will execute, WB, no hazards yet |
| 6 | lbi r5, 43 | Will execute, WB, no hazards yet |
| 7 | lbi r6, 43 | Will execute, WB, no hazards yet |
| 8 | lbi r7, 43 | Will execute, WB, no hazards yet |
| 9 | ld r1, r0, 0 | Will execute, WB, no hazards yet |
| 10 | NOP | RAW on r1 due to st r5, r1, 0 instruction. Stall |
| 11 | NOP | Stall again. RAW on r1 due to st r5, r1, 0 instruction |
| 12 | st r5, r1, 0 | Processed in writeback stage. Done |
| 13 | ld r1, r0, 2 | Processed in writeback stage. Done. No hazard on r1 |
| 14 | NOP | RAW on r1 due to st r6 r1, 1 instruction. Stall |
| 15 | NOP | RAW on r1 due to st r6 r1, 1 instruction. Stall |
| 16 | st r6, r1, 1 | Processed in writeback stage. Done |
| 17 | ld r1, r0, 4 | Processed in writeback stage. Done |
| 18 | NOP | RAW on r1 due to st r7 r1, 1 instruction. Stall |
| 19 | NOP | RAW on r1 due to st r7 r1, 1 instruction. Stall |
| 20 | st r7, r1, 1 | Processed in writeback stage. Done |
| 21 | halt | done |