CSE460 Lab Assignment 2

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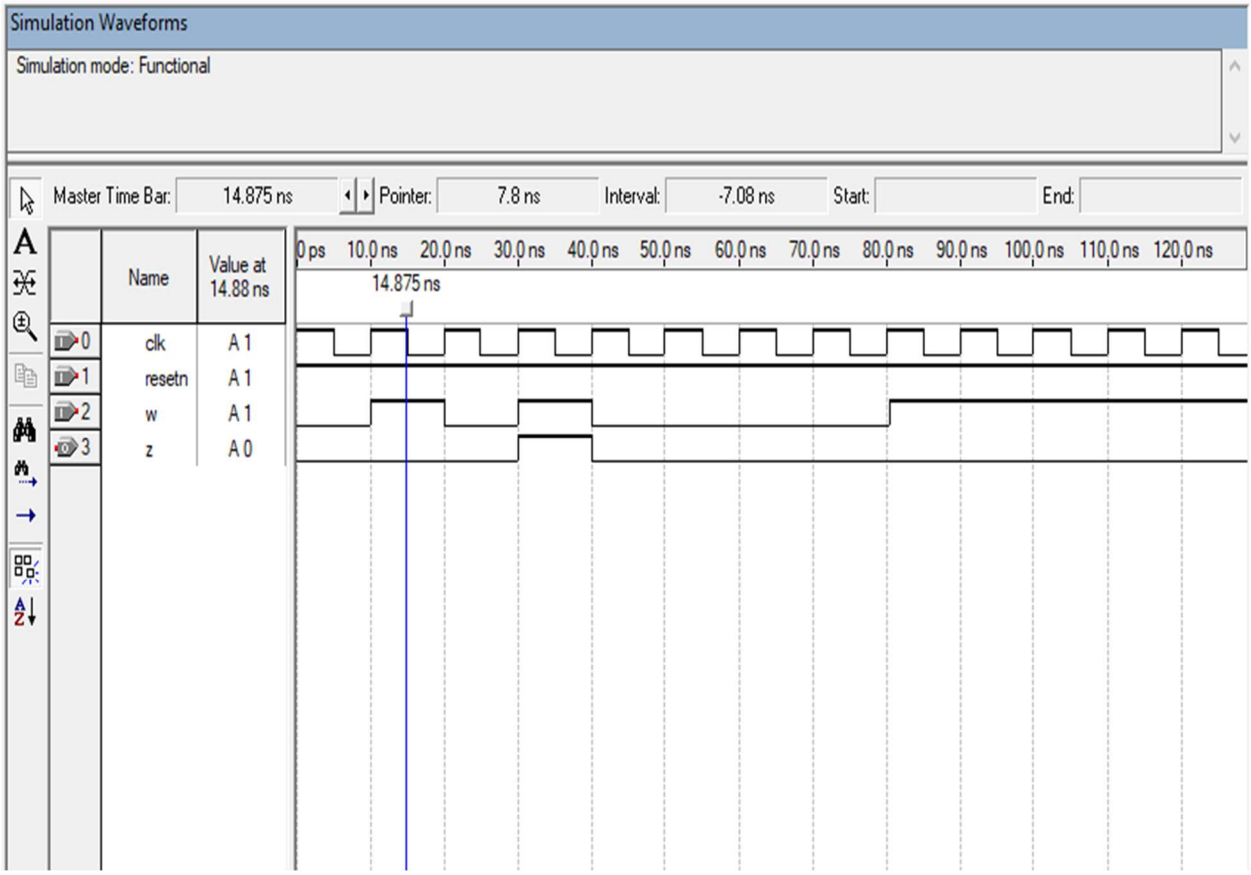
Section 3


```
module Assignment2(w,clk,resetn,z);

input w,clk,resetn;
output z;

reg [1:0] y,Y;

parameter [1:0] A = 2'b00, B = 2'b01, C = 2'b11, D = 2'b10;

always @(w,y)
begin
    case(y)
        A:
        begin
            if(w) Y = B;
            else Y = A;
        end
```

```
        B:
        begin
            if(w) Y = B;
            else Y = C;
        end
        C:
        begin
            if(w) Y = D;
            else Y = A;
        end
        D:
        begin
            if(w) Y = B;
            else Y = C;
        end
    endcase
end

always @(negedge resetn, posedge clk)
    if(resetn == 0) y <= A;
    else y <= Y;

assign z = (y==D);
endmodule
```

Output Waveform:



This finite state machine detects any pattern of 1, 0, 1 in the past 3 clock cycles and shows an output of z=1 only for the following case. The output is always z=0 otherwise.