عمرو مسلم

# Computer Architecture Questions

(جميع الإجابات في آخر الملف)

## Choose:

(أسئلة وضعت في امتحانات سابقة)

1. RAID level __ has the highest disk overhead of all RAID types.
   a) 0 b) 1 c) 3 d) 5
2. Disk arrays may be consolidated or virtualized in a ____.
   a) RAID b) NAS c) SAN d) SAS
3. What is the minimum number of disks required for RAID 1? __ .
   a) 1 b) 2 c) 4 d) 5
4. The _____ was designed to provide a powerful and flexible instruction set within the constraints of a 16-bit minicomputer.
   a) PDP-10 b) PDP-11 c) VAX d) ARM
5. The cache bridges the speed gap between _____ and ____.
   a) RAM and ROM b) Processor and RAM
   c) RAM and Secondary memory d) None of the mentioned
6. The ____ is the part of the computer that sequences and executes instructions.
   a) CPU b) memory c) bus d) input/output devices
7. A high-speed, special-purpose network that integrates different types of data storage devices into a single storage system and connects them to computing resources across an entire organization is called a _____.
   a) network-attached storage b) storage area network
   c) storage as a service d) enterprise data storage solution
8. Load/store architecture: operate instructions operate only on _____.
   a) Memory b) Register c) immediate d) register indirect
9. The use of multiple processors on the same chip is referred to as _____ and provides the potential to increase performance without increasing the clock rate.
   a) multicore b) GPU c) data channels d) MPC
10. A measurement of how many tasks a computer can accomplish in a certain amount of time is called a _____.
    a) throughput b) application analysis c) cycle speed d) real-time system
11. Employed to temporarily hold the right-hand instruction from word in memory.
    a) MBR b) MAR c) IBR d) PC
12. A computer consists of _____, memory cells, and interconnections among these elements.
    a) circuits b) CPU c) gates d) chips
13. Specifies the address in memory of the word to be written from or read into the memory address register. ____.
    a) MBR b) MAR c) IBR d) PC
14. _____ manages the computer's resources and orchestrates the performance of its functional parts.
    a) Data Movement b) Control c) Data processing d) Data storage
15. Updating bank statement show operations involving _____.
    a) Data Movement b) Control c) Data processing d) Data storage
16. Embedded Systems have extreme resource constraints in terms of memory processor size, time, and _____.
    a) Power consumption b) Energy consumption c) speed d) cost
17. Transferring data from one peripheral or communications line to another is _____.
    a) Data Movement b) Control c) Data processing d) Data storage
18. _____, consisting of a number of conducting wires to which all the other components attach.
    a) System bus b) memory c) CPU d) I/O

19. If a system is 64-bit machine, then the length of each word will be _____.
    a) 4 bytes b) 8 bytes c) 16 bytes d) 32 bytes
20. The _____ processors are vulnerable to a new class of Denial of Service (DoS) attacks because the memory system is “unfairly” shared among multiple cores.
    a) single-core b) multi-core c) super scalar d) dual core
21. In most contemporary systems fixed-length sectors are used, with _____ bytes being the nearly universal sector size.
    a) 512 b) 265 c) 128 d) 64
22. _____ is example that apply orthogonal ISA.
    a) VAX b) ARM c) MIPS d) X86
23. SAN component interconnect device such as _____.
    a) Storage arrays b) switches c) management software d) cables
24. A _____ expresses operations in a concise algebraic form using variables.
    a) high-level language b) opcode c) machine language d) register
25. The ARM architecture only _____ instructions access memory locations.
    a) data processing b) status register access c) load and store d) branch
26. NAS component Head unit is _____.
    a) CPU b) NIC c) Protocols d) SCSI
27. _____ multiple layers of memory between the processor and main memory.
    a) Cache Memory b) Controller c) RAM d) CPU
28. _____ contains a word to be stored in memory or sent to the I/O unit.
    a) Memory buffer register b) Memory address register
    c) Instruction register d) Instruction buffer register
29. The decoded instruction is stored in ___.
    a) Register b) PC c) IR d) MDR
30. A higher level only needs to know about the interface to the lower level, not how the lower level is implemented refer to _____.
    a) ISA b) Microarchitecture c) Abstraction d) Purpose of computing
31. Unexpected Slowdowns in Multi-core because _____.
    a) L2 cash b) L3 cash c) Dram controller d) Row buffer
32. The DRAM controller reorders streams requests to the open row over other requests (even older ones) to _____ DRAM throughput.
    a) maximize b) minimize c) equalize d) optimization
33. DRAM bank unavailable while refreshed refer to _____.
    a) Energy consumption b) Performance degradation c) QoS/impact d) DRAM capacity scaling
34. In the case of, Zero-address instruction method the operands are stored in _____.
    a) Registers b) Accumulators c) Push down stack d) Cache
35. The addressing mode, where you directly specify the operand value is _____.
    a) Immediate b) Direct c) Definite d) Relative
36. Cache memory acts between _____ and _____.
    a) CPU and RAM b) RAM and ROM c) CPU and Hard Disk d) None of these
37. The CISC stands for _____.
    a) Computer Instruction Set Compliment b) Complete Instruction Set Compliment
    c) Computer Indexed Set Components d) Complex Instruction Set Computer
38. The computer architecture aimed at reducing the time of execution of instructions is _____.
    a) CISC b) RISC c) ISA d) ANNA

39. Both the CISC and RISC architectures have been developed to reduce the _____.
    a) Cost b) Time delay c) Semantic gap d) All of the mentioned
40. In CISC architecture most of the complex instructions are stored in _____.
    a) Register b) Diodes c) CMOS d) Transistors
41. Which of the architecture is power efficient? _____ .
    a) CISC b) RISC c) ISA d) IANA
42. The throughput of a super scalar processor is _____.
    a) less than 1 b) 1 c) more than 1 d) not known
43. When the processor executes multiple instructions at a time is said to use _____.
    a) Single issue b) Multiplicity c) Visualization d) Multiple issues
44. The _____ plays a very vital role in case of super scalar processors.
    a) Compilers b) Motherboard c) Memory d) Peripherals
45. A stack organized computer has _____ address instruction.
    a) 3 b) 2 c) 1 d) 0
46. The disk drive is connected to the system by using the _____.
    a) PCI bus b) SCSI bus c) HDMI d) ISA
47. ARM stands for _____.
    a) Advanced Rate Machines b) Advanced RISC Machines
    c) Artificial Running Machines d) Aviary Running Machines
48. The main importance of ARM micro-processors is providing operation with _____.
    a) Low cost and low power consumption b) Higher degree of multi-tasking
    c) Lower error or glitches d) Efficient memory management
49. ARM processors where basically designed for _____.
    a) Main frame systems b) Distributed systems
    c) Mobile systems d) Super computers
50. In the ARM, PC is implemented using _____.
    a) Caches b) Heaps c) General purpose register d) Stack
51. The instruction, ADD R1, R2, R3 is decoded as _____.
    a) R1<-[R1]+[R2]+[R3] b) R3<-[R1]+[R2]
    c) R3<-[R1]+[R2]+[R3] d) R1<-[R2]+[R3]
52. _____ converts the programs written in assembly language into machine instructions.
    a) Machine compiler b) Interpreter c) Assembler d) Converter
53. The instructions like MOV or ADD are called as _____.
    a) OP-Code b) Operators c) Commands d) Operand
54. A source program is usually in _____.
    a) Assembly Language b) Machine Level Language c) High-level language d) Natural language
55. What is used to increase the apparent size of physical memory.
    a) Disks b) Hard-disk c) Virtual memory d) Secondary memory
56. During instruction execution, an instruction is read into an _____ in the processor.
    a) Memory buffer register (MBR) b) Address register (AD)
    c) Instruction register (IR) d) Index register (IR)
57. Which computer program is used to convert whole program into the machine language at a time?
    a) Simulator b) Compiler c) Interpreter d) Commander
58. The input devices use _____ to store the data received.
    a) Primary Memory b) Secondary Memory c) Buffer d) External Memory

59. In RISC architecture, memory access is limited to instructions: _____.
    a) MOV and IMP  b) ST and LD  c) PUSH and POP  d) CALL and RET
60. Two processors A and B have clock frequencies of 700 Mhz and 900 Mhz respectively. Suppose A can execute an instruction with an average of 3 steps and B can execute with an average of 5 steps, For the execution of the same instruction which processor is faster?
    a) A  b) B  c) Both take the same time  d) Insufficient information
61. The _____ format is usually used to store data.
    a) BCD  b) Decimal  c) Hexadecimal  d) Octal

## Put ✓ or X:

(أسئلة وضعت في امتحانات سابقة)

1. DRAM controllers commonly used scheduling policy (FR-FCFS). ( )
2. Processor Is the computer component that interprets and executes instructions. ( )
3. Alpha ISA contains a doubly linked list data type. ( )
4. CPU interconnection is a mechanism that provides for communication among CPU, main memory, and I/O. ( )
5. DRAM cells need to be refreshed because reading changes the voltage level of the capacitor in a cell and capacitors leak current. ( )
6. Two-level global branch prediction is microarchitecture. ( )
7. DRAM controllers designed to minimize DRAM data throughput. ( )
8. Deeply Embedded Systems is not programmable once the program logic for the device has been burned into ROM. ( )
9. Program counter is advanced sequentially except for control transfer instructions. ( )
10. ISA change more slowly than microarchitecture. ( )
11. The type of memory assignment used in Intel processors is Little Endian. ( )
12. RAID 5 apply disk striping with dedicated parity driver. ( )
13. RAID level 1 does not over any redundancy at all. ( )
14. During the transfer of data between the processor and memory we use register. ( )
15. Memory and Registers are types of locations can hold source and destination. ( )
16. ARM ISA use Load/Store architecture addressing mode. ( )
17. SAN allowing multiple clients to access files at the same time with very high performance. ( )
18. Alpha ISA SCAN opcode operates on character strings; PUSH\POP. ( )
19. Orthogonal ISA refer all addressing modes can be used with instruction types. ( )
20. Potentially many instructions can execute at the same time in control flow order. ( )
21. In dataflow order each instruction specifies “who” should receive the result. ( )
22. RAID levels 4 through 6 make use of a virtual access technique that allows separate I/O requests to be satisfied in parallel. ( )
23. Programmer cannot access pipeline registers directly. ( )
24. Interfaces between the computer and peripherals is an example of an organizational attribute. ( )
25. Both the structure and functioning of a computer are, in essence, simple. ( )
26. When data are moved over longer distances, to or from a remoted device, the process is known as data transport. ( )
27. The SAN advantage is no distance limitation. ( )
28. RAID provide fault tolerance for shared data and applications. ( )
29. Many transistors can be produces at the same time on a single wafer of silicon. ( )

30. Dedicated processor defined by the processor's ability to execute complex operating systems. ( )
31. Deeply Embedded Systems use a microcontroller rather than a microprocessor. ( )
32. Internet download to disk is example of processing from/to storage. ( )
33. Updating bank statement is example of processing from storage to I/O. ( )
34. Moore observed number of transistors that could be put on a single chip was doubling every year. ( )
35. The cost of computer logic and memory circuitry has fallen at a dramatic rate is the consequences of Moore's law. ( )
36. Can evaluate a modern processor by performing hands-on RTL and C-level implementation. ( )
37. A floating-point unit that uses wide floating-point values for additional accuracy is Microarchitecture. ( )
38. Predicated instruction execution is ISA. ( )
39. A row-conflict memory access takes significantly longer than a row-hit access ( )
40. The ARM processors don't support Byte addressability. ( )
41. The disadvantage of non-uniform decode is restricts instruction format. ( )
42. The RISC processor has a more complicated design than CISC. ( )
43. Immediate addressing moves operand at address in A6 to data registers 5. ( )
44. A modern "super scalar" processor that can execute two or more instruction at once is consider a single core processor. ( )

## Choose: (أسئلة مهمة)

1. Both the structure and functioning of a computer are, in essence, simple. a. True b. False
2. A computer must be able to process, store, move, and control data. a. True b. False
3. Computer technology is changing at a _____ pace.
   A. Slow B. Slow to medium C. Rapid D. Non-existent
4. Computer _____ refers to those attributes that have a direct impact on the logical execution of a program.
   A. Organization B. Specifics C. Design D. Architecture
5. Architectural attributes include _____ .
   A. I/O mechanisms B. Control signals C. Interfaces D. Memory technology used
6. _____ attributes include hardware details transparent to the programmer.
   A. Interface B. Organizational C. Memory D. Architectural
7. It is a(n) _____ design issue whether a computer will have a multiply instruction.
   A. Architectural B. Memory C. Elementary D. Organizational
8. It is a(n) _____ issue whether the multiply instruction will be implemented by a special multiply unit or by a mechanism that makes repeated use of the add unit of the system.
   A. Architectural B. Memory C. Mechanical D. Organizational
9. A _____ system is a set of interrelated subsystems.
   A. Secondary B. Hierarchical C. Complex D. Functional
10. An I/O device is referred to as a _____.
    A. CPU B. Control device C. Peripheral D. Register
11. When data are moved over longer distances, to or from a remote device, the process is known as _____.
    A. Data communications B. Registering C. Structuring D. Data transport
12. The _____ stores data.
    A. System bus B. I/O C. Main memory D. Control unit
13. The _____ moves data between the computer and its external environment.
    A. Data transport B. I/O C. Register D. CPU interconnection

14. A common example of system interconnection is by means of a _____.
    A. Register B. System bus C. Data transport D. Control device
15. A _____ is a mechanism that provides for communication among CPU, main memory, and I/O.
    A. System interconnection B. CPU interconnection C. Peripheral D. Processor
16. _____ provide storage internal to the CPU.
    A. Control units B. ALUs C. Main memory D. Registers
17. The _____ performs the computer's data processing functions.
    A. Register B. CPU interconnection C. ALU D. System bus
18. The smallest entity of memory is called _____
    a) Cell b) Block c) Instance d) Unit
19. When using the Big-Endian assignment to store a number, the sign bit of the number is stored in _____
    a) The higher order byte of the word b) The lower order byte of the word
    c) Can't say d) None of the mentioned
20. The key factor/s in commercial success of a computer are _____.
    a) Performance b) Cost c) Speed d) Both Performance and Cost.
21. _____ have been developed specifically for pipelined systems.
    a) Utility software b) Speed up utilities c) Optimizing compilers d) None of the mentioned
22. The fetch and execution cycles are interleaved with the help of _____
    a) Modification in processor architecture b) Clock c) Special unit d) Control unit
23. The pipelining process is also called as _____
    a) Superscalar operation b) Assembly line operation c) Von Neumann cycle d) None of the mentioned
24. Each stage in pipelining should be completed within _____ cycle.
    a) 1 b) 2 c) 3 d) 4
25. To increase the speed of memory access in pipelining, we make use of _____
    a) Special memory locations b) Special purpose registers c) Cache d) Buffers
26. The Sun micro systems processors usually follow _____ architecture.
    a) CISC b) ISA c) ULTRA SPARC d) RISC
27. Both the CISC and RISC architectures have been developed to reduce the _____
    a) Cost b) Time delay c) Semantic gap d) All of the mentioned
28. Out of the following which is not a CISC machine.
    a) IBM 370/168 b) VAX 11/780 c) Intel 80486 d) Motorola A567
29. Pipe-lining is a unique feature of _____
    a) RISC b) CISC c) ISA d) IANA
30. In CISC architecture most of the complex instructions are stored in _____
    a) Register b) Diodes c) CMOS d) Transistors
31. The collection of the above-mentioned entities where data is stored is called _____
    a) Block b) Set c) Word d) Byte
32. An 24-bit address generates an address space of _____ locations.
    a) 1024 b) 4096 c) 248 d) 16,777,216
33. If a system is 64-bit machine, then the length of each word will be _____
    a) 4 bytes b) 8 bytes c) 16 bytes d) 12 bytes
34. The type of memory assignment used in Intel processors is _____
    a) Little Endian b) Big Endian c) Medium Endian d) None of the mentioned
35. To get the physical address from the logical address generated by CPU we use _____
    a) MAR b) MMU c) Overlays d) TLB

36. _____ method is used to map logical addresses of variable length onto physical memory.
    a) Paging b) Overlays c) Segmentation d) Paging with segmentation
37. During the transfer of data between the processor and memory we use _____
    a) Cache b) TLB c) Buffers d) Registers
38. Physical memory is divided into sets of finite size called as _____
    a) Frames b) Pages c) Blocks d) Vectors
39. The CISC stands for _____
    a) Computer Instruction Set Compliment b) Complete Instruction Set Compliment
    c) Computer Indexed Set Components d) Complex Instruction set computer
40. The computer architecture aimed at reducing the time of execution of instructions is _____
    a) CISC b) RISC c) ISA d) ANNA
41. The RISC processor has a more complicated design than CISC. a) True b) False
42. The iconic feature of the RISC machine among the following is _____
    a) Reduced number of addressing modes b) Increased memory size
    c) Having a branch delay slot d) All of the mentioned
43. Which of the architecture is power efficient?
    a) CISC b) RISC c) ISA d) IANA
44. ARM stands for _____
    a) Advanced Rate Machines b) Advanced RISC Machines
    c) Artificial Running Machines d) Aviary Running Machines
45. The main importance of ARM micro-processors is providing operation with _____
    a) Low cost and low power consumption b) Higher degree of multi-tasking
    c) Lower error or glitches d) Efficient memory management
46. ARM processors where basically designed for _____
    a) Main frame systems b) Distributed systems c) Mobile systems d) Super computers
47. The ARM processors don't support Byte addressability. a) True b) False
48. The address space in ARM is _____ a) 224 b) 264 c) 216 d) 232
49. The address system supported by ARM systems is/are _____
    a) Little Endian b) Big Endian c) X-Little Endian d) Both Little & Big Endian
50. Memory can be accessed in ARM systems by _____ instructions.
    i) Store ii) MOVE iii) Load iv) arithmetic v) logical
    a) i, ii, iii b) i, ii c) i, iv, v d) iii, iv, v
51. RISC stands for _____
    a) Restricted Instruction Sequencing Computer b) Restricted Instruction Sequential Compiler
    c) Reduced Instruction Set Computer d) Reduced Induction Set Computer
52. In the ARM, PC is implemented using _____
    a) Caches b) Heaps c) General purpose register d) Stack
53. The additional duplicate register used in ARM machines are called as _____
    a) Copied-registers b) Banked registers c) EXtra registers d) Extential registers
54. The banked registers are used for _____
    a) Switching between supervisor and interrupt mode b) Extended storing
    c) Same as other general purpose registers d) None of the mentioned
55. Each instruction in ARM machines is encoded into _____ Word.
    a) 2 byte b) 3 byte c) 4 byte d) 8 byte
56. All instructions in ARM are conditionally executed. a) True b) False

57. The addressing mode where the EA of the operand is the contents of Rn is _____
    a) Pre-indexed mode
    b) Pre-indexed with write back mode
    c) Post-indexed mode
    d) None of the mentioned
58. The effective address of the instruction written in Post-indexed mode, MOVE[Rn]+Rm is _____
    a) EA = [Rn]  b) EA = [Rn + Rm]  c) EA = [Rn] + Rm  d) EA = [Rm] + Rn
59. The _____ format is usually used to store data.  a) BCD  b) Decimal  c) Hexadecimal  d) Octal
60. The 8-bit encoding format used to store data in a computer is _____
    a) ASCII  b) EBCDIC  c) ANCI  d) USCII
61. A source program is usually in _____
    a) Assembly language  b) Machine level language  c) High-level language  d) Natural language
62. Which memory device is generally made of semiconductors?
    a) RAM  b) Hard-disk  c) Floppy disk  d) Cd disk
63. The small extremely fast, RAM's are called as _____
    a) Cache  b) Heaps  c) Accumulators  d) Stacks
64. The ALU makes use of _____ to store the intermediate results.
    a) Accumulators  b) Registers  c) Heap  d) Stack
65. The control unit controls other units by generating _____
    a) Control signals  b) Timing signals  c) Transfer signals  d) Command Signals
66. _____ are numbers and encoded characters, generally used as operands.
    a) Input  b) Data  c) Information  d) Stored Values
67. The Input devices can send information to the processor.
    a) When the SIN status flag is set
    b) When the data arrives regardless of the SIN flag
    c) Neither of the cases
    d) Either of the cases
68. _____ bus structure is usually used to connect I/O devices.
    a) Single bus  b) Multiple bus  c) Star bus  d) Rambus
69. The I/O interface required to connect the I/O device to the bus consists of _____
    a) Address decoder and registers
    b) Control circuits
    c) Address decoder, registers and Control circuits
    d) Only Control circuits
70. To reduce the memory access time, we generally make use of _____
    a) Heaps  b) Higher capacity RAM's  c) SDRAM's  d) Cache's
71. _____ is generally used to increase the apparent size of physical memory.
    a) Secondary memory  b) Virtual memory  c) Hard-disk  d) Disks
72. MFC stands for _____
    a) Memory Format Caches
    b) Memory Function Complete
    c) Memory Find Command
    d) Mass Format Command
73. The time delay between two successive initiations of memory operation _____
    a) Memory access time  b) Memory search time  c) Memory cycle time  d) Instruction delay
74. In pipelining the task which requires the least time is performed first.  a) True  b) False
75. If a unit completes its task before the allotted time period, then _____
    a) It'll perform some other task in the remaining time
    b) Its time gets reallocated to a different task
    c) It'll remain idle for the remaining time
    d) None of the mentioned
76. The periods of time when the unit is idle is called as _____
    a) Stalls  b) Bubbles  c) Hazards  d) Both Stalls and Bubbles
77. The contention for the usage of a hardware device is called _____
    a) Structural hazard  b) Stalk  c) Deadlock  d) None of the mentioned

78. The situation wherein the data of operands are not available is called _____
    a) Data hazard  b) Stock  c) Deadlock  d) Structural hazard
79. The decoded instruction is stored in _____
    a) IR  b) PC  c) Registers  d) MDR
80. The instruction -> Add LOCA, R0 does _____
    a. Adds the value of LOCA to R0 and stores in the temp register
    b. Adds the value of R0 to the address of LOCA
    c. Adds the values of both LOCA and R0 and stores it in R0
    d. Adds the value of LOCA with a value in accumulator and stores it in R0
81. Which registers can interact with the secondary storage?  a) MAR  b) PC  c) IR  d) R0
82. During the execution of a program which gets initialized first?
    a) MDR  b) IR  c) PC  d) MAR
83. Which of the register/s of the processor is/are connected to Memory Bus?
    a) PC  b) MAR  c) IR  d) Both PC and MAR
84. ISP stands for _____
    a) Instruction Set Processor  b) Information Standard Processing
    c) Interchange Standard Protocol  d) Interrupt Service Procedure
85. The internal components of the processor are connected by _____
    a) Processor intra-connectivity circuitry  b) Processor bus  c) Memory bus  d) Rambus
86. _____ is used to choose between incrementing the PC or performing ALU operations.
    a) Conditional codes  b) Multiplexer  c) Control unit  d) None of the mentioned
87. The registers, ALU and the interconnection between them are collectively called as _____
    a) process route  b) information trail  c) information path  d) data path
88. _____ is used to store data in registers.
    a) D flip flop  b) JK flip flop  c) RS flip flop  d) None of the mentioned
89. Which of the following is true about Computer Organization?
    i. It deals with high-level design issues.
    ii. It involves Logic (Instruction sets, Addressing modes, Data types, Cache optimization).
    iii. Computer Organization tells us how exactly all the units in the system are arranged and interconnected.
    iv. None of the Above
90. The program written and before being compiled or assembled is called _____.
    A. Start Program  B. Intermediate program  C. Source Program  D. Natural Program
91. The _____ is the computational center of the CPU.
    A. Registers  B. ALU  C. Flip-Flop  D. Multiplexer
92. The input devices use _____ to store the data received
    A. Primary Memory  B. Secondary Memory  C. Buffer  D. External Memory
93. The I/O devices are connected to the CPU via _____.
    A. SDRAM's  B. Control circuits  C. Signals  D. BUS
94. An optimizing Compiler does _____
    A. Better compilation of the given piece of code
    B. Takes advantage of the type of processor and reduces its process time
    C. Does better memory management  D. All of the above
95. Which bus is used to connect the monitor to the CPU?
    A. Single Bus  B. SCSI Bus  C. Multiple Bus  D. Rambus
96. In the ARM Architecture Only _____ Instructions Access Memory Locations.
    a. Branch  b. Status Register Access  c. Data Processing  d. load and store

## Additional Questions:

(أسئلة أقل أهمية)

1. The disk system consists of which of the following?
   i. Disk ii. Disk drive iii. Disk controller
   a) i and ii b) i, ii and iii c) ii and iii d) i
2. The set of corresponding tracks on all surfaces of a stack of disks form a _____
   a) Cluster b) Cylinder c) Group d) Set
3. The data can be accessed from the disk using _____
   a) Surface number b) Sector number c) Track number d) All of the mentioned
4. The read and write operations usually start at _____ of the sector.
   a) Center b) Middle c) From the last used point d) Boundaries
5. To distinguish between two sectors we make use of _____
   a) Inter sector gap b) Splitting bit c) Numbering bit d) None of the mentioned
6. The _____ process divides the disk into sectors and tracks.
   a) Creation b) Initiation c) Formatting d) Modification
7. The access time is composed of _____
   a) Seek time b) Rotational delay c) Latency d) Both Seek time and Rotational delay
8. The disk drive is connected to the system by using the _____
   a) PCI bus b) SCSI bus c) HDMI d) ISA
9. _____ is used to deal with the difference in the transfer rates between the drive and the bus.
   a) Data repeaters b) Enhancers c) Data buffers d) None of the mentioned
10. _____ is used to detect and correct the errors that may occur during data transfers.
    a) ECC b) CRC c) Checksum d) None of the mentioned
11. The throughput of a super scalar processor is _____
    a) less than 1 b) 1 c) More than 1 d) Not Known
12. When the processor executes multiple instructions at a time it is said to use _____
    a) single issue b) Multiplicity c) Visualization d) Multiple issues
13. The _____ plays a very vital role in case of super scalar processors.
    a) Compilers b) Motherboard c) Memory d) Peripherals
14. If an exception is raised and the succeeding instructions are executed completely, then the processor is said to have _
    a) Exception handling b) Imprecise exceptions c) Error correction d) None of the mentioned
15. In super-scalar mode, all the similar instructions are grouped and executed together . a) True b) False
16. In super-scalar processors, _____ mode of execution is used.
    a) In-order b) Post order c) Out of order d) None of the mentioned
17. Since it uses the out of order mode of execution, the results are stored in _____
    a) Buffers b) Special memory locations c) Temporary registers d) TLB
18. The step where in the results stored in the temporary register is transferred into the permanent register is called as _
    a) Final step b) Commitment step c) Last step d) Inception step
19. A special unit used to govern the out of order execution of the instructions is called as _____
    a) Commitment unit b) Temporal unit c) Monitor d) Supervisory unit
20. The commitment unit uses a queue called _____
    a) Record buffer b) Commitment buffer c) Storage buffer d) None of the mentioned
21. _____ converts the programs written in assembly language into machine instructions.
    a) Machine compiler b) Interpreter c) Assembler d) Converter
22. The instructions like MOV or ADD are called as _____
    a) OP-Code b) Operators c) Commands d) None of the mentioned

23. The alternate way of writing the instruction, ADD #5,R1 is _____
    a) ADD [5],[R1]; b) ADDI 5,R1; c) ADDIME 5,[R1]; d) There is no other way
24. Instructions which won't appear in the object program are called as _____
    a) Redundant instructions b) Exceptions c) Comments d) Assembler Directives
25. The assembler directive EQU, when used in the instruction: Sum EQU 200 does _____
    a) Finds the first occurrence of Sum and assigns value 200 to it
    b) Replaces every occurrence of Sum with 200
    c) Re-assigns the address of Sum by adding 200 to its original address
    d) Assigns 200 bytes of memory starting the location of Sum
26. The purpose of the ORIGIN directive is _____
    a) To indicate the starting position in memory, where the program block is to be stored
    b) To indicate the starting of the computation code
    c) To indicate the purpose of the code
    d) To list the locations of all the registers used
27. The directive used to perform initialization before the execution of the code is _____
    a) Reserve b) Store c) Dataword d) EQU
28. _____ directive is used to specify and assign the memory required for the block of code.
    a) Allocate b) Assign c) Set d) Reserve
29. _____ directive specifies the end of execution of a program.
    a) End b) Return c) Stop d) Terminate
30. The last statement of the source program should be _____
    a) Stop b) Return c) OP d) End
31. When dealing with the branching code the assembler _____
    a) Replaces the target with its address
    b) Does not replace until the test condition is satisfied
    c) Finds the Branch offset and replaces the Branch target with it
    d) Replaces the target with the value specified by the DATAWORD directive
32. The assembler stores all the names and their corresponding values in _____
    a) Special purpose Register b) Symbol Table c) Value map Set d) None of the mentioned
33. The assembler stores the object code in _____
    a) Main memory b) Cache c) RAM d) Magnetic disk
34. The utility program used to bring the object code into memory for execution is _____
    a) Loader b) Fetcher c) Extractor d) Linker
35. To overcome the problems of the assembler in dealing with branching code we use _____
    a) Interpreter b) Debugger c) Op-Assembler d) Two-pass assembler

# Answers

## Choose:

1. RAID level __ has the highest disk overhead of all RAID types.
   a) 0 **b) 1** c) 3 d) 5
2. Disk arrays may be consolidated or virtualized in a ____.
   a) RAID b) NAS **c) SAN** d) SAS
3. What is the minimum number of disks required for RAID 1? __ .
   a) 1 **b) 2** c) 4 d) 5
4. The _____ was designed to provide a powerful and flexible instruction set within the constraints of a 16-bit minicomputer.
   a) PDP-10 **b) PDP-11** c) VAX d) ARM
5. The cache bridges the speed gap between _____ and ____.
   a) RAM and ROM **b) Processor and RAM**
   c) RAM and Secondary memory d) None of the mentioned
6. The ____ is the part of the computer that sequences and executes instructions.
   **a) CPU** b) memory c) bus d) input/output devices
7. A high-speed, special-purpose network that integrates different types of data storage devices into a single storage system and connects them to computing resources across an entire organization is called a _____.
   a) network-attached storage **b) storage area network**
   c) storage as a service d) enterprise data storage solution
8. Load/store architecture: operate instructions operate only on _____.
   a) Memory **b) Register** c) immediate d) register indirect
9. The use of multiple processors on the same chip is referred to as _____ and provides the potential to increase performance without increasing the clock rate.
   **a) multicore** b) GPU c) data channels d) MPC
10. A measurement of how many tasks a computer can accomplish in a certain amount of time is called a _____.
    **a) throughput** b) application analysis c) cycle speed d) real-time system
11. Employed to temporarily hold the right-hand instruction from word in memory.
    a) MBR b) MAR **c) IBR** d) PC
12. A computer consists of _____, memory cells, and interconnections among these elements.
    a) circuits b) CPU **c) gates** d) chips
13. Specifies the address in memory of the word to be written from or read into the memory address register. ____.
    a) MBR **b) MAR** c) IBR d) PC
14. _____ manages the computer's resources and orchestrates the performance of its functional parts.
    a) Data Movement **b) Control** c) Data processing d) Data storage
15. Updating bank statement show operations involving _____.
    a) Data Movement b) Control **c) Data processing** d) Data storage
16. Embedded Systems have extreme resource constraints in terms of memory processor size, time, and _____.
    **a) Power consumption** b) Energy consumption c) speed d) cost
17. Transferring data from one peripheral or communications line to another is _____.
    **a) Data Movement** b) Control c) Data processing d) Data storage
18. _____, consisting of a number of conducting wires to which all the other components attach.
    **a) System bus** b) memory c) CPU d) I/O

19. If a system is 64-bit machine, then the length of each word will be _____.
    a) 4 bytes **b) 8 bytes** c) 16 bytes d) 32 bytes
20. The _____ processors are vulnerable to a new class of Denial of Service (DoS) attacks because the memory system is “unfairly” shared among multiple cores.
    a) single-core **b) multi-core** c) super scalar d) dual core
21. In most contemporary systems fixed-length sectors are used, with _____ bytes being the nearly universal sector size.
    **a) 512** b) 265 c) 128 d) 64
22. _____ is example that apply orthogonal ISA.
    **a) VAX** b) ARM c) MIPS d) X86
23. SAN component interconnect device such as _____.
    a) Storage arrays **b) switches** c) management software d) cables
24. A _____ expresses operations in a concise algebraic form using variables.
    **a) high-level language** b) opcode c) machine language d) register
25. The ARM architecture only _____ instructions access memory locations.
    a) data processing b) status register access **c) load and store** d) branch
26. NAS component Head unit is _____.
    **a) CPU** b) NIC c) Protocols d) SCSI
27. _____ multiple layers of memory between the processor and main memory.
    **a) Cache Memory** b) Controller c) RAM d) CPU
28. _____ contains a word to be stored in memory or sent to the I/O unit.
    **a) Memory buffer register** b) Memory address register
    c) Instruction register d) Instruction buffer register
29. The decoded instruction is stored in ___.
    a) Register b) PC **c) IR** d) MDR
30. A higher level only needs to know about the interface to the lower level, not how the lower level is implemented refer to _____.
    a) ISA b) Microarchitecture **c) Abstraction** d) Purpose of computing
31. Unexpected Slowdowns in Multi-core because _____.
    a) L2 cash b) L3 cash **c) Dram controller** d) Row buffer
32. The DRAM controller reorders streams requests to the open row over other requests (even older ones) to _____ DRAM throughput.
    **a) maximize** b) minimize c) equalize d) optimization
33. DRAM bank unavailable while refreshed refer to _____.
    a) Energy consumption **b) Performance degradation** c) QoS/impact d) DRAM capacity scaling
34. In the case of, Zero-address instruction method the operands are stored in _____.
    a) Registers b) Accumulators **c) Push down stack** d) Cache
35. The addressing mode, where you directly specify the operand value is _____.
    **a) Immediate** b) Direct c) Definite d) Relative
36. Cache memory acts between _____ and _____.
    **a) CPU and RAM** b) RAM and ROM c) CPU and Hard Disk d) None of these
37. The CISC stands for _____.
    a) Computer Instruction Set Compliment b) Complete Instruction Set Compliment
    c) Computer Indexed Set Components **d) Complex Instruction Set Computer**
38. The computer architecture aimed at reducing the time of execution of instructions is _____.
    a) CISC **b) RISC** c) ISA d) ANNA

39. Both the CISC and RISC architectures have been developed to reduce the _____.
    a) Cost b) Time delay **c) Semantic gap** d) All of the mentioned
40. In CISC architecture most of the complex instructions are stored in _____.
    a) Register b) Diodes c) CMOS **d) Transistors**
41. Which of the architecture is power efficient? _____ .
    a) CISC **b) RISC** c) ISA d) IANA
42. The throughput of a super scalar processor is _____.
    a) less than 1 b) 1 **c) more than 1** d) not known
43. When the processor executes multiple instructions at a time is said to use _____.
    a) Single issue b) Multiplicity c) Visualization **d) Multiple issues**
44. The _____ plays a very vital role in case of super scalar processors.
    **a) Compilers** b) Motherboard c) Memory d) Peripherals
45. A stack organized computer has _____ address instruction.
    a) 3 b) 2 c) 1 **d) 0**
46. The disk drive is connected to the system by using the _____.
    a) PCI bus **b) SCSI bus** c) HDMI d) ISA
47. ARM stands for **_____**.
    a) Advanced Rate Machines **b) Advanced RISC Machines**
    c) Artificial Running Machines d) Aviary Running Machines
48. The main importance of ARM micro-processors is providing operation with _____**.**
    **a) Low cost and low power consumption** b) Higher degree of multi-tasking
    c) Lower error or glitches d) Efficient memory management
49. ARM processors where basically designed for _____.
    a) Main frame systems b) Distributed systems
    **c) Mobile systems** d) Super computers
50. In the ARM, PC is implemented using _____.
    a) Caches b) Heaps **c) General purpose register** d) Stack
51. The instruction, ADD R1, R2, R3 is decoded as _____.
    a) R1<-[R1]+[R2]+[R3] b) R3<-[R1]+[R2]
    c) R3<-[R1]+[R2]+[R3] **d) R1<-[R2]+[R3]**
52. _____ converts the programs written in assembly language into machine instructions.
    a) Machine compiler b) Interpreter **c) Assembler** d) Converter
53. The instructions like MOV or ADD are called as _____.
    **a) OP-Code** b) Operators c) Commands d) Operand
54. A source program is usually in _____.
    a) Assembly Language b) Machine Level Language **c) High-level language** d) Natural language
55. What is used to increase the apparent size of physical memory.
    a) Disks b) Hard-disk **c) Virtual memory** d) Secondary memory
56. During instruction execution, an instruction is read into an _____ in the processor.
    a) Memory buffer register (MBR) b) Address register (AD)
    **c) Instruction register (IR)** d) Index register (IR)
57. Which computer program is used to convert whole program into the machine language at a time?
    a) Simulator **b) Compiler** c) Interpreter d) Commander
58. The input devices use _____ to store the data received.
    a) Primary Memory b) Secondary Memory **c) Buffer** d) External Memory

59. In RISC architecture, memory access is limited to instructions: _____.
    a) MOV and IMP **b) ST and LD** c) PUSH and POP d) CALL and RET
60. Two processors A and B have clock frequencies of 700 Mhz and 900 Mhz respectively. Suppose A can execute an instruction with an average of 3 steps and B can execute with an average of 5 steps, For the execution of the same instruction which processor is faster?
    **a) A** b) B c) Both take the same time d) Insufficient information
61. The _____ format is usually used to store data.
    **a) BCD** b) Decimal c) Hexadecimal d) Octal

## Put ✓ or X:

1. DRAM controllers commonly used scheduling policy (FR-FCFS). (✓)
2. Processor Is the computer component that interprets and executes instructions. (✓)
3. Alpha ISA contains a doubly linked list data type. (X)
4. CPU interconnection is a mechanism that provides for communication among CPU, main memory, and I/O. (X)
5. DRAM cells need to be refreshed because reading changes the voltage level of the capacitor in a cell and capacitors leak current. (✓)
6. Two-level global branch prediction is microarchitecture. (✓)
7. DRAM controllers designed to minimize DRAM data throughput. (X)
8. Deeply Embedded Systems is not programmable once the program logic for the device has been burned into ROM. (✓)
9. Program counter is advanced sequentially except for control transfer instructions. (✓)
10. ISA change more slowly than microarchitecture. (✓)
11. The type of memory assignment used in Intel processors is Little Endian. (✓)
12. RAID 5 apply disk striping with dedicated parity driver. (X)
13. RAID level 1 does not over any redundancy at all. (X)
14. During the transfer of data between the processor and memory we use register. (✓)
15. Memory and Registers are types of locations can hold source and destination operands. (✓)
16. ARM ISA use Load/Store architecture addressing mode. (✓)
17. SAN allowing multiple clients to access files at the same time with very high performance. (✓)
18. Alpha ISA SCAN opcode operates on character strings; PUSH\POP. (X)
19. Orthogonal ISA refer all addressing modes can be used with instruction types. (✓)
20. Potentially many instructions can execute at the same time in control flow order. (X)
21. In dataflow order each instruction specifies “who” should receive the result. (✓)
22. RAID levels 4 through 6 make use of a virtual access technique that allows separate I/O requests to be satisfied in parallel. (✓)
23. Programmer cannot access pipeline registers directly. (✓)
24. Interfaces between the computer and peripherals is an example of an organizational attribute. (✓)
25. Both the structure and functioning of a computer are, in essence, simple. (✓)
26. When data are moved over longer distances, to or from a remoted device, the process is known as data transport. (X)
27. The SAN advantage is no distance limitation. (✓)
28. RAID provide fault tolerance for shared data and applications. (✓)
29. Many transistors can be produces at the same time on a single wafer of silicon. (✓)

30. Dedicated processor defined by the processor's ability to execute complex operating systems. (X)
31. Deeply Embedded Systems use a microcontroller rather than a microprocessor. (✓)
32. Internet download to disk is example of processing from/to storage. (X)
33. Updating bank statement is example of processing from storage to I/O. (X)
34. Moore observed number of transistors that could be put on a single chip was doubling every year. (✓)
35. The cost of computer logic and memory circuitry has fallen at a dramatic rate is the consequences of Moore's law. (✓)
36. Can evaluate a modern processor by performing hands-on RTL and C-level implementation. (✓)
37. A floating-point unit that uses wide floating-point values for additional accuracy is Microarchitecture. (✓)
38. Predicated instruction execution is ISA. (✓)
39. A row-conflict memory access takes significantly longer than a row-hit access. (✓)
40. The ARM processors don't support Byte addressability. (X)
41. The disadvantage of non-uniform decode is restricts instruction format. (X)
42. The RISC processor has a more complicated design than CISC. **(**X**)**
43. Immediate addressing moves operand at address in A6 to data registers 5. (X)
44. A modern "super scalar" processor that can execute two or more instruction at once is consider a single core processor. (✓)

## Choose:

1. Both the structure and functioning of a computer are, in essence, simple. **a. True** b. False
2. A computer must be able to process, store, move, and control data. **a. True** b. False
3. Computer technology is changing at a _____ pace.
   A. Slow B. Slow to medium **C. Rapid** D. Non-existent
4. Computer _____ refers to those attributes that have a direct impact on the logical execution of a program.
   A. Organization B. Specifics C. Design **D. Architecture**
5. Architectural attributes include _____ .
   **A. I/O mechanisms** B. Control signals C. Interfaces D. Memory technology used
6. _____ attributes include hardware details transparent to the programmer.
   A. Interface **B. Organizational** C. Memory D. Architectural
7. It is a(n) _____ design issue whether a computer will have a multiply instruction.
   **A. Architectural** B. Memory C. Elementary D. Organizational
8. It is a(n) _____ issue whether the multiply instruction will be implemented by a special multiply unit or by a mechanism that makes repeated use of the add unit of the system.
   A. Architectural B. Memory C. Mechanical **D. Organizational**
9. A _____ system is a set of interrelated subsystems.
   A. Secondary **B. Hierarchical** C. Complex D. Functional
10. An I/O device is referred to as a _____.
    A. CPU B. Control device **C. Peripheral** D. Register
11. When data are moved over longer distances, to or from a remote device, the process is known as _____.
    **A. Data communications** B. Registering C. Structuring D. Data transport
12. The _____ stores data.
    A. System bus B. I/O **C. Main memory** D. Control unit
13. The _____ moves data between the computer and its external environment.
    A. Data transport **B. I/O** C. Register D. CPU interconnection

14. A common example of system interconnection is by means of a _____.
    A. Register **B. System bus** C. Data transport D. Control device
15. A _____ is a mechanism that provides for communication among CPU, main memory, and I/O.
    **A. System interconnection** B. CPU interconnection C. Peripheral D. Processor
16. _____ provide storage internal to the CPU.
    A. Control units B. ALUs C. Main memory **D. Registers**
17. The _____ performs the computer's data processing functions.
    A. Register B. CPU interconnection **C. ALU** D. System bus
18. The smallest entity of memory is called _____
    a) **Cell** b) Block c) Instance d) Unit
19. When using the Big-Endian assignment to store a number, the sign bit of the number is stored in _____
    **a) The higher order byte of the word** b) The lower order byte of the word
    c) Can't say d) None of the mentioned
20. The key factor/s in commercial success of a computer are _____.
    a) Performance b) Cost c) Speed **d) Both Performance and Cost.**
21. _____ have been developed specifically for pipelined systems.
    a) Utility software b) Speed up utilities **c) Optimizing compilers** d) None of the mentioned
22. The fetch and execution cycles are interleaved with the help of _____
    a) Modification in processor architecture **b) Clock** c) Special unit d) Control unit
23. The pipelining process is also called as _____
    a) Superscalar operation **b) Assembly line operation** c) Von Neumann cycle d) None of the mentioned
24. Each stage in pipelining should be completed within _____ cycle.
    **a) 1** b) 2 c) 3 d) 4
25. To increase the speed of memory access in pipelining, we make use of _____
    a) Special memory locations b) Special purpose registers **c) Cache** d) Buffers
26. The Sun micro systems processors usually follow _____ architecture.
    a) CISC b) ISA c) ULTRA SPARC **d) RISC**
27. Both the CISC and RISC architectures have been developed to reduce the _____
    a) Cost b) Time delay **c) Semantic gap** d) All of the mentioned
28. Out of the following which is not a CISC machine.
    a) IBM 370/168 b) VAX 11/780 c) Intel 80486 **d) Motorola A567**
29. Pipe-lining is a unique feature of _____
    **a) RISC** b) CISC c) ISA d) IANA
30. In CISC architecture most of the complex instructions are stored in _____
    a) Register b) Diodes c) CMOS **d) Transistors**
31. The collection of the above-mentioned entities where data is stored is called _____
    **a) Block** b) Set c) Word d) Byte
32. An 24-bit address generates an address space of _____ locations.
    a) 1024 b) 4096 c) 248 **d) 16,777,216**
33. If a system is 64-bit machine, then the length of each word will be _____
    a) 4 bytes **b) 8 bytes** c) 16 bytes d) 12 bytes
34. The type of memory assignment used in Intel processors is _____
    a) **Little Endian** b) Big Endian c) Medium Endian d) None of the mentioned
35. To get the physical address from the logical address generated by CPU we use _____
    a) MAR **b) MMU** c) Overlays d) TLB

36. _____ method is used to map logical addresses of variable length onto physical memory.
    a) Paging b) Overlays **c) Segmentation** d) Paging with segmentation
37. During the transfer of data between the processor and memory we use _____
    a) Cache b) TLB c) Buffers **d) Registers**
38. Physical memory is divided into sets of finite size called as _____
    **a) Frames** b) Pages c) Blocks d) Vectors
39. The CISC stands for _____
    a) Computer Instruction Set Compliment b) Complete Instruction Set Compliment
    c) Computer Indexed Set Components **d) Complex Instruction set computer**
40. The computer architecture aimed at reducing the time of execution of instructions is _____
    a) CISC **b) RISC** c) ISA d) ANNA
41. The RISC processor has a more complicated design than CISC. a) True **b) False**
42. The iconic feature of the RISC machine among the following is _____
    a) Reduced number of addressing modes b) Increased memory size
    **c) Having a branch delay slot** d) All of the mentioned
43. Which of the architecture is power efficient?
    a) CISC **b) RISC** c) ISA d) IANA
44. ARM stands for _____
    a) Advanced Rate Machines **b) Advanced RISC Machines**
    c) Artificial Running Machines d) Aviary Running Machines
45. The main importance of ARM micro-processors is providing operation with _____
    **a) Low cost and low power consumption** b) Higher degree of multi-tasking
    c) Lower error or glitches d) Efficient memory management
46. ARM processors where basically designed for _____
    a) Main frame systems b) Distributed systems **c) Mobile systems** d) Super computers
47. The ARM processors don't support Byte addressability. a) True **b) False**
48. The address space in ARM is _____ a) 224 b) 264 c) 216 **d) 232**
49. The address system supported by ARM systems is/are _____
    a) Little Endian b) Big Endian c) X-Little Endian **d) Both Little & Big Endian**
50. Memory can be accessed in ARM systems by _____ instructions.
    i) Store ii) MOVE iii) Load iv) arithmetic v) logical
    a) i, ii, iii **b) i, ii** c) i, iv, v d) iii, iv, v
51. RISC stands for _____
    a) Restricted Instruction Sequencing Computer b) Restricted Instruction Sequential Compiler
    **c) Reduced Instruction Set Computer** d) Reduced Induction Set Computer
52. In the ARM, PC is implemented using _____
    a) Caches b) Heaps **c) General purpose register** d) Stack
53. The additional duplicate register used in ARM machines are called as _____
    a) Copied-registers **b) Banked registers** c) EXtra registers d) Extential registers
54. The banked registers are used for _____
    **a) Switching between supervisor and interrupt mode** b) Extended storing
    c) Same as other general purpose registers d) None of the mentioned
55. Each instruction in ARM machines is encoded into _____ Word.
    a) 2 byte b) 3 byte **c) 4 byte** d) 8 byte
56. All instructions in ARM are conditionally executed. **a) True** b) False

57. The addressing mode where the EA of the operand is the contents of Rn is _____
    a) Pre-indexed mode  b) Pre-indexed with write back mode
    **c) Post-indexed mode**  d) None of the mentioned
58. The effective address of the instruction written in Post-indexed mode, MOVE[Rn]+Rm is _____
    **a) EA = [Rn]**  b) EA = [Rn + Rm]  c) EA = [Rn] + Rm  d) EA = [Rm] + Rn
59. The _____ format is usually used to store data.  **a) BCD**  b) Decimal  c) Hexadecimal  d) Octal
60. The 8-bit encoding format used to store data in a computer is _____
    a) ASCII  **b) EBCDIC**  c) ANCI  d) USCII
61. A source program is usually in _____
    a) Assembly language  b) Machine level language  **c) High-level language**  d) Natural language
62. Which memory device is generally made of semiconductors?
    **a) RAM**  b) Hard-disk  c) Floppy disk  d) Cd disk
63. The small extremely fast, RAM's are called as _____
    **a) Cache**  b) Heaps  c) Accumulators  d) Stacks
64. The ALU makes use of _____ to store the intermediate results.
    **a) Accumulators**  b) Registers  c) Heap  d) Stack
65. The control unit controls other units by generating _____
    a) Control signals  **b) Timing signals**  c) Transfer signals  d) Command Signals
66. _____ are numbers and encoded characters, generally used as operands.
    a) Input  **b) Data**  c) Information  d) Stored Values
67. The Input devices can send information to the processor.
    **a) When the SIN status flag is set**  b) When the data arrives regardless of the SIN flag
    c) Neither of the cases  d) Either of the cases
68. _____ bus structure is usually used to connect I/O devices.
    **a) Single bus**  b) Multiple bus  c) Star bus  d) Rambus
69. The I/O interface required to connect the I/O device to the bus consists of _____
    a) Address decoder and registers  b) Control circuits
    **c) Address decoder, registers and Control circuits**  d) Only Control circuits
70. To reduce the memory access time, we generally make use of _____
    a) Heaps  b) Higher capacity RAM's  c) SDRAM's  **d) Cache's**
71. _____ is generally used to increase the apparent size of physical memory.
    a) Secondary memory  **b) Virtual memory**  c) Hard-disk  d) Disks
72. MFC stands for _____
    a) Memory Format Caches  **b) Memory Function Complete**
    c) Memory Find Command  d) Mass Format Command
73. The time delay between two successive initiations of memory operation _____
    a) Memory access time  b) Memory search time  **c) Memory cycle time**  d) Instruction delay
74. In pipelining the task which requires the least time is performed first.  a) True  **b) False**
75. If a unit completes its task before the allotted time period, then _____
    a) It'll perform some other task in the remaining time  b) Its time gets reallocated to a different task
    **c) It'll remain idle for the remaining time**  d) None of the mentioned
76. The periods of time when the unit is idle is called as _____
    a) Stalls  b) Bubbles  c) Hazards  **d) Both Stalls and Bubbles**
77. The contention for the usage of a hardware device is called _____
    **a) Structural hazard**  b) Stalk  c) Deadlock  d) None of the mentioned

78. The situation wherein the data of operands are not available is called _____
**a) Data hazard** b) Stock c) Deadlock d) Structural hazard
79. The decoded instruction is stored in _____
**a) IR** b) PC c) Registers d) MDR
80. The instruction -> Add LOCA, R0 does _____
a. Adds the value of LOCA to R0 and stores in the temp register
b. Adds the value of R0 to the address of LOCA
**c. Adds the values of both LOCA and R0 and stores it in R0**
d. Adds the value of LOCA with a value in accumulator and stores it in R0
81. Which registers can interact with the secondary storage?
**a) MAR** b) PC c) IR d) R0
82. During the execution of a program which gets initialized first?
a) MDR b) IR **c) PC** d) MAR
83. Which of the register/s of the processor is/are connected to Memory Bus?
a) PC **b) MAR** c) IR d) Both PC and MAR
84. ISP stands for _____
**a) Instruction Set Processor** b) Information Standard Processing
c) Interchange Standard Protocol d) Interrupt Service Procedure
85. The internal components of the processor are connected by _____
a) Processor intra-connectivity circuitry **b) Processor bus** c) Memory bus d) Rambus
86. _____ is used to choose between incrementing the PC or performing ALU operations.
a) Conditional codes **b) Multiplexer** c) Control unit d) None of the mentioned
87. The registers, ALU and the interconnection between them are collectively called as _____
a) process route b) information trail c) information path **d) data path**
88. _____ is used to store data in registers.
**a) D flip flop** b) JK flip flop c) RS flip flop d) None of the mentioned
89. Which of the following is true about Computer Organization?
i. It deals with high-level design issues.
ii. It involves Logic (Instruction sets, Addressing modes, Data types, Cache optimization).
**iii. Computer Organization tells us how exactly all the units in the system are arranged and interconnected.**
iv. None of the Above
90. The program written and before being compiled or assembled is called _____.
A. Start Program B. Intermediate program **C. Source Program** D. Natural Program
91. The _____ is the computational center of the CPU.
A. Registers **B. ALU** C. Flip-Flop D. Multiplexer
92. The input devices use _____ to store the data received
A. Primary Memory B. Secondary Memory **C. Buffer** D. External Memory
93. The I/O devices are connected to the CPU via _____.
A. SDRAM's B. Control circuits C. Signals **D. BUS**
94. An optimizing Compiler does _____
A. Better compilation of the given piece of code
**B. Takes advantage of the type of processor and reduces its process time**
C. Does better memory management D. All of the above
95. Which bus is used to connect the monitor to the CPU?
A. Single Bus **B. SCSI Bus** C. Multiple Bus D. Rambus
96. In the ARM Architecture Only _____ Instructions Access Memory Locations.
a. Branch b. Status Register Access c. Data Processing **d. load and store**

# Additional Questions:

1. The disk system consists of which of the following?
   i. Disk ii. Disk drive iii. Disk controller
   a) i and ii **b) i, ii and iii** c) ii and iii d) i
2. The set of corresponding tracks on all surfaces of a stack of disks form a _____
   a) Cluster **b) Cylinder** c) Group d) Set
3. The data can be accessed from the disk using _____
   a) Surface number b) Sector number c) Track number **d) All of the mentioned**
4. The read and write operations usually start at _____ of the sector.
   a) Center b) Middle c) From the last used point **d) Boundaries**
5. To distinguish between two sectors we make use of _____
   **a) Inter sector gap** b) Splitting bit c) Numbering bit d) None of the mentioned
6. The _____ process divides the disk into sectors and tracks.
   a) Creation b) Initiation **c) Formatting** d) Modification
7. The access time is composed of _____
   a) Seek time b) Rotational delay c) Latency **d) Both Seek time and Rotational delay**
8. **The disk drive is connected to the system by using the _____**
   a) PCI bus **b) SCSI bus** c) HDMI d) ISA
9. _____ is used to deal with the difference in the transfer rates between the drive and the bus.
   a) Data repeaters b) Enhancers **c) Data buffers** d) None of the mentioned
10. _____ is used to detect and correct the errors that may occur during data transfers.
    **a) ECC** b) CRC c) Checksum d) None of the mentioned
11. **The throughput of a super scalar processor is _____**
    a) less than 1 b) 1 **c) More than 1** d) Not Known
12. **When the processor executes multiple instructions at a time it is said to use _____**
    a) single issue b) Multiplicity c) Visualization **d) Multiple issues**
13. The _____ plays a very vital role in case of super scalar processors.
    **a) Compilers** b) Motherboard c) Memory d) Peripherals
14. If an exception is raised and the succeeding instructions are executed completely, then the processor is said to have _
    a) Exception handling **b) Imprecise exceptions** c) Error correction d) None of the mentioned
15. In super-scalar mode, all the similar instructions are grouped and executed together. **a) True** b) False
16. In super-scalar processors, _____ mode of execution is used.
    a) In-order b) Post order **c) Out of order** d) None of the mentioned
17. Since it uses the out of order mode of execution, the results are stored in _____
    a) Buffers b) Special memory locations **c) Temporary registers** d) TLB
18. The step where in the results stored in the temporary register is transferred into the permanent register is called as _
    a) Final step **b) Commitment step** c) Last step d) Inception step
19. A special unit used to govern the out of order execution of the instructions is called as _____
    **a) Commitment unit** b) Temporal unit c) Monitor d) Supervisory unit
20. The commitment unit uses a queue called _____
    **a) Record buffer** b) Commitment buffer c) Storage buffer d) None of the mentioned
21. _____ converts the programs written in assembly language into machine instructions.
    a) Machine compiler b) Interpreter **c) Assembler** d) Converter
22. The instructions like MOV or ADD are called as _____
    **a) OP-Code** b) Operators c) Commands d) None of the mentioned

23. The alternate way of writing the instruction, ADD #5,R1 is _____
    a) ADD [5],[R1]; **b) ADDI 5,R1;** c) ADDIME 5,[R1]; d) There is no other way
24. Instructions which won't appear in the object program are called as _____
    a) Redundant instructions b) Exceptions c) Comments **d) Assembler Directives**
25. The assembler directive EQU, when used in the instruction: Sum EQU 200 does _____
    a) Finds the first occurrence of Sum and assigns value 200 to it
    **b) Replaces every occurrence of Sum with 200**
    c) Re-assigns the address of Sum by adding 200 to its original address
    d) Assigns 200 bytes of memory starting the location of Sum
26. The purpose of the ORIGIN directive is _____
    **a) To indicate the starting position in memory, where the program block is to be stored**
    b) To indicate the starting of the computation code
    c) To indicate the purpose of the code
    d) To list the locations of all the registers used
27. The directive used to perform initialization before the execution of the code is _____
    a) Reserve b) Store **c) Dataword** d) EQU
28. _____ directive is used to specify and assign the memory required for the block of code.
    a) Allocate b) Assign c) Set **d) Reserve**
29. _____ directive specifies the end of execution of a program.
    a) End **b) Return** c) Stop d) Terminate
30. The last statement of the source program should be _____
    a) Stop b) Return c) OP **d) End**
31. When dealing with the branching code the assembler _____
    a) Replaces the target with its address
    b) Does not replace until the test condition is satisfied
    c) Finds the Branch offset and replaces the Branch target with it
    d) Replaces the target with the value specified by the DATAWORD directive
32. The assembler stores all the names and their corresponding values in _____
    a) Special purpose Register **b) Symbol Table**
    c) Value map Set d) None of the mentioned
33. The assembler stores the object code in _____
    a) Main memory b) Cache c) RAM **d) Magnetic disk**
34. The utility program used to bring the object code into memory for execution is _____
    **a) Loader** b) Fetcher c) Extractor d) Linker
35. To overcome the problems of the assembler in dealing with branching code we use _____
    a) Interpreter b) Debugger c) Op-Assembler **d) Two-pass assembler**