Computer Architecture Questions

عمرو مسلم (جميع الإجابات في آخر الملف)

Ch	noose:			(أسئلة وضعت في امتحانات سابقة)
1.	RAID level has the high	hest disk overhead of all RAID typ	oes.	
	a) 0	b) 1	c) 3	d) 5
2.	Disk arrays may be conso	lidated or virtualized in a		
	a) RAID	b) NAS	c) SAN	d) SAS
3.	What is the minimum nu	mber of disks required for RAID 1	ι? <u> </u>	
	a) 1	b) 2	c) 4	d) 5
4.	The was designed	ed to provide a powerful and flex	ible instruction set withi	n the constraints of a 16-bit
	minicomputer.			
	a) PDP-10	b) PDP-11	c) VAX	d) ARM
5.	The cache bridges the spe	eed gap between and <code>.</code>	·	
	a) RAM and ROM		b) Processor and RAN	Л
	c) RAM and Secondary m	emory	d) None of the menti	oned
6.	The is the part of th	e computer that sequences and	executes instructions.	
	a) CPU	b) memory	c) bus	d) input/output devices
7.	A high-speed, special-pur	pose network that integrates dif	ferent types of data stor	age devices into a single storage
	system and connects the	m to computing resources across	an entire organization is	s called a
	a) network-attached stora	age	b) storage area netwo	ork
	c) storage as a service		d) enterprise data sto	orage solution
8.	Load/store architecture:	operate instructions operate only	y on	
	a) Memory	b) Register	c) immediate	d) register indirect
9.	The use of multiple proce	essors on the same chip is referre	ed to as and pro	vides the potential to increase
	performance without inc	reasing the clock rate.		
	a) multicore	b) GPU	c) data channels	d) MPC
10.	A measurement of how r	nany tasks a computer can accon	nplish in a certain amour	nt of time is called a
	a) throughput	b) application analysis	c) cycle speed	d) real-time system
11.	Employed to temporarily	hold the right-hand instruction f	rom word in memory.	
	a) MBR	b) MAR	c) IBR	d) PC
12.	A computer consists of _	, memory cells, and interco	onnections among these	elements.
	a) circuits	b) CPU	c) gates	d) chips
13.	Specifies the address in n	nemory of the word to be writter	n from or read into the n	nemory address register
	a) MBR	b) MAR	c) IBR	d) PC
14.	manages the co	mputer's resources and orchestr	ates the performance of	its functional parts.
	a) Data Movement	b) Control	c) Data processing	d) Data storage
15.	Updating bank statement	t show operations involving	·	
	a) Data Movement	b) Control	c) Data processing	d) Data storage
16.	Embedded Systems have	extreme resource constraints in	terms of memory proces	ssor size, time, and
	a) Power consumption	b) Energy consumption	c) speed	d) cost
17.	Transferring data from or	ne peripheral or communications	line to another is	·
	a) Data Movement	b) Control	c) Data processing	d) Data storage
18.	, consisting	g of a number of conducting wire	es to which all the other	components attach.
	a) System hus	h) memory	c) CPI I	4) I\O

19.	If a system is 64-bit machin	ne, then the length o	of each word v	vill be .		,	
	a) 4 bytes			c) 16 bytes		d) 32 bytes	
20.	The processors ar	•		•		nuse the memory syste	m
	is "unfairly" shared among			, ,		, ,	
	a) single-core	•		c) super scalar		d) dual core	
21.	In most contemporary syst					•	ze.
	a) 512	b) 265		c) 128		d) 64	
22.	is example that a	•		,		,	
	a) VAX			c) MIPS		d) X86	
23.	SAN component interconne	•		,		,	
	a) Storage arrays			c) management softwa	re	d) cables	
24.	A express					,	
	a) high-level language	•	_	c) machine language		d) register	
25.	The ARM architecture only					, 0	
	a) data processing					d) branch	
26.	NAS component Head unit			,		,	
	a) CPU	b) NIC		c) Protocols		d) SCSI	
27.	multiple	•	etween the pr	ocessor and main mem	ory.	,	
	a) Cache Memory			c) RAM	•	d) CPU	
28.		•		d in memory or sent to	the I/O u	ınit.	
	a) Memory buffer register		Memory add				
	c) Instruction register	d)	Instruction b	uffer register			
29.	The decoded instruction is	stored in		-			
	a) Register	b) PC		c) IR	d) MDF	₹	
30.	A higher level only needs to	o know about the in	terface to the	lower level, not how th	ne lower	level is implemented	
	refer to						
	a) ISA	b) Microarchitectu	ire	c) Abstraction	d) Purp	ose of computing	
31.	Unexpected Slowdowns in	Multi-core because		·			
	a) L2 cash	b) L3 cash		c) Dram controller	d) Row	buffer	
32.	The DRAM controller reord	lers streams request	s to the open	row over other reques	ts (even d	older ones) to	
	DRAM throughput.						
	a) maximize	b) minimize		c) equalize	d) optii	mization	
33.	DRAM bank unavailable wh	nile refreshed refer t					
	a) Energy consumption	b) Performance de	gradation	c) QoS/impact	d) DRA	M capacity scaling	
34.	In the case of, Zero-address	s instruction method	d the operand	s are stored in		•	
	a) Registers	b) Accumulators		c) Push down stack	d) Cach	ie	
35.	The addressing mode, whe	re you directly spec	ify the operan	nd value is			
	a) Immediate	b) Direct		c) Definite	d) Rela	tive	
36.	Cache memory acts betwe	en and	·				
	a) CPU and RAM	b) RAM and ROM		c) CPU and Hard Disk	d) Non	e of these	
37.	The CISC stands for		·•				
	a) Computer Instruction Se			b) Complete Instructio	n Set Cor	mpliment	
	c) Computer Indexed Set C	omponents		d) Complex Instruction	Set Com	puter	
38.	The computer architecture	aimed at reducing t	the time of ex	ecution of instructions i	s	_·	
	a) CISC b) RISC	c)	ISA	d) ANNA			

20	Poth the CISC and PISC architectures has	ia haan dayalanad t	a raduca tha	1
33.	Both the CISC and RISC architectures have a) Cost b) Time delay	•	d) All of the me	
40	In CISC architecture most of the complex			intolled
40.	-	c) CMOS		
/ 11	Which of the architecture is power effici			
41.	a) CISC b) RISC		d) IANA	
12	The throughput of a super scalar process		•	
42.			 d) not known	
42	a) less than 1 b) 1	•	•	
43.	When the processor executes multiple in			
4.4			d) Multiple issu	ies
44.	The plays a very vital role in			
	a) Compilers b) Motherboard	•	· · ·	
45.	A stack organized computer has	_		
	a) 3 b) 2	-, -	d) 0	
46.	The disk drive is connected to the system			
	a) PCI bus b) SCSI bus	c) HDMI	d) ISA	
47.	ARM stands for			
	a) Advanced Rate Machines	b) Advanced RIS	SC Machines	
	c) Artificial Running Machines	d) Aviary Runnii	ng Machines	
48.	The main importance of ARM micro-pro-	cessors is providing	operation with	·
	a) Low cost and low power consumption	b) Higher degre	e of multi-tasking	
	c) Lower error or glitches	d) Efficient men	nory management	
49.	ARM processors where basically designed	ed for	•	
	a) Main frame systems	b) Distributed s	ystems	
	c) Mobile systems	d) Super compu	iters	
50.	In the ARM, PC is implemented using		·	
	a) Caches b) Heaps	c) General purp	ose register	d) Stack
51.	The instruction, ADD R1, R2, R3 is decod	ed as	·	
	a) R1<-[R1]+[R2]+[R3]	b) R3<-[R1]+[R2	<u>!]</u>	
	c) R3<-[R1]+[R2]+[R3]	d) R1<-[R2]+[R3	3]	
52.	converts the programs v	written in assembly	language into machine i	nstructions.
	a) Machine compiler b) Interpret	er	c) Assembler	d) Converter
53.	The instructions like MOV or ADD are ca	lled as		
	a) OP-Code b) Operator	S	c) Commands	d) Operand
54.	A source program is usually in	·		
	a) Assembly Language b) Machine	Level Language	c) High-level language	d) Natural language
55.	What is used to increase the apparent si	ze of physical memo	ory.	
	a) Disks b) Hard-disk	(c) Virtual memory	d) Secondary memory
56.	During instruction execution, an instruct	ion is read into an _	in th	e processor.
	a) Memory buffer register (MBR)		b) Address register (AD)
	c) Instruction register (IR)		d) Index register (IR)	
57.	Which computer program is used to con	vert whole program	into the machine langu	age at a time?
	a) Simulator b) Compiler		c) Interpreter	d) Commander
58.	The input devices use to store	the data received.		
	a) Primary Memory b) Secondar		c) Buffer	d) External Memory

59.	. In RISC architecture, memory access is limited to instructions: _			
	a) MOV and IMP b) ST and LD c)	PUSH and POP	d) CALL and RET	
60.	. Two processors A and B have clock frequencies of 700 Mhz and	900 Mhz respective	ly. Suppose A can execute	an
	instruction with an average of 3 steps and B can execute with a	n average of 5 steps,	For the execution of the s	ame
	instruction which processor is faster?			
		Insufficient informat	tion	
61.	The format is usually used to store data.	0.1.1		
	a) BCD b) Decimal c) Hexadecimal d)	Octal		
Ρu	ut √ or X:	'بقرّ)	ئلة وضعت في امتحانات سا	(أس
1.	DRAM controllers commonly used scheduling policy (FR-FCFS).			()
2.	Processor Is the computer component that interprets and exec	utes instructions.		()
3.	Alpha ISA contains a doubly linked list data type.			()
4.	CPU interconnection is a mechanism that provides for commun	ication among CPU,	main memory, and I/O.	()
5.	DRAM cells need to be refreshed because reading changes the	voltage level of the o	capacitor in a cell and capa	citors
	leak current.			()
6.	Two-level global branch prediction is microarchitecture.			()
7.	DRAM controllers designed to minimize DRAM data throughpu	t.		()
8.	Deeply Embedded Systems is not programmable once the prog	ram logic for the dev	rice has been burned into	
	ROM.			()
9.	Program counter is advanced sequentially except for control tra	insfer instructions.		()
10.	. ISA change more slowly than microarchitecture.			()
11.	. The type of memory assignment used in Intel processors is Littl	e Endian.		()
12.	RAID 5 apply disk striping with dedicated parity driver.			()
13.	RAID level 1 does not over any redundancy at all.			()
14.	During the transfer of data between the processor and memory	y we use register.		()
15.	. Memory and Registers are types of locations can hold source a	nd destination.		()
16.	ARM ISA use Load/Store architecture addressing mode.			()
17.	. SAN allowing multiple clients to access files at the same time w	ith very high perforn	nance.	()
18.	Alpha ISA SCAN opcode operates on character strings; PUSH\PG)P.		()
19.	. Orthogonal ISA refer all addressing modes can be used with ins	truction types.		()
20.	Potentially many instructions can execute at the same time in c	ontrol flow order.		()
21.	. In dataflow order each instruction specifies "who" should recei	ve the result.		()
22.	RAID levels 4 through 6 make use of a virtual access technique	that allows separate	I/O requests to be satisfie	d in
	parallel.			()
23.	Programmer cannot access pipeline registers directly.			()
24.	Interfaces between the computer and peripherals is an example	e of an organizationa	ll attribute.	()
25.	. Both the structure and functioning of a computer are, in essent	ce, simple.		()
26.	. When data are moved over longer distances, to or from a remo	ted device, the proc	ess is known as	
	data transport.			()
27.	The SAN advantage is no distance limitation.			()
28.	RAID provide fault tolerance for shared data and applications.			()
29.	. Many transistors can be produces at the same time on a single	wafer of silicon.		()

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30.	Dedicated processor define	ed by the processor's ability to e	execute complex operatir	ng systems.	()
31.	Deeply Embedded Systems	use a microcontroller rather th	an a microprocessor.		()
	. Internet download to disk is example of processing from/to storage. ()				
	. Updating bank statement is example of processing from storage to I/O. ()				
	. Moore observed number of transistors that could be put on a single chip was doubling every year. ()				
		and memory circuitry has faller	• .		()
36		ocessor by performing hands-on	RTI and C-level impleme	antation	()
	•		•		()
	Predicated instruction exec	ses wide floating-point values fo	or additional accuracy is	wiicroarchitecture.	()
			120		
		ess takes significantly longer tha	an a row-nit access		()
	•	support Byte addressability.			()
		niform decode is restricts instru			()
		nore complicated design than CI			()
	_	ves operand at address in A6 to	_		()
44.	A modern "super scalar" pi	rocessor that can execute two o	r more instruction at one	ce is consider a single	
	processor.				()
Ch	ioose:			(;	(أسئلة مهم
1.	Both the structure and fun-	ctioning of a computer are, in e	ssence, simple. a. Tru	e b. False	
2.	A computer must be able t	o process, store, move, and con	trol data. a. Tru	e b. False	
3.	Computer technology is ch	anging at a pace.			
	A. Slow	B. Slow to medium	C. Rapid	D. Non-existent	
4.	Computer refer	rs to those attributes that have a	a direct impact on the log	gical execution of a p	rogram.
	A. Organization	B. Specifics	C. Design	D. Architecture	
5.	Architectural attributes inc	lude			
	A. I/O mechanisms	B. Control signals	C. Interfaces	D. Memory techno	ology used
6.	attributes inclu	de hardware details transparen	t to the programmer.		
	A. Interface	B. Organizational	•	D. Architectural	
7.	It is a(n) design	issue whether a computer will	, ,		
	A. Architectural	•	C. Elementary	<u>-</u>	
8.		whether the multiply instruction		a special multiply ur	nit or by a
	·	peated use of the add unit of the			
_	A. Architectural	B. Memory	C. Mechanical	D. Organizational	
9.		set of interrelated subsystems.			
4.0	A. Secondary		C. Complex	D. Functional	
10.	An I/O device is referred to		C De deleced	D. D. Lister	
4.4	A. CPU	B. Control device	C. Peripheral	-	
11.		r longer distances, to or from a	· ·		·
12	A. Data communications		C. Structuring	D. Data transport	
12.	The stores data		C Main maman	D. Control:t	
12	A. System bus	B. I/O ta between the computer and it	C. Main memory		
13.	A. Data transport		C. Register	D. CPU interconne	ection
	, a bata transport	5. 1/ 0	C. INCEISTEI	D. C. O IIICEICOIIIIE	

14.	. A common example of system interconnection is by means o	of a
	A. Register B. System bus	C. Data transport D. Control device
15.	. A is a mechanism that provides for communication	on among CPU, main memory, and I/O.
	A. System interconnection B. CPU interconnection	C. Peripheral D. Processor
16.	provide storage internal to the CPU.	
	A. Control units B. ALUs	C. Main memory D. Registers
17.	. The performs the computer's data processing fu	unctions.
	A. Register B. CPU interconnection	C. ALU D. System bus
18.	. The smallest entity of memory is called	
	a) Cell b) Block	c) Instance d) Unit
19.	. When using the Big-Endian assignment to store a number, th	he sign bit of the number is stored in
	a) The higher order byte of the word	b) The lower order byte of the word
	c) Can't say	d) None of the mentioned
20.	. The key factor/s in commercial success of a computer are	·
	a) Performance b) Cost	c) Speed d) Both Performance and Cost.
21.	have been developed specifically for pipelined syste	ems.
	a) Utility software b) Speed up utilities	c) Optimizing compilers d) None of the mentioned
22.	. The fetch and execution cycles are interleaved with the help	of
	a) Modification in processor architecture b) Clock	c) Special unit d) Control unit
23.	. The pipelining process is also called as	
	a) Superscalar operation b) Assembly line operation	c) Von Neumann cycle d) None of the mentioned
24.	. Each stage in pipelining should be completed within	cycle.
	a) 1 b) 2 c) 3 d) 4	
25.	. To increase the speed of memory access in pipelining, we ma	ake use of
	a) Special memory locations b) Special purpose regis	
26.	. The Sun micro systems processors usually follow arch	
	a) CISC b) ISA c) ULTRA SPARC	d) RISC
27.	. Both the CISC and RISC architectures have been developed t	to reduce the
	a) Cost b) Time delay c) Semantic gap	d) All of the mentioned
28.	. Out of the following which is not a CISC machine.	
	a) IBM 370/168 b) VAX 11/780 c) Intel 80486	d) Motorola A567
29.	. Pipe-lining is a unique feature of	
	a) RISC b) CISC c) ISA	d) IANA
30.	. In CISC architecture most of the complex instructions are sto	ored in
	a) Register b) Diodes c) CMOS	d) Transistors
31.	. The collection of the above-mentioned entities where data is	is stored is called
	a) Block b) Set c) Word	d) Byte
32.	. An 24-bit address generates an address space of loca	ations.
	a) 1024 b) 4096 c) 248	d) 16,777,216
33.	. If a system is 64-bit machine, then the length of each word v	will be
	a) 4 bytes b) 8 bytes c) 16 bytes	d) 12 bytes
34.	. The type of memory assignment used in Intel processors is _	
	a) Little Endian b) Big Endian c) Medium Endi	ian d) None of the mentioned
35.	. To get the physical address from the logical address generate	ed by CPU we use
	a) MAR b) MMU c) Overlays	d) TLB

36.	method is us	sed to map logica	al addresses of va	ariable length	onto physic	al memory.	,
	a) Paging	b) Overlays	c) Segmentation	n d) Pa	ging with se	gmentation	
37.	During the transfer	of data betweer	the processor a	nd memory w	e use		
	a) Cache	b) TLB	c) Buffers	d) Re	gisters		
38.	Physical memory is	divided into sets	s of finite size cal	led as			
	a) Frames	b) Pages	c) Blocks	d) Ve	ctors		
39.	The CISC stands for						
	a) Computer Instru	ction Set Compli	ment	b) Complete	Instruction S	Set Complimen	t
	c) Computer Indexe	ed Set Componer	nts	d) Complex Ir	nstruction se	et computer	
40.	The computer arch	itecture aimed a	t reducing the tir	ne of execution	on of instruc	tions is	
	a) CISC	b) RISC	c) ISA	d) ANNA			
41.	The RISC processor	has a more com	plicated design t	han CISC.	a) True	b) False	
42.	The iconic feature of	of the RISC mach	ine among the fo	ollowing is			
	a) Reduced number	r of addressing n	nodes	b) Increased	memory size	е	
	c) Having a branch	delay slot		d) All of the r	nentioned		
43.	Which of the archit	ecture is power	efficient?				
	a) CISC	b) RISC	c) ISA	d) IANA			
44.	ARM stands for						
	a) Advanced Rate N	Nachines	b) Adva	nced RISC Ma	chines		
	c) Artificial Running	g Machines	d) Aviar	y Running Ma	chines		
45.	The main importan	ce of ARM micro	-processors is pr	oviding opera	tion with		
	a) Low cost and low	v power consum	ption b) High	er degree of n	nulti-tasking	5	
	c) Lower error or gl			ent memory r	nanagemen	t	
46.	ARM processors wh						
	•		•	•	-	•	d) Super computers
	The ARM processor		-	-	a) True	· ·	
	The address space				b) 264	c) 216	d) 232
49.	The address system						
	a) Little Endian	b) Big E		•		d) Both Little &	Big Endian
50.	Memory can be acc						
	i) Store	ii) MOVE	iii) Load	•	ithmetic	v) logic	al
	a) i, ii, iii	b) i, ii		c) i, iv, v	(d) iii, iv, v	
51.	RISC stands for						
	a) Restricted Instru	•		-		truction Sequer	·
	c) Reduced Instruct	•		d) Re	duced Indu	ction Set Comp	uter
52.	In the ARM, PC is in			١.٥			N 6: 1
	a) Caches	b) Hear		•	neral purpo	_	d) Stack
53.	The additional dup	_				_	N =
	a) Copied-registers		ed registers	c) EX	tra registers	;	d) Extential registers
54.	The banked registe						
	a) Switching betwe	•	·	е		ded storing	
	c) Same as other ge		_			of the mention	ea
55.	Each instruction in						
- -	a) 2 byte	b) 3 byte	c) 4 byt		d) 8 byte		
56.	All instructions in A	kivi are conditio	nally executed.	a) Trı	ie l	b) False	

57.	The addressing mode where	the EA of the operand i	s the cont	tents of Rn is			
	a) Pre-indexed mode		b) Pre-ind	dexed with write back	mode		
	c) Post-indexed mode		d) None	of the mentioned			
58.	The effective address of the i	nstruction written in Po	st-indexe	d mode, MOVE[Rn]+R	m is		
	a) EA = [Rn] b) EA = [F	Rn + Rm]	c) EA = [F	Rn] + Rm	d) EA =	[Rm] + Rn	
59.	The format is usually	used to store data.	a) BCD	b) Decimal	c) Hexa	decimal	d) Octa
	The 8-bit encoding format us						
		o) EBCDIC		c) ANCI	d) USCII	I	
61.	A source program is usually in	n					
	a) Assembly language k		ige c	:) High-level language	d) Natu	ral language	
62.	Which memory device is gene	erally made of semicon	ductors?				
		o) Hard-disk		c) Floppy disk	d) Cd di	sk	
63.	The small extremely fast, RAM	M's are called as			•		
	a) Cache			c) Accumulators	d) Stack	:S	
64.	The ALU makes use of	to store the interme	diate resu	ilts.			
	a) Accumulators				d) Stack		
65.	The control unit controls other						
	a) Control signals				d) Comi	mand Signals	
66.	are numbers and enc				•	· ·	
		o) Data) Information	d) Store	d Values	
67.	The Input devices can send in	nformation to the proce	essor.		•		
	a) When the SIN status flag is	· · · · · · · · · · · · · · · · · · ·) When the data arriv	es regard	less of the SIN	I flag
	c) Neither of the cases			d) Either of the cases	_		_
68.	bus structure is usual	lly used to connect I/O	devices.				
	a) Single bus			c) Star bus	d) Raml	ous	
69.	The I/O interface required to				•		
	a) Address decoder and regis	ters	t) Control circuits			
	c) Address decoder, registers	and Control circuits	c	d) Only Control circuits	5		
70.	To reduce the memory access						
	a) Heaps	o) Higher capacity RAM	's c	c) SDRAM's	d) Cach	e's	
71.	is generally used to in	ncrease the apparent si	ze of phys	sical memory.			
	a) Secondary memory	o) Virtual memory	c	c) Hard-disk	d) Disks		
72.	MFC stands for						
	a) Memory Format Caches		k	o) Memory Function C	omplete		
	c) Memory Find Command		c	d) Mass Format Comm	and		
73.	The time delay between two	successive initiations o	f memory	operation			
	a) Memory access time	o) Memory search time	c	c) Memory cycle time		d) Instruction	delay
74.	In pipelining the task which re	equires the least time is	s perform	ed first.		a) True	b) False
75.	If a unit completes its task be	efore the allotted time p	period, the	en			
	a) It'll perform some other ta	ask in the remaining tim	ne b) Its time gets realloc	ated to a	different task	
	c) It'll remain idle for the rem	naining time	C	d) None of the mentio	ned		
76.	The periods of time when the	e unit is idle is called as					
		o) Bubbles c) Hazaı		d) Both Stalls a	nd Bubbl	es	
77.	The contention for the usage	of a hardware device is	s called				
	a) Structural hazard	o) Stalk c) Dead	lock	d) None of the	mention	ed	

78.	The situation where	ein the data of ope	rands are not av	ailable is called			1
	a) Data hazard	·	c) Deadlo		— uctural hazar	d	
79.	The decoded instru	-		·			
	a) IR		c) Registe	ers d) MD)R		
80.	The instruction -> A	•	• •	·			
	a. Adds the value o			np register			
	b. Adds the value o			, 0			
	c. Adds the values	of both LOCA and I	RO and stores it	in RO			
				or and stores it in RO			
	Which registers can				b) PC	c) IR	d) R0
	During the execution		•	•	,	,	,
	a) MDR		_	i) MAR			
83.	•			ted to Memory Bus?			
	a) PC			d) Both PC and MAR			
84.	ISP stands for	•		.,			
-	a) Instruction Set Pi		b) Information Standa	rd Processing	<u> </u>	
	c) Interchange Stan			l) Interrupt Service Pr	_	,	
85.	The internal compo			·			
	a) Processor intra-c	-) Processor bus	c) Memory	/ hus	d) Rambus
86.	•	•	•	PC or performing ALU			a,
	a) Conditional code		Multiplexer		-	None of the	mentioned
87.	•	•	•	hem are collectively	-		
•	a) process route			ail c) information			
88	is used to			an cynnormation	i patir a j	data patri	
00.	a) D flip flop	_		c) RS flip flop	d)	None of the	mentioned
89.	Which of the follow				۵,	Trone or the	····circioned
05.	i. It deals with high	_	_	120110111			
	J	•		es, Data types, Cache	ontimization	1	
	_		_	units in the system a	-		nected
	v. None of the Abo		cactly all the	antis in the system a	ic arrangea a	ma micercon	necteu.
			compiled or as	sembled is called	•		
50.	A. Start Program	_		C. Source Program		Program	
91	The is the	· · · · · · · · · · · · · · · · · · ·	•	•	D. Hatarar	1 TOBIUM	
J = .	A. Registers	B. ALU		C. Flip-Flop	D. Multiple	exer	
92	The input devices u			, ,	D. Wartipi	.ACI	
J	A. Primary Memory				D	External Me	emory
93	The I/O devices are				υ.	External ivid	
55.	A. SDRAM's	B. Control		 C. Signals	D	BUS	
9/1	An optimizing Com			C. Signals	D.	503	
J . .	A. Better compilation						
	B. Takes advantage			cas its process time			
	C. Does better men		essor and reduc	ces its process time	D	All of the ab	nove
۵E	Which bus is used t	,	itar to the CDU	2	D.	חוו טו נווב מג	JUVE
<i>9</i> 3.	A. Single Bus	B. SCSI Bu		r C. Multiple Bu	ıs D	Rambus	
96	_			is Access Memory Loc		Namuu3	
50.	a. Branch		instruction Register Access	-		load and sto	aro.
	a. Dianch	ม. วเสเนร เ	register Access	c. Data FIOLES	osnig U.	ivau allu stt	ЛС

Additional Questions:

1.	The disk system co	nsists of which	of the following?	?			
	i. Disk	ii. Disk drive	iii. Dis	k controller			
	a) i and ii b) i, ii	and iii c) ii a	and iii d) i				
2.	The set of corresp	onding tracks o	on all surfaces of a	stack of disks for	m a		
	a) Cluster b) Cyl	nder c) Gr	oup d) Set				
3.	The data can be a	cessed from th	ne disk using				
	a) Surface number	b) Se	ctor number	c) Track numbe	er d) All (of the mentioned	
4.	The read and write	e operations us	ually start at	of the sector.			
	a) Center	b) M	iddle	c) From the las	t used point	d) Boundaries	
5.	To distinguish bety	ween two secto	ors we make use c	of			
	a) Inter sector gap	b) Sp	olitting bit	c) Numbering b	oit d) Nor	ne of the mentioned	
6.	The process	divides the di	sk into sectors and	d tracks.			
	a) Creation	b) In	itiation	c) Formatting	d) Mo	dification	
7.	The access time is	composed of _					
	a) Seek time	b) Ro	otational delay	c) Latency	d) Bot	h Seek time and Rota	tional delay
8.	The disk drive is co	onnected to the	e system by using	the			
	a) PCI bus	b) S0	CSI bus	c) HDMI	d) ISA		
9.	is used to	deal with the	difference in the	transfer rates bet	ween the drive	and the bus.	
	a) Data repeaters	b) Er	hancers	c) Data buffers	d) Nor	ne of the mentioned	
10.	is used to	detect and co	rrect the errors th	nat may occur dur	ring data transfe	ers.	
	a) ECC	b) CI	RC	c) Checksum	d) Nor	ne of the mentioned	
11.	The throughput of	a super scalar	processor is				
	a) less than 1	b) 1		c) More than 1	d) Not	Known	
12.	When the process	or executes mu	ultiple instructions	s at a time it is sai	d to use		
	a) single issue	b) M	ultiplicity	c) Visualization	d) Mu	ltiple issues	
13.	The plays	a very vital role	e in case of super	scalar processors.			
	a) Compilers	b) M	otherboard	c) Memory	d) Per	ipherals	
14.	If an exception is r	aised and the s	succeeding instruc	ctions are execute	ed completely, t	hen the processor is s	said to have _
	a) Exception hand	ling b) In	nprecise exception	ns c) Error correct	ion d) Noi	ne of the mentioned	
15.	In super-scalar mo	de, all the sim	lar instructions ar	re grouped and ex	ecuted togethe	r . a) True	b) False
16.	In super-scalar pro	cessors,	mode of exec	cution is used.			
	a) In-order	b) Post orde		c) Out of order		d) None of the mer	ntioned
17.	Since it uses the o	ut of order mo	de of execution, t	he results are sto	red in		
	a) Buffers	b) Special mo	emory locations	c) Temporary re	egisters	d) TLB	
18.	The step where in	the results sto	red in the tempor	ary register is tra	nsferred into th	e permanent register	is called as _
	a) Final step	b) Commitm	ent step	c) Last step		d) Inception step	
19.	A special unit used	to govern the	out of order exec	cution of the instr	uctions is called	as	
	a) Commitment u	nit b) Te	mporal unit	c) Mon	itor	d) Supervisory unit	
20.	The commitment	unit uses a que	ue called				
	a) Record buffer	b) Co	ommitment buffe	r c) Stora	age buffer	d) None of the mer	ntioned
21.	conve	erts the progra	ms written in asse	embly language in	to machine inst	ructions.	
	a) Machine compi	ler	b) Interpreter	c) Asse	mbler	d) Converter	
22.	The instructions li	ke MOV or ADI	are called as				
	a) OP-Code	b) Operators	c) Cor	mmands	d) None of the	mentioned	

23	. The alternate way	of writing the instr	uction, ADD #5	,R1 is	
	a) ADD [5],[R1];	b) ADDI :	5,R1;	c) ADDIME 5,[R1];	d) There is no other way
24	. Instructions which	won't appear in th	ne object progra	am are called as	
	a) Redundant instr	uctions I	o) Exceptions	c) Comments	d) Assembler Directives
25	. The assembler dire	ective EQU, when ι	ised in the insti	ruction: Sum EQU 200 o	loes
	a) Finds the first of	occurrence of Sum	and assigns va	lue 200 to it	
	b) Replaces every	occurrence of Sur	n with 200		
	c) Re-assigns the	address of Sum by	adding 200 to	its original address	
	d) Assigns 200 by	tes of memory sta	rting the location	on of Sum	
26	. The purpose of the	ORIGIN directive	is		
	a) To indicate the	starting position i	n memory, whe	ere the program block is	s to be stored
	b) To indicate the	starting of the co	mputation code	2	
	c) To indicate the	purpose of the co	de		
	d) To list the locat	tions of all the regi	sters used		
27				ne execution of the cod	e is
	a) Reserve b) Stor			d) EQU	
28			_	mory required for the b	block of code.
	a) Allocate	, 0	-	d) Reserve	
29	directive spe				
	a) End	b) Return	•	d) Terminate	
30	. The last statement				
	a) Stop	•	•	d) End	
31	. When dealing with	_		er	
	a) Replaces the ta	_			
	b) Does not repla				
	c) Finds the Bran			_	
22	·	_		he DATAWORD directiv	
32				ponding values in	
22		_	· -	c) Value map S	Set d) None of the mentioned
33	. The assembler stor	-		All Name and Constitution	
2.4	a) Main memory	•	c) RAM	d) Magnetic disk	ua ta
34				to memory for executio	on is
25	a) Loader b) Feto	•	•		a we use
33	· · · · · · · · · · · · · · · · · · ·			ng with branching code	
	a) Interpreter	b) Debug	ggei	c) Op-Assembler	d) Two-pass assembler

Answers

Choose:

1.	RAID level $_$ has the	highest disk overhead of a	all RAID types.		
	a) 0	b) 1	c) 3	d) 5	
2.	Disk arrays may be co	nsolidated or virtualized i	n a		
	a) RAID	b) NAS	c) SAN	d) SAS	
3.	What is the minimum	number of disks required	l for RAID 1?		
	a) 1	b) 2	c) 4	d) 5	
4.	The was desi	gned to provide a powerf	ul and flexible instr	uction set within t	he constraints of a 16-bit
	minicomputer.				
	a) PDP-10	b) PDP-11	c) VAX	d) ARM	
5.	The cache bridges the	speed gap between	and		
	a) RAM and ROM	b) Process	or and RAM		
	c) RAM and Secondary	y memory d) None of	the mentioned		
6.	The is the part o	f the computer that sequ	ences and executes	instructions.	
	a) CPU b) memory c)	bus d) inp	ut/output devices	
7.	A high-speed, special-	purpose network that int	egrates different typ	oes of data storage	e devices into a single storage
	system and connects	them to computing resou	rces across an entire	e organization is ca	alled a
	a) network-attached s	torage b)	storage area netwo	rk	
	c) storage as a service	d)	enterprise data stor	age solution	
8.	Load/store architectu	re: operate instructions o	perate only on	·	
	a) Memory	b) Register	c) imn	nediate	d) register indirect
9.	The use of multiple pr	ocessors on the same chi	p is referred to as $_$	and provid	des the potential to increase
	performance without	increasing the clock rate.			
	a) multicore	b) GPU	c) data	a channels	d) MPC
10.	A measurement of ho	w many tasks a computer	can accomplish in a	a certain amount o	of time is called a
	a) throughput	b) application anal	ysis c) cycl	e speed	d) real-time system
11.	Employed to tempora	rily hold the right-hand in	struction from word	d in memory.	
	a) MBR	b) MAR	c) IBR		d) PC
12.	A computer consists of	of, memory cells, a	and interconnection	s among these ele	ements.
	a) circuits	b) CPU	c) gat	es	d) chips
13.	Specifies the address	in memory of the word to	be written from or	read into the mer	mory address register
	a) MBR	b) MAR	c) IBR		d) PC
14.	manages the	computer's resources an	d orchestrates the p	performance of its	functional parts.
	a) Data Movement	b) Control	· ·	a processing	d) Data storage
15.	Updating bank statem	ent show operations invo	olving	·	
	a) Data Movement	b) Control	c) Dat	a processing	d) Data storage
16.	Embedded Systems ha	ave extreme resource con	straints in terms of	memory processo	r size, time, and
	a) Power consumptio	n b) Energy consump	otion c) spe	ed	d) cost
17.	Transferring data from	one peripheral or comm	unications line to a	nother is	
	a) Data Movement	b) Control	c) Dat	a processing	d) Data storage
18.	, consis	ting of a number of cond			mponents attach.
	a) System bus	b) memory	c) CPL	J	d) I/O

19.	If a system is 64-bit machin	e, then the length of eac	ch word will be	
	a) 4 bytes	b) 8 bytes	c) 16 bytes	d) 32 bytes
20.	The processors are	e vulnerable to a new cla	ass of Denial of Service (DoS) at	ttacks because the memory system
	is "unfairly" shared among	multiple cores.		
	a) single-core	b) multi-core	c) super scalar	d) dual core
21.	In most contemporary syste	ems fixed-length sectors	are used, with bytes bei	ing the nearly universal sector size.
	a) 512	b) 265	c) 128	d) 64
22.	is example that ap	ply orthogonal ISA.		
	a) VAX	b) ARM	c) MIPS	d) X86
23.	SAN component interconne	ect device such as	·	
	a) Storage arrays	b) switches	c) management softw	vare d) cables
24.	A express	ses operations in a concis	se algebraic form using variable	es.
	a) high-level language			
25.	The ARM architecture only	instruc	ctions access memory locations	S.
	a) data processing			d) branch
26.	NAS component Head unit	is		
	a) CPU	b) NIC	c) Protocols	d) SCSI
27.	multiple I	ayers of memory between	en the processor and main me	mory.
	a) Cache Memory			d) CPU
28.		contains a word to	be stored in memory or sent to	o the I/O unit.
	a) Memory buffer register		b) Memory address re	egister
	c) Instruction register		d) Instruction buffer r	register
29.	The decoded instruction is	stored in		
	a) Register b) PC		c) IR	d) MDR
30.	A higher level only needs to	know about the interfa	ce to the lower level, not how	the lower level is implemented
	refer to			
	a) ISA b) Micr	roarchitecture	c) Abstraction	d) Purpose of computing
31.	Unexpected Slowdowns in	Multi-core because	·	
	a) L2 cash b) L3 ca	ash	c) Dram controller	d) Row buffer
32.	The DRAM controller reord	ers streams requests to	the open row over other reque	ests (even older ones) to
	DRAM throughput.			
	a) maximize b) mini	mize	c) equalize	d) optimization
33.	DRAM bank unavailable wh	ile refreshed refer to	·	
	a) Energy consumption	b) Performance degrad	dation c) QoS/impact	d) DRAM capacity scaling
34.	In the case of, Zero-address	instruction method the	operands are stored in	·
	a) Registers	b) Accumulators	c) Push down stack	d) Cache
35.	The addressing mode, whe	re you directly specify th	e operand value is	
	a) Immediate	b) Direct	c) Definite	d) Relative
36.	Cache memory acts between	en and		
	a) CPU and RAM	b) RAM and ROM	c) CPU and Hard Disk	d) None of these
37.	The CISC stands for		·	
			b) Complete Instruction Set C	ompliment
	c) Computer Indexed Set Co	omponents	d) Complex Instruction Set Co	omputer
38.	The computer architecture	aimed at reducing the ti	me of execution of instructions	s is
	a) CISC b) RISC	c) ISA	d) ANNA	

	5 11 11 0100 15100					1
39.	Both the CISC and RISC a		-			
40	•	ime delay	,	•	-	ne mentioned
40.	In CISC architecture mos	•				
		Diodes	•) Transis	tors
41.	Which of the architectur					
	a) CISC b) R		•		l) IANA	
42.	The throughput of a sup	er scalar processo				
	a) less than 1 b) 1		c) more than 1		l) not kno	
43.	When the processor exe	ecutes multiple ins	tructions at a tim	e is said to use		·
	a) Single issue b) N	Jultiplicity	c) Visualization	n d	l) Multipl	le issues
44.	The plays a	very vital role in o	case of super scal	ar processors.		
	a) Compilers b) N	Notherboard	c) Memory	d	l) Periphe	erals
45.	A stack organized comp	uter has	address instruction	on.		
	a) 3 b) 2		c) 1	d	I) O	
46.	The disk drive is connec	ted to the system	by using the	·		
	a) PCI bus b) S	CSI bus	c) HDMI	d	l) ISA	
47.	ARM stands for					
	a) Advanced Rate Mach	ines	b) Adv	anced RISC Machin	nes	
	c) Artificial Running Mad	chines	_	ary Running Machin		
48.	The main importance of			-		
	a) Low cost and low pov			her degree of multi		
	c) Lower error or glitche	· ·		cient memory mana	_	
49.	ARM processors where		· ·	•	Ü	
	a) Main frame systems	, , , , , , ,		ributed systems		
	c) Mobile systems		-	er computers		
50.	In the ARM, PC is imple	mented using	•	•		
	a) Caches			eral purpose regist	er d)) Stack
51.	The instruction, ADD R1	· · · · · · · · · · · · · · · · · · ·		-	·	
	-\ D4 + [D4] + [D2] + [D2]	,				
	c) R3<-[R1]+[R2]+[R3]		-	:-[R2]+[R3]		
52.	convert	ts the programs w	-		chine inst	ructions.
	a) Machine compiler			c) Assembler		Converter
53.	The instructions like MC	· · · · · · · · · · · · · · · · · · ·		•	- ,	
	a) OP-Code	b) Operators		c) Commands	d)	Operand
54.	A source program is usu	<i>'</i>		,	- ,	,
	a) Assembly Language			c) High-level lang	uage d)	Natural language
55.	What is used to increase			_	,	
	a) Disks	b) Hard-disk		-	v d)	Secondary memory
56.	During instruction execu	•	n is read into an		•	•
	a) Memory buffer regist			b) Address registe		
	c) Instruction register (I	•		d) Index register (
57	Which computer progra	-	ert whole program	•		e at a time?
<i></i>		b) Compiler	,	c) Interpreter		Commander
58	The input devices use	•	he data received	•	u)	,
55.	a) Primary Memory			c) Buffer	۲)	External Memory
	, ,	e, secondary	,	s,c.	u,	

59.	In RISC architecture, mer	mory access is limited	to instructions:										
	a) MOV and IMP	b) ST and LD	c) PUSH and POP	d) CALL and RET									
60.	Two processors A and B have clock frequencies of 700 Mhz and 900 Mhz respectively. Suppose A can execute an												
		instruction with an average of 3 steps and B can execute with an average of 5 steps, For the execution of the same											
	instruction which proces												
.	a) A	b) B	c) Both take the same time	d) Insufficient inforr	nation								
61.	The format is usu	· ·		d) Octol									
	a) BCD	b) Decimal	c) Hexadecimal	d) Octal									
Pυ	ıt √ or X:												
1.	DRAM controllers comm	only used scheduling ¡	policy (FR-FCFS).		(√)								
2.	Processor Is the compute	er component that into	erprets and executes instructions.		(√)								
3.	Alpha ISA contains a dou	bly linked list data typ	e.		(X)								
4.	CPU interconnection is a	mechanism that prov	ides for communication among CPU	, main memory, and I/0	o. (X)								
5.	DRAM cells need to be re	efreshed because read	ling changes the voltage level of the	capacitor in a cell and	capacitors								
	leak current.				(√)								
6.	Two-level global branch	orediction is microarch	nitecture.		(√)								
7.	DRAM controllers design	ed to minimize DRAM	data throughput.		(X)								
8.	Deeply Embedded Syster	ns is not programmab	le once the program logic for the de	evice has been burned	into								
	ROM.				(√)								
9.	Program counter is adva	nced sequentially exce	ept for control transfer instructions.		(√)								
10.	ISA change more slowly t	han microarchitecture	e.		(√)								
11.	The type of memory assi	gnment used in Intel p	processors is Little Endian.		(√)								
12.	RAID 5 apply disk striping	g with dedicated parity	y driver.		(X)								
13.	RAID level 1 does not over	er any redundancy at a	all.		(X)								
14.	During the transfer of da	ta between the proces	ssor and memory we use register.		(√)								
15.	Memory and Registers a	re types of locations ca	an hold source and destination oper	ands.	(√)								
16.	ARM ISA use Load/Store	architecture addressir	ng mode.		(√)								
17.	SAN allowing multiple cli	ents to access files at	the same time with very high perfo	rmance.	(√)								
18.	Alpha ISA SCAN opcode o	operates on character	strings; PUSH\POP.		(X)								
19.	Orthogonal ISA refer all a	ddressing modes can	be used with instruction types.		(√)								
20.	Potentially many instruct	ions can execute at th	e same time in control flow order.		(X)								
21.	In dataflow order each in	struction specifies "w	ho" should receive the result.		(√)								
22.	RAID levels 4 through 6 r	nake use of a virtual a	ccess technique that allows separat	e I/O requests to be sat	tisfied in								
	parallel.				(√)								
23.	Programmer cannot acce	ess pipeline registers d	irectly.		(√)								
24.	Interfaces between the o	omputer and periphe	rals is an example of an organization	nal attribute.	(√)								
25.	Both the structure and fu	unctioning of a compu	ter are, in essence, simple.		(√)								
26.	When data are moved ov	ver longer distances, to	o or from a remoted device, the pro	cess is known as									
	data transport.				(X)								
27.	The SAN advantage is no	distance limitation.			(√)								
28.	RAID provide fault tolera	nce for shared data ar	nd applications.		(√)								
29.	Many transistors can be	produces at the same	time on a single wafer of silicon.		(√)								

						و مسامم				
30.	Dedicated processor defir	ned by the processor's a	ability to execute complex	operating syst	ems.	(X)				
	31. Deeply Embedded Systems use a microcontroller rather than a microprocessor.									
	32. Internet download to disk is example of processing from/to storage.									
	Updating bank statement					(X) (X)				
	Moore observed number			as doubling o	verv vear	(√)				
	The cost of computer logi		,	_		()				
55.	of Moore's law.	e and memory eneartry	nas fancii at a afamatic re	ite is the cons	equences	(√)				
26	Can evaluate a modern pr	rocossor by porforming	hands on PTI and Clovel	implomontatio	an.	(√)				
				-						
	A floating-point unit that		t values for additional acc	uracy is iviicio	architecture.	(√)				
	Predicated instruction exe		La constitución de la constitución			(v)				
	A row-conflict memory ac		_	ess.		(√)				
	The ARM processors don'		•			(X)				
	The disadvantage of non-					(X)				
	The RISC processor has a					(X)				
	Immediate addressing mo	·	_			(X)				
44.	A modern "super scalar"	processor that can exec	ute two or more instruction	on at once is co	onsider a single					
	processor.					(√)				
CŁ	noose:									
CI	1005e.									
	Both the structure and fu		•	a. True	b. False					
2.	A computer must be able	to process, store, move	e, and control data.	a. True	b. False					
3.	Computer technology is c	hanging at a	pace.							
	A. Slow	B. Slow to medium	C. Rapid	D. Non-exist	tent					
4.	Computer refe	ers to those attributes t	hat have a direct impact o	n the logical e	xecution of a p	rogram.				
	A. Organization	B. Specifics	C. Design	D. Architect	ure					
5.	Architectural attributes in	clude								
	A. I/O mechanisms				technology use	∍d				
6.	attributes incl									
	A. Interface	J	C. Memory		ural					
7.	It is a(n) desig									
	A. Architectural	B. Memory	C. Elementary	D. Organiza						
8.	It is a(n) issue	• •	·	ented by a spe	cial multiply ur	iit or by a				
	mechanism that makes re	•	•							
	A. Architectural	B. Memory	C. Mechanical	D. Organiza	tional					
9.	A system is a									
	A. Secondary		C. Complex	D. Function	al					
10.	An I/O device is referred t									
	A. CPU	B. Control device	C. Peripheral	_						
11.	When data are moved over	_		-		·				
	A. Data communications		C. Structuring	D. Data tran	sport					
12.	The stores dat									
	A. System bus		C. Main memory		nit					
13.	The moves d									
	A. Data transport	B. I/O	C. Register	D. CPU inter	rconnection					

14.	A common example of s	ystem interc	onnection is k	oy means o	f a		·
	A. Register	B. Syste	m bus		C. Data transport	D. Control d	evice
15.	A is a mecha	nism that pr	ovides for cor	nmunicatio	on among CPU, main	memory, and I/	0.
	A. System interconnecti	on B. CPU i	nterconnectio	n	C. Peripheral	D. Processor	-
16.	provide stora	age internal	to the CPU.				
	A. Control units	B. ALUs			C. Main memory	D. Registers	
17.	The perform	ns the comp	uter's data pr	ocessing fu	nctions.		
	A. Register	B. CPU i	nterconnectio	n	C. ALU	D. System b	us
18.	The smallest entity of m	emory is call	ed				
	a) Cell	b) Block			c) Instance	d) Unit	
19.	When using the Big-End	ian assignme	ent to store a	number, th	e sign bit of the nun	nber is stored in	
	a) The higher order byte	of the wor	t t		b) The lower order b	oyte of the word	
	c) Can't say				d) None of the ment	tioned	
20.	The key factor/s in comm	nercial succe	ss of a compu	uter are	·		
	a) Performance	b) Cost		c) Spe	eed	d) Both Perf	formance and Cost
21.	have been deve	loped specif	ically for pipe	lined syste	ms.		
	a) Utility software	b) Speed	d up utilities	c) Op	timizing compilers	d) None of t	he mentioned
22.	The fetch and execution	cycles are in	terleaved wit	the help	of		
	a) Modification in proces	ssor archited	ture	b) Clo	c) S	pecial unit	d) Control unit
23.	The pipelining process is	also called	as				
	a) Superscalar operation	b) Asser	nbly line ope	ration	c) Von Neumann cyc	cle d) None o	f the mentioned
24.	Each stage in pipelining	should be co	mpleted with	nin	cycle.		
	a) 1 b) 2	c) 3	d) 4				
25.	To increase the speed of	memory ac	cess in pipelin	ning, we ma	ike use of		
	a) Special memory locat	ions	b) Special pur	pose regist	cers c) C	ache	d) Buffers
26.	The Sun micro systems p	rocessors us	sually follow _	archi	tecture.		
	a) CISC	b) ISA		c) ULTRA	A SPARC	d) RISC	
27.	Both the CISC and RISC a	architectures	have been de	eveloped to	reduce the	-	
	a) Cost	b) Time	delay	c) Sema	ntic gap	d) All of the	mentioned
28.	Out of the following whi	ch is not a C	ISC machine.				
	a) IBM 370/168	b) VAX 1	1/780	c) Intel 8	30486	d) Motorola	A567
29.	Pipe-lining is a unique fe	ature of					
	a) RISC	b) CISC		c) ISA		d) IANA	
30.	In CISC architecture mos	t of the com	plex instructi	ons are sto	red in		
	a) Register	b) Diode	!S	c) CMOS	5	d) Transisto	rs
31.	The collection of the abo	ove-mention	ed entities wl	here data is	stored is called		
	a) Block	b) Set		c) Word		d) Byte	
32.	An 24-bit address genera	ates an addr	ess space of _	loca	tions.		
	a) 1024	b) 4096		c) 248		d) 16,777,21	L6
33.	If a system is 64-bit mac	hine, then th	e length of ea	ach word w	vill be		
	a) 4 bytes	b) 8 byte	es	c) 16 by	tes	d) 12 bytes	
34.	The type of memory ass	ignment use	d in Intel prod	cessors is _			
	a) Little Endian	b) Big Er	ndian	c) Mediu	um Endian	d) None of t	he mentioned
35.	To get the physical addre	ess from the	logical addres	ss generate	d by CPU we use		
	a) MAR b) N	IMU	c) Overlays		d) TLB		

36.	method is us	sed to map logic	al addresses of v	ariable length o	nto physica	l memory.	,
	a) Paging	b) Overlays	c) Segmentation	on d) Pag	ing with seg	gmentation	
37.	During the transfer	of data betwee	n the processor	and memory we	use	_	
	a) Cache	b) TLB	c) Buffers	d) Reg	isters		
38.	Physical memory is	divided into set	s of finite size ca	ılled as			
	a) Frames	b) Pages	c) Blocks	d) Vec	tors		
39.	The CISC stands for						
	a) Computer Instru	ction Set Compl	iment	b) Complete Ir	struction S	et Compliment	
	c) Computer Indexe	· ·		d) Complex In:		-	
40.	The computer arch				of instruct	ions is	
	a) CISC	b) RISC	c) ISA	d) ANNA			
	The RISC processor					b) False	
42.	The iconic feature		_				
	a) Reduced numbe	_	modes	-	eased mem	•	
	c) Having a branch	-		d) All d	of the ment	ioned	
43.	Which of the archit	-		-			
	•	b) RISC	c) ISA	d) IANA			
44.	ARM stands for			_			
	a) Advanced Rate N						
	c) Artificial Running		-	,			
45.	The main importan						
	a) Low cost and lov	-	_	_	_		
4.0	c) Lower error or gl		-	cient memory m	anagement		
46.	ARM processors wh	-			a) Mabila	avatama d) (
47	a) Main frame syste		•	•	=	systems d) S	super computers
	The ARM processor The address space			a) 224	a) True	-	d) 232
	The address system			· ·	b) 204	C) 210	u) 232
43.	a) Little Endian		Endian	c) X-Little Endi	- an d) Both Little & Big	Endian
50	Memory can be acc			•		, both Little & big	Liidiaii
50.	i) Store	ii) MOVE			hmetic	v) logical	
	a) i, ii, iii	•	•	•		v, 108.001	
51.	RISC stands for		2, 3, 12, 1	-,,,			
	a) Restricted Instru		g Computer	b) Res	tricted Instr	uction Sequential	Compiler
	c) Reduced Instruc	•	•	·		tion Set Computer	•
52.	In the ARM, PC is ir	-		,		·	
	a) Caches			eral purpose re	gister	d) Stack	
53.	The additional dup	licate register us	sed in ARM mach	nines are called a	as		
	a) Copied-registers	b) Banked regi	i sters c) EXtr	a registers	d) Extential register	·s
54.	The banked registe	rs are used for _					
	a) Switching between	en supervisor a	and interrupt mo	ode	b) Extend	ed storing	
	c) Same as other ge	eneral purpose r	egisters		d) None c	of the mentioned	
55.	Each instruction in	ARM machines	is encoded into _	Wo	rd.		
	a) 2 byte	b) 3 byte	c) 4 by	te	d) 8 byte		
56.	All instructions in A	RM are condition	nally executed.	a) True	e b) False	

57.	The addressing mode where the	e EA of the o	perand is the co	ntents o	f Rn is					
	a) Pre-indexed mode b) Pre-indexed with write back mode									
	c) Post-indexed mode		d) None of the	mention	ed					
58.	i8. The effective address of the instruction written in Post-indexed mode, MOVE[Rn]+Rm is									
	a) EA = [Rn] b) I	EA = [Rn + Rn	n]	c) EA =	[Rn] + Rm		d) $EA = [Rm] +$	Rn		
59.	The format is usually us	sed to store d	ata. a) BCD		b) Decimal	c) Hexad	decimal	d) Octal		
60.	The 8-bit encoding format used	l to store data	a in a computer	is	_					
	a) ASCII b) I	EBCDIC		c) ANCI			d) USCII			
61.	A source program is usually in _									
	a) Assembly language b) I	Machine leve	l language	c) High	-level language		d) Natural lang	guage		
62.	Which memory device is genera	ally made of	semiconductors	?						
	a) RAM b) Hard-dis	sk	c) Floppy disk		d) Cd disk					
63.	The small extremely fast, RAM's	s are called a	s							
	a) Cache b) Heaps		c) Accumulators	S	d) Stacks					
64.	The ALU makes use of	to store the	intermediate res	sults.						
	a) Accumulators b) Registers	S	c) Heap		d) Stack					
65.	The control unit controls other	units by gene	erating							
	a) Control signals b) Timing s	signals	c) Transfer signa	als	d) Command Sig	gnals				
66.	are numbers and encod	ded character	s, generally used	d as ope	rands.					
	a) Input b) Data		c) Information		d) Stored Value	S				
67.	The Input devices can send information to the processor.									
	a) When the SIN status flag is set b) When the data arrives regardless of the SIN flag									
	c) Neither of the cases		d) Eithe	er of the	cases					
68.	bus structure is usually	used to conr	ect I/O devices.							
	a) Single bus b)	Multiple bus	c) Star l	ous	d) Ram	bus				
69.	The I/O interface required to co	onnect the I/O	O device to the b	ous cons	ists of					
	a) Address decoder and register	rs	b) Cont	rol circu	its					
	c) Address decoder, registers a	nd Control ci	rcuits d) Only	Control	circuits					
70.	To reduce the memory access to	ime, we gene	erally make use o	of	_					
	•	Higher capac	•		c) SDRAM's		d) Cache's			
71.	is generally used to incr			ysical m						
	a) Secondary memory b) '	Virtual mem	ory		c) Hard-disk		d) Disks			
72.	MFC stands for									
	a) Memory Format Caches	-	•	•						
	•	· ·	Format Comma							
73.	The time delay between two su									
	,	Memory sear		-	nory cycle time		d) Instruction	-		
	In pipelining the task which req					a) True	b) Fals	se		
75.	If a unit completes its task befo		-							
	a) It'll perform some other task		ning time		me gets realloca		different task			
	c) It'll remain idle for the rema	_		d) Non	e of the mention	ed				
76.	The periods of time when the u					_				
	•	Bubbles	c) Hazards		d) Both Stalls a	nd Bubb	les			
77.	The contention for the usage of					_				
	a) Structural hazard b) S	Stalk	c) Deadlock		d) None of the	mention	ed			

78. T	he situation wherein	the data of operan	ds are not availa	able is called			
а) Data hazard	b) Stock	c) Deadlock	d) Str	uctural ha	azard	
79. T	he decoded instructi	on is stored in					
а) IR	b) PC	c) Registers	d) M[OR		
80. T	he instruction -> Add	d LOCA, R0 does					
a.	Adds the value of L	OCA to RO and stor	es in the temp r	egister			
b.	Adds the value of F	RO to the address of	LOCA				
c.	Adds the values of	both LOCA and R0	and stores it in	R0			
d.	Adds the value of L	OCA with a value in	n accumulator ai	nd stores it in RO			
81. V	/hich registers can in	teract with the sec	ondary storage?				
а) MAR	b) PC	c) IR		d) R0		
82. D	uring the execution	of a program which	gets initialized f	first?			
) MDR	b) IR	c) P(d) MAR	}	
83. V	hich of the register,	s of the processor	s/are connected	I to Memory Bus?	•		
) PC	b) MAR	c) IR		d) Both	n PC and MAR	₹
84. IS	SP stands for						
а) Instruction Set Pro	cessor	b) In	formation Standa	ard Proces	sing	
C	Interchange Standa	rd Protocol	d) In	terrupt Service P	rocedure		
85. T	he internal compone	ents of the processo	r are connected	by			
a) Processor intra-con	nectivity circuitry	b) P	rocessor bus	c) Mem	nory bus	d) Rambus
86	is used to cho	ose between increr	nenting the PC o	or performing ALL	J operatio	ns.	
a) Conditional codes	b) IV	lultiplexer	c) Control uni	t	d) None of t	the mentioned
87. T	he registers, ALU and	d the interconnection	n between ther	n are collectively	called as _		
a) process route	b) in	formation trail	c) information	n path	d) data path	า
88	is used to sto	ore data in registers					
а) D flip flop	b) JK	flip flop	c) RS flip flop		d) None of t	the mentioned
89. V	hich of the followin	g is true about Com	puter Organizat	ion?			
	It deals with high-l	_					
	It involves Logic (In	•	ressing modes, [Data types, Cache	optimizat	tion).	
	Computer Organiz		_		-		rconnected.
	None of the Above		•	•		J	
90. T	he program written a	and before being co	mpiled or assen	nbled is called		•	
	· -	. Intermediate prog		ource Program			
	he is the c						
	. Registers	B. ALU		C. Flip-Flop		D. Multiplex	ær
	he input devices use		he data received	• •			
	. Primary Memory			C. Buffer		D. External I	Memory
	he I/O devices are co	•	•			DI EXCETTATI	vicino, y
	. SDRAM's	B. Control ci		_· C. Signals		D. BUS	
	n optimizing Compile		cuits	C. Signais		D. DO3	
	. Better compilation		of code				
	. Takes advantage of			its process time			
	_		sor and reduces	s its process time		D All of the	ahaya
	. Does better memoi	,	rtotha CDUD			D. All of the	above
	Which bus is used to o			Iultiala Dua	D D===	hus	
	. Single Bus	B. SCSI Bus		Iultiple Bus	D. Ram	.uus	
	the ARM Architectu					المسامعا الم	-1
a	. Branch b	. Status Register Ac	cess C. Da	ata Processing		d. load and	store

Additional Questions:

1.	The disk system of	onsists of	which of the	e following?					
	i. Disk	ii. Disk	drive	iii. Disk coi	ntroller				
	a) i and ii b) i, i	i and iii	c) ii and iii	d) i					
2.	The set of corresp	oonding tr	acks on all s	urfaces of a stac	k of disks fo	orm a			
	a) Cluster b) Cy	linder	c) Group	d) Set					
3.	The data can be a	ccessed fr	om the disk	using					
	a) Surface number	er b) Sect	or number	c) Track nu	mber	d) A	II of the mentio	ned	
4.	The read and wri	te operatio	ons usually s	tart at c	of the sector	r.			
	a) Center	b) Mido	dle	c) From th	e last used _l	point d) B	oundaries		
5.	To distinguish bet	ween two	sectors we	make use of					
	a) Inter sector ga	p b) Split	ting bit	c) Number	ing bit	d) N	lone of the men	tioned	
6.	The proces	ss divides t	he disk into	sectors and trad	cks.				
	a) Creation	b) Initia	ntion	c) Formatt	ing	d) N	Modification		
7.	The access time i	s compose	d of						
	a) Seek time	b) Rota	tional delay	c) Latency		d) B	oth Seek time a	nd Rotation	nal delay
8.	The disk drive is	connected	to the syst	em by using the					
	a) PCI bus	b) SCSI	bus	c) HDMI		d) IS	SA		
9.	is used t	o deal wit	h the differe	ence in the trans	fer rates be	tween the driv	ve and the bus.		
	a) Data repeaters		b) Enhance	ers c)	Data buffer	s d) N	lone of the men	tioned	
10.	is used t	o detect a	nd correct t	he errors that m	nay occur du	uring data tran	sfers.		
	a) ECC	b) CRC	c) (Checksum		d) N	lone of the men	tioned	
11.	The throughput of	of a super	scalar proce	essor is					
	a) less than 1		b) 1	c) More th	an 1	d) N	lot Known		
12.	When the proces	sor execu	tes multiple	instructions at	a time it is	said to use			
	a) single issue		b) Multipli	city c)	Visualizatio	n d) N	/lultiple issues		
13.	The plays	a very vita	al role in cas	e of super scala	r processor	s.			
	a) Compilers		b) Motherl	ooard c)	Memory	d) P	eripherals		
14.	If an exception is	raised and	I the succee	ding instruction	s are execut	ted completely	, then the proce	ssor is said	to have _
	a) Exception hand	_	-	-					ned
15.	In super-scalar m	ode, all th	e similar ins	tructions are gro	ouped and e	executed toget	her. a) T	rue	b) False
16.	In super-scalar pr	ocessors,	m	ode of executio	n is used.				
	a) In-order		b) Post ord	er	c) Out	t of order	d) None of t	he mention	ned
17.	Since it uses the	out of orde	er mode of e	execution, the re	sults are sto	ored in	-		
	a) Buffers	b) Spec	ial memory	locations	c) Ten	nporary regist	ers d) T	LB	
18.	The step where in	n the resul	ts stored in	the temporary r	egister is tra	ansferred into	the permanent	register is ca	alled as _
	a) Final step	b) Com	mitment st	e p c)	Last step	d) Ir	nception step		
19.	A special unit use	ed to gover	n the out of	order execution	n of the inst	ructions is call	ed as		
	a) Commitment	unit	b) ¹	Temporal unit		c) Monitor	d) S	upervisory	unit
20.	The commitment	unit uses	a queue cal	led					
	a) Record buffer		b) Commit	ment buffer	c) Sto	rage buffer	d) None of t	he mention	ned
21.	con\	erts the p	rograms wri	tten in assembly	/ language i	nto machine ir	nstructions.		
	a) Machine comp	iler	b)	Interpreter	c) Ass	embler	d) Converte	r	
22.	The instructions I	ike MOV o	r ADD are c	alled as					
	a) OP-Code	b) Ope	rators	c) Comma	nds	d) None of t	he mentioned		

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23	. The alternate way	_			
	a) ADD [5],[R1];	-		c) ADDIME 5,[R1];	d) There is no other way
24				m are called as	
	a) Redundant inst		, ,	c) Comments	•
25				uction: Sum EQU 200	does
	a) Finds the first		_	ue 200 to it	
	b) Replaces ever	•			
			,	its original address	
	d) Assigns 200 by		_	on of Sum	
26	The purpose of th				
			_	ere the program bloc	k is to be stored
	•	e starting of the c	•		
	c) To indicate the				
2-	d) To list the loca		_		1
27		•		e execution of the co	de is
20	a) Reserve b) Sto	•		d) EQU	block of and
28			_	mory required for the	block of code.
20	a) Allocate	b) Assign	c) Set	d) Reserve	
25	directive spa) End		•	d) Terminate	
30	. The last statemen				
30	a) Stop	b) Return		 d) End	
21	. When dealing with	•	•	•	
J.	a) Replaces the t				
	b) Does not repla	_		ied	
	•	nch offset and rep			
	•	·		he DATAWORD directi	ve
32	· ·	_		onding values in	
	a) Special purpose		•		
	c) Value map Set				
33	. The assembler sto	•			
	a) Main memory	b) Cache	c) RAM	d) Magnetic disk	
34	. The utility prograr	m used to bring th	e object code int	o memory for executi	on is
	a) Loader b) Fet	cher c) Extra	actor d) Linke	r	
35	. To overcome the p	problems of the a	ssembler in dealii	ng with branching cod	le we use
	a) Interpreter	b) Deb	ugger	c) Op-Assembler	d) Two-pass assembler

اللهم صلِ وسلم وبارك على نبينا محمد.