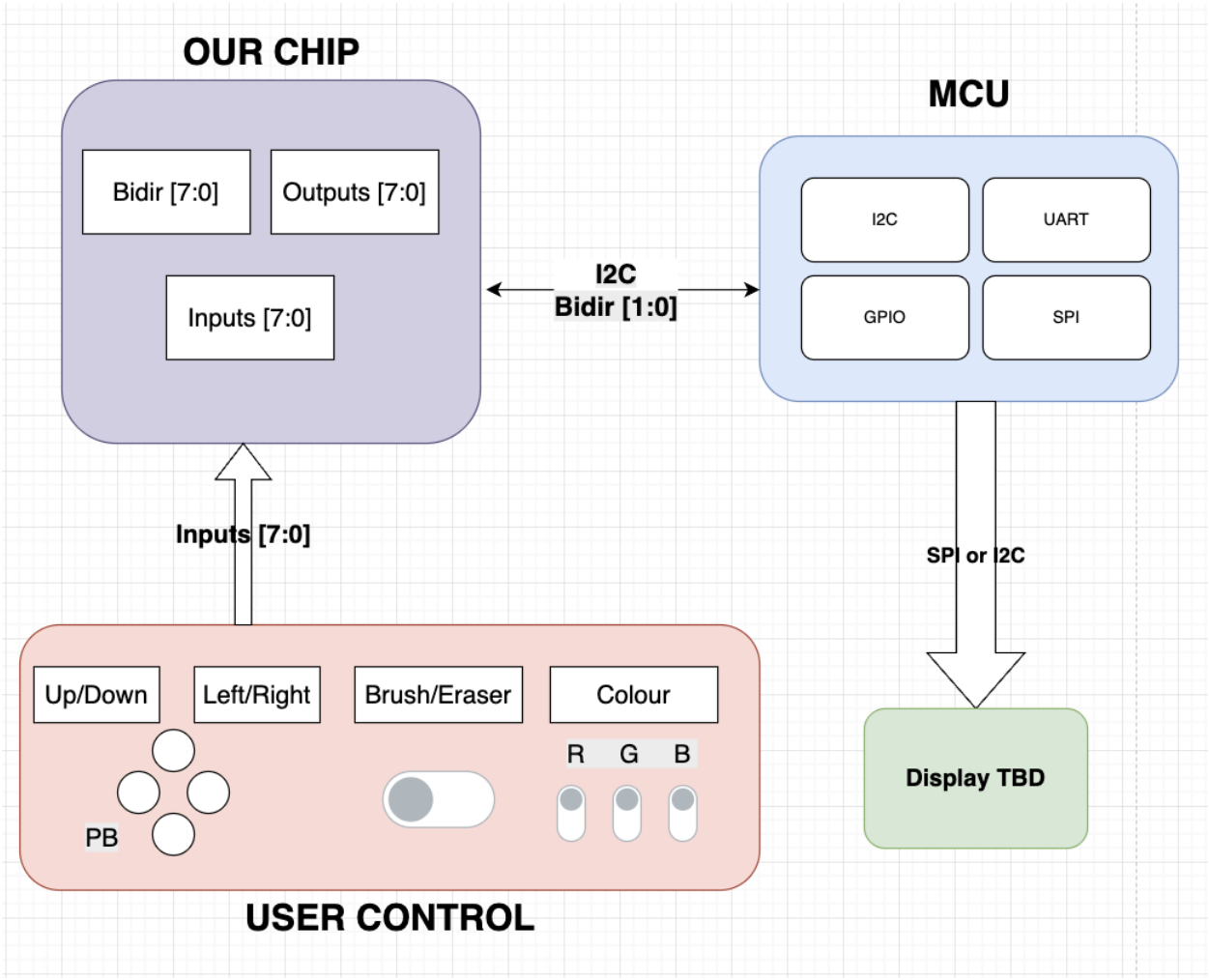
Tiny Tapeout Design Document

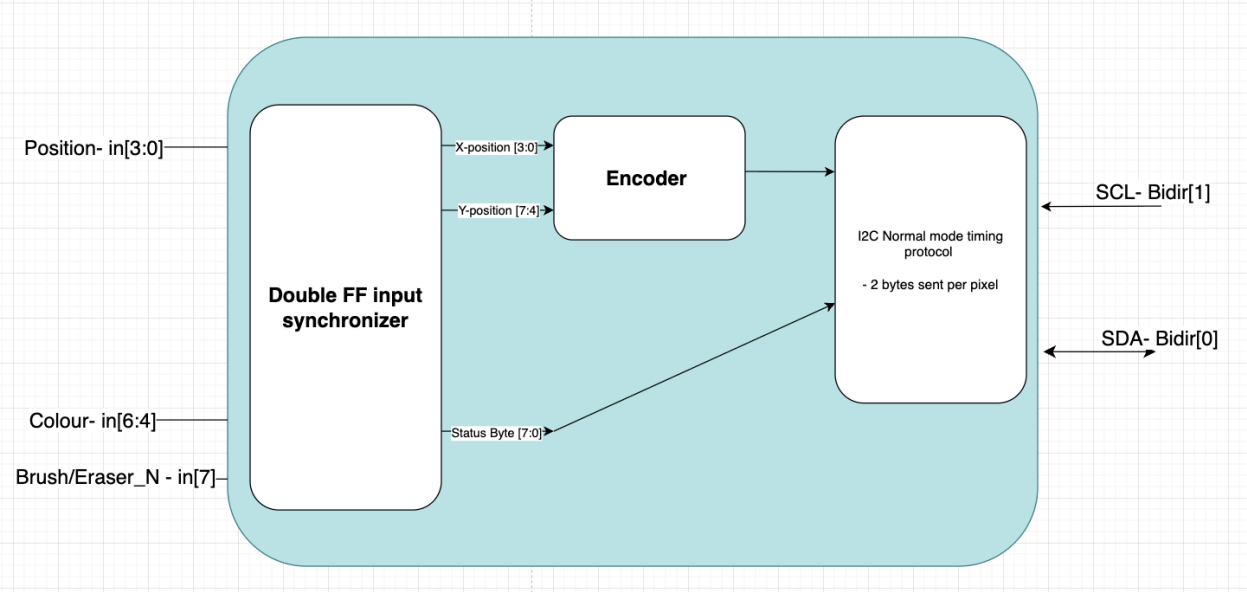
By Ahmad and Armita

1) Block Diagram

Application Block Diagram



Chip Block Diagram



2) List of IO assignments

PIN	Assignment	Description
Input [3:0]	Position Push button	Active low edge-triggered
Input [3]	Up	
Input [2]	Down	
Input [1]	Right	
Input [0]	Left	
Input [6:4]	Colour select	Dual-state switch
Input [6]	Red	
Input [5]	Green	
Input [4]	Blue	
Input [7]	Brush/Eraser_N	Dual-state switch
BidirIN[1:0]	I2C communication	Slave to MCU
Input [1]	SCL	
Input [0]	SDA	

3) Project Schedule

Week	Focus	Tasks
1	Specification	Finalize chip role (user inputs → I^2C outputs). Freeze I/O assignments. Define which bits encode **Up/Down/Left/Right**, **Brush/Eraser**, **RGB color**. Draft application block diagram.
2	FSM Design	Create FSM diagrams for input handling (debounce + edge detection). Define I^2C transaction protocol (what bytes get sent on button press/release). Document register map.
3	RTL – Input Handling	Implement input synchronizers and debouncers. Build logic for active-low pushbutton detection. Verify edge-triggered operation in simulation.
4	RTL – Control Encoding	Map inputs [7:0] to a structured control word (e.g. DIR[3:0], COLOR[2:0], TOOL[0]). Create "status byte" format for I^2C. Write unit testbenches to confirm encoding.
5	RTL – I^2C Slave	Implement minimal I^2C slave block (SCL, SDA). Add registers for control word. Support basic read (MCU polls state). Write simulation testbench for I^2C protocol.
6	RTL – Integration	Connect input FSM to I^2C slave registers. Ensure correct timing (edge-detected inputs update state, MCU reads clean values). Run end-to-end sim: input press → I^2C read → correct byte output.
7	Verification – Stress Tests	Simulate simultaneous button presses, switch toggling, bouncing. Verify I^2C behavior with back-to-back reads. Check glitch-free state transitions.

8	Tapeout Prep	Clean RTL (lint, synthesis checks). Run OpenLane flow (synth, place & route). Confirm area and pin constraints fit Tiny Tapeout rules. Finalize diagrams, FSM charts, and I/O documentation.
9	Final Verification	Rerun full testbench suite on post-synthesis netlist. Validate I^2C read timing margins. Double-check edge cases (reset state, all inputs high/low).
10	Submission	Freeze GitHub repo (RTL, testbenches, docs). Generate final GDS and metadata. Submit to Tiny Tapeout. Begin MCU firmware to read I^2C and forward commands to display.
Post-Tapeout	Demo Phase	Write MCU firmware: read I^2C bytes from chip, decode control word, update display. Build physical demo with buttons + toggle switches. Connect to chosen display (LED matrix, OLED, or VGA-lite).