#### **CPE301 – SPRING 2019**

# Design Assignment 2B

Student Name: Armon Latifi Student #: 2000698173

Student Email: latifa1@unlv.nevada.edu

Primary Github address: https://github.com/armonlatifi

Directory: https://github.com/armonlatifi/sub\_da/tree/master/DA2B

### Submit the following for all Labs:

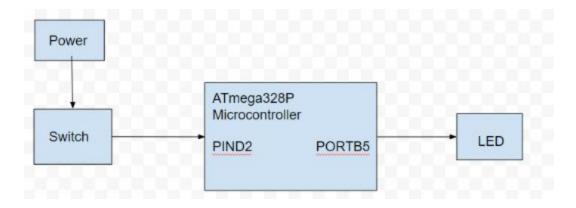
1. In the document, for each task submit the modified or included code (only) with highlights and justifications of the modifications. Also, include the comments.

- Use the previously create a Github repository with a random name (no CPE/301, Lastname, Firstname). Place all labs under the root folder ESD301/DA, sub-folder named LABXX, with one document and one video link file for each lab, place modified asm/c files named as LabXX-TYY.asm/c.
- 3. If multiple asm/c files or other libraries are used, create a folder LabXX-TYY and place these files inside the folder.
- 4. The folder should have a) Word document (see template), b) source code file(s) and other include files, c) text file with youtube video links (see template).

#### 1. COMPONENTS LIST AND CONNECTION BLOCK DIAGRAM w/ PINS

List of Components used:

- Assembler
- Simulator
- Debugger
- Breadboard
- Atmega328P
- Wires
- Microusb cord
- Atmel studio 7
- Arudino Multi-function shield



### 2. INITIAL/MODIFIED/DEVELOPED CODE OF TASK 1/A

part\_1.asm

start:

.include <m328pdef.inc>

.ORG 0 ;reset

JMP main

.ORG 0x02

JMP ex0\_isr

main:

LDI R20,HIGH(RAMEND)

OUT SPH,R20

LDI R20,LOW(RAMEND) OUT SPL,R20 ;initialize stack

LDI R20,0x2 ;make INT0 falling edge triggered

STS EICRA,R20

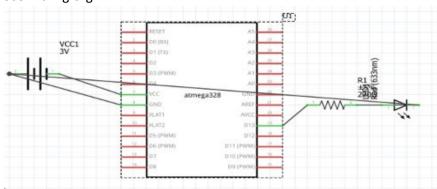
SBI DDRB,2 ;set port b as output SBI PORTD,2 ;pull-up activated

LDI R20,1<<INT0 OUT EIMSK,R20 SEI ;enable interrupts

```
ex0_isr:
        IN R21,PORTB
       LDI R22,(1<<2)
        EOR R21,R22
        OUT PORTB,R21
        RETI
part_1.c
#include <avr/io.h>
#include <avr/interrupt.h>
#include <avr/delay.h>
int main(void)
        DDRB = 1<<2;
        PORTD = 1<<2;
        DDRC = 0x00;
        EICRA = 0x02;
        EIMSK = (1 << INT0);
       sei();
  while (1)
  {
               PORTB = (1 << 2);
               _delay_ms(12500);
}
ISR(INT0_vect)
{
        PORTB ^= (1<<2);
        _delay_ms(12500);
}
```

#### 3. SCHEMATICS

Use fritzing.org

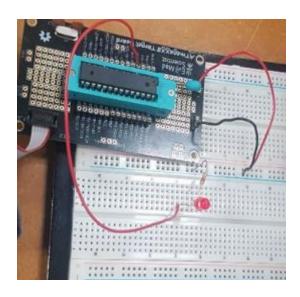


## 4. SCREENSHOTS OF EACH TASK OUTPUT (ATMEL STUDIO OUTPUT)

Cycle Counter 12 Cycle Counter 12

Frequency 16.000 MHz Frequency 16.000 MHz Stop Watch 0.75 µs Stop Watch 0.75 µs

## 5. SCREENSHOT OF EACH DEMO (BOARD SETUP)



### 6. GITHUB LINK OF THIS DA

https://github.com/armonlatifi/sub\_da/tree/master/DA2B

**Student Academic Misconduct Policy** 

http://studentconduct.unlv.edu/misconduct/policy.html

"This assignment submission is my own, original work".

NAME OF THE STUDENT