Assignment-2: Pipelining

Arnab Das, u1014840

February 13, 2018

1 *Pipelining Performance*

i.

In a single cycle processor, with IPC/CPI = 1, the CPU time will be

$$CPU\_time = IC \times CT = 1000 \times 10ns = 10\mu s$$

ii.

We denote the 1ns aditional delay for pipeline registers as

$$T_{ovh} = 1ns$$

Let T denote the cycle time for a single-cycle processor. In this case, $T = 10ns$. Let T_{ovh} denote the additional delay at every pipeline stage. Hence, $T_{ovh} = 1ns$. The cycle time for the unpipelined case will be

$$CT_{unpipe} = T + T_{ovh}$$

and the cycle time for the 10-stage pipelined case will be

$$CT_{pipe} = \frac{T}{10} + T_{ovh}$$

For the unpipelined case, it flushes 1 instruction per cycle since no stalls are required due to absence of hazards. For the 10-stage pipelined case, every 10 cycles req1uires 2 additional stall cycles. Thus it flushes 10 instructions every 12 cycles. Hence the CPI for the pipelined case will be

$$CPI_{pipe} = \frac{\#cycles}{\#instr} = \frac{12}{10} = 1.2$$

Since the instrcution count in both cases is the same, the execution times will be

$$\begin{aligned} Exec\_Time_{unpipe} &= IC_{unpipe} \times CPI_{unpipe} \times CT_{unpipe} = 1000 \cdot 1 \cdot (T + T_{ovh}) \\ Exec\_Time_{pipe} &= IC_{pipe} \times CPI_{pipe} \times CT_{pipe} = 1000 \cdot 1.2 \cdot (\frac{T}{10} + T_{ovh}) \end{aligned}$$

Thus, we get the following speedup

$$\begin{aligned} Speedup &= \frac{Exec\_Time_{unpipe}}{Exec\_Time_{pipe}} \\ &= \frac{1000 \cdot 1 \cdot (T + T_{ovh})}{1000 \cdot 1.2 \cdot (\frac{T}{10} + T_{ovh})} \\ &= \frac{11}{1.2 \cdot (1+1)} = \mathbf{4.58} \end{aligned}$$

2 Control Hazards

Let the total number of intructions be x. Given that only branch instructions introduce stalls. The total number of branch instructions
,

$$\#total\ branches = 20\%\ of\ x = \frac{x}{5}$$

Each branch introduces 2 additional stall cycles. Given that in the case of a branch being taken, it is allowed to move two instructions from the taken side into the branch delay slot, wich implies that in case of 60% of the branches being taken some useful work is being done in the stall cycles and hence there is effectively no stall cycles in the *taken* case. The remaining 40% of the branches which results in branches not being taken consequently leads to 2 stall cycles each. Number of branch instructions not taken will be

$$\#\ \text{branches not taken} = 40\%\ of\ \frac{x}{5} = \frac{2x}{25}$$

and total number of stalls introduced will be

$$\#\ total\ stalls = 2 \times \#\ \text{branches not taken} = \frac{4x}{25}$$

Hence, total number of cycles

$$\#\ total\ cycles = \#\ useful\ cycles + \#\ stall\ cycles = x + \frac{4x}{25} = \frac{29x}{25}$$

Hence, the expected CPI will be

$$CPI_{expected} = \frac{\#\ total\ cycles}{\#\ total\ instrs} = \frac{\frac{29x}{25}}{x} = \mathbf{1.16}$$

3 Multi-cycle Intructions

4 Points of Production and Consumption

In the unpipelined processor, it is given that the total circuit delay to execute an instruction is $T = 36ns$, with a latch overhead of $T_{ovh} = 0.5ns$. In the unpipelined case, the distance between POC and POP does not matters since the cycle time includes the duration spent in the entire circuit. Hence, the unpipelined cycle time will be

$$CT_{unpipe} = T + T_{ovh} = 36.5ns$$

and its throughput(IPS) will be

$$IPS_{unpipe} = \frac{1}{36.5 \times 10^{-9}} = \mathbf{27.39 \times 10^6}$$

In case of a 12 stage pipelined processor, the time spent per stage in the combinational circuit(excluding the latching stage) is

$$T' = T/12 = 3ns$$