Assignment-4: Memory Hierarchy: Cache

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1 Cache Hierarchy

All the 2000 load instructions will access L1-cache to check for a hit. Since the tag and data access in L1 is parallel, hence the lookup for all 2000 instructions is 1 cycle each(equqal to the tag access time). Hence, the time spent in the lookup for the L1 cache is

$$L1_t = 2000 \; cycles$$

Given the L1-cache hit rate is 50%, hence number of instructions($say\ n_2$) that get forwarded to the L2 cache is 1000. All n_2 instructions will be required to access the tag, but only the hits gets to access data. Thus the time spent in the L2 cache lookup and data access is

$$\begin{aligned} L2_t &= n_2 \times 3 + (55\%\ of\ n_2) \times 18 \\ L2_t &= 1000 \times 3 + (55\%\ of\ 100) \times 18 = 3000 + 550 \times 18 = 3000 + 9900 = 12900\ cycles \end{aligned}$$

Given the hit rate of L2 cache is 55%, hence number of instructions(n_3) that get forwarded to the L3 cache is 450. Given the hit rate of L3 is 75%, then the time spent in L3 cache lookup and data access is

$$\begin{aligned} L3_t &= n_3 \times 25 + (75\% of\ n_3) \times 85 \\ L3_t &= 450 \times 25 + (75\% of\ 450) \times 85 = 11250 + 28687.5 = 39937.5\ cycles \end{aligned}$$

Given the hit rate of L3 cache is 75%, hence of instructions(n_M) that gets forwarded to Main memory is 112.5. Then time spent in Main Memory access will be

$$MM_t = n_M \times 400 = 112.5 \times 440 = 49500$$

Thus, total number of cycles required to complete all 2000 load instructions is

$$Total\ Time\ = L1_t + L2_t + L3_t + MM_t = 2000 + 12900 + 39937.5 + 49500 = 104337.5\ cycles$$

2 Performance Metric

$$\begin{aligned} Hit\ time,\ t_h &= 5\ cycles \\ Miss\ Penalty,\ t_m &= 150\ cycles \\ Miss\ Rate,\ r_m &= = 0.2 \\ AMAT &= t_h + r_m t_m = 5 + 0.2 \times 150 = 35 \end{aligned}$$

3 Cache Addressing

Given the Main Memory is 8GB, hence the required number of bits required for this address space is 33 bits.

L1 cache

$$
\begin{aligned}
\text{Cache Size} &= 32KB \\
\text{Block Size} &= 16B = 2^4B \\
\text{hence, Offset bits} &= 4 \\
\text{Number of Blocks} &= \frac{\textit{Cache size}}{\textit{Block Size}} = \frac{32KB}{16B} = \frac{2^5 \times 2^{10}}{2^4} = 2^{11} \\
\text{hence, index bits} &= 11 \\
\text{hence, Tag bits} &= 33 - 4 - 11 = 18 \\
\text{Tag Array Size} &= 2^{11} \times 18bits = 2^8 \times 18B = 4.5KB \\
\text{Data Array Size} &= \text{Same as the cache size} = 32KB \\
\text{Total Size} &= 32KB + 4.5KB = 36.5KB
\end{aligned}
$$

L2 cache

$$
\begin{aligned}
\text{number of ways} &= 4 \\
\text{Each cache line size} &= 64B = 2^6B \\
\text{hence, Offset bits} &= 6 \\
\text{Block size} &= 4 \times 64B = 256B = 2^8B \\
\text{Cache Size} &= 1MB = 2^{20}B \\
\text{Number of Blocks} &= \frac{\textit{Cache Size}}{\textit{Block Size}} = \frac{2^{20}}{2^8} = 2^{12} \\
\text{hence, index bits} &= 12 \\
\text{hence, Tag bits} &= 33 - 6 - 12 = 15 \\
\text{Tag Array Size} &= 4 \times 2^{12} \times 15bits = 2^{11} \times 15B = 30KB \\
\text{Data Array Size} &= \text{Same as cache size} = 1MB \\
\text{Total Size} &= 30KB + 1MB
\end{aligned}
$$

4 Cache Replacement Policies

Program-1

The following figures details the application of the ideal, LRU and MRU replacement policies to program-1.

Prog-1	Ideal				
	SET-1		SET-2		Misses
	way-1	way-2	way1	way-2	
C	C				1
A	C	A			1
B	C	B			1
D	C	B	D		1
B	C	B	D		
F	C	B	D	F	1
C	C	B	D	F	
E	C	B	D	E	1
A	A	B	D	E	1
D	A	B	D	E	
B	A	B	D	E	
F	A	B	F	E	1
A	A	B	F	E	
B	A	B	F	E	
C	C	B	F	E	1
E	C	B	F	E	
B	C	B	F	E	
A	A	B	F	E	1
F	A	B	F	E	
D	A	B	D	E	1
# Miss	**11**				
%Miss	**55**				

Figure 1: Program-1 Ideal replacement

To summarize, the miss rates for program-1 will be

$$\begin{aligned} Ideal &= 55\% \\ LRU &= 75\% \\ MRU &= 55\% \end{aligned}$$

Prog-1	LRU				
	SET-1		SET-2		Misses
	way-1	way-2	way1	way-2	
C	C				1
A	C	A			1
B	B	A			1
D	B	A	D		1
B	B	A	D		
F	B	A	D	F	1
C	B	C	D		1
E	B	C	E	F	1
A	A	C	E	F	1
D	A	C	E	D	1
B	A	B	E	D	1
F	A	B	F	D	1
A	A	B	F	D	
B	A	B	F	D	
C	C	B	F	D	1
E	C	B	F	E	1
B	C	B	F	E	
A	A	B	F	E	1
F	A	B	F	E	
D	A	B	F	D	1
# Miss	**15**				
%Miss	**75**				

Figure 2: Program-1 LRU replacement

Program-2

The following figures details the application of the ideal, LRU and MRU replacement policies to program-2.

To summarize, the miss rates for program-2 will be

$$\begin{aligned} Ideal &= 45\% \\ LRU &= 50\% \\ MRU &= 60\% \end{aligned}$$

Prog-1	LRU				
	SET-1		SET-2		Misses
	way-1	way-2	way1	way-2	
C	C				1
A	C	A			1
B	C	B			1
D	C	B	D		1
B	C	B	D		
F	C	B	D	F	1
C	C	B	D	F	
E	C	B	D	E	1
A	A	B	D	E	1
D	A	B	D	E	
B	A	B	D	E	
F	A	B	F	E	1
A	A	B	F	E	
B	A	B	F	E	
C	A	C	F	E	1
E	A	C	F	E	
B	A	B	F	E	1
A	A	B	F	E	
F	A	B	F	E	
D	A	B	D	E	1
# Miss	**11**				
%Miss	**55**				

Figure 3: Program-1 MRU replacement

Prog-2	Ideal				
	SET-1		SET-2		Misses
	way-1	way-2	way1	way-2	
D			D		1
F			D	F	1
C	C		D	F	1
B	C	B	D	F	1
A	C	A	D	F	1
A	C	A	D	F	
F	C	A	D	F	
C	C	A	D	F	
D	C	A	D	F	
D	C	A	D	F	
A	C	A	D	F	
B	B	A	D	F	1
A	B	A	D	F	
B	B	A	D	F	
C	B	C	D	F	1
E	B	C	D	E	1
B	B	C	D	E	
A	B	A	D	E	1
B	B	A	D	E	
D	B	A	D	E	
# Miss	**9**				
%Miss	**45**				

Figure 4: Program-2 Ideal replacement

Prog-2	LRU				
	SET-1		SET-2		Misses
	way-1	way-2	way1	way-2	
D			D		1
F			D	F	1
C	C		D	F	1
B	C	B	D	F	1
A	A	B	D	F	1
A	A	B	D	F	
F	A	B	D	F	
C	A	C	D	F	1
D	A	C	D	F	
D	A	C	D	F	
A	A	C	D	F	
B	A	B	D	F	1
A	A	B	D	F	
B	A	B	D	F	
C	C	B	D	F	1
E	C	B	D	E	1
B	C	B	D	E	
A	A	B	D	E	1
B	A	B	D	E	
D	A	B	D	E	
# Miss	**10**				
%Miss	**50**				

Figure 5: Program-2 LRU replacement

Prog-2	LRU				
	SET-1		SET-2		Misses
	way-1	way-2	way1	way-2	
D			D		1
F			D	F	1
C	C		D	F	1
B	C	B	D	F	1
A	C	A	D	F	1
A	C	A	D	F	
F	C	A	D	F	
C	C	A	D	F	
D	C	A	D	F	
D	C	a	D	F	
A	C	A	D	F	
B	C	B	D	F	1
A	C	A	D	F	1
B	C	B	D	F	1
C	C	B	D	F	
E	C	B	E	F	1
B	C	B	E	F	
A	C	A	E	F	1
B	C	B	E	F	1
D	C	B	D	F	1
# Miss	**12**				
%Miss	**60**				

Figure 6: Program-2 MRU replacement