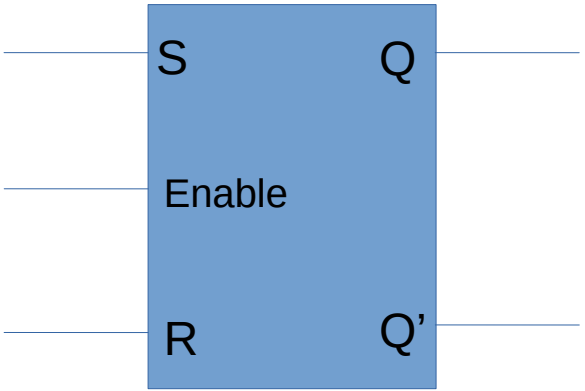
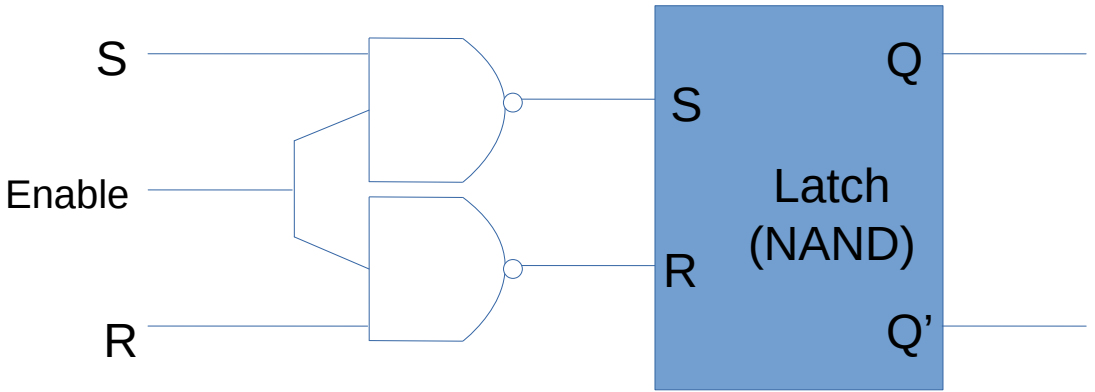
Switching Circuit & Logic Design

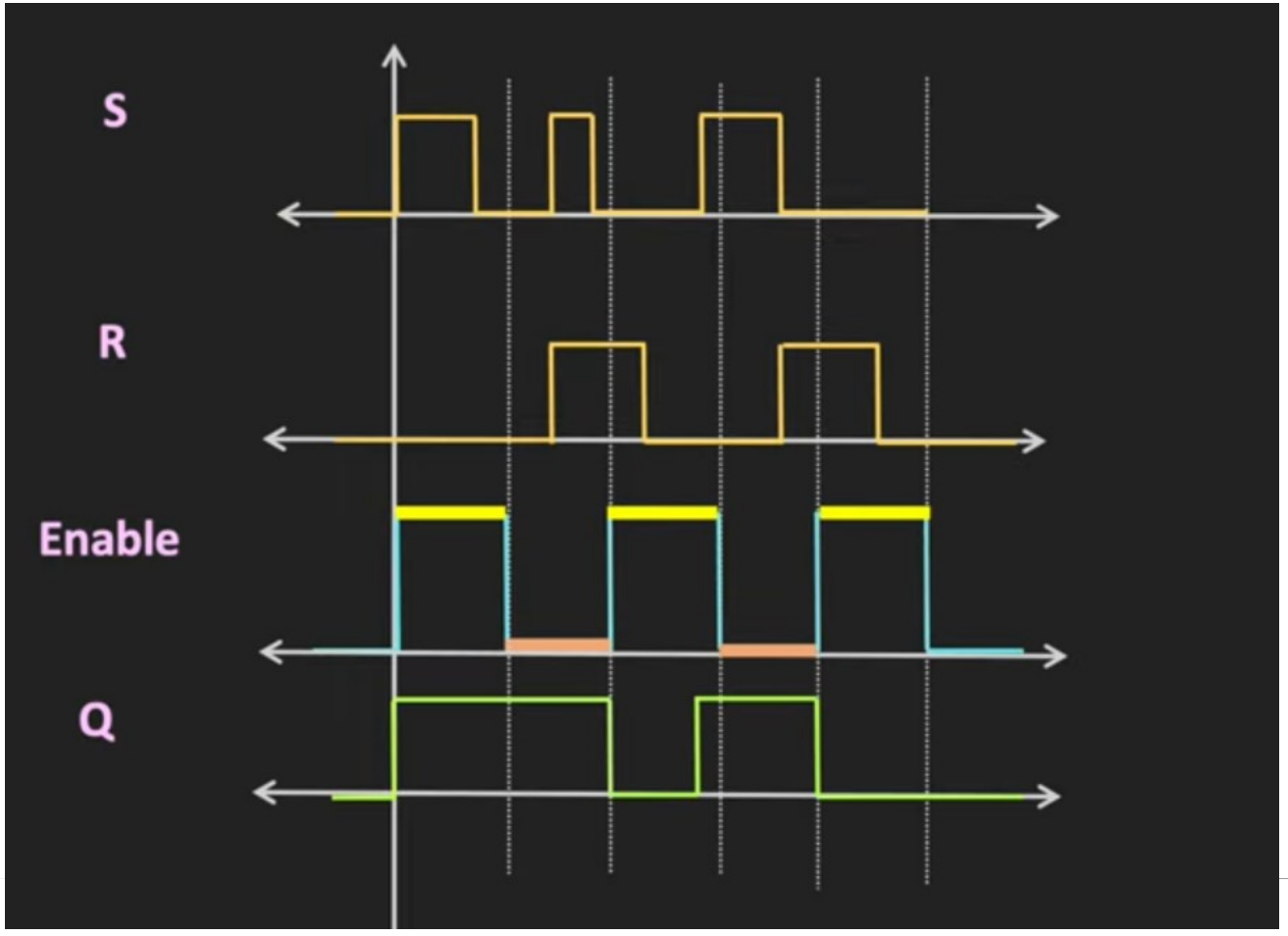
Lecture 21 : Flip-Flop

Gated SR Latch – SR Flip-Flop

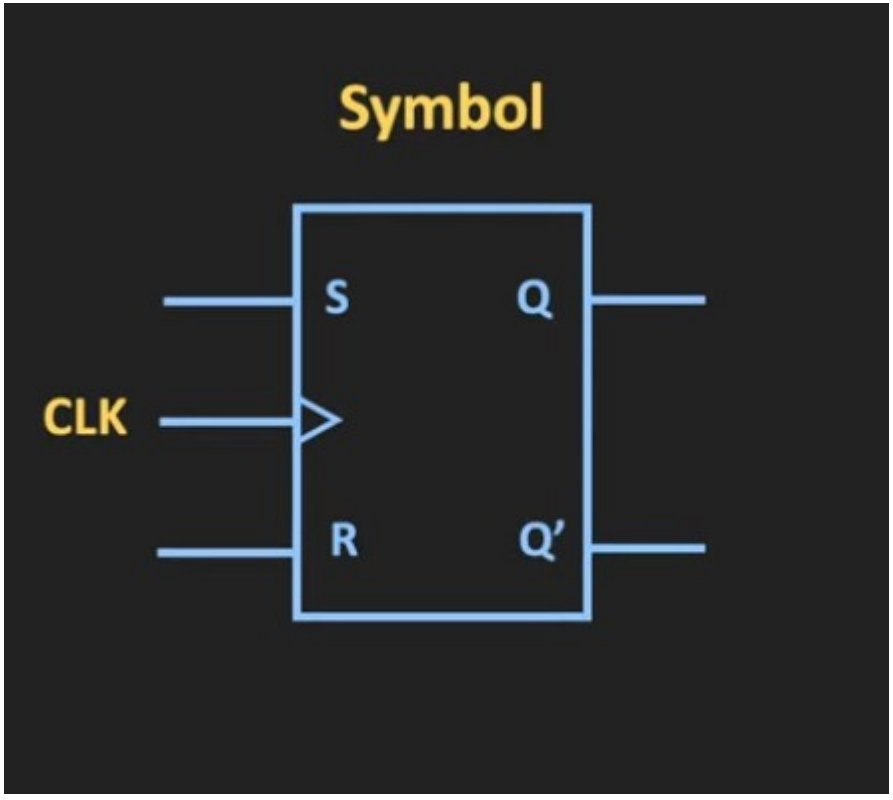


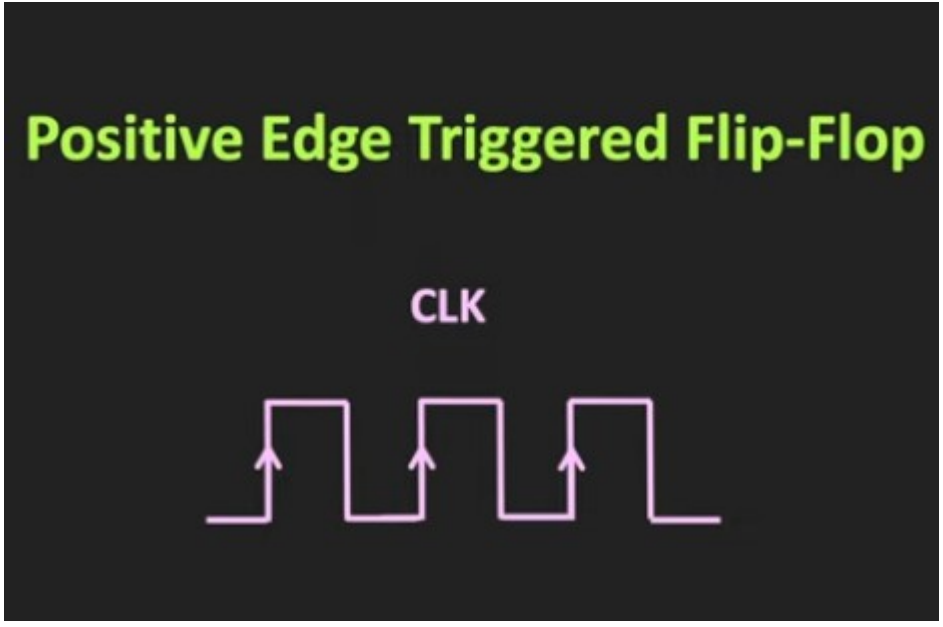


Gated SR Latch – SR Flip-Flop

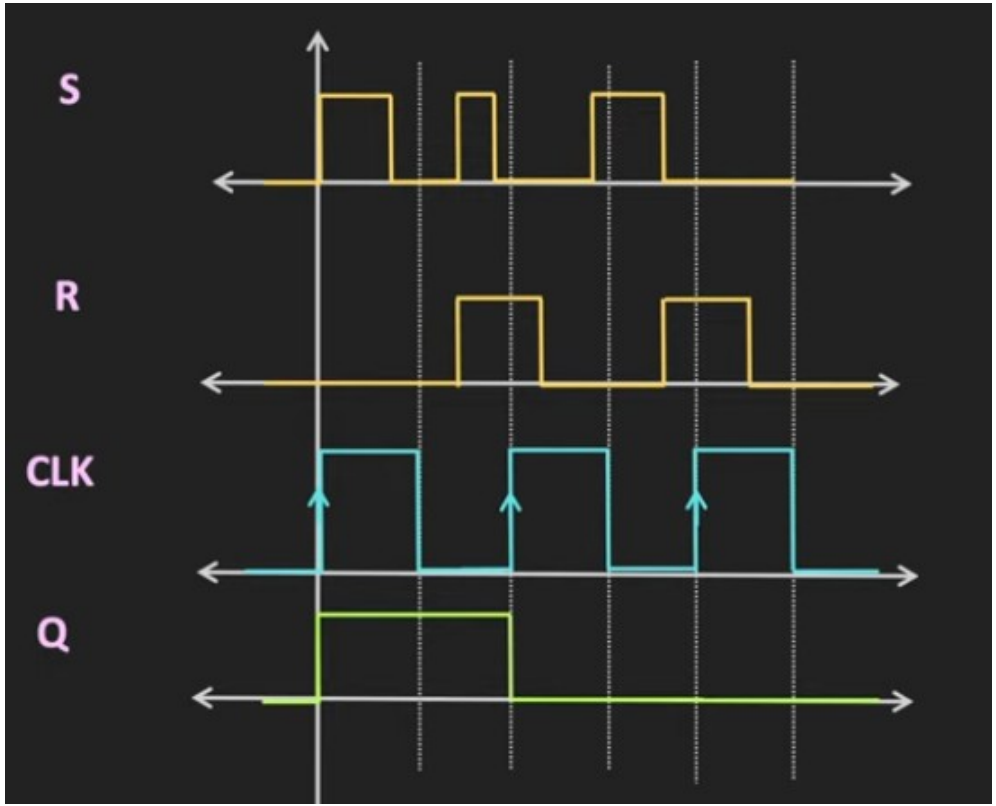


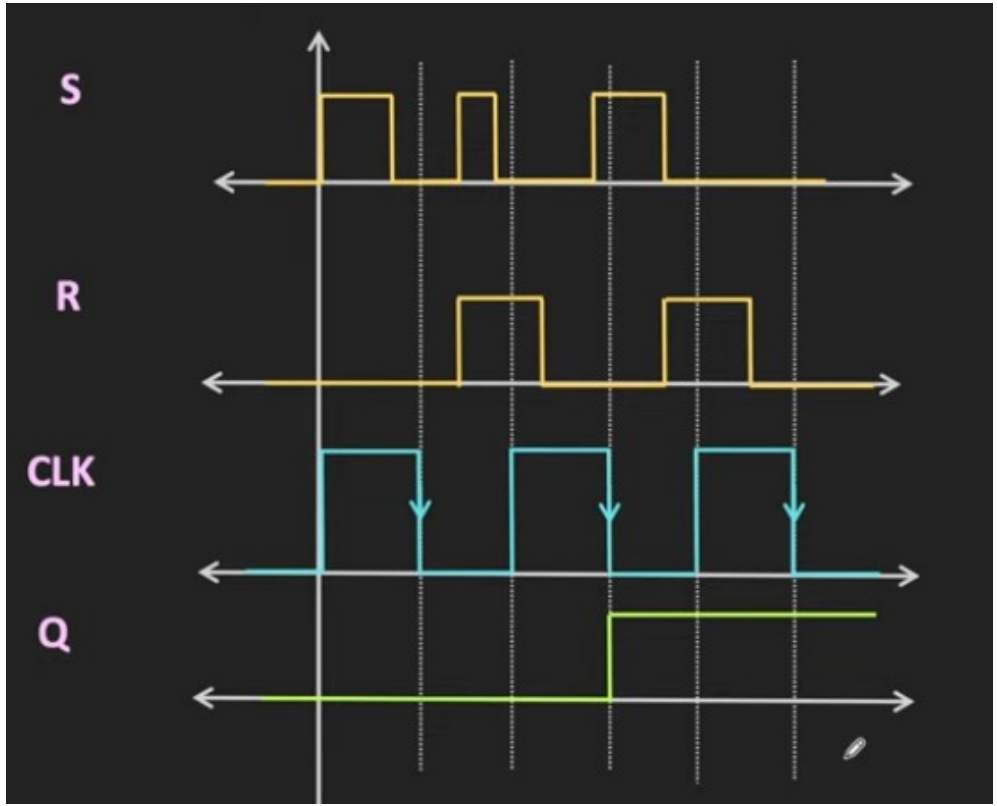
SR Flip-Flop





CLK	S	R	Q_n (Present State)	Q_{n+1} (Next State)	State
0	X	X	0 1	0 1	No Change
↑	0	0	0 1	0 1	No Change
↑	0	1	0 1	0 0	RESET
↑	1	0	0 1	1 1	SET
↑	1	1	0 1	X X	Forbidden


S
R
CLK
Q

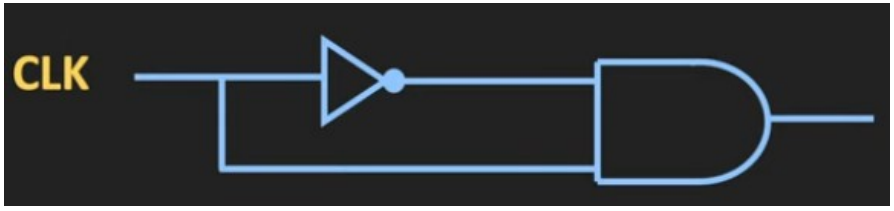

S
R
CLK
Q

Characteristic Equation of SR FF

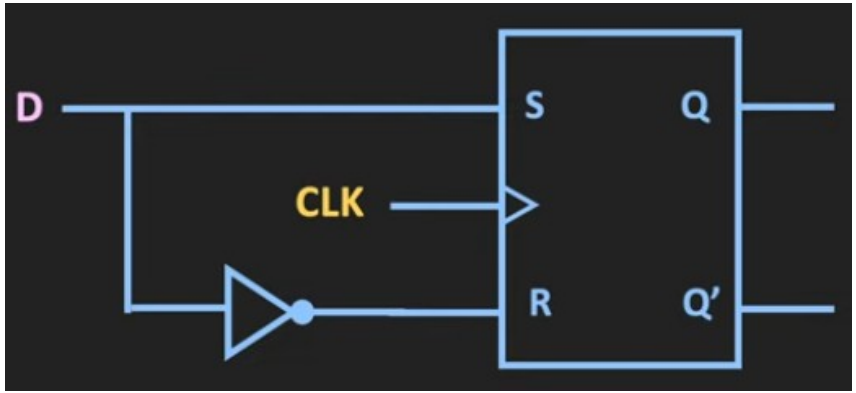
$Q_{n+1} = F(Q_n, S, R)$

Q_n (Present State)	S	R	Q_{n+1} (Next State)
0	0	0	0
1	0	0	1
0	0	1	0
1	0	1	0
0	1	0	1
1	1	0	1
0	1	1	X
1	1	1	X

Clock Transition Detection Circuit



D Flip-Flop



CLK	D	S	R	Q_n	Q_{n+1}
0	X	X	X	0 1	0 1
↑	0	0	1	0/1	0
↑	1	1	0	0/1	1