Arnav Patil

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EDUCATION

University of Toronto — Sept 2023 – Apr 2027
BASc. in Electrical and Computer Engineering with PEY Co-Op — *Toronto, Canada*
- **GPA: 3.60/4.00** with recognition on Dean's Honours List
- **Minor in Engineering Business**

SELECTED COURSES

Languages: C/C++, **Verilog**, **RISC-V Assembly**, Python (NumPy & pandas), MATLAB
Hardware Courses: Computer Architecture, Analog & Digital Electronics, Digital Systems
Software Courses: Operating Systems, Embedded Programming, Object-Oriented Programming

EXPERIENCE

FPGA Research Intern — Feb 2025 – Present
Department of Electrical & Computer Engineering, University of Toronto — *Toronto, Canada*
- Researching at **Prof. Roman Genov's** Intelligent Sensory Microsystems Lab with the **CMOS Imaging Team**.
- Developing RTL and hardware-software co-design for FPGA-controlled coded-exposure time-of-flight imaging.
- Extending a custom Python API for user control, enabling rapid prototyping in computer vision experiments.

Teaching Assistant — Incoming Sept 2025
Faculty of Applied Science & Engineering, University of Toronto — *Toronto, Canada*
- **APS100 Orientation to Engineering:** transition to engineering studies, academic skills, and career pathways.

ML Compute Platform Developer — Sept 2024 – Apr 2025
University of Toronto Machine Intelligence Student Team — *Toronto, Canada*
- Developed a compute platform for UTMIST to optimize ML jobs using GPU accelerated cloud computing.
- Wrote an API to create teams and users, and to access various cloud platforms and check GPU availability.
- Worked with a team of developers to deploy the platform and establish monthly feature release cycles.

SELECTED PROJECTS

NIOS-V Sonar System on an FPGA | Source Code Repository
- Integrated ultrasonic sensor and servo motor into the FPGA-based NIOS-V soft processor via GPIO ports.
- Designed & implemented BJT pull-up/pull-down networks for safe 3.3V-to-5V signal interfacing on FPGA.
- Engineered time-sensitive sensor polling using machine timer, avoiding interrupts for timing precision.

Blackjack Arcade Game on an FPGA | Presentation Slides
- Developed a digital blackjack game using finite state machines (FSMs) on a DE1-SoC FPGA, handling complex game states such as dealing, betting, and scoring in real-time to simulate card-counting experience.
- Wrote a Python script to reformat memory initialization files (.mif), fixing compatibility issues between an instructor-provided legacy conversion tool and modern IPs.

EXTRACURRICULAR ACTIVITIES

Member, Policies & Structures Committee — Jun 2025 – Present
University of Toronto Engineering Society — *Toronto, Canada*
- Supporting EngSoc's legislative foundation and deliberating on policies impacting a 5000+ strong student body.

Sustainability Director — Apr 2024 – May 2025
University of Toronto Engineering Society — *Toronto, Canada*
- Oversaw 5 initiatives, and wrote a Sustainability Policy to support discourse and action on environmental matters.