

# Arnav Patil

[arnav.patil@mail.utoronto.ca](mailto:arnav.patil@mail.utoronto.ca) | (587) 830-1203 | [linkedin.com/in/arnavpatil](https://www.linkedin.com/in/arnavpatil) | [arnav-patil-12.github.io](https://arnav-patil-12.github.io)

## EDUCATION

### University of Toronto

Sept 2023 – Apr 2028

*BASc. in Electrical and Computer Engineering with PEY Co-op*

*Toronto, ON*

- **GPA: 3.58/4.00** with recognition on Dean's Honours List
- **Minor in Engineering Business/Economics**

## COURSEWORK

**Languages & Tools:** C/C++, (System)Verilog, Python, RISC-V Assembly, Quartus Prime, Vivado, Cadence Virtuoso

**Hardware Courses:** Computer Architecture, Analog & Digital Electronics, Computer Hardware, Signal Processing

**Software Courses:** Operating Systems, Machine Learning, Embedded Programming, Object-Oriented Languages

**Math Courses:** Multivariable Calculus, Linear Algebra, Complex Analysis, Probability, Finance & Microeconomics

## EXPERIENCE

### Digital IC Design Engineer (PEY)

Incoming May 2026

*Marvell Technology*

*Toronto, ON*

- Will be responsible for block- and chip-level RTL design and verification for Marvell's 10 – 224 Gbps SerDes IP.

### Teaching Assistant

Sept 2025 – Dec 2025

*University of Toronto*

*Toronto, ON*

- Facilitating 40-student tutorials for **APS100 Orientation to Engineering**, expanding on lecture content.
- Leading discussions on engineering and ethics, becoming a well-rounded engineer, and CEAB accreditation.
- Providing mentorship on the transition to engineering studies, academic skills & strategies, and career pathways.

### FPGA Engineer Intern

May 2025 – Aug 2025

*Intelligent Sensory Microsystems Lab*

*Toronto, ON*

- Researching with Prof. Roman Genov's **ISML** group on novel CMOS-based time-of-flight imaging technologies.
- Achieved 800 Mbps sensor throughput by optimizing timing and implemented the SPI & I2C protocols in Verilog.
- Verification of sensor schematics on Cadence Virtuoso, ensuring that functional and timing requirements are met.

### Systems Design Engineer

Oct 2024 – Apr 2025

*University of Toronto Machine Intelligence Student Team*

*Toronto, ON*

- Developed a compute platform for UTMIST to schedule AI/ML jobs using GPU-accelerated cloud computing.
- Wrote a Python API to create teams and users, and to access various cloud platforms and check GPU availability.
- Worked with a team of compute developers to deploy the platform and establish a monthly feature release cycle.

## SELECTED PROJECTS

### Nios-V Sonar System |

- Integrated an ultrasonic sensor and servo motor into the FPGA-based Nios-V soft processor via GPIO ports.
- Designed & implemented BJT pull-up/pull-down networks for safe voltage conversion between FPGA and sensor.
- Implemented polling using machine timer, calculating distance between 20 cm to 2 m within 1 cm of precision.

### DE1-SoC Arcade Game |

- Developed a blackjack game on an FPGA, handling complex game states such as dealing, betting, and scoring.
- Simplified hardware peripheral control from top-level modules by writing API-like wrapper RTL over Altera IP.
- Fixed version compatibility issues in provided IP by writing a **Python script** to re-format memory files (.mif).

## ACTIVITIES & SOCIETIES

### Policies & Structures Committee Member

Jun 2025 – Present

*University of Toronto Engineering Society*

- Supporting EngSoc's legislative foundation and deliberating on policies impacting a 5000-strong student body.

### Sustainability Director

Apr 2024 – May 2025

*University of Toronto Engineering Society*

- Oversaw 5 initiatives and wrote a **Sustainability Policy** to support discourse/action on environmental matters.