

# Arnav Patil

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## EDUCATION

### University of Toronto

Sept 2023 – Apr 2028

*BASc. in Electrical and Computer Engineering with PEY Co-op*

*Toronto, Canada*

- **GPA: 3.60/4.00** with recognition on Dean's Honours List
- **Minor in Engineering Business / Economics**

## COURSEWORK

**Languages & Tools:** C/C++, Verilog/SystemVerilog, Python, Assembly, Quartus Prime, Vivado, Cadence Virtuoso

**Hardware Courses:** Computer Architecture, Analog & Digital Electronics, Computer Hardware, Signal Processing

**Software Courses:** Operating Systems, Computer Networks, Embedded Programming, Object-Oriented Languages

## EXPERIENCE

### Digital IC Design Intern

Incoming May 2026

*Marvell Technology*

*Toronto, Canada*

- Will be responsible for block- and chip-level RTL design and verification for Marvell's 10 – 224 Gbps SerDes IP.

### Teaching Assistant

Sept 2025 – Present

*Faculty of Applied Science & Engineering*

*Toronto, Canada*

- Facilitating 40-student tutorials for **APS100 Orientation to Engineering** and expanding on lecture content.
- Leading discussions on the transition to engineering studies, time-management strategies, and career pathways.

### FPGA Engineer Intern

Feb 2025 – Aug 2025

*Department of Electrical & Computer Engineering*

*Toronto, Canada*

- Researching with Prof. Roman Genov's **ISML** research group on CMOS-based depth-sensing imaging technology.
- Achieved 800 Mbps throughput by optimizing sensor IC timing, ideal for time-of-flight imaging applications.
- Implemented the SPI and I2C protocols in Verilog to interface with the integrated circuit and board peripherals.
- Verification of sensor schematics on Cadence Virtuoso, ensuring that functional and timing requirements are met.

### Systems Design Engineer

Sept 2024 – Apr 2025

*University of Toronto Machine Intelligence Student Team*

*Toronto, Canada*

- Developed a compute platform for UTMIST to optimize AI/ML jobs using GPU-accelerated cloud computing.
- Wrote an API to create teams and users, and to access various cloud platforms and check GPU availability.

## SELECTED PROJECTS

### Nios-V Sonar System | [Source Code](#)

- Integrated an ultrasonic sensor and servo motor into the FPGA-based Nios-V soft processor via GPIO ports.
- Designed & implemented BJT pull-up/pull-down networks for safe voltage conversion between FPGA and sensor.
- Implemented polling using machine timer, calculating distance between 20 cm to 2 m within 1 cm of precision.

### DE1-SoC Arcade Game | [Presentation Slides](#)

- Developed a blackjack game on an FPGA, handling complex game states such as dealing, betting, and scoring.
- Simplified hardware peripheral control from top-level modules by writing API-like wrapper RTL over Altera IP.
- Fixed compatibility issues in provided IP by writing a **Python script** to re-format memory initialization files.

## ACTIVITIES & SOCIETIES

### Policies and Structures Committee Member

Jun 2025 – Present

*University of Toronto Engineering Society*

- Supporting EngSoc's legislative foundation and deliberating on policies impacting a 5000-strong student body.

### Sustainability Director

Apr 2024 – May 2025

*University of Toronto Engineering Society*

- Oversaw 5 initiatives and wrote a **Sustainability Policy** to support discourse/action on environmental matters.