Arnav Patil

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Education

University of Toronto Sept 2023 – Apr 2027
BASc. in Electrical and Computer Engineering with PEY Co-op *Toronto, Canada*

- **GPA: 3.60/4.00** with recognition on Dean's Honours List
- **Minor in Engineering Business / Economics**
- **Awards:** UofT National Book Award, Alexander Rutherford Award, Royal Canadian Legion Medal of Excellence
- **Clubs:** Engineering Society, IEEE UofT Student Branch, Hart House Chess Club, UofT Machine Intelligence

Coursework

Languages: C/C++, **Verilog/SystemVerilog**, **RISC-V Assembly**, Python, Tcl, MATLAB, Simulink
Hardware Courses: Computer Architecture, Analog & Digital Electronics, Digital Logic, Signals & Systems
Software Courses: Operating Systems, Embedded Systems, Computer Networks, Data Structures & Algorithms
Math Courses: Multivariable Calculus, Linear Algebra, Complex Analysis, Probability, Microeconomics

Experience

Digital Design Intern Starts May 2026
Marvell Technology, Inc. *Toronto, Canada*

- Will be responsible for block- and chip-level RTL design and verification for Marvell's 10 - 224 Gbps SerDes IP.

Teaching Assistant Sept 2025 – Present
Faculty of Applied Science and Engineering *Toronto, Canada*

- **APS100 Orientation to Engineering:** transition to engineering studies, academic skills, and career pathways.

FPGA Research Intern Feb 2025 – Aug 2025
Department of Electrical and Computer Engineering *Toronto, Canada*

- Researching at Prof. Roman Genov's Intelligent Sensory Microsystems Lab with the CMOS Imaging Team.
- Achieved 800 Mbps throughput by optimizing sensor IC timing, ideal for time-of-flight imaging applications.
- Implemented the SPI and I2C protocols in Verilog to interface with the integrated circuit and board peripherals.
- Verification of 3 sensor designs on Cadence Virtuoso, ensuring that functionality and timing requirements are met.

Systems Design Engineer Sept 2024 – Apr 2025
University of Toronto Machine Intelligence Student Team *Toronto, Canada*

- Developed a compute platform for UTMIST to optimize AI/ML jobs using GPU accelerated cloud computing.
- Wrote an API to create teams and users, and to access various cloud platforms and check GPU availability.
- Worked with a team of developers to deploy the platform and established monthly feature release cycles.

Selected Projects

OptiRoute: A Low-Latency Wayfinder

- Developed algorithms and UI for an urban mapping system in modern C++ in a competitive design course.
- Implemented multithreading to process GiB-size databases while observing coherency, resulting in 2-5x speedup.
- Optimized algorithms for mathematical calculations and wayfinding (A* algorithm) to minimize cost on RAM.

Nios-V Sonar System | Source Code

- Integrated an ultrasonic sensor and servo motor into the FPGA-based Nios-V soft processor via GPIO ports.
- Designed & implemented BJT pull-up/pull-down networks for safe voltage conversion between FPGA and sensor.
- Implemented polling using machine timer, calculating distance between 20 cm to 2 m within 1 cm of precision.

DE1-SoC Blackjack Arcade Game | Presentation Slides

- Developed a blackjack game on an FPGA, handling complex game states such as dealing, betting, and scoring.
- Simplified hardware peripheral control from top-level modules by writing API-like wrapper RTL over Altera IP.
- Fixed compatibility issues in provided IP by writing a Python script to format memory initialization files (`.mif`).