

Arnav Patil

arnav.patil@mail.utoronto.ca | (587) 830-1203 | [linkedin.com/in/arnavpatil](https://www.linkedin.com/in/arnavpatil) | [arnav-patil-12.github.io](https://github.com/arnav-patil-12)

EDUCATION

University of Toronto

Sept 2023 – Apr 2027

BASc. in Electrical and Computer Engineering with PEY Co-Op

Toronto, ON

- **GPA: 3.60/4.00 with recognition on Dean's Honours List**
- **Extracurriculars:** UofT Engineering Society, IEEE UofT Student Branch, UofT Machine Intelligence Team

TECHNICAL SKILLS

Languages & Tools: **C/C++**, **RISC-V Assembly**, **Verilog**, **Python** (NumPy & pandas), MATLAB, Git, LaTeX

Hardware Courses: **Digital Systems**, **Computer Organization**, **Electronics**, Circuit Analysis

Software Courses: **Object-Oriented Programming**, Software Design, Computer Fundamentals

EXPERIENCE

FPGA Research Intern

Feb 2025 – Ongoing

Department of Electrical and Computer Engineering, University of Toronto

Toronto, ON

- Researching at **Prof. Roman Genov's Intelligent Sensory Microsystems Lab** with the **CMOS Imaging Team**.
- **Developing high-speed digital designs** for next-gen 3D imaging, blending hardware & signal processing.
- **FPGA-controlled laser modulation** and real-time synchronization for **Epipolar Time-of-Flight** imaging.

ML Compute Platform Developer

Sept 2024 – Ongoing

University of Toronto Machine Intelligence Student Team

Toronto, ON

- Developing a compute platform for UTMIST to optimize ML jobs using **GPU accelerated cloud computing**.
- Working with a team of developers to **deploy the platform** and establish **monthly feature release cycles**.

SELECTED PROJECTS

NIOS-V Sonar System on an FPGA | [GitHub Repository](#)

- Integrated ultrasonic sensor and servo motor into the FPGA-based NIOS-V soft processor via **GPIO ports**.
- Designed & implemented **BJT pull-up/pull-down networks** for safe 3.3V-to-5V signal interfacing on FPGA.
- Engineered **time-sensitive sensor polling using machine timer**, avoiding interrupts for timing precision.

Blackjack Implementation on an FPGA | [Winner Winner Chicken Dinner!](#)

- Developed a digital blackjack game using finite state machines (FSMs) on a DE1-SoC FPGA, handling **complex game states** such as dealing, betting, and scoring in real-time to **simulate card-counting experience**.
- Wrote a [Python script](#) to reformat memory initialization files, **fixing compatibility issues between provided legacy tools and modern IP cores**.

Personal Website | [Personal Portfolio Website](#)

- Customized a Hugo theme to **create a static portfolio website**, showcasing coursework and achievements.
- Deployed the site on GitHub Pages using a **continuous development pipeline** integrated into the repository through **GitHub Actions**, which automatically rebuilds and redeploys the site after each push.
- Integrated **Google Analytics 4** into the site to track insights and analyze which course pages are most popular.

EXTRACURRICULAR ACTIVITIES

Sustainability Director

Apr 2024 – Ongoing

University of Toronto Engineering Society

Toronto, ON

- **Oversaw 7+ projects**, from launching a **Sustainability Policy** to divesting clubs from fossil fuel sponsors.
- **Organized** a research team to conduct a study of the Engineering Society's and Faculty's historical and present carbon footprint and practices, and collecting student voices for sustainability in the curriculum.

First Year Engineering Class Representative

Sept 2023 – Sept 2024

University of Toronto Engineering Society

Toronto, ON

- Represented **70+ students** as a liaison between students, the Engineering Society, and the Faculty.
- Collaborating with EngSoc & Faculty members such as the Vice-President Academic, Vice-Dean First Year, and groups of professors to develop solutions enhancing **more than 1400 first-year students'** academic experience.