# Arnav Patil

arnav.patil@mail.utoronto.ca | (587) 830–1203 | linkedin.com/in/arnavpatil | arnav-patil-12.github.io

## Education

**University of Toronto** Sept 2023 – Apr 2027
*BASc. in Electrical and Computer Engineering + PEY Co-Op* *Toronto, Canada*

- **GPA: 3.60/4.00** with recognition on Dean's Honours List
- **Minor in Engineering Business**
- **Awards:** UofT National Book Award, Alexander Rutherford Award, Royal Canadian Legion Medal of Excellence

## Selected Courses

**Languages: C/C++**, **Verilog**, **RISC-V Assembly**, Python, MATLAB, Git, LaTeX
**Hardware Courses:** Computer Architecture, Digital Systems, Analog & Digital Electronics, Signals & Systems
**Software Courses:** Operating Systems, Embedded Programming, Data Structures & Algorithms
**Math Courses:** Microeconomics, Probability, Multivariable Calculus, Linear Algebra, Complex Analysis

## Experience

**Teaching Assistant** Sept 2025 – Present
*Faculty of Applied Science & Engineering* *Toronto, Canada*

- **APS100 Orientation to Engineering:** transition to engineering studies, academic skills, and career pathways.

**FPGA Research Intern** Feb 2025 – Present
*Department of Electrical & Computer Engineering* *Toronto, Canada*

- Researching at **Prof. Roman Genov's** Intelligent Sensory Microsystems Lab with the **CMOS Imaging Team**.
- Implementing the SPI and I2C protocols in Verilog to interface with board peripherals and the integrated circuit.
- Verification of image sensor ICs on Cadence Virtuoso, ensuring functionality and performance for three designs.

**ML Compute Platform Developer** Sept 2024 – Apr 2025
*University of Toronto Machine Intelligence Student Team* *Toronto, Canada*

- Developed a compute platform for UTMIST to optimize ML jobs using GPU accelerated cloud computing.
- Wrote an API to create teams and users, and to access various cloud platforms and check GPU availability.
- Worked with a team of developers to deploy the platform and establish monthly feature release cycles.

## Projects

**NIOS-V Sonar System on an FPGA** | Source Code Repository

- Integrated ultrasonic sensor and servo motor into the FPGA-based NIOS-V soft processor via GPIO ports.
- Designed & implemented BJT pull-up/pull-down networks for safe 3.3V-to-5V signal interfacing on FPGA.
- Engineered time-sensitive sensor polling using machine timer, avoiding interrupts for timing precision.

**Blackjack Arcade Game on an FPGA** | Presentation Slides

- Developed a digital blackjack game using finite state machines (FSMs) on a DE1-SoC FPGA, handling complex game states such as dealing, betting, and scoring in real-time to simulate card-counting experience.
- Wrote a Python script to reformat memory initialization files (.mif), fixing compatibility issues in provided IP.

## Extracurricular Activities

**Member, Policies & Structures Committee** Jun 2025 – Present
*University of Toronto Engineering Society*

- Supporting EngSoc's legislative foundation and deliberating on policies impacting a 5000+ strong student body.

**Sustainability Director** Apr 2024 – May 2025
*University of Toronto Engineering Society*

- Oversaw 5 initiatives, and wrote a Sustainability Policy to support discourse and action on environmental matters.