ECE 3337

Electronic Circuits

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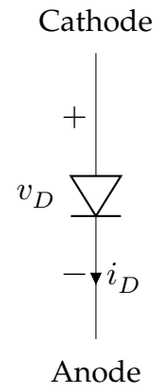
1 Introduction & Review

This course deals with analysis and design of electronic circuits, to understand the basics of this course, we will need to learn to analyze basic transistor and diode circuits, this will be reviewed below.

1.1 The Diode

A **diode** is shown in the circuit below.



An ideal diode acts as a one-way current path that only allows flow from cathode to anode.

- When $v_D > 0$ the diode acts as a **short-circuit** and is said to be **forward-biased**
- When $v_D < 0$ the diode acts as an **open-circuit** and is said to be **reverse-biased**

The **diode voltage,** v_D is defined as the voltage from anode to cathode:

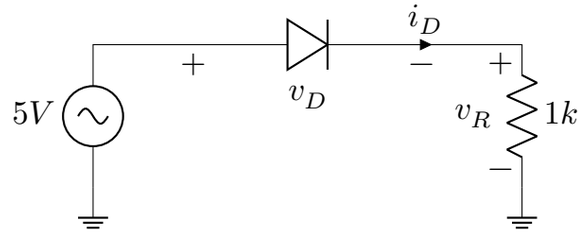
$$v_D = v_{\text{cathode}} - v_{\text{anode}}$$

1.1.1 The Constant Voltage-Drop Model

Diodes are **non-linear** elements, they actually follow an exponential i-v curve, but this makes manual analysis next to impossible, so in order to analyze circuits with diodes, we introduce the **constant voltage-drop model** where we assume that the diode voltage v_D has a fixed value if the diode is forward-biased, usually this value is assumed to be 0.7 V. This means that

- When $v_D > 0.7$ the diode is forward-biased
- When $v_D < 0.7$ the diode is reverse-biased

Lets deal with a simple example using this model, lets find v_R in the circuit below



In order to solve diode circuits, we must follow the steps below:

1. Make a guess for each diode's biasing (forward, reverse)
2. Analyze the circuit as if the guesses are correct
3. Validate the guesses to see if they are correct based on the biasing conditions

For this circuit lets assume that the diode is forward-biased and write KVL

$$
\begin{aligned}
v_{\text{src}} &= v_D + v_R \\
v_{\text{src}} &= v_D + 1k(i_D) \\
v_{\text{src}} - v_D &= 1k(i_D) \\
i_D = \frac{v_{\text{src}} - v_D}{1k} &= \frac{5 - 0.7}{1k} = 4.3\text{mA}
\end{aligned}
$$

In this case, when guessing that our diode is forward-biased, our $i_D > 0$, so our guess was correct. And the circuit operates as we guessed with 4.3 mA flowing through it If we assume that the diode is reverse-biased, we must validate that $v_D < 0.7$

1.1.2 Biasing & Non-Linear Elements

Since we are often dealing with non-linear elements in this course, a big part is modelling how they respond to **small signals** Since the i-v curve of a diode is exponential we must essentially find the point on the i-v curve where the diode is operating, this point is called a **biasing-point** or **bias**

Once we find this point, we can assume local-linearity of the i-v curve for a small enough signal.

1.1.3 The Small Signal Model

In order to find out how we can model diodes with small signal fluctuations we must derive it ourselves the exponential model of a diode can be written below.

$$i_D = I_s \left[\exp\left(\frac{v_D}{V_T}\right) - 1 \right]$$

Now lets suppose we add some fluctuations in the voltage and current Δv_D and Δi_D respectively

$$i_D + \Delta i_D = I_s \left[\exp\left(\frac{v_D + \Delta v_D}{V_T}\right) - 1 \right]$$

Lets also ignore the 1 term since it can be insignificant for sufficiently large values of v_D

$$i_D + \Delta i_D = I_s \left[\exp\left(\frac{v_D + \Delta v_D}{V_T}\right) \right]$$

$$i_D + \Delta i_D = I_s \exp\left(\frac{v_D}{V_T}\right) \exp\left(\frac{\Delta v_D}{V_T}\right)$$

if Δv_D is small we can use the fourier-series exapansion to approximate it: $\exp(x) = 1 + x$

$$i_D + \Delta i_D = I_s \exp\left(\frac{v_D}{V_T}\right)\left[1 + \frac{\Delta v_D}{V_T}\right]$$

$$i_D + \Delta i_D = I_s \exp\left(\frac{v_D}{V_T}\right) + \Delta v_D \cdot \frac{I_s \exp\left(\frac{v_D}{V_T}\right)}{V_T}$$

With our approximation from earlier we can sub in i_D to get the following

$$i_D + \Delta i_D = i_D + \frac{i_D}{V_T} \cdot \Delta v_D$$

This means that

$$\Delta i_D = \frac{i_D}{V_T} \cdot \Delta v_D$$

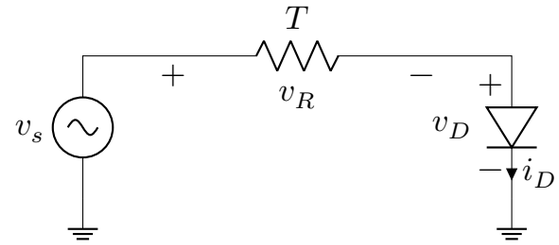
Giving us a simple linear small-signal model of a resistor, so during ac-analysis we can swap out our forward-biased diodes for resistors of value r_D

$$r_D = \frac{V_T}{i_D}$$

1.1.4 Small Signal Model: Example

Now lets do an example, where we need to find the diode voltage v_D

- $v_s = 10 + \sin \omega t$ V
- $R = 10$ k
- $V_T = 25$ mV



As always we start with DC analysis to find the bias point of the diode.

Assume diode is forward-biased:

$$v_s = v_R + v_D$$

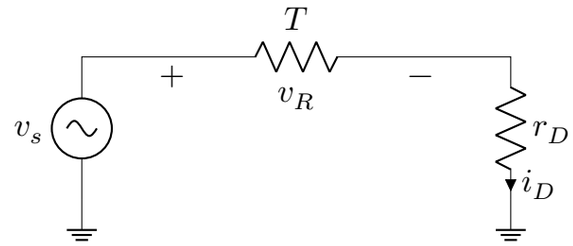
$$v_s = R(i_D) + 0.7$$

$$i_D = \frac{v_s - 0.7}{R} = \frac{10 - 0.7}{10k} = 0.93\text{mA}$$

So our guess was correct since $i_D > 0$, this gives a bias-point of $(0.7\text{V}, 0.93\text{mA})$

Now lets look at the AC part, with the small signal model, replacing the diode with the resistor

$$r_D = \frac{V_T}{i_D} = \frac{25mV}{0.93mA} = 27\Omega$$



This gives the AC part of our v_D as

$$v_D = \left(\frac{r_D}{r_D + R}\right) \cdot v_s$$

$$v_D = \left(\frac{27}{27 + 10k}\right) \cdot \sin \omega t = 2.7m \cdot \sin \omega t \text{V}$$

In order for the small signal model to be accurate we require that the small signal voltage fulctuation $v_D < V_T$ Here $2.7mV < 25mV$ so this is quite accurate of an approximation.

All in all our complete $v_D(t)$ becomes the sum of the DC and AC points:

$$v_D(t) = 0.7 + 2.7\text{m} \cdot \sin \omega t \text{ V}$$

1.1.5 The Flowchart for Diode Analysis

Now with a bunch under our belt we can create a basic flowchart for diode circuit analysis

1. DC Analysis, make assumptions for each diode's operating mode
2. Validate the assumptions
    1. Forward-Biased $\rightarrow i_D > 0$
    2. Reverse-Biased $\rightarrow v_D < 0.7$
3. Find small-signal resistance $r_D = \frac{V_T}{i_D}$

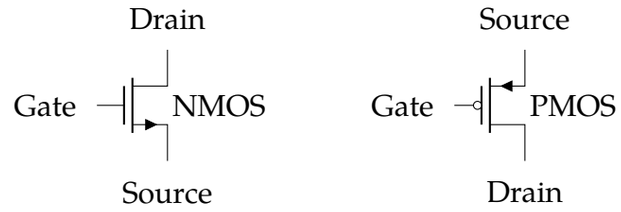
4. AC analysis, replcae forward biased diodes with a resistor r_D and reverse-biased with open circuits
5. Combine DC and AC analysis answers for the total voltages

1.2 Transistors

A **transistor** is a three terminal device. At a high-level it functions as an electrically controlled switch. There are many flavours of transistors but the most basic ones are the **MOSFET** and the **BJT**. MOSFET is an acronym for Metal Oxide Semiconductor Field-Effect Transistor, BJT is an acronym for Bipolar Junction Transistor. This chapter will cover the basics of each device, and basic circuit analysis with them.

1.2.1 The MOSFET

The MOSFET is a type of transistor, and it features three terminals. The **Gate** G, **Source** S, and **Drain** D. It also comes in two flavours NMOS and PMOS, the circuit symbols for each are shown below, with their terminals labelled



An easy way to differ the two is to use the arrow, the arrow always denotes the Source terminal, and the N in NMOS means "Not pointing inwards".

The Gate essentially acts as the transistors control input, The N and P in PMOS and NMOS signify the logic level required to close the switch, This means the following:

- NMOS transistors are "turned-on" when their gate voltage v_G is high
- PMOS transistors are "turned-on" when their gate voltage v_G is low

In reality its a little more complicated, but this makes it easy to remember which is which.

1.2.2 Operating Regions of a FET

Unsurprisingly FETs are also non-linear devices, and they actually have a very similar approach to diodes for circuit analysis. We first make an assumption about the operating region of the device, these three regions, **Cutoff** , **Triode** , and **Saturation** will be introduced now.

Note that for NMOS, v_{th} is a positive value, and it is a negative value for PMOS, this is why we have the flipped sign convention here.

Operating Region	Conditions (NMOS)	Conditions (PMOS)	Drain Current (i_D)
Cutoff	$v_{GS} < v_{th}$	$v_{GS} > v_{th}$	$i_D = 0$
Triode	$v_{GS} > v_{th}$ and $0 \leq v_{DS} \leq v_{GS} - v_{th}$	$v_{GS} < v_{th}$ and $0 \geq v_{DS} \geq v_{GS} - v_{th}$	$i_D = k\left[(v_{GS} - v_{th})v_{DS} - \frac{1}{2}(v_{DS})^2\right]$
Saturation	$v_{GS} > v_{th}$ and $v_{DS} > v_{GS} - v_{th}$	$v_{GS} < v_{th}$ and $v_{DS} < v_{GS} - v_{th}$	$i_D = \frac{1}{2}k(v_{GS} - v_{th})^2$

In the table above, the value k is a predefined quantity in units of $\frac{\text{A}}{\text{V}^2}$ There is also another thing, the drain current i_D should always be positive in Triode or Saturation Regions, this means that in NMOS current flows *out* of the source, and flows *into* the source for PMOS.

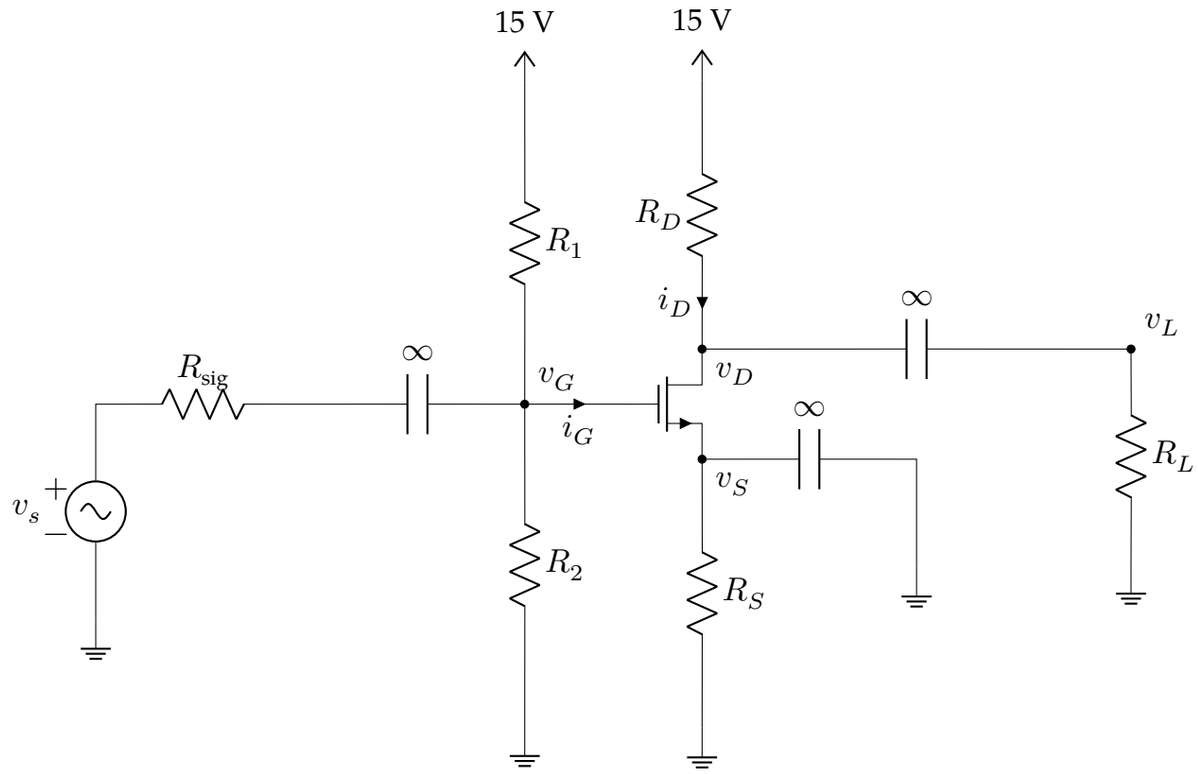
Note that the gate of a FET does not accept any current, in other words $i_G = 0$ in every region above. When designing electronic amplifiers, we often want to bias our FETs in the saturation region.

1.2.3 DC Analysis of a FET

Lets start with a quick example of DC analysis with a NMOS amplifier, for this problem we will assume the following

- $k = 2\ \frac{\text{mA}}{\text{V}^2}$
- $V_A = 100$ V
- $v_{th} = 1$ V
- $R_1 = 10$M
- $R_2 = 5$M
- $R_D = 7.5$k
- $R_S = 3$k

- R_L = 10k



Lets start by finding the gate voltage, since $i_G = 0$ it acts as a voltage divider, we can formulate a simple expression for it. Note that we can ignore everything on the other side of the infinite capactiors, as they will block all DC signals, these capacitors will come into play when we go through AC analysis

$$v_G = \frac{R_2}{R_1 + R_2} \cdot (15) = 5\text{V}$$

We can also find the source voltage if we know the drain current

$$v_S = R_s i_D = 3(i_D)$$

This means that our gate-source voltage v_{GS} can be found as follows:

$$v_{GS} = v_G - v_S = \frac{R_2}{R_1 + R_2} \cdot (15) - R_s i_D = 5 - 3(i_D)$$

Lets assume saturation and use the drain-current equation from the table above, plugging in $k = 2$ here as well:

$$i_D = \frac{1}{2} k (v_{GS} - v_{th})^2 = (5 - 3(i_D) - 1)^2$$

$$0 = 16 - 25(i_D) + 9(i_D)^2$$

Solving this gives two solutions:

- $i_D = 1$ mA
- $i_D = 1.78$ mA

Now we must use the conditions from the table above to see which is correct. Lets quickly rewrite the terminal voltage relations:

- $v_G = 5$
- $v_S = 3(i_D)$
- $v_D = 15 - 7.5(i_D)$

We must choose an answer that satifies the following

- $v_{GS} > v_{th}$
- $v_{DS} > v_{GS} - v_{th}$

The correct answer here is $i_D = 1$ mA as the other answer doesnt satisfy both inequalities above.

This means that we have found the DC Biasing point of our MOSFET, and since our conditions are both satisfied with $i_D = 1mA$ we are certain that our initial guess of the operating region is correct.

1.2.4 Small Signal Models of a MOSFET

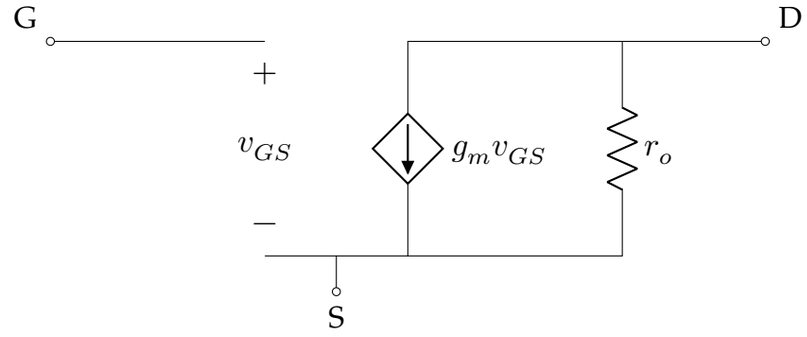
There are two versions of the small-signal model of a MOSFET, the **pi-model** and the **T-model**. Both are equivalent, but analysis might be easier with one rather than another.

These models require two parameters for full use with the early-effect resistance r_o, in problems where we neglect it, we can replace this resistor with an open-circuit:

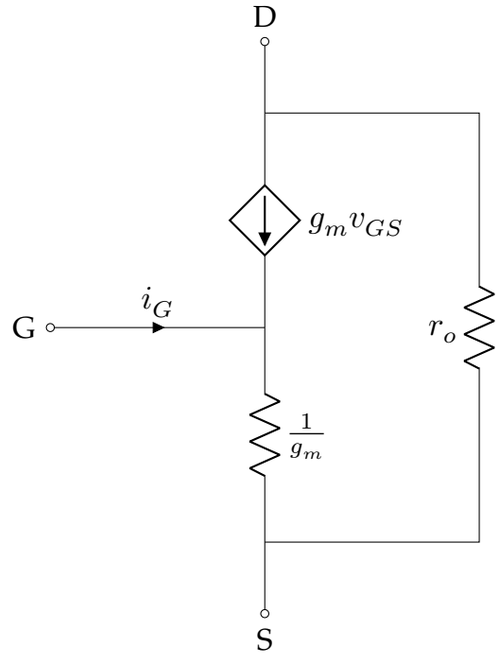
$$g_m = \frac{2i_D}{v_{GS} - v_{th}}$$

$$r_o = \frac{V_A}{i_D}$$

The Pi Model is shown below



The T-model is also shown here:



1.2.5 Example: Small Signal Operation of a MOSFET

Lets continue our previous example, extending it to include small signal operation. Recall that we found the following bias point after DC analysis

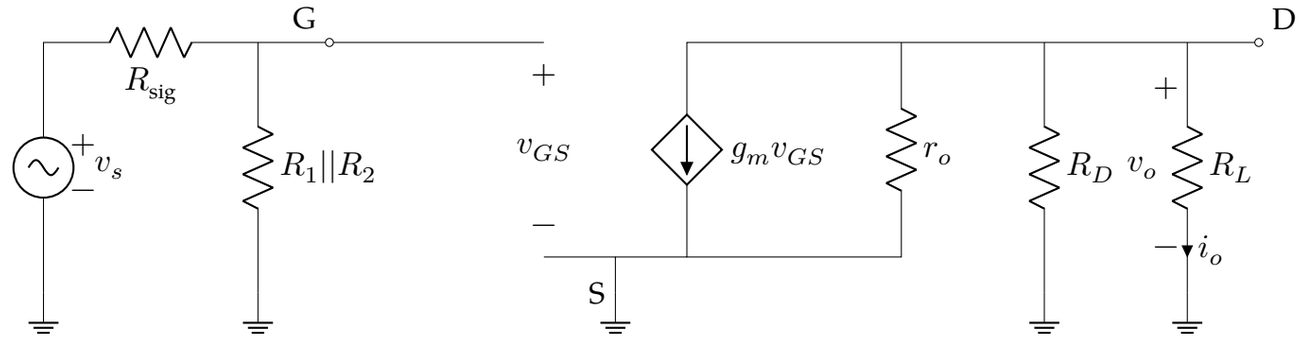
- $i_D = 1$ mA
- $v_{GS} = 2$ V

We always start by finding the small signal parameters g_m and r_o

$$g_m = \frac{2i_D}{v_{GS} - v_{th}} = \frac{2m}{2-1} = 2\frac{\text{mA}}{\text{V}}$$

$$r_o = \frac{V_A}{i_D} = \frac{100}{1m} = 100k\Omega$$

Now we can use either model to analyze the circuit during AC fluctuations, this involves replacing all caps with short-circuits. We will be using the π-model for this example



Now lets start by finding in input and output resistance R_{in} and R_{out} Usually there are arrows to denote where each starts from, in this case our input resistance starts from after R_{sig} and our output resistance starts before R_L.

This gives

$$R_{\text{in}} = R_1||R_2$$
$$R_{\text{out}} = r_o||R_D$$

Next lets find the signal-voltage to gate-source voltage ratio, this is a simple voltage divider

$$v_{GS} = \frac{R_1||R_2}{R_1||R_2 + R_{\text{sig}}} \cdot v_s = \frac{R_{\text{in}}}{R_{\text{in}} + R_{\text{sig}}} \cdot v_s$$

$$\frac{v_{GS}}{v_s} = \frac{R_{\text{in}}}{R_{\text{in}} + R_{\text{sig}}}$$

Next lets fine the output voltage (voltage across R_L) to gate-source voltage ratio, We know that we can group the three resistors into one, and thus the current flowing through all three must add up to $g_m v_{GS}$ This gives us our expression

$$v_o = 0 - i_D \cdot (r_o || R_D || R_L) = -g_m v_{GS} \cdot (r_o || R_D || R_L)$$
$$\frac{v_o}{v_{GS}} = -g_m \left(r_o || R_D || R_L\right)$$

Altogether we can find the total signal to output voltage gain, by combining the gains of both stages above. This gives us the total-ac-gain of the amplifier.

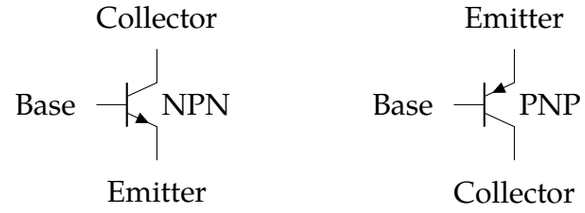
$$\frac{v_o}{v_s} = \frac{v_o}{v_{GS}} \cdot \frac{v_{GS}}{v_s} = -g_m \left(r_o || R_D || R_L\right) \cdot \frac{R_{\text{in}}}{R_{\text{in}} + R_{\text{sig}}}$$

1.2.6 The BJT

The BJT is the other type of transistor, it functionals similarly to the MOSFET, except that it a current-controlled switch, it also has different terminal names.

- The **Base, B** of a BJT acts like the Gate of a MOSFET
- The **Collector, C** of a BJT acts like the Drain of a MOSFET
- The **Emitter, E** of a BJT acts like the Source of a MOSFET

The BJT also comes in two flavours (NPN, and PNP). The circuit symbols for each is shown below. Note that the terminal with the arrow is always the Emitter, and NPN can be distinguished by remebering it means that the arrow is "not-poiting inwards"



Also note that the base actually accepts a current this time, the base-current i_B flows into the base for NPN, and out of the base for PNP BJTs, such that the below is always held true

$$i_B + i_C = i_E$$

1.2.7 Operating Regions of a BJT

Like with MOSFETS, the BJT is also a non-linear device. The BJT is literally made up of two diodes, so the operating region depends on the biasing of the **Emitter-Base Junction (EBJ)** abd the **Collector-Base Junction (CBJ)** . A short table is provided below

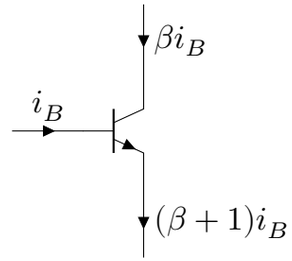
Operating Region	CBJ Biasing	EBJ Biasing
Cutoff	Reverse	Reverse
Active	Reverse	Forward
Reverse-Active	Forward	Reverse
Saturation	Active	Active

Note that the Active region for BJT is the desired region for amplifiers, the saturation mode in BJTs is not similar to the saturation region for MOSFETs Now we can take a look at the characteristics and conditions for each state above

Operating Region	Condition (NPN)	Condition (PNP)	Current Flow
Cutoff	$v_E > v_B$ and $v_C > v_B$	$v_B > v_E$ and $v_B > v_C$	$i_C = \beta i_B$ and $i_C = \frac{\beta}{1+\beta} i_E$
Active	$v_E < v_B < v_C$	$v_E > v_B > v_C$	
Reverse-Active	$v_E > v_B > v_C$	$v_E < v_B < v_C$	
Saturation	$v_B > v_E$ and $v_B > v_C$	$v_E > v_B$ and $v_C > v_B$	

1.2.8 Current Rules of a BJT

Since the base of a BJT permits current flow, often the voltage divider at the base is now actually a current divider, this is easy to deal with by replacing it with a thevenin equivalent and contininuing the DC analysis. The current relation rules of a BJT in active mode is not easy to remember though, below is a short schematic representation of the equations



$$i_E = i_B + i_C \tag{1}$$

$$i_C = \beta i_B \tag{2}$$

2 Frequency Response

2.1 Amplifier Behaviour

2.1.1 Transfer Function of a Transistor Amplifier

The typical transfer function of an amplifier has **band-pass** characteristic, This means that the **transfer function** $H(s)$ can be represented as a aggregation as shown below:

$$H(s) = A_M \cdot F_L(s) \cdot F_H(s)$$

Where,

- A_M is the midband-gain of the amplifier (found through DC + small signal analysis assuming caps are shorts)
- $F_L(s)$ is the lower-band behaviour (typically high-pass)
- $F_H(s)$ is the higher-band behaviour (typically low-pass)

We should also note that since this is a band-pass, there are both an upper and lower cutoff (3 dB) frequency.

- The **lower 3 dB frequency** is f_L, it is present in $F_L(s)$
- The **upper 3 dB frequency** is f_H, it is present in $F_H(s)$

The region left of f_L is called the **lower-band**, and the region right of f_H is called the **higher-band**, lastly the region in between is called the **mid-band**. At the midband, the transfer functions F_L and F_H approach unity, giving the midband-gain of A_M.

The span of the mid-band is said to be the **bandwidth, ψ** of the amplifier, and it can be found with

$$\psi = |f_H - f_L|$$

Often in these amplifier designs, one can introduce a trade-off between gain and bandwidth. So to measure the quality of an amplifier we introduce the **gain-bandwidth product GBW** Which is the midband-gain multiplied by the bandwidth

$$\text{GBW} = \psi \cdot |A_M|$$

2.1.2 Low, Middle, and High Frequency Analaysis

In order to find this midband-gain A_M we analyze the amplifier equivalent small-signal circuit, with the assumptions that the coupling and bypass capacitors act as perfect short circuits, and that the internal parasitic capacitances of the transistor are acting as perfect open circuits.

For finding the low-frequency behaviour F_L the overall behaviour can be approximated as $H_L(s) \approx H(s)$ shown below, due to the negligible impact of F_H

$$H_L(s) = A_M F_L(s)$$

Analysis of lower-band behaviour we must take into account only the non-parasitic capacitances, as these will have a non-negligible higher-impedance at lower frequencies, But we can still assume that the internal parastic capactances are still treated as perfect open-circuits.

For the high-frequency behaviour, once again we can approximate it as $H_H(s) \approx H(s)$

$$H_H(s) = A_M F_H(s)$$

Here we must take into account the internal parasitic capacitances, as they are now no-longer negligible. However every other capacitor can be treated ass a perfect short-circuit

2.1.3 The Short Circuit Time Constant Method

This method is a simpler way of finding the approximate behaviour through finding the dominant pole, $\omega_L = 2\pi f_L$ of F_L. It works by approximating it as below. From here onwards This method will be referred to as SC-τ

Note: This method works best with real poles, not with complex-conjugate poles, Here we only have RC circuits, which all have real-poles

$$F_L(s) \approx \frac{s}{s + \omega_L}$$

To estimate the dominant-pole, we analyze the low-frequency equivalent circuit (parastic caps are open, all other caps remain) and analyze each capacitor one at a time, setting all other capacitors to short-circuits. While analyzing each capacitor we must determine the resistance it sees in total on either side, and add both sides up.

$$R_{\text{cap}} = R_{\text{LHS}} + R_{\text{RHS}}$$

Doing this for each capacitor, we can find each capacitor's time constant

$$\tau = \frac{1}{RC}$$

Then we can add all of the time constants up, to obtain an approximation of ω_L

$$F_L(s) = \frac{s}{s + \omega_L}$$

Where,

$$\omega_L = \sum_i \tau_i = \sum_i \frac{1}{R_{C_i} C_i}$$

2.1.4 The Open Circuit Time Constant Method

Similarly to SC-τ, we can use the Open circuit alternative to determine behaviour at high-frequency, once again we approximate F_H here through the dominant pole $\omega_H = 2\pi f_H$ This method also only works best with purely real poles. Going forward this method will be referred to as OC-τ

$$F_H(s) \approx \frac{1}{1 + \frac{s}{\omega_H}}$$

To estimate the dominant-pole we analyze the high-frequency circuit (parastic caps present, other caps are all shorts) and do the exact same thing as in SC-τ. We find each capacitors time-constant

$$\tau = \frac{1}{RC}$$

But note that we have a reciprocal term in our approximate transfer function here, so we must add the reciprocals of the time-constants in this case to obtain an approximation of ω_H

$$F_H(s) = \frac{1}{1 + \frac{s}{\omega_H}}$$

Where,

$$\omega_H = \sum_i \frac{1}{\tau_i} = \sum_i R_{C_i} C_i$$

MOS BJT (1Q, or 2Q)

DC analysis + small signal model (Rin Rout, gains, fH fL,)