CS M152A - Introduction to Digital Design Lab

Project 4: Finite State Machine Design - Vending Machine

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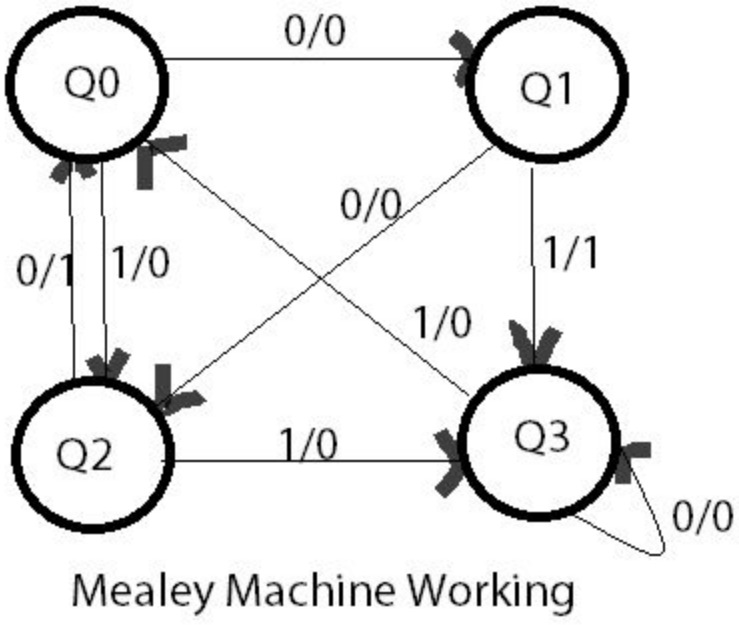
Introduction and Background:

The main goal of this lab is to build and simulate a finite state machine (FSM). Specifically, it requires us to design an FSM representing a vending machine that matches a certain specified behavior, and then run through simulations of the vending machine. This lab is only based on simulation - it does not use an FPGA.

Finite State Machines (FSMs) are particularly helpful in modeling sequential circuits since they can show transitions between the initial state, intermediate states, and finite states. These transitions are defined based on different inputs and the current state. Therefore, it may be the case that not every state is reachable from each other. I personally find that drawing out FSM diagrams resembles a Directed Acyclic Graph (DAG) in computer science, except that any possible “weights” on the edges are replaced with permissible inputs and corresponding outputs. It provides a very systematic way of observing a flow of actions through the network, which ensures that all cases are accounted for.

In particular, there are two types of FSMs - Moore Machines and Mealy Machines. Moore machines are those where the next state is only dependent on the current state. Mealy Machines are more complex - the next state is dependent on the current inputs as well as the current state. Given the nature of required interactions, designing the vending machine indicates that we need a Mealy Machine.

Example of a Mealy Machine FSM Diagram



In the example Mealy Machine above, there are 4 possible states one binary input.

Design Description:

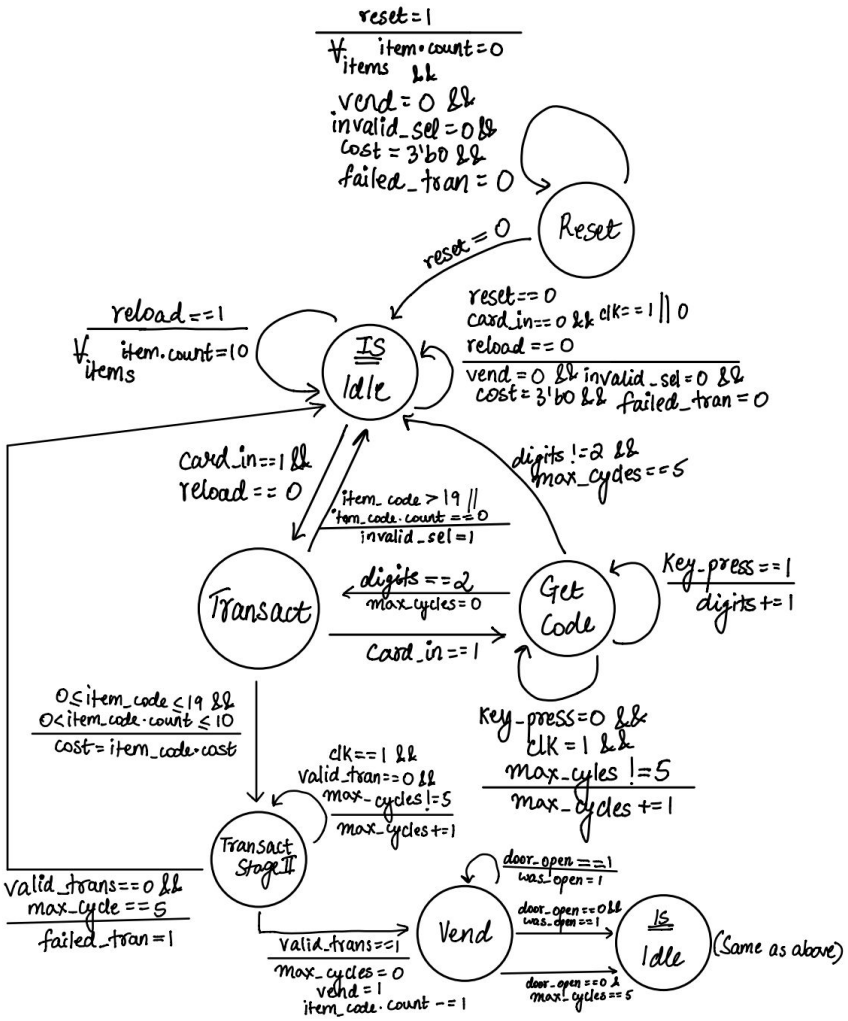
For the vending_machine.v top-level module that needs to be designed, the table below lists the various inputs and outputs.

INPUT	SIZE/ BEHAVIOR
CLK	1 bit. System clock (T= 10 ns)
RESET	1 bit. Set all item counters,outputs to 0 and go to the idle state.
RELOAD	1 bit. Reload the machine (set all item counters to 10)
CARD_IN	1 bit. Stays high as long as the card remains inserted.
ITEM_CODE <3:0>	4-bit signal to input item code. The 2 digit item code is entered one digit at a time. Must be entered while the card is inserted.
KEY_PRESS	1 bit. ITEM_CODE is valid for read when this signal is high.
VALID_TRAN	1 bit. HIGH = transaction using the inserted card is valid (can go high any time after item selection is determined to be valid)
DOOR_OPEN	1 bit. HIGH = The vending machine door is open (This can occur any time after the 'VEND' goes high.)

OUTPUTS:

OUTPUT	SIZE/BEHAVIOR
VEND	1 bit. Set to HIGH once the transaction is deemed to be valid. Set to LOW once DOOR_OPEN goes high and then low/ or if the door does not open in 5 clock cycles.
INVALID_SEL	1 bit. Set to HIGH if: 1. Only 1 digit of ITEM_CODE is entered and there is no 2nd digit after 5 clock cycles 2. The 2 digit ITEM_CODE is invalid (Ex. 23) 3. The counter for one of the items is 0.
COST<2:0>	3 bits. Set to 000 by default. Set to the cost of an item once item code is entered, and remains at this value until a new transaction begins. (Ex. $5 = 101)
FAILED_TRAN	1 bit. Set to 1 if VALID_TRAN signal does not go high within 5 clock cycles of determining the ITEM_CODE

Based on this spec, below is an attached version of my FSM diagram. However, this changed quite a bit during the process of implementation - however, it still provides a high level idea of how all of these aspects are interconnected.



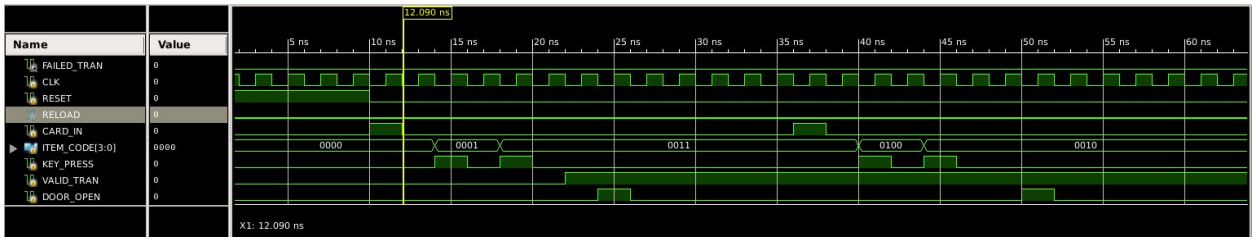
I am purposely choosing not to attach a picture of the semantics because there was nothing interesting to see beyond the same schematic diagram provided in the spec for this lab.

The basic intuition behind my code is that it has 11 states - idle, reload, vending, etc. as well as 6 states to represent the 6 sets snack items based on their cost in the vending machines. Items with the same cost have been treated the same way in the vending machine - the only thing that's independent for both of them is their cost as well as their counts.

The design overall has 4 always blocks mapping to an always block to update current state, next_state, outputs as well as the actual counter. Each of them handles different parts of hte program itself - results in a separation of concerns.

During reset, all outputs are set to 0. For reload, all counts are set to 10. Fruther details are provided in the video itself and in the table above.

Simulation:




```
ISim P.20131013 (signature 0xfbc00daa)
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
Vend=0, Cost=0, Invalid_sel=0, Failed_tran=0
Vend=1, Cost=4, Invalid_sel=0, Failed_tran=0
ISim>
```

In particular, two simulations were tried. The first was a regular item by selecting item 13. The output, as observed in from both the waveforms and the output console indicate that the transaction was successful - Vend is 1 and Cost is 4, with no failures during the transaction. The simulation waveforms also indicate that KEY_PRESS is only set to high when an ITEM_CODE is being passed in, and that VALID_TRAN is set to 1 after VEND state has been entered. DOOR_OPEN increases to 1 and goes back to 0 to indicate taking out an item, after which the simulation returns to the IDLE state.

The second simulation that was attempted was that of an invalid transaction where an incorrect ITEM_CODE was passed in - in particular, the item code selected was 42, which is >19. The waveforms do indicate that 4 was selected first and 2 was selected second. However, this transaction does fail as expected, and INVALID_SEL is set to 1 as expected.

One bug that I found is that the behavior can often be a bit unpredictable, which is because I use a combination of sequential and combinational logic - I didn't just stick to one. However, I kept running into an array of errors while trying to stick to one, therefore I let this be.

// Synthesis Report

```
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  1) Synthesis Options Summary
  2) HDL Parsing
  3) HDL Elaboration
  4) HDL Synthesis
       4.1) HDL Synthesis Report
  5) Advanced HDL Synthesis
       5.1) Advanced HDL Synthesis Report
  6) Low Level Synthesis
  7) Partition Report
  8) Design Summary
       8.1) Primitive and Black Box Usage
       8.2) Device utilization summary
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8.3) Partition Resource Summary
8.4) Timing Report
     8.4.1) Clock Information
     8.4.2) Asynchronous Control Signals Information
     8.4.3) Timing Summary
     8.4.4) Timing Details
     8.4.5) Cross Clock Domains Report

```
=========================================================================
*                     Synthesis Options Summary                         *
=========================================================================
---- Source Parameters
Input File Name                    : "vending_machine.prj"
Ignore Synthesis Constraint File   : NO

---- Target Parameters
Output File Name                   : "vending_machine"
Output Format                      : NGC
Target Device                      : xc7a100t-3-csg324

---- Source Options
Top Module Name                    : vending_machine
Automatic FSM Extraction           : YES
FSM Encoding Algorithm             : Auto
Safe Implementation                : No
FSM Style                          : LUT
RAM Extraction                     : Yes
RAM Style                          : Auto
ROM Extraction                     : Yes
Shift Register Extraction          : YES
ROM Style                          : Auto
Resource Sharing                   : YES
Asynchronous To Synchronous        : NO
Shift Register Minimum Size        : 2
Use DSP Block                      : Auto
Automatic Register Balancing       : No

---- Target Options
LUT Combining                      : Auto
Reduce Control Sets                : Auto
Add IO Buffers                     : YES
Global Maximum Fanout              : 100000
Add Generic Clock Buffer(BUFG)     : 32
Register Duplication               : YES
Optimize Instantiated Primitives   : NO
Use Clock Enable                   : Auto
Use Synchronous Set                : Auto
Use Synchronous Reset              : Auto
Pack IO Registers into IOBs        : Auto
Equivalent register Removal        : YES

---- General Options
Optimization Goal                  : Speed
Optimization Effort                : 1
Power Reduction                    : NO
Keep Hierarchy                     : No
Netlist Hierarchy                  : As_Optimized
RTL Output                         : Yes
Global Optimization                : AllClockNets
Read Cores                         : YES
Write Timing Constraints           : NO
Cross Clock Analysis               : NO
Hierarchy Separator                : /
Bus Delimiter                      : <>
Case Specifier                     : Maintain
```

```
Slice Utilization Ratio            : 100
BRAM Utilization Ratio             : 100
DSP48 Utilization Ratio            : 100
Auto BRAM Packing                  : NO
Slice Utilization Ratio Delta      : 5

=========================================================================


=========================================================================
*                           HDL Parsing                                 *
=========================================================================
Analyzing Verilog file "/home/ise/Project4V2/vending_machine.v" into library work
Parsing module <vending_machine>.

=========================================================================
*                            HDL Elaboration                            *
=========================================================================

Elaborating module <vending_machine>.
WARNING:HDLCompiler:413 - "/home/ise/Project4V2/vending_machine.v" Line 296: Result of 8-bit
expression is truncated to fit in 5-bit target.

=========================================================================
*                            HDL Synthesis                              *
=========================================================================

Synthesizing Unit <vending_machine>.
    Related source file is "/home/ise/Project4V2/vending_machine.v".
        IDLE = 32'b00000000000000000000000000000000
        STATE_RELOAD = 32'b00000000000000000000000000000001
        SELECTION = 32'b00000000000000000000000000000010
        VEND_STATE = 32'b00000000000000000000000000001001
        GET_CODE = 32'b00000000000000000000000000001011
        SNACK_COST_1 = 32'b00000000000000000000000000000011
        SNACK_COST_2 = 32'b00000000000000000000000000000100
        SNACK_COST_3 = 32'b00000000000000000000000000000101
        SNACK_COST_4 = 32'b00000000000000000000000000000110
        SNACK_COST_5 = 32'b00000000000000000000000000000111
        SNACK_COST_6 = 32'b00000000000000000000000000001000
    Found 3-bit register for signal <cycles>.
    Found 4-bit register for signal <current_state>.
    Found 4-bit subtractor for signal <counter_0[3]_GND_1_o_sub_134_OUT> created at line 393.
    Found 4-bit subtractor for signal <counter_1[3]_GND_1_o_sub_136_OUT> created at line 395.
    Found 4-bit subtractor for signal <counter_2[3]_GND_1_o_sub_138_OUT> created at line 397.
    Found 4-bit subtractor for signal <counter_3[3]_GND_1_o_sub_140_OUT> created at line 399.
    Found 4-bit subtractor for signal <counter_4[3]_GND_1_o_sub_142_OUT> created at line 401.
    Found 4-bit subtractor for signal <counter_5[3]_GND_1_o_sub_144_OUT> created at line 403.
    Found 4-bit subtractor for signal <counter_6[3]_GND_1_o_sub_146_OUT> created at line 405.
    Found 4-bit subtractor for signal <counter_7[3]_GND_1_o_sub_148_OUT> created at line 407.
    Found 4-bit subtractor for signal <counter_8[3]_GND_1_o_sub_150_OUT> created at line 409.
    Found 4-bit subtractor for signal <counter_9[3]_GND_1_o_sub_152_OUT> created at line 411.
    Found 4-bit subtractor for signal <counter_10[3]_GND_1_o_sub_154_OUT> created at line 413.
    Found 4-bit subtractor for signal <counter_11[3]_GND_1_o_sub_156_OUT> created at line 415.
    Found 4-bit subtractor for signal <counter_12[3]_GND_1_o_sub_158_OUT> created at line 417.
    Found 4-bit subtractor for signal <counter_13[3]_GND_1_o_sub_160_OUT> created at line 419.
    Found 4-bit subtractor for signal <counter_14[3]_GND_1_o_sub_162_OUT> created at line 421.
    Found 4-bit subtractor for signal <counter_15[3]_GND_1_o_sub_164_OUT> created at line 423.
    Found 4-bit subtractor for signal <counter_16[3]_GND_1_o_sub_166_OUT> created at line 425.
    Found 4-bit subtractor for signal <counter_17[3]_GND_1_o_sub_168_OUT> created at line 427.
    Found 4-bit subtractor for signal <counter_18[3]_GND_1_o_sub_170_OUT> created at line 429.
    Found 4-bit subtractor for signal <counter_19[3]_GND_1_o_sub_172_OUT> created at line 431.
    Found 3-bit adder for signal <cycles[2]_GND_1_o_add_91_OUT> created at line 238.
    Found 5-bit adder for signal <item_code[4]_GND_1_o_add_109_OUT> created at line 308.
    Found 4x4-bit multiplier for signal <n0574> created at line 296.
    Found 16x10-bit Read Only RAM for signal <_n0871>
```

WARNING:Xst:737 - Found 1-bit latch for signal <next_state<3>>. Latches may be generated from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <next_state<2>>. Latches may be generated from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs, as they may lead to timing problems.
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WARNING:Xst:737 - Found 1-bit latch for signal <next_state<0>>. Latches may be generated from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs, as they may lead to timing problems.
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WARNING:Xst:737 - Found 1-bit latch for signal <counter_12<1>>. Latches may be generated from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <counter_12<0>>. Latches may be generated from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <counter_13<3>>. Latches may be generated from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <counter_13<2>>. Latches may be generated from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <counter_13<1>>. Latches may be generated from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <counter_13<0>>. Latches may be generated from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <counter_14<3>>. Latches may be generated from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <counter_14<2>>. Latches may be generated from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <counter_14<1>>. Latches may be generated from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <counter_14<0>>. Latches may be generated from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <counter_15<3>>. Latches may be generated from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <counter_15<2>>. Latches may be generated from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <counter_15<1>>. Latches may be generated from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <counter_15<0>>. Latches may be generated from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <counter_16<3>>. Latches may be generated from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <counter_16<2>>. Latches may be generated from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <counter_16<1>>. Latches may be generated from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <counter_16<0>>. Latches may be generated from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <counter_17<3>>. Latches may be generated from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <counter_17<2>>. Latches may be generated from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <counter_17<1>>. Latches may be generated from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <counter_17<0>>. Latches may be generated from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs, as they may lead to timing problems.

```
WARNING:Xst:737 - Found 1-bit latch for signal <counter_18<3>>. Latches may be generated from
incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs,
as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <counter_18<2>>. Latches may be generated from
incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs,
as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <counter_18<1>>. Latches may be generated from
incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs,
as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <counter_18<0>>. Latches may be generated from
incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs,
as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <counter_19<3>>. Latches may be generated from
incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs,
as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <counter_19<2>>. Latches may be generated from
incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs,
as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <counter_19<1>>. Latches may be generated from
incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs,
as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <counter_19<0>>. Latches may be generated from
incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs,
as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <VEND>. Latches may be generated from
incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs,
as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <COST<2>>. Latches may be generated from
incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs,
as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <COST<1>>. Latches may be generated from
incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs,
as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <COST<0>>. Latches may be generated from
incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs,
as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <sel_cycle_flag>. Latches may be generated from
incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs,
as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <FAILED_TRAN>. Latches may be generated from
incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD designs,
as they may lead to timing problems.
    Found 3-bit comparator greater for signal <cycles[2]_PWR_1_o_LessThan_11_o> created at
line 108
    Found 5-bit comparator lessequal for signal <n0012> created at line 116
    Found 5-bit comparator lessequal for signal <n0022> created at line 128
    Found 5-bit comparator lessequal for signal <n0024> created at line 128
    Found 5-bit comparator lessequal for signal <n0035> created at line 139
    Found 5-bit comparator lessequal for signal <n0037> created at line 139
    Found 5-bit comparator lessequal for signal <n0048> created at line 150
    Found 5-bit comparator lessequal for signal <n0050> created at line 150
    Found 3-bit comparator greater for signal <PWR_1_o_cycles[2]_LessThan_93_o> created at
line 241
    Found 4-bit comparator equal for signal <current_state[3]_GND_1_o_equal_103_o> created at
line 254
    Found 4-bit comparator greater for signal <ITEM_CODE[3]_PWR_1_o_LessThan_106_o> created at
line 291
    Summary:
       inferred   1 RAM(s).
       inferred   1 Multiplier(s).
       inferred  22 Adder/Subtractor(s).
       inferred   7 D-type flip-flop(s).
       inferred 102 Latch(s).
       inferred  11 Comparator(s).
       inferred 147 Multiplexer(s).
Unit <vending_machine> synthesized.
```

```
=========================================================================
HDL Synthesis Report

Macro Statistics
# RAMs                                                  : 1
 16x10-bit single-port Read Only RAM                   : 1
# Multipliers                                           : 1
 4x4-bit multiplier                                    : 1
# Adders/Subtractors                                    : 22
 3-bit adder                                           : 1
 4-bit subtractor                                      : 20
 5-bit adder                                           : 1
# Registers                                             : 2
 3-bit register                                        : 1
 4-bit register                                        : 1
# Latches                                               : 102
 1-bit latch                                           : 102
# Comparators                                           : 11
 3-bit comparator greater                              : 2
 4-bit comparator equal                                : 1
 4-bit comparator greater                              : 1
 5-bit comparator lessequal                            : 7
# Multiplexers                                          : 147
 1-bit 2-to-1 multiplexer                              : 126
 4-bit 2-to-1 multiplexer                              : 20
 5-bit 2-to-1 multiplexer                              : 1

=========================================================================

=========================================================================
*                       Advanced HDL Synthesis                          *
=========================================================================

WARNING:Xst:1293 - FF/Latch <digits_3> has a constant value of 0 in block <vending_machine>.
This FF/Latch will be trimmed during the optimization process.

Synthesizing (advanced) Unit <vending_machine>.
The following registers are absorbed into counter <cycles>: 1 register on signal <cycles>.
INFO:Xst:3231 - The small RAM <Mram__n0871> will be implemented on LUTs in order to maximize
performance and save block RAM resources. If you want to force its implementation on block,
use option/constraint ram_style.
    ----------------------------------------------------------------------
    | ram_type           | Distributed                         |          |
    ----------------------------------------------------------------------
    | Port A                                                   |          |
    |     aspect ratio   | 16-word x 10-bit                    |          |
    |     weA            | connected to signal <GND>           | high     |
    |     addrA          | connected to signal <current_state> |          |
    |     diA            | connected to signal <GND>           |          |
    |     doA            | connected to internal node          |          |
    ----------------------------------------------------------------------
Unit <vending_machine> synthesized (advanced).

=========================================================================
Advanced HDL Synthesis Report

Macro Statistics
# RAMs                                                  : 1
 16x10-bit single-port distributed Read Only RAM       : 1
# Multipliers                                           : 1
 4x4-bit multiplier                                    : 1
# Adders/Subtractors                                    : 21
 4-bit subtractor                                      : 20
 5-bit adder                                           : 1
# Counters                                              : 1
```

```
 3-bit up counter                                      : 1
# Registers                                            : 4
 Flip-Flops                                            : 4
# Comparators                                          : 11
 3-bit comparator greater                              : 2
 4-bit comparator equal                                : 1
 4-bit comparator greater                              : 1
 5-bit comparator lessequal                            : 7
# Multiplexers                                         : 147
 1-bit 2-to-1 multiplexer                              : 126
 4-bit 2-to-1 multiplexer                              : 20
 5-bit 2-to-1 multiplexer                              : 1

=========================================================================

=========================================================================
*                        Low Level Synthesis                            *
=========================================================================
WARNING:Xst:1293 - FF/Latch <digits_3> has a constant value of 0 in block <vending_machine>.
This FF/Latch will be trimmed during the optimization process.

Optimizing unit <vending_machine> ...

Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block vending_machine, actual ratio is 0.
FlipFlop current_state_0 has been replicated 1 time(s)
FlipFlop current_state_2 has been replicated 1 time(s)
FlipFlop current_state_3 has been replicated 1 time(s)
Latch VEND has been replicated 1 time(s) to handle iob=true attribute.

Final Macro Processing ...

=========================================================================
Final Register Report

Macro Statistics
# Registers                                            : 10
 Flip-Flops                                            : 10

=========================================================================

=========================================================================
*                          Partition Report                             *
=========================================================================

Partition Implementation Status
-------------------------------

  No Partitions were found in this design.

-------------------------------

=========================================================================
*                           Design Summary                              *
=========================================================================

Top Level Output File Name         : vending_machine.ngc

Primitive and Black Box Usage:
------------------------------
# BELS                             : 195
#      LUT2                        : 27
#      LUT3                        : 32
#      LUT4                        : 46
#      LUT5                        : 63
```

```
#      LUT6                        : 27
# FlipFlops/Latches                : 112
#      FD                          : 3
#      FDR                         : 7
#      LD                          : 102
# Clock Buffers                    : 1
#      BUFGP                       : 1
# IO Buffers                       : 16
#      IBUF                        : 10
#      OBUF                        : 6

Device utilization summary:
---------------------------

Selected Device : 7a100tcsg324-3


Slice Logic Utilization:
 Number of Slice Registers:             106  out of  126800     0%
 Number of Slice LUTs:                  195  out of  63400     0%
    Number used as Logic:               195  out of  63400     0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:    201
   Number with an unused Flip Flop:      95  out of    201    47%
   Number with an unused LUT:             6  out of    201     2%
   Number of fully used LUT-FF pairs:   100  out of    201    49%
   Number of unique control sets:        33

IO Utilization:
 Number of IOs:                         17
 Number of bonded IOBs:                 17  out of    210     8%
    IOB Flip Flops/Latches:              6

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:               1  out of     32     3%

---------------------------
Partition Resource Summary:
---------------------------

  No Partitions were found in this design.

---------------------------


=========================================================================
Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
-----------------------------------------------------------------------------------------------+-----
--------------------+-------+
Clock Signal                                                                                   |
Clock buffer(FF name)   | Load  |
-----------------------------------------------------------------------------------------------+-----
--------------------+-------+
Mmux_current_state[3]_GND_16_o_Mux_422_o11(Mmux_current_state[3]_GND_16_o_Mux_422_o11:O)|
NONE(*)(item_code_flag) | 1     |
current_state[3]_GND_7_o_Mux_412_o(Mmux_current_state[3]_GND_7_o_Mux_412_o11:O)         |
NONE(*)(item_code_3)    | 5     |
```

```
current_state[3]_GND_20_o_Mux_429_o(Mmux_current_state[3]_GND_20_o_Mux_429_o11:O)       |
NONE(*)(counter_0_3)    | 4     |
current_state[3]_GND_28_o_Mux_437_o(Mmux_current_state[3]_GND_28_o_Mux_437_o11:O)       |
NONE(*)(counter_2_3)    | 4     |
current_state[3]_GND_52_o_Mux_461_o(Mmux_current_state[3]_GND_52_o_Mux_461_o11:O)       |
NONE(*)(counter_8_2)    | 4     |
current_state[3]_GND_80_o_Mux_489_o(Mmux_current_state[3]_GND_80_o_Mux_489_o11:O)       |
NONE(*)(counter_15_3)   | 4     |
current_state[3]_GND_92_o_Mux_501_o(Mmux_current_state[3]_GND_92_o_Mux_501_o11:O)       |
NONE(*)(counter_18_1)   | 4     |
current_state[3]_GND_64_o_Mux_473_o(Mmux_current_state[3]_GND_64_o_Mux_473_o11:O)       |
NONE(*)(counter_11_3)   | 4     |
current_state[3]_GND_72_o_Mux_481_o(Mmux_current_state[3]_GND_72_o_Mux_481_o11:O)       |
NONE(*)(counter_13_3)   | 4     |
current_state[3]_GND_48_o_Mux_457_o(Mmux_current_state[3]_GND_48_o_Mux_457_o11:O)       |
NONE(*)(counter_7_3)    | 4     |
current_state[3]_GND_96_o_Mux_505_o(Mmux_current_state[3]_GND_96_o_Mux_505_o11:O)       |
NONE(*)(counter_19_3)   | 4     |
current_state[3]_GND_84_o_Mux_493_o(Mmux_current_state[3]_GND_84_o_Mux_493_o11:O)       |
NONE(*)(counter_16_3)   | 4     |
current_state[3]_GND_40_o_Mux_449_o(Mmux_current_state[3]_GND_40_o_Mux_449_o11:O)       |
NONE(*)(counter_5_3)    | 4     |
current_state[3]_GND_68_o_Mux_477_o(Mmux_current_state[3]_GND_68_o_Mux_477_o11:O)       |
NONE(*)(counter_12_2)   | 4     |
current_state[3]_GND_32_o_Mux_441_o(Mmux_current_state[3]_GND_32_o_Mux_441_o11:O)       |
NONE(*)(counter_3_3)    | 4     |
current_state[3]_GND_36_o_Mux_445_o(Mmux_current_state[3]_GND_36_o_Mux_445_o11:O)       |
NONE(*)(counter_4_1)    | 4     |
current_state[3]_GND_44_o_Mux_453_o(Mmux_current_state[3]_GND_44_o_Mux_453_o11:O)       |
NONE(*)(counter_6_3)    | 4     |
current_state[3]_GND_88_o_Mux_497_o(Mmux_current_state[3]_GND_88_o_Mux_497_o11:O)       |
NONE(*)(counter_17_3)   | 4     |
current_state[3]_GND_24_o_Mux_433_o(Mmux_current_state[3]_GND_24_o_Mux_433_o11:O)       |
NONE(*)(counter_1_3)    | 4     |
current_state[3]_GND_76_o_Mux_485_o(Mmux_current_state[3]_GND_76_o_Mux_485_o11:O)       |
NONE(*)(counter_14_3)   | 4     |
current_state[3]_GND_60_o_Mux_469_o(Mmux_current_state[3]_GND_60_o_Mux_469_o11:O)       |
NONE(*)(counter_10_3)   | 4     |
current_state[3]_GND_56_o_Mux_465_o(Mmux_current_state[3]_GND_56_o_Mux_465_o11:O)       |
NONE(*)(counter_9_3)    | 4     |
current_state[3]_GND_2_o_Mux_83_o(Mmux_current_state[3]_GND_2_o_Mux_83_o16:O)           |
NONE(*)(next_state_2)   | 4     |
CLK                                                                                     |
BUFGP                   | 10    |
current_state[3]_GND_16_o_Mux_422_o(Mmux_current_state[3]_GND_16_o_Mux_422_o12:O)       |
NONE(*)(get_cycle_flag) | 1     |
current_state[3]_GND_12_o_Mux_417_o(Mmux_current_state[3]_GND_12_o_Mux_417_o11:O)       |
NONE(*)(digits_0)       | 2     |
current_state[3]_GND_18_o_Mux_426_o(Mmux_current_state[3]_GND_18_o_Mux_426_o11:O)       |
NONE(*)(INVALID_SEL)    | 1     |
current_state[3]_GND_19_o_Mux_428_o(Mmux_current_state[3]_GND_19_o_Mux_428_o1:O)        |
NONE(*)(vend_cycle_flag)| 1     |
Mmux_current_state[3]_GND_7_o_Mux_412_o12(Mmux_current_state[3]_GND_7_o_Mux_412_o121:O) |
NONE(*)(VEND)           | 2     |
Mram__n08715(Mram__n087151:O)                                                           |
NONE(*)(COST_2)         | 3     |
current_state[3]_GND_104_o_Mux_515_o(Mmux_current_state[3]_GND_104_o_Mux_515_o11:O)     |
NONE(*)(sel_cycle_flag) | 1     |
current_state[3]_GND_105_o_Mux_517_o(Mmux_current_state[3]_GND_105_o_Mux_517_o11:O)     |
NONE(*)(FAILED_TRAN)    | 1     |
--------------------------------------------------------------------------------------+-----
--------------------+-------+
(*) These 31 clock signal(s) are generated by combinatorial logic,
and XST is not able to identify which are the primary clock signals.
Please use the CLOCK_SIGNAL constraint to specify the clock signal(s) generated by
combinatorial logic.
```

```
INFO:Xst:2169 - HDL ADVISOR - Some clock signals were not automatically buffered by XST with
BUFG/BUFR resources. Please use the buffer_type constraint in order to insert these buffers to
the clock signals to help prevent skew problems.

Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design

Timing Summary:
---------------
Speed Grade: -3

   Minimum period: 1.614ns (Maximum Frequency: 619.732MHz)
   Minimum input arrival time before clock: 1.903ns
   Maximum output required time after clock: 0.751ns
   Maximum combinational path delay: No path found

Timing Details:
---------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'current_state[3]_GND_7_o_Mux_412_o'
  Clock period: 1.523ns (frequency: 656.599MHz)
  Total number of paths / destination ports: 15 / 5
-------------------------------------------------------------------------
Delay:               1.523ns (Levels of Logic = 2)
  Source:            item_code_2 (LATCH)
  Destination:       item_code_3 (LATCH)
  Source Clock:      current_state[3]_GND_7_o_Mux_412_o falling
  Destination Clock: current_state[3]_GND_7_o_Mux_412_o falling

  Data Path: item_code_2 to item_code_3
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LD:G->Q              11   0.472   0.558  item_code_2 (item_code_2)
     LUT6:I3->O            2   0.097   0.299  Madd_item_code[4]_GND_1_o_add_109_OUT_cy<2>11
(Madd_item_code[4]_GND_1_o_add_109_OUT_cy<2>)
     LUT6:I5->O            1   0.097   0.000
Mmux_current_state[3]_item_code[4]_wide_mux_382_OUT<0>131
(current_state[3]_item_code[4]_wide_mux_382_OUT<3>)
     LD:D                     -0.028          item_code_3
    ----------------------------------------
    Total                      1.523ns (0.666ns logic, 0.857ns route)
                                       (43.7% logic, 56.3% route)

=========================================================================
Timing constraint: Default period analysis for Clock 'current_state[3]_GND_20_o_Mux_429_o'
  Clock period: 1.135ns (frequency: 880.980MHz)
  Total number of paths / destination ports: 10 / 4
-------------------------------------------------------------------------
Delay:               1.135ns (Levels of Logic = 1)
  Source:            counter_0_2 (LATCH)
  Destination:       counter_0_3 (LATCH)
  Source Clock:      current_state[3]_GND_20_o_Mux_429_o falling
  Destination Clock: current_state[3]_GND_20_o_Mux_429_o falling

  Data Path: counter_0_2 to counter_0_3
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LD:G->Q               3   0.472   0.566  counter_0_2 (counter_0_2)
     LUT5:I1->O            1   0.097   0.000
current_state[3]_counter_0[3]_wide_mux_388_OUT<3>1
(current_state[3]_counter_0[3]_wide_mux_388_OUT<3>)
```

```
     LD:D                     -0.028          counter_0_3
    ----------------------------------------
    Total                      1.135ns (0.569ns logic, 0.566ns route)
                                       (50.1% logic, 49.9% route)

==========================================================================
Timing constraint: Default period analysis for Clock 'current_state[3]_GND_28_o_Mux_437_o'
  Clock period: 1.135ns (frequency: 880.980MHz)
  Total number of paths / destination ports: 10 / 4
--------------------------------------------------------------------------
Delay:               1.135ns (Levels of Logic = 1)
  Source:            counter_2_2 (LATCH)
  Destination:       counter_2_3 (LATCH)
  Source Clock:      current_state[3]_GND_28_o_Mux_437_o falling
  Destination Clock: current_state[3]_GND_28_o_Mux_437_o falling

  Data Path: counter_2_2 to counter_2_3
                               Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LD:G->Q               3   0.472   0.566  counter_2_2 (counter_2_2)
     LUT5:I1->O            1   0.097   0.000
current_state[3]_counter_2[3]_wide_mux_390_OUT<3>1
(current_state[3]_counter_2[3]_wide_mux_390_OUT<3>)
     LD:D                     -0.028          counter_2_3
    ----------------------------------------
    Total                      1.135ns (0.569ns logic, 0.566ns route)
                                       (50.1% logic, 49.9% route)

==========================================================================
Timing constraint: Default period analysis for Clock 'current_state[3]_GND_52_o_Mux_461_o'
  Clock period: 1.135ns (frequency: 880.980MHz)
  Total number of paths / destination ports: 10 / 4
--------------------------------------------------------------------------
Delay:               1.135ns (Levels of Logic = 1)
  Source:            counter_8_2 (LATCH)
  Destination:       counter_8_3 (LATCH)
  Source Clock:      current_state[3]_GND_52_o_Mux_461_o falling
  Destination Clock: current_state[3]_GND_52_o_Mux_461_o falling

  Data Path: counter_8_2 to counter_8_3
                               Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LD:G->Q               3   0.472   0.566  counter_8_2 (counter_8_2)
     LUT5:I1->O            1   0.097   0.000
current_state[3]_counter_8[3]_wide_mux_396_OUT<3>1
(current_state[3]_counter_8[3]_wide_mux_396_OUT<3>)
     LD:D                     -0.028          counter_8_3
    ----------------------------------------
    Total                      1.135ns (0.569ns logic, 0.566ns route)
                                       (50.1% logic, 49.9% route)

==========================================================================
Timing constraint: Default period analysis for Clock 'current_state[3]_GND_80_o_Mux_489_o'
  Clock period: 1.135ns (frequency: 880.980MHz)
  Total number of paths / destination ports: 10 / 4
--------------------------------------------------------------------------
Delay:               1.135ns (Levels of Logic = 1)
  Source:            counter_15_2 (LATCH)
  Destination:       counter_15_3 (LATCH)
  Source Clock:      current_state[3]_GND_80_o_Mux_489_o falling
  Destination Clock: current_state[3]_GND_80_o_Mux_489_o falling

  Data Path: counter_15_2 to counter_15_3
                               Gate     Net
```

```
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LD:G->Q               3   0.472   0.566  counter_15_2 (counter_15_2)
     LUT5:I1->O            1   0.097   0.000
current_state[3]_counter_15[3]_wide_mux_403_OUT<3>1
(current_state[3]_counter_15[3]_wide_mux_403_OUT<3>)
     LD:D                 -0.028          counter_15_3
    ----------------------------------------
    Total                      1.135ns (0.569ns logic, 0.566ns route)
                                       (50.1% logic, 49.9% route)

==========================================================================
Timing constraint: Default period analysis for Clock 'current_state[3]_GND_92_o_Mux_501_o'
  Clock period: 1.135ns (frequency: 880.980MHz)
  Total number of paths / destination ports: 10 / 4
--------------------------------------------------------------------------
Delay:               1.135ns (Levels of Logic = 1)
  Source:            counter_18_2 (LATCH)
  Destination:       counter_18_3 (LATCH)
  Source Clock:      current_state[3]_GND_92_o_Mux_501_o falling
  Destination Clock: current_state[3]_GND_92_o_Mux_501_o falling

  Data Path: counter_18_2 to counter_18_3
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LD:G->Q               3   0.472   0.566  counter_18_2 (counter_18_2)
     LUT5:I1->O            1   0.097   0.000
current_state[3]_counter_18[3]_wide_mux_406_OUT<3>1
(current_state[3]_counter_18[3]_wide_mux_406_OUT<3>)
     LD:D                 -0.028          counter_18_3
    ----------------------------------------
    Total                      1.135ns (0.569ns logic, 0.566ns route)
                                       (50.1% logic, 49.9% route)

==========================================================================
Timing constraint: Default period analysis for Clock 'current_state[3]_GND_64_o_Mux_473_o'
  Clock period: 1.135ns (frequency: 880.980MHz)
  Total number of paths / destination ports: 10 / 4
--------------------------------------------------------------------------
Delay:               1.135ns (Levels of Logic = 1)
  Source:            counter_11_2 (LATCH)
  Destination:       counter_11_3 (LATCH)
  Source Clock:      current_state[3]_GND_64_o_Mux_473_o falling
  Destination Clock: current_state[3]_GND_64_o_Mux_473_o falling

  Data Path: counter_11_2 to counter_11_3
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LD:G->Q               3   0.472   0.566  counter_11_2 (counter_11_2)
     LUT5:I1->O            1   0.097   0.000
current_state[3]_counter_11[3]_wide_mux_399_OUT<3>1
(current_state[3]_counter_11[3]_wide_mux_399_OUT<3>)
     LD:D                 -0.028          counter_11_3
    ----------------------------------------
    Total                      1.135ns (0.569ns logic, 0.566ns route)
                                       (50.1% logic, 49.9% route)

==========================================================================
Timing constraint: Default period analysis for Clock 'current_state[3]_GND_72_o_Mux_481_o'
  Clock period: 1.135ns (frequency: 880.980MHz)
  Total number of paths / destination ports: 10 / 4
--------------------------------------------------------------------------
Delay:               1.135ns (Levels of Logic = 1)
  Source:            counter_13_2 (LATCH)
```

```
  Destination:       counter_13_3 (LATCH)
  Source Clock:      current_state[3]_GND_72_o_Mux_481_o falling
  Destination Clock: current_state[3]_GND_72_o_Mux_481_o falling

  Data Path: counter_13_2 to counter_13_3
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LD:G->Q               3   0.472   0.566  counter_13_2 (counter_13_2)
     LUT5:I1->O            1   0.097   0.000
current_state[3]_counter_13[3]_wide_mux_401_OUT<3>1
(current_state[3]_counter_13[3]_wide_mux_401_OUT<3>)
     LD:D                     -0.028          counter_13_3
    ----------------------------------------
    Total                      1.135ns (0.569ns logic, 0.566ns route)
                                       (50.1% logic, 49.9% route)

==========================================================================
Timing constraint: Default period analysis for Clock 'current_state[3]_GND_48_o_Mux_457_o'
  Clock period: 1.135ns (frequency: 880.980MHz)
  Total number of paths / destination ports: 10 / 4
--------------------------------------------------------------------------
Delay:               1.135ns (Levels of Logic = 1)
  Source:            counter_7_2 (LATCH)
  Destination:       counter_7_3 (LATCH)
  Source Clock:      current_state[3]_GND_48_o_Mux_457_o falling
  Destination Clock: current_state[3]_GND_48_o_Mux_457_o falling

  Data Path: counter_7_2 to counter_7_3
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LD:G->Q               3   0.472   0.566  counter_7_2 (counter_7_2)
     LUT5:I1->O            1   0.097   0.000
current_state[3]_counter_7[3]_wide_mux_395_OUT<3>1
(current_state[3]_counter_7[3]_wide_mux_395_OUT<3>)
     LD:D                     -0.028          counter_7_3
    ----------------------------------------
    Total                      1.135ns (0.569ns logic, 0.566ns route)
                                       (50.1% logic, 49.9% route)

==========================================================================
Timing constraint: Default period analysis for Clock 'current_state[3]_GND_96_o_Mux_505_o'
  Clock period: 1.135ns (frequency: 880.980MHz)
  Total number of paths / destination ports: 10 / 4
--------------------------------------------------------------------------
Delay:               1.135ns (Levels of Logic = 1)
  Source:            counter_19_2 (LATCH)
  Destination:       counter_19_3 (LATCH)
  Source Clock:      current_state[3]_GND_96_o_Mux_505_o falling
  Destination Clock: current_state[3]_GND_96_o_Mux_505_o falling

  Data Path: counter_19_2 to counter_19_3
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LD:G->Q               3   0.472   0.566  counter_19_2 (counter_19_2)
     LUT5:I1->O            1   0.097   0.000
current_state[3]_counter_19[3]_wide_mux_407_OUT<3>1
(current_state[3]_counter_19[3]_wide_mux_407_OUT<3>)
     LD:D                     -0.028          counter_19_3
    ----------------------------------------
    Total                      1.135ns (0.569ns logic, 0.566ns route)
                                       (50.1% logic, 49.9% route)

==========================================================================
```

```
Timing constraint: Default period analysis for Clock 'current_state[3]_GND_84_o_Mux_493_o'
  Clock period: 1.139ns (frequency: 877.732MHz)
  Total number of paths / destination ports: 10 / 4
-------------------------------------------------------------------------
Delay:               1.139ns (Levels of Logic = 1)
  Source:            counter_16_2 (LATCH)
  Destination:       counter_16_3 (LATCH)
  Source Clock:      current_state[3]_GND_84_o_Mux_493_o falling
  Destination Clock: current_state[3]_GND_84_o_Mux_493_o falling

  Data Path: counter_16_2 to counter_16_3
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LD:G->Q               4   0.472   0.570  counter_16_2 (counter_16_2)
     LUT5:I1->O            1   0.097   0.000
current_state[3]_counter_16[3]_wide_mux_404_OUT<3>1
(current_state[3]_counter_16[3]_wide_mux_404_OUT<3>)
     LD:D                     -0.028          counter_16_3
    ----------------------------------------
    Total                      1.139ns (0.569ns logic, 0.570ns route)
                                       (49.9% logic, 50.1% route)

=========================================================================
Timing constraint: Default period analysis for Clock 'current_state[3]_GND_40_o_Mux_449_o'
  Clock period: 1.135ns (frequency: 880.980MHz)
  Total number of paths / destination ports: 10 / 4
-------------------------------------------------------------------------
Delay:               1.135ns (Levels of Logic = 1)
  Source:            counter_5_2 (LATCH)
  Destination:       counter_5_3 (LATCH)
  Source Clock:      current_state[3]_GND_40_o_Mux_449_o falling
  Destination Clock: current_state[3]_GND_40_o_Mux_449_o falling

  Data Path: counter_5_2 to counter_5_3
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LD:G->Q               3   0.472   0.566  counter_5_2 (counter_5_2)
     LUT5:I1->O            1   0.097   0.000
current_state[3]_counter_5[3]_wide_mux_393_OUT<3>1
(current_state[3]_counter_5[3]_wide_mux_393_OUT<3>)
     LD:D                     -0.028          counter_5_3
    ----------------------------------------
    Total                      1.135ns (0.569ns logic, 0.566ns route)
                                       (50.1% logic, 49.9% route)

=========================================================================
Timing constraint: Default period analysis for Clock 'current_state[3]_GND_68_o_Mux_477_o'
  Clock period: 1.135ns (frequency: 880.980MHz)
  Total number of paths / destination ports: 10 / 4
-------------------------------------------------------------------------
Delay:               1.135ns (Levels of Logic = 1)
  Source:            counter_12_2 (LATCH)
  Destination:       counter_12_3 (LATCH)
  Source Clock:      current_state[3]_GND_68_o_Mux_477_o falling
  Destination Clock: current_state[3]_GND_68_o_Mux_477_o falling

  Data Path: counter_12_2 to counter_12_3
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LD:G->Q               3   0.472   0.566  counter_12_2 (counter_12_2)
     LUT5:I1->O            1   0.097   0.000
current_state[3]_counter_12[3]_wide_mux_400_OUT<3>1
(current_state[3]_counter_12[3]_wide_mux_400_OUT<3>)
```

```
     LD:D                     -0.028          counter_12_3
    ----------------------------------------
    Total                      1.135ns (0.569ns logic, 0.566ns route)
                                       (50.1% logic, 49.9% route)

=========================================================================
Timing constraint: Default period analysis for Clock 'current_state[3]_GND_32_o_Mux_441_o'
  Clock period: 1.135ns (frequency: 880.980MHz)
  Total number of paths / destination ports: 10 / 4
-------------------------------------------------------------------------
Delay:               1.135ns (Levels of Logic = 1)
  Source:            counter_3_2 (LATCH)
  Destination:       counter_3_3 (LATCH)
  Source Clock:      current_state[3]_GND_32_o_Mux_441_o falling
  Destination Clock: current_state[3]_GND_32_o_Mux_441_o falling

  Data Path: counter_3_2 to counter_3_3
                               Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LD:G->Q               3   0.472   0.566  counter_3_2 (counter_3_2)
     LUT5:I1->O            1   0.097   0.000
current_state[3]_counter_3[3]_wide_mux_391_OUT<3>1
(current_state[3]_counter_3[3]_wide_mux_391_OUT<3>)
     LD:D                     -0.028          counter_3_3
    ----------------------------------------
    Total                      1.135ns (0.569ns logic, 0.566ns route)
                                       (50.1% logic, 49.9% route)

=========================================================================
Timing constraint: Default period analysis for Clock 'current_state[3]_GND_36_o_Mux_445_o'
  Clock period: 1.135ns (frequency: 880.980MHz)
  Total number of paths / destination ports: 10 / 4
-------------------------------------------------------------------------
Delay:               1.135ns (Levels of Logic = 1)
  Source:            counter_4_2 (LATCH)
  Destination:       counter_4_3 (LATCH)
  Source Clock:      current_state[3]_GND_36_o_Mux_445_o falling
  Destination Clock: current_state[3]_GND_36_o_Mux_445_o falling

  Data Path: counter_4_2 to counter_4_3
                               Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LD:G->Q               3   0.472   0.566  counter_4_2 (counter_4_2)
     LUT5:I1->O            1   0.097   0.000
current_state[3]_counter_4[3]_wide_mux_392_OUT<3>1
(current_state[3]_counter_4[3]_wide_mux_392_OUT<3>)
     LD:D                     -0.028          counter_4_3
    ----------------------------------------
    Total                      1.135ns (0.569ns logic, 0.566ns route)
                                       (50.1% logic, 49.9% route)

=========================================================================
Timing constraint: Default period analysis for Clock 'current_state[3]_GND_44_o_Mux_453_o'
  Clock period: 1.135ns (frequency: 880.980MHz)
  Total number of paths / destination ports: 10 / 4
-------------------------------------------------------------------------
Delay:               1.135ns (Levels of Logic = 1)
  Source:            counter_6_2 (LATCH)
  Destination:       counter_6_3 (LATCH)
  Source Clock:      current_state[3]_GND_44_o_Mux_453_o falling
  Destination Clock: current_state[3]_GND_44_o_Mux_453_o falling

  Data Path: counter_6_2 to counter_6_3
                               Gate     Net
```

```
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LD:G->Q               3   0.472   0.566  counter_6_2 (counter_6_2)
     LUT5:I1->O            1   0.097   0.000
current_state[3]_counter_6[3]_wide_mux_394_OUT<3>1
(current_state[3]_counter_6[3]_wide_mux_394_OUT<3>)
     LD:D                 -0.028          counter_6_3
    ----------------------------------------
    Total                      1.135ns (0.569ns logic, 0.566ns route)
                                       (50.1% logic, 49.9% route)

=========================================================================
Timing constraint: Default period analysis for Clock 'current_state[3]_GND_88_o_Mux_497_o'
  Clock period: 1.135ns (frequency: 880.980MHz)
  Total number of paths / destination ports: 10 / 4
-------------------------------------------------------------------------
Delay:               1.135ns (Levels of Logic = 1)
  Source:            counter_17_2 (LATCH)
  Destination:       counter_17_3 (LATCH)
  Source Clock:      current_state[3]_GND_88_o_Mux_497_o falling
  Destination Clock: current_state[3]_GND_88_o_Mux_497_o falling

  Data Path: counter_17_2 to counter_17_3
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LD:G->Q               3   0.472   0.566  counter_17_2 (counter_17_2)
     LUT5:I1->O            1   0.097   0.000
current_state[3]_counter_17[3]_wide_mux_405_OUT<3>1
(current_state[3]_counter_17[3]_wide_mux_405_OUT<3>)
     LD:D                 -0.028          counter_17_3
    ----------------------------------------
    Total                      1.135ns (0.569ns logic, 0.566ns route)
                                       (50.1% logic, 49.9% route)

=========================================================================
Timing constraint: Default period analysis for Clock 'current_state[3]_GND_24_o_Mux_433_o'
  Clock period: 1.135ns (frequency: 880.980MHz)
  Total number of paths / destination ports: 10 / 4
-------------------------------------------------------------------------
Delay:               1.135ns (Levels of Logic = 1)
  Source:            counter_1_2 (LATCH)
  Destination:       counter_1_3 (LATCH)
  Source Clock:      current_state[3]_GND_24_o_Mux_433_o falling
  Destination Clock: current_state[3]_GND_24_o_Mux_433_o falling

  Data Path: counter_1_2 to counter_1_3
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LD:G->Q               3   0.472   0.566  counter_1_2 (counter_1_2)
     LUT5:I1->O            1   0.097   0.000
current_state[3]_counter_1[3]_wide_mux_389_OUT<3>1
(current_state[3]_counter_1[3]_wide_mux_389_OUT<3>)
     LD:D                 -0.028          counter_1_3
    ----------------------------------------
    Total                      1.135ns (0.569ns logic, 0.566ns route)
                                       (50.1% logic, 49.9% route)

=========================================================================
Timing constraint: Default period analysis for Clock 'current_state[3]_GND_76_o_Mux_485_o'
  Clock period: 1.135ns (frequency: 880.980MHz)
  Total number of paths / destination ports: 10 / 4
-------------------------------------------------------------------------
Delay:               1.135ns (Levels of Logic = 1)
  Source:            counter_14_2 (LATCH)
```

```
  Destination:       counter_14_3 (LATCH)
  Source Clock:      current_state[3]_GND_76_o_Mux_485_o falling
  Destination Clock: current_state[3]_GND_76_o_Mux_485_o falling

  Data Path: counter_14_2 to counter_14_3
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LD:G->Q               3   0.472   0.566  counter_14_2 (counter_14_2)
     LUT5:I1->O            1   0.097   0.000
current_state[3]_counter_14[3]_wide_mux_402_OUT<3>1
(current_state[3]_counter_14[3]_wide_mux_402_OUT<3>)
     LD:D                     -0.028          counter_14_3
    ----------------------------------------
    Total                      1.135ns (0.569ns logic, 0.566ns route)
                                       (50.1% logic, 49.9% route)

==========================================================================
Timing constraint: Default period analysis for Clock 'current_state[3]_GND_60_o_Mux_469_o'
  Clock period: 1.135ns (frequency: 880.980MHz)
  Total number of paths / destination ports: 10 / 4
--------------------------------------------------------------------------
Delay:               1.135ns (Levels of Logic = 1)
  Source:            counter_10_2 (LATCH)
  Destination:       counter_10_3 (LATCH)
  Source Clock:      current_state[3]_GND_60_o_Mux_469_o falling
  Destination Clock: current_state[3]_GND_60_o_Mux_469_o falling

  Data Path: counter_10_2 to counter_10_3
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LD:G->Q               3   0.472   0.566  counter_10_2 (counter_10_2)
     LUT5:I1->O            1   0.097   0.000
current_state[3]_counter_10[3]_wide_mux_398_OUT<3>1
(current_state[3]_counter_10[3]_wide_mux_398_OUT<3>)
     LD:D                     -0.028          counter_10_3
    ----------------------------------------
    Total                      1.135ns (0.569ns logic, 0.566ns route)
                                       (50.1% logic, 49.9% route)

==========================================================================
Timing constraint: Default period analysis for Clock 'current_state[3]_GND_56_o_Mux_465_o'
  Clock period: 1.135ns (frequency: 880.980MHz)
  Total number of paths / destination ports: 10 / 4
--------------------------------------------------------------------------
Delay:               1.135ns (Levels of Logic = 1)
  Source:            counter_9_2 (LATCH)
  Destination:       counter_9_3 (LATCH)
  Source Clock:      current_state[3]_GND_56_o_Mux_465_o falling
  Destination Clock: current_state[3]_GND_56_o_Mux_465_o falling

  Data Path: counter_9_2 to counter_9_3
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LD:G->Q               3   0.472   0.566  counter_9_2 (counter_9_2)
     LUT5:I1->O            1   0.097   0.000
current_state[3]_counter_9[3]_wide_mux_397_OUT<3>1
(current_state[3]_counter_9[3]_wide_mux_397_OUT<3>)
     LD:D                     -0.028          counter_9_3
    ----------------------------------------
    Total                      1.135ns (0.569ns logic, 0.566ns route)
                                       (50.1% logic, 49.9% route)

==========================================================================
```

```
Timing constraint: Default period analysis for Clock 'current_state[3]_GND_12_o_Mux_417_o'
  Clock period: 1.117ns (frequency: 894.935MHz)
  Total number of paths / destination ports: 4 / 2
--------------------------------------------------------------------------------
Delay:               1.117ns (Levels of Logic = 1)
  Source:            digits_1 (LATCH)
  Destination:       digits_0 (LATCH)
  Source Clock:      current_state[3]_GND_12_o_Mux_417_o falling
  Destination Clock: current_state[3]_GND_12_o_Mux_417_o falling

  Data Path: digits_1 to digits_0
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LD:G->Q               9   0.472   0.548  digits_1 (digits_1)
     LUT4:I1->O            1   0.097   0.000
Mmux_current_state[3]_digits[3]_wide_mux_383_OUT<0>11
(current_state[3]_digits[3]_wide_mux_383_OUT<0>)
     LD:D                     -0.028          digits_0
    ----------------------------------------
    Total                      1.117ns (0.569ns logic, 0.548ns route)
                                       (50.9% logic, 49.1% route)

================================================================================
Timing constraint: Default period analysis for Clock 'CLK'
  Clock period: 1.614ns (frequency: 619.732MHz)
  Total number of paths / destination ports: 33 / 3
--------------------------------------------------------------------------------
Delay:               1.614ns (Levels of Logic = 2)
  Source:            cycles_1 (FF)
  Destination:       cycles_1 (FF)
  Source Clock:      CLK rising
  Destination Clock: CLK rising

  Data Path: cycles_1 to cycles_1
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FD:C->Q               7   0.361   0.539  cycles_1 (cycles_1)
     LUT3:I0->O            1   0.097   0.511  Mcount_cycles_val_SW1 (N13)
     LUT5:I2->O            1   0.097   0.000  cycles_1_rstpot (cycles_1_rstpot)
     FD:D                      0.008          cycles_1
    ----------------------------------------
    Total                      1.614ns (0.563ns logic, 1.051ns route)
                                       (34.9% logic, 65.1% route)

================================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock
'Mmux_current_state[3]_GND_16_o_Mux_422_o11'
  Total number of paths / destination ports: 1 / 1
--------------------------------------------------------------------------------
Offset:              0.303ns (Levels of Logic = 1)
  Source:            KEY_PRESS (PAD)
  Destination:       item_code_flag (LATCH)
  Destination Clock: Mmux_current_state[3]_GND_16_o_Mux_422_o11 falling

  Data Path: KEY_PRESS to item_code_flag
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             6   0.001   0.302  KEY_PRESS_IBUF (KEY_PRESS_IBUF)
     LD:D                     -0.028          item_code_flag
    ----------------------------------------
    Total                      0.303ns (0.001ns logic, 0.302ns route)
                                       (0.3% logic, 99.7% route)
```

```
================================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'current_state[3]_GND_7_o_Mux_412_o'
  Total number of paths / destination ports: 25 / 5
--------------------------------------------------------------------------------
Offset:              1.903ns (Levels of Logic = 4)
  Source:            ITEM_CODE<2> (PAD)
  Destination:       item_code_4 (LATCH)
  Destination Clock: current_state[3]_GND_7_o_Mux_412_o falling

  Data Path: ITEM_CODE<2> to item_code_4
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             6   0.001   0.402  ITEM_CODE_2_IBUF (ITEM_CODE_2_IBUF)
     LUT2:I0->O            2   0.097   0.515  Mmult_n0574_Madd_cy<3>11
(Mmult_n0574_Madd_cy<3>)
     LUT6:I3->O            1   0.097   0.693
Madd_item_code[4]_GND_1_o_add_109_OUT_cy<3>11_SW0 (N10)
     LUT6:I0->O            1   0.097   0.000
Mmux_current_state[3]_item_code[4]_wide_mux_382_OUT<0>14
(current_state[3]_item_code[4]_wide_mux_382_OUT<4>)
     LD:D                 -0.028          item_code_4
    ----------------------------------------
    Total                      1.903ns (0.292ns logic, 1.611ns route)
                                       (15.3% logic, 84.7% route)

================================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'current_state[3]_GND_2_o_Mux_83_o'
  Total number of paths / destination ports: 11 / 3
--------------------------------------------------------------------------------
Offset:              1.731ns (Levels of Logic = 4)
  Source:            KEY_PRESS (PAD)
  Destination:       next_state_3 (LATCH)
  Destination Clock: current_state[3]_GND_2_o_Mux_83_o falling

  Data Path: KEY_PRESS to next_state_3
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             6   0.001   0.579  KEY_PRESS_IBUF (KEY_PRESS_IBUF)
     LUT4:I0->O            2   0.097   0.561  KEY_PRESS_cycles[2]_AND_2_o1
(KEY_PRESS_cycles[2]_AND_2_o)
     LUT6:I2->O            2   0.097   0.299  current_state<1>1 (current_state<1>_mmx_out)
     LUT3:I2->O            1   0.097   0.000  Mmux_current_state[3]_next_state[0]_Mux_88_o24
(current_state[3]_next_state[0]_Mux_88_o)
     LD:D                 -0.028          next_state_0
    ----------------------------------------
    Total                      1.731ns (0.292ns logic, 1.439ns route)
                                       (16.9% logic, 83.1% route)

================================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'CLK'
  Total number of paths / destination ports: 7 / 7
--------------------------------------------------------------------------------
Offset:              0.657ns (Levels of Logic = 1)
  Source:            RESET (PAD)
  Destination:       current_state_0 (FF)
  Destination Clock: CLK rising

  Data Path: RESET to current_state_0
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             7   0.001   0.307  RESET_IBUF (RESET_IBUF)
     FDR:R                     0.349          current_state_0
    ----------------------------------------
```

```
    Total                      0.657ns (0.350ns logic, 0.307ns route)
                                       (53.2% logic, 46.8% route)

==========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'current_state[3]_GND_16_o_Mux_422_o'
  Total number of paths / destination ports: 1 / 1
--------------------------------------------------------------------------
Offset:              0.416ns (Levels of Logic = 2)
  Source:            KEY_PRESS (PAD)
  Destination:       get_cycle_flag (LATCH)
  Destination Clock: current_state[3]_GND_16_o_Mux_422_o falling

  Data Path: KEY_PRESS to get_cycle_flag
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             6   0.001   0.318  KEY_PRESS_IBUF (KEY_PRESS_IBUF)
     LUT2:I1->O            1   0.097   0.000  Mmux_current_state[3]_get_cycle_flag_Mux_421_o11
(current_state[3]_get_cycle_flag_Mux_421_o)
     LD:D                     -0.028          get_cycle_flag
    ----------------------------------------
    Total                      0.416ns (0.098ns logic, 0.318ns route)
                                       (23.5% logic, 76.5% route)

==========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'Mram__n08715'
  Total number of paths / destination ports: 3 / 3
--------------------------------------------------------------------------
Offset:              0.751ns (Levels of Logic = 1)
  Source:            COST_2 (LATCH)
  Destination:       COST<2> (PAD)
  Source Clock:      Mram__n08715 falling

  Data Path: COST_2 to COST<2>
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LD:G->Q               1   0.472   0.279  COST_2 (COST_2)
     OBUF:I->O                 0.000          COST_2_OBUF (COST<2>)
    ----------------------------------------
    Total                      0.751ns (0.472ns logic, 0.279ns route)
                                       (62.8% logic, 37.2% route)

==========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock
'Mmux_current_state[3]_GND_7_o_Mux_412_o12'
  Total number of paths / destination ports: 1 / 1
--------------------------------------------------------------------------
Offset:              0.751ns (Levels of Logic = 1)
  Source:            VEND_1 (LATCH)
  Destination:       VEND (PAD)
  Source Clock:      Mmux_current_state[3]_GND_7_o_Mux_412_o12 falling

  Data Path: VEND_1 to VEND
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LD:G->Q               1   0.472   0.279  VEND_1 (VEND_1)
     OBUF:I->O                 0.000          VEND_OBUF (VEND)
    ----------------------------------------
    Total                      0.751ns (0.472ns logic, 0.279ns route)
                                       (62.8% logic, 37.2% route)

==========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'current_state[3]_GND_18_o_Mux_426_o'
  Total number of paths / destination ports: 1 / 1
```

```
--------------------------------------------------------------------------------
Offset:              0.751ns (Levels of Logic = 1)
  Source:            INVALID_SEL (LATCH)
  Destination:       INVALID_SEL (PAD)
  Source Clock:      current_state[3]_GND_18_o_Mux_426_o falling

  Data Path: INVALID_SEL to INVALID_SEL
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LD:G->Q               1   0.472   0.279  INVALID_SEL (INVALID_SEL_OBUF)
     OBUF:I->O                 0.000          INVALID_SEL_OBUF (INVALID_SEL)
    ----------------------------------------
    Total                      0.751ns (0.472ns logic, 0.279ns route)
                                       (62.8% logic, 37.2% route)

================================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'current_state[3]_GND_105_o_Mux_517_o'
  Total number of paths / destination ports: 1 / 1
--------------------------------------------------------------------------------
Offset:              0.751ns (Levels of Logic = 1)
  Source:            FAILED_TRAN (LATCH)
  Destination:       FAILED_TRAN (PAD)
  Source Clock:      current_state[3]_GND_105_o_Mux_517_o falling

  Data Path: FAILED_TRAN to FAILED_TRAN
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LD:G->Q               1   0.472   0.279  FAILED_TRAN (FAILED_TRAN_OBUF)
     OBUF:I->O                 0.000          FAILED_TRAN_OBUF (FAILED_TRAN)
    ----------------------------------------
    Total                      0.751ns (0.472ns logic, 0.279ns route)
                                       (62.8% logic, 37.2% route)

================================================================================

Cross Clock Domains Report:
--------------------------

Clock to Setup on destination clock CLK
---------------------------------------+---------+---------+---------+---------+
                                       | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock                           |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------------------------------+---------+---------+---------+---------+
CLK                                    |    1.614|         |         |         |
Mmux_current_state[3]_GND_7_o_Mux_412_o12|         |    1.746|         |         |
current_state[3]_GND_104_o_Mux_515_o   |         |    1.280|         |         |
current_state[3]_GND_16_o_Mux_422_o    |         |    1.756|         |         |
current_state[3]_GND_19_o_Mux_428_o    |         |    1.619|         |         |
current_state[3]_GND_2_o_Mux_83_o      |         |    0.773|         |         |
---------------------------------------+---------+---------+---------+---------+

Clock to Setup on destination clock Mmux_current_state[3]_GND_7_o_Mux_412_o12
---------------+---------+---------+---------+---------+
               | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock   |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------+---------+---------+---------+---------+
CLK            |         |         |    1.136|         |
---------------+---------+---------+---------+---------+

Clock to Setup on destination clock Mram__n08715
---------------+---------+---------+---------+---------+
               | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock   |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------+---------+---------+---------+---------+
```

CLK			1.122	

Clock to Setup on destination clock current_state[3]_GND_104_o_Mux_515_o

	Src:Rise	Src:Fall	Src:Rise	Src:Fall
Source Clock	Dest:Rise	Dest:Rise	Dest:Fall	Dest:Fall
CLK			1.120	

Clock to Setup on destination clock current_state[3]_GND_105_o_Mux_517_o

	Src:Rise	Src:Fall	Src:Rise	Src:Fall
Source Clock	Dest:Rise	Dest:Rise	Dest:Fall	Dest:Fall
CLK			1.136	

Clock to Setup on destination clock current_state[3]_GND_12_o_Mux_417_o

	Src:Rise	Src:Fall	Src:Rise	Src:Fall
Source Clock	Dest:Rise	Dest:Rise	Dest:Fall	Dest:Fall
CLK			1.136	
Mmux_current_state[3]_GND_16_o_Mux_422_o11			1.153	
current_state[3]_GND_12_o_Mux_417_o			1.117	

Clock to Setup on destination clock current_state[3]_GND_16_o_Mux_422_o

	Src:Rise	Src:Fall	Src:Rise	Src:Fall
Source Clock	Dest:Rise	Dest:Rise	Dest:Fall	Dest:Fall
CLK			0.959	

Clock to Setup on destination clock current_state[3]_GND_18_o_Mux_426_o

	Src:Rise	Src:Fall	Src:Rise	Src:Fall
Source Clock	Dest:Rise	Dest:Rise	Dest:Fall	Dest:Fall
CLK			1.122	

Clock to Setup on destination clock current_state[3]_GND_19_o_Mux_428_o

	Src:Rise	Src:Fall	Src:Rise	Src:Fall
Source Clock	Dest:Rise	Dest:Rise	Dest:Fall	Dest:Fall
CLK			1.136	

Clock to Setup on destination clock current_state[3]_GND_20_o_Mux_429_o

	Src:Rise	Src:Fall	Src:Rise	Src:Fall
Source Clock	Dest:Rise	Dest:Rise	Dest:Fall	Dest:Fall
CLK			1.263	
current_state[3]_GND_20_o_Mux_429_o			1.135	

Clock to Setup on destination clock current_state[3]_GND_24_o_Mux_433_o

	Src:Rise	Src:Fall	Src:Rise	Src:Fall
Source Clock	Dest:Rise	Dest:Rise	Dest:Fall	Dest:Fall

CLK			1.263	
current_state[3]_GND_24_o_Mux_433_o			1.135	

Clock to Setup on destination clock current_state[3]_GND_28_o_Mux_437_o

	Src:Rise	Src:Fall	Src:Rise	Src:Fall
Source Clock	Dest:Rise	Dest:Rise	Dest:Fall	Dest:Fall
CLK			1.263	
current_state[3]_GND_28_o_Mux_437_o			1.135	

Clock to Setup on destination clock current_state[3]_GND_2_o_Mux_83_o

	Src:Rise	Src:Fall	Src:Rise	Src:Fall
Source Clock	Dest:Rise	Dest:Rise	Dest:Fall	Dest:Fall
CLK			2.051	
current_state[3]_GND_12_o_Mux_417_o			2.166	
current_state[3]_GND_20_o_Mux_429_o			3.838	
current_state[3]_GND_24_o_Mux_433_o			3.048	
current_state[3]_GND_28_o_Mux_437_o			5.399	
current_state[3]_GND_32_o_Mux_441_o			4.618	
current_state[3]_GND_36_o_Mux_445_o			3.102	
current_state[3]_GND_40_o_Mux_449_o			3.873	
current_state[3]_GND_44_o_Mux_453_o			5.443	
current_state[3]_GND_48_o_Mux_457_o			4.663	
current_state[3]_GND_52_o_Mux_461_o			5.006	
current_state[3]_GND_56_o_Mux_465_o			4.226	
current_state[3]_GND_60_o_Mux_469_o			3.446	
current_state[3]_GND_64_o_Mux_473_o			2.656	
current_state[3]_GND_68_o_Mux_477_o			3.971	
current_state[3]_GND_72_o_Mux_481_o			3.181	
current_state[3]_GND_76_o_Mux_485_o			5.531	
current_state[3]_GND_7_o_Mux_412_o			3.259	
current_state[3]_GND_80_o_Mux_489_o			4.751	
current_state[3]_GND_84_o_Mux_493_o			2.528	
current_state[3]_GND_88_o_Mux_497_o			3.179	
current_state[3]_GND_92_o_Mux_501_o			2.573	
current_state[3]_GND_96_o_Mux_505_o			1.793	

Clock to Setup on destination clock current_state[3]_GND_32_o_Mux_441_o

	Src:Rise	Src:Fall	Src:Rise	Src:Fall
Source Clock	Dest:Rise	Dest:Rise	Dest:Fall	Dest:Fall
CLK			1.263	
current_state[3]_GND_32_o_Mux_441_o			1.135	

Clock to Setup on destination clock current_state[3]_GND_36_o_Mux_445_o

	Src:Rise	Src:Fall	Src:Rise	Src:Fall
Source Clock	Dest:Rise	Dest:Rise	Dest:Fall	Dest:Fall
CLK			1.263	
current_state[3]_GND_36_o_Mux_445_o			1.135	

Clock to Setup on destination clock current_state[3]_GND_40_o_Mux_449_o

	Src:Rise	Src:Fall	Src:Rise	Src:Fall
Source Clock	Dest:Rise	Dest:Rise	Dest:Fall	Dest:Fall

CLK			1.263	
current_state[3]_GND_40_o_Mux_449_o			1.135	

Clock to Setup on destination clock current_state[3]_GND_44_o_Mux_453_o

	Src:Rise	Src:Fall	Src:Rise	Src:Fall
Source Clock	Dest:Rise	Dest:Rise	Dest:Fall	Dest:Fall
CLK			1.263	
current_state[3]_GND_44_o_Mux_453_o			1.135	

Clock to Setup on destination clock current_state[3]_GND_48_o_Mux_457_o

	Src:Rise	Src:Fall	Src:Rise	Src:Fall
Source Clock	Dest:Rise	Dest:Rise	Dest:Fall	Dest:Fall
CLK			1.263	
current_state[3]_GND_48_o_Mux_457_o			1.135	

Clock to Setup on destination clock current_state[3]_GND_52_o_Mux_461_o

	Src:Rise	Src:Fall	Src:Rise	Src:Fall
Source Clock	Dest:Rise	Dest:Rise	Dest:Fall	Dest:Fall
CLK			1.263	
current_state[3]_GND_52_o_Mux_461_o			1.135	

Clock to Setup on destination clock current_state[3]_GND_56_o_Mux_465_o

	Src:Rise	Src:Fall	Src:Rise	Src:Fall
Source Clock	Dest:Rise	Dest:Rise	Dest:Fall	Dest:Fall
CLK			1.263	
current_state[3]_GND_56_o_Mux_465_o			1.135	

Clock to Setup on destination clock current_state[3]_GND_60_o_Mux_469_o

	Src:Rise	Src:Fall	Src:Rise	Src:Fall
Source Clock	Dest:Rise	Dest:Rise	Dest:Fall	Dest:Fall
CLK			1.263	
current_state[3]_GND_60_o_Mux_469_o			1.135	

Clock to Setup on destination clock current_state[3]_GND_64_o_Mux_473_o

	Src:Rise	Src:Fall	Src:Rise	Src:Fall
Source Clock	Dest:Rise	Dest:Rise	Dest:Fall	Dest:Fall
CLK			1.263	
current_state[3]_GND_64_o_Mux_473_o			1.135	

Clock to Setup on destination clock current_state[3]_GND_68_o_Mux_477_o

	Src:Rise	Src:Fall	Src:Rise	Src:Fall
Source Clock	Dest:Rise	Dest:Rise	Dest:Fall	Dest:Fall
CLK			1.263	
current_state[3]_GND_68_o_Mux_477_o			1.135	

Clock to Setup on destination clock current_state[3]_GND_72_o_Mux_481_o

Source Clock	Src:Rise|Dest:Rise	Src:Fall|Dest:Rise	Src:Rise|Dest:Fall	Src:Fall|Dest:Fall
CLK			1.263	
current_state[3]_GND_72_o_Mux_481_o			1.135	

Clock to Setup on destination clock current_state[3]_GND_76_o_Mux_485_o

Source Clock	Src:Rise|Dest:Rise	Src:Fall|Dest:Rise	Src:Rise|Dest:Fall	Src:Fall|Dest:Fall
CLK			1.263	
current_state[3]_GND_76_o_Mux_485_o			1.135	

Clock to Setup on destination clock current_state[3]_GND_7_o_Mux_412_o

Source Clock	Src:Rise|Dest:Rise	Src:Fall|Dest:Rise	Src:Rise|Dest:Fall	Src:Fall|Dest:Fall
CLK			2.240	
Mmux_current_state[3]_GND_16_o_Mux_422_o11			2.081	
current_state[3]_GND_12_o_Mux_417_o			2.080	
current_state[3]_GND_7_o_Mux_412_o			1.523	

Clock to Setup on destination clock current_state[3]_GND_80_o_Mux_489_o

Source Clock	Src:Rise|Dest:Rise	Src:Fall|Dest:Rise	Src:Rise|Dest:Fall	Src:Fall|Dest:Fall
CLK			1.263	
current_state[3]_GND_80_o_Mux_489_o			1.135	

Clock to Setup on destination clock current_state[3]_GND_84_o_Mux_493_o

Source Clock	Src:Rise|Dest:Rise	Src:Fall|Dest:Rise	Src:Rise|Dest:Fall	Src:Fall|Dest:Fall
CLK			1.263	
current_state[3]_GND_84_o_Mux_493_o			1.139	

Clock to Setup on destination clock current_state[3]_GND_88_o_Mux_497_o

Source Clock	Src:Rise|Dest:Rise	Src:Fall|Dest:Rise	Src:Rise|Dest:Fall	Src:Fall|Dest:Fall
CLK			1.263	
current_state[3]_GND_88_o_Mux_497_o			1.135	

Clock to Setup on destination clock current_state[3]_GND_92_o_Mux_501_o

Source Clock	Src:Rise|Dest:Rise	Src:Fall|Dest:Rise	Src:Rise|Dest:Fall	Src:Fall|Dest:Fall
CLK			1.263	
current_state[3]_GND_92_o_Mux_501_o			1.135	

```
Clock to Setup on destination clock current_state[3]_GND_96_o_Mux_505_o
---------------------------------+---------+---------+---------+---------+
                                 | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock                     |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------------------------+---------+---------+---------+---------+
CLK                              |         |         |    1.263|         |
current_state[3]_GND_96_o_Mux_505_o|         |         |    1.135|         |
---------------------------------+---------+---------+---------+---------+

=========================================================================


Total REAL time to Xst completion: 9.00 secs
Total CPU time to Xst completion: 8.63 secs

-->


Total memory usage is 603872 kilobytes

Number of errors   :    0 (   0 filtered)
Number of warnings :  105 (   0 filtered)
Number of infos    :    2 (   0 filtered)
```

Conclusion:

Overall, the Verilog design does model the overall expected behavior from the Vending Machine FSM. This required the creation of multiple intermediate states that could be used to simulate a vending machine.

One of the biggest challenges I had was creating 2D arrays that actually be synthesized. I kept getting Verilog errors for various different aspects (especially my arrays for counters and costs). Therefore, I had to switch to implementing each counter independently, and switched to using 6 states to represent the object with various costs. The second issue I had was not knowing to use negedge in my test bench, causing unpredictable behaviour as well as lack of change of states from time to time. The third issue I had was creating counters to keep track of the missed cycles in between different states - for this, I realized that the only way to do it was to create and manage independent flags - very similar to what is seen in C code.

This lab was definitely challenging and much harder than it initially looked.