CS M152A - Introduction to Digital Design Lab

Project 1: Getting to know Verilog and Xilinx ISE

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Introduction and Requirements

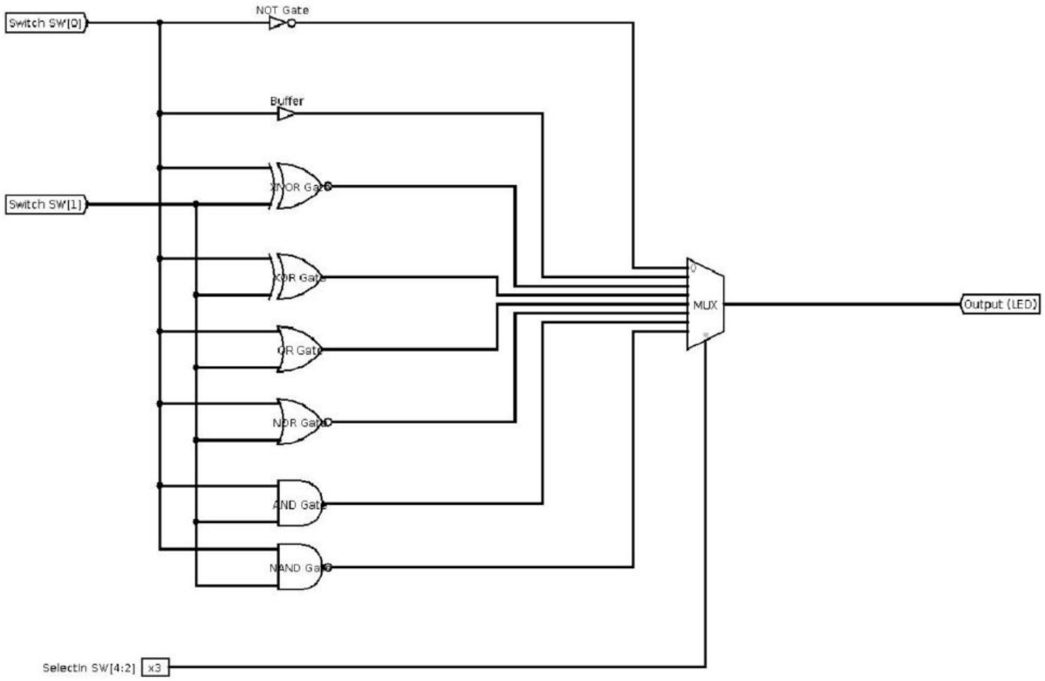
The main goal of this lab is to explore simple combinational and sequential circuits. In particular, it focuses on understanding different aspects of Verilog, especially how to write a module, understand schematics, validating different designs, writing test benches, and visualizing and interpreting simulations. In this lab, four different modules were designed:

1. An 8:1 multiplexer using a combination of gates such as NAND, AND, NOR, etc.
2. A 4-bit counter using a gate-level hardware description based on a given schematic.
3. A 4-bit counter using a higher-level abstraction without flip-flops and gate-level logic.
4. A 1Hz clock-divider from a 10KHz input clock.

Each of the four tasks has its own corresponding project, where a single module or a group of modules were used to simulate the required behavior, and a corresponding test bench was created for simulation. The inputs to the design and the hardware required for their implementations are described in-depth in the next section.

Design Description

8:1 Multiplexer

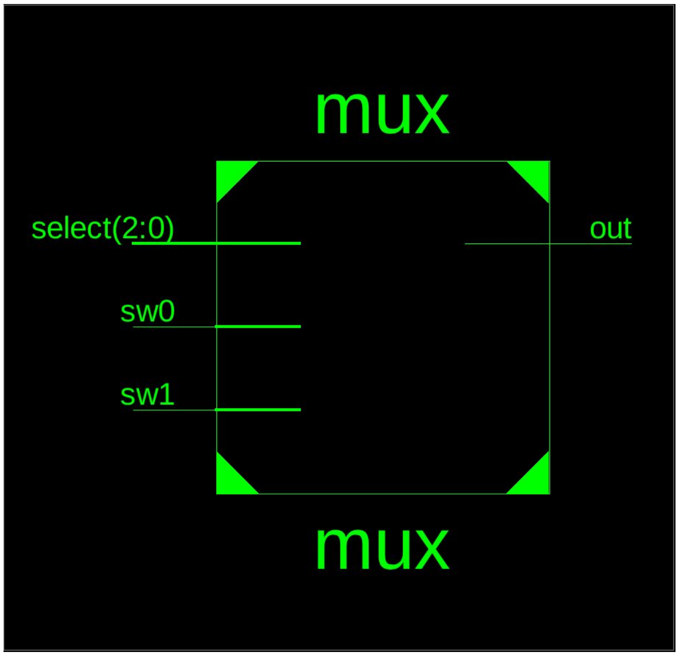


Based on the above schematic, we can see that there are three inputs and one output for the 8:1 MUX.

Name in module	Type	Input or Output	Size	Hardware Map (from Schematic)
sw0	wire	Input	1 bit	Switch SW[0]
sw1	wire	Input	1 bit	Switch SW[1]
select	wire	Input	3 bits	Selectin SW[4:2]
out	reg	Output	1 bit	Output LED

To model the hardware components, sw0 and sw1 were mapped to wires of 1 bit each, and the Switch SW[4:2] (select) was also mapped to a 3-bit wire. The output is a register instead of an LED, returning either 0 or 1 depending on which bit is selected using *select*, thereby allowing it to function as a multiplexer. If we were to use a .ucf file, the switches would be mapped to their respective nets, and out would be mapped to one of the LEDs available on the Nexsy3 FPGA board.

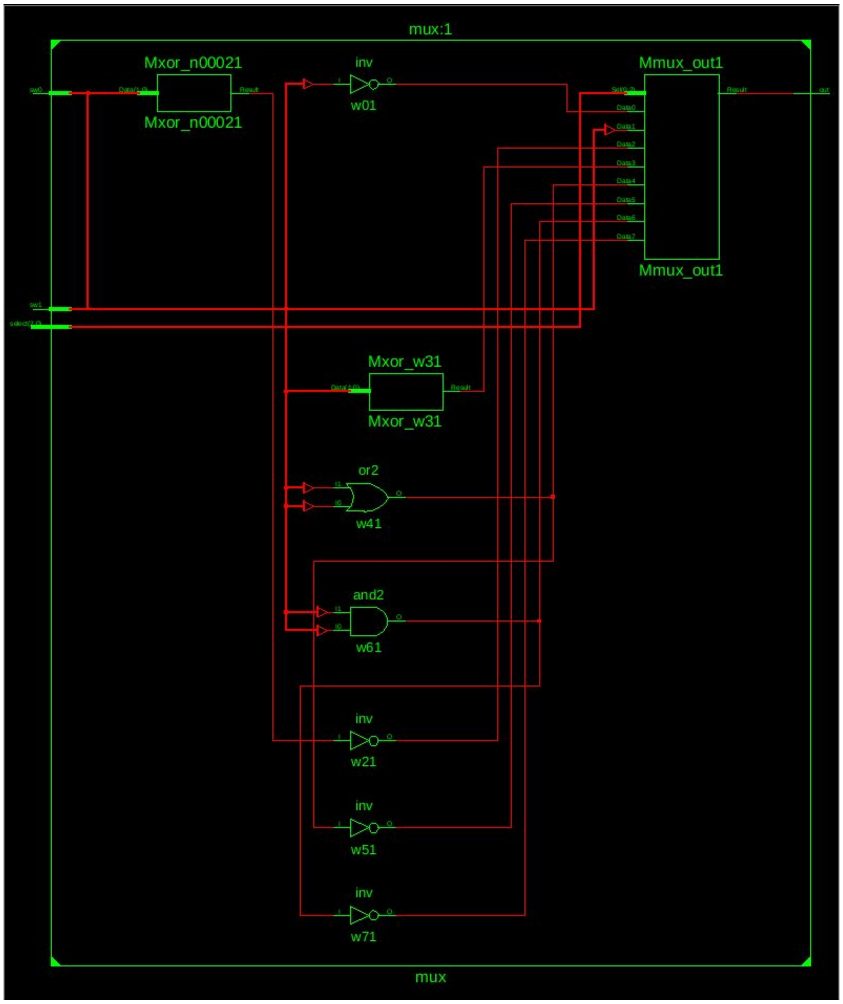
The mux was implemented as a single top-level module called *mux* with no other nested modules.



The selectin input, sw0, and sw1 switches were wrapped in an always@ block to ensure that the output register will be updated anytime any of these values change. Based on the wiring in the schematic, we can see that each of the 8 channels in the MUX have a different output based on the gate/logic combination connected to that particular channel:

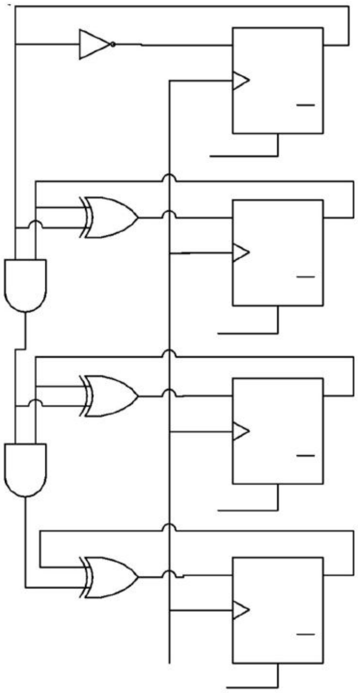
Select	Gate Logic
000	NOT: sw0
001	BUFFER: sw0
010	XNOR: sw0, sw1
011	XOR: sw0, sw1
100	OR: sw0, sw1
101	NOR: sw0, sw1
110	AND: sw0, sw1
111	NAND: sw0, sw1

This can be seen in the detailed top-level module diagram.



In this schematic, it is interesting to note that the not gate is implemented as an inverter *INV*, and the XNOR gate is implemented as an *XOR* followed by an *INV*. The input selectin can be changed during simulation to observe values from different channels based on the values for the input wires sw0 and sw1.

4-bit counter using the schematic



The way a 4-bit counter works is that it starts at an initial state (IS), say 0000, and increments to the next state (NS), 0001, at each clock cycle/ positive edge of the clock. When the IS is 1111, it must go back to 0000 (the new NS). Based on the above schematic, we can see that this is a sequential circuit that can be modeled using positive edge-triggered D flip-flops to simulate.

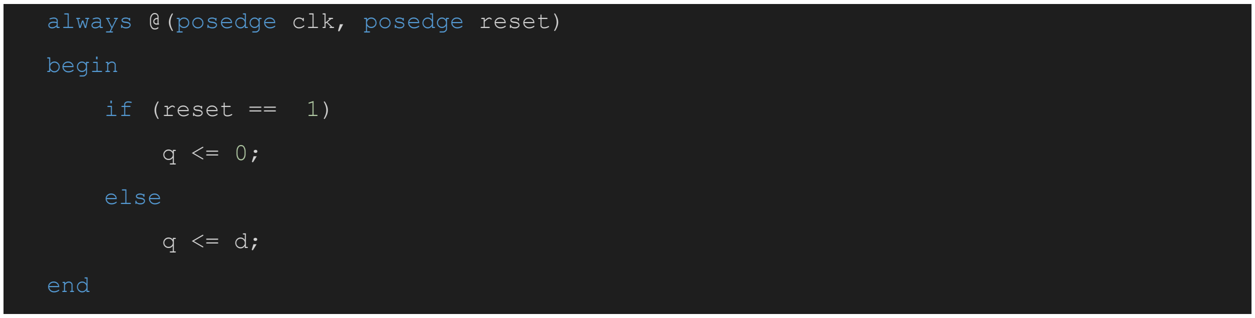
Therefore, since there are no predefined primitives or modules for D flip-flops, we must design a D flip-flop module from scratch that will be used to simulate the top level counter module. For the D flip-flop:

Name in module	Type	Input or Output	Size
clk	wire	Input	1 bit
reset	wire	Input	1 bit
d	wire	Input	1 bit
q	reg	Output	1 bit

The D-Flip Flop makes use of both reset and clk, which are positive edge triggered. d corresponds to input data, and q corresponds to the output from the flip-flop. For the D-Flip Flop, we can draw the excitation table as follows:

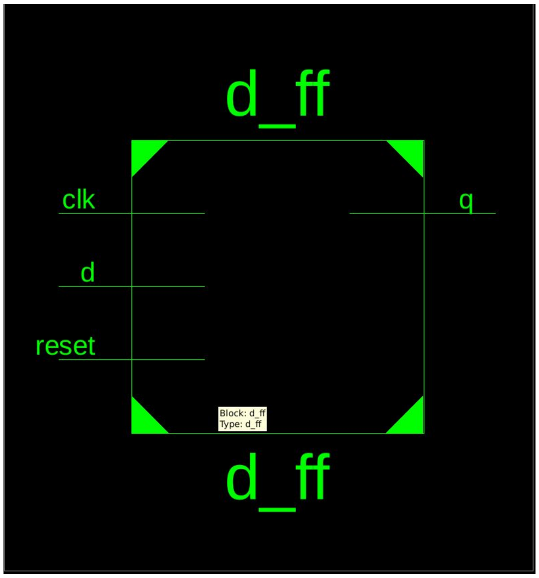
Present State (Q)	Input (D)	Next State (Q+)
0	0	0
0	1	1
1	0	0
1	1	1

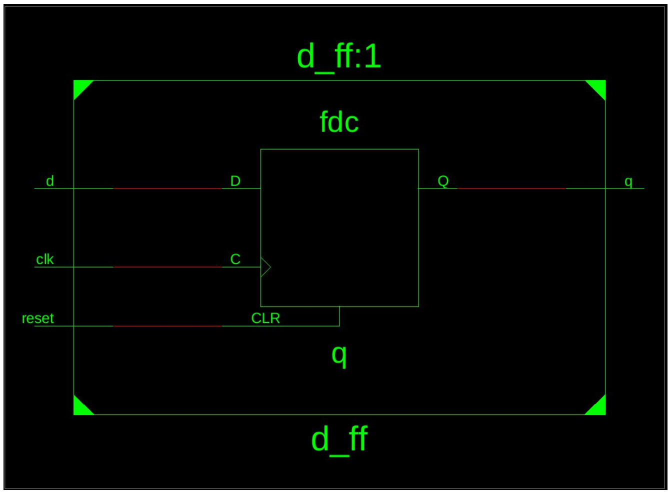
Therefore, based on the excitation table, we can determine that Q+ = D. To simulate this behavior, it was easy to model the flip flop so that q = d after every clock cycle:



```
always @(posedge clk, posedge reset)
begin
    if (reset ==  1)
        q <= 0;
    else
        q <= d;
end
```

For the D-flip flop, here are the top-level and detailed schematic diagrams:





Since there are 4 flip-flops in the output, it makes sense that there are 4 inputs that go into the schematic counter. Therefore,

Name in module	Type	Input or Output	Size
clk	wire	Input	1 bit
reset	wire	Input	1 bit
d0	wire	Input	1 bit
d1	wire	Input	1 bit
d2	wire	Input	1 bit
d3	wire	Input	1 bit
result	reg	Output	4 bits

To determine the behavior of the 4-bit counter top-level module itself, a truth table was created as follows:

Present State (Q3 Q2 Q1 Q0)	Next State (Q3+ Q2+ Q1+ Q0+)	D3	D2	D1	D0
0000	0001	0	0	0	1
0001	0010	0	0	1	0
0010	0011	0	0	1	1
0011	0100	0	1	0	0
0100	0101	0	1	0	1
0101	0110	0	1	1	0
0110	0111	0	1	1	1
0111	1000	1	0	0	0
1000	1001	1	0	0	1
1001	1010	1	0	1	0
1010	1011	1	0	1	1
1011	1100	1	1	0	0

1100	1101	1	1	0	1
1101	1110	1	1	1	0
1110	1111	1	1	1	1
1111	0000	0	0	0	0

The truth table was used to create K-maps for D3+, D2+, D1+, and D0+. From the K-maps, it was seen that:

- D3: Q3Q2′ + Q3Q0′ + Q3Q1′ + Q3’Q2Q1Q0
- D2+: Q2Q0′ + Q2Q1′ + Q2’Q1Q0
- D1+: Q1’Q0 + Q1Q0′ = Q1 ⊕ Q0
- D0+: Q0′

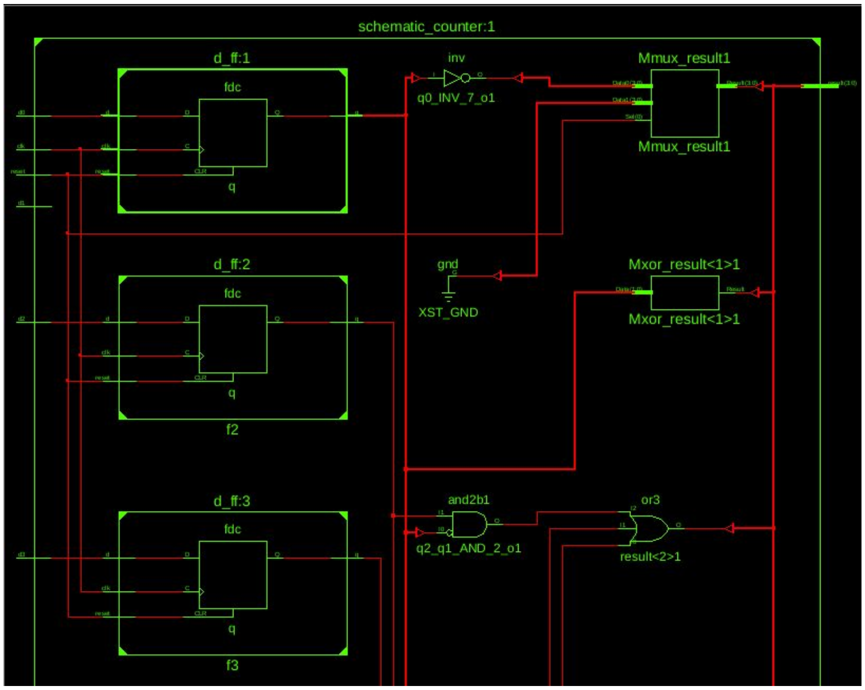
<u>Module Interaction</u>: The top-level module, *schematic_counter*, creates 4 instances of D flip-flop modules, *d_ff*. In these modules, the same clk and reset signals are passed, but different d and q signals are passed, with specific d and q signals for each of the 4 *d_ff* modules.

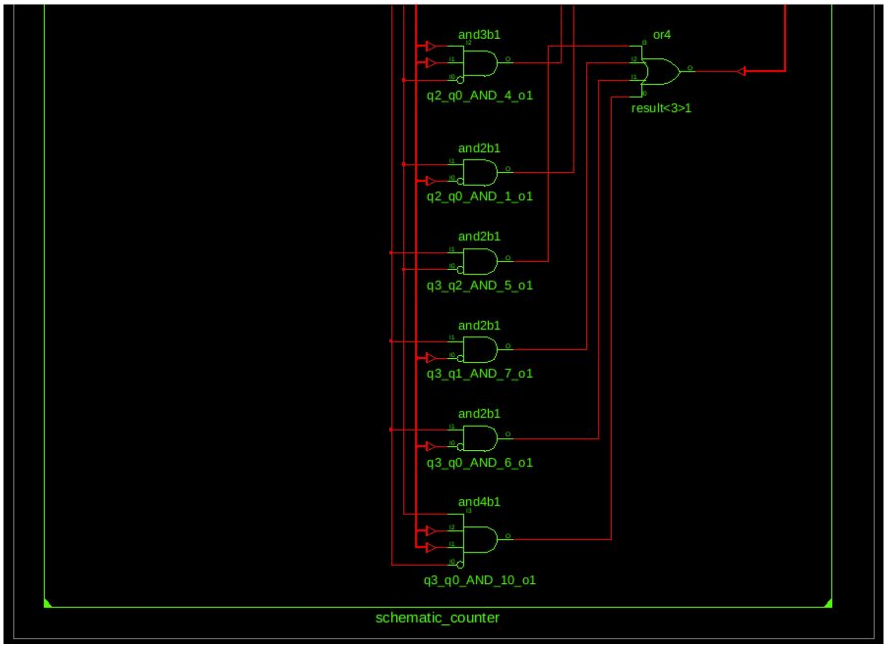
```
// Create and initialize 4 d-flop-flops
d_ff f0(.clk(clk), .reset(reset), .d(d0), .q(q0));
d_ff f1(.clk(clk), .reset(reset), .d(d1), .q(q1));
d_ff f2(.clk(clk), .reset(reset), .d(d2), .q(q2));
d_ff f3(.clk(clk), .reset(reset), .d(d3), .q(q3));
```

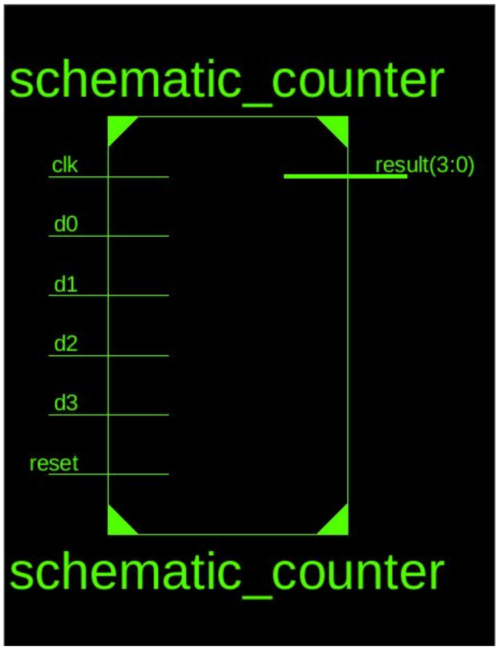
Since we know the relationship between the previous state and next state for each of the 4 data wires, D3 - D0, we can simply update these using the following always block:

```
always @(reset, q0, q1, q2, q3)
begin
    if (reset ==  1)
        result <= 4'b0;
    else
        //D0 = Q0′
        result[0] <= ~q0;
        //D1 = Q1'Q0 + Q1Q0′  = Q1 ⊕ Q0
        result[1] <= q1^q0;
        //D2 = Q2Q0′ + Q2Q1′ + Q2'Q1Q0
        result[2] <= (q2&(~q0))|(q2&(~q1))|((~q2)&q1&q0);
        //D3 = Q3Q2′ + Q3Q0′ + Q3Q1′ + Q3'Q2Q1Q0
        result[3] <= (q3&(~q2))|(q3&(~q0))|(q3&(~q1))|((~q3)&q2&q1&q0);
end
```

The reason the always@ block does not include clk, is because changes in clk are already handled by the individual d_ff modules. result, which is a 4-bit register, updates each of its bits based on the relationships we mapped from the k-maps. Therefore, this ensures that we capture the logic correctly. Here is the detailed level schematic for the 4-bit schematic counter (split into two so each part can be zoomed into).







4-bit counter using higher-level abstraction

The third module created for this lab was the same 4-bit counter, but with a higher-level abstraction that VHDL provides. Instead of using gates and flip-flops, which then requires us to create k-maps and excitation tables, we can instead just use a 4-bit register that starts at 0000 and increment it to current value += 1 at each trigger of the positive edge of the clock. Naturally then, because of bit overflow, once the counter reaches 1111, it will go back to 0000, which is the expected and desired behavior. The advantage of using this is manifold: simpler logic, faster debugging, simpler module design (can be seen from the schematic), and only one higher-level module. Therefore, this module will only require the following input and output wires and registers:

Name in module	Type	Input or Output	Size
clk	wire	Input	1 bit
reset	wire	Input	1 bit
a	reg	Output	4 bit

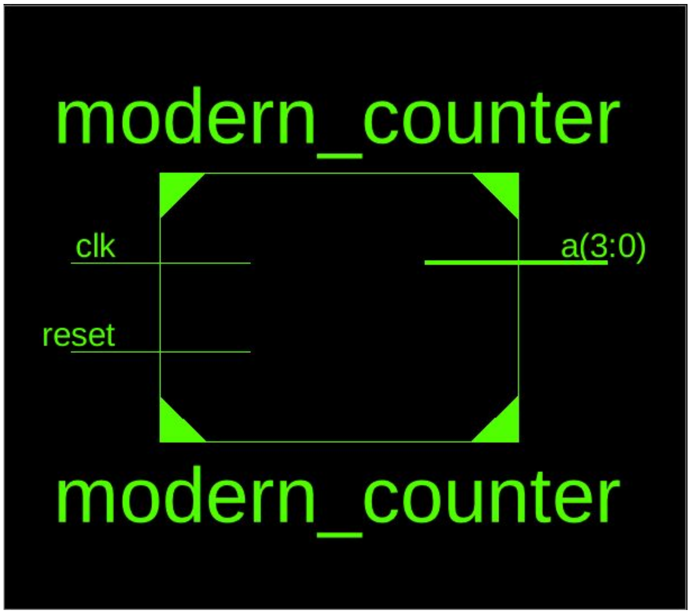
We initialize a to 0000 before simulating the incremental counts for each positive edge-triggered clock signal. This can be done simply using the code block shown below:

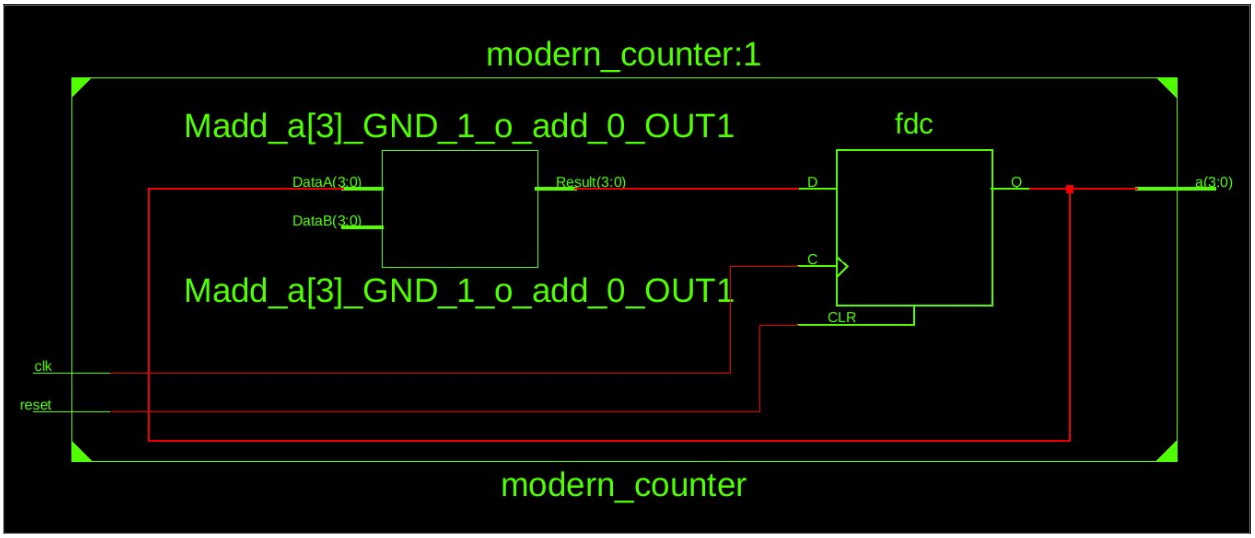
```
always@(posedge clk, posedge reset)
begin
```

```
        if (reset)
            a <= 4'b0000;
        else
            a <= a + 1'b1;
    end
```

This always@ block simply increments a by one bit every clock cycle and resets a to 0000 if the reset positive edge is triggered during a simulation.

Of course, because of the simpler design, we get a much simpler top and detailed level schematic for this counter.





Clock-divider

The project required us to convert a 10KHz clock to a 1Hz clock signal. This has two parts - The first, is to design a module that can actually simulate a 1Hz signal for a 10Hz clock, and the second is to actually simulate a 10KHz clock on the test bench. Both components are challenging in their own respects for this part.

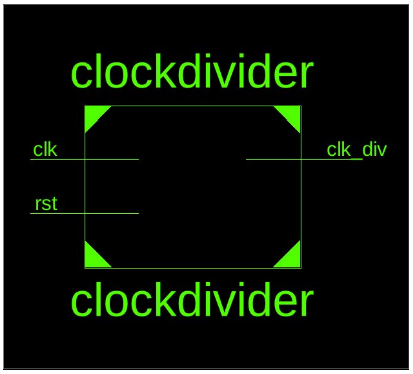
Therefore, using ideas from the high-level 4-bit counter, this module can be designed as follows:

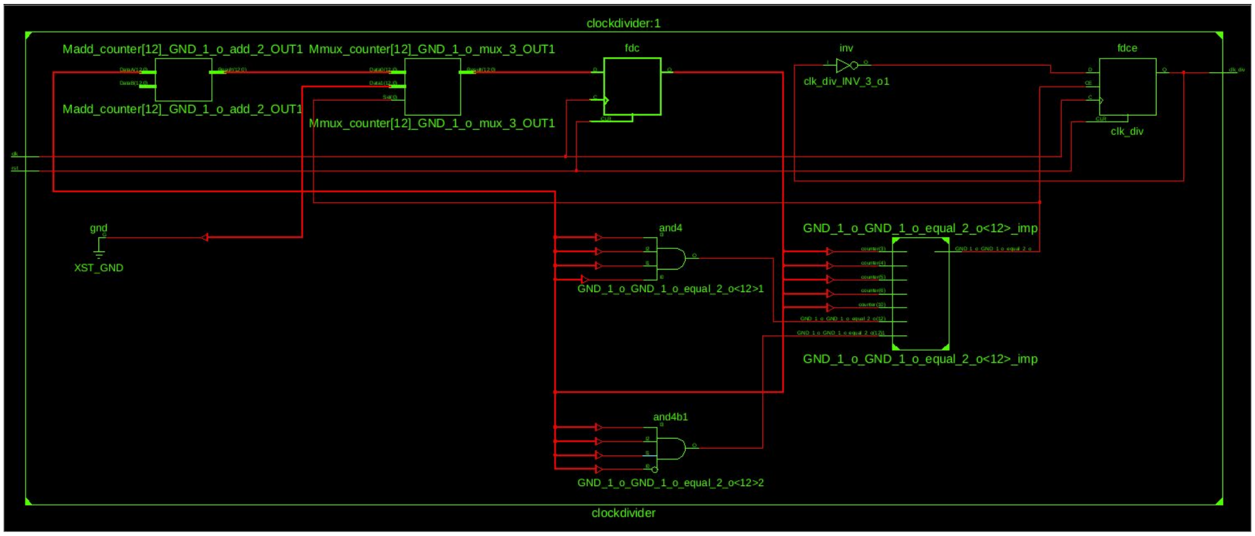
Name in module	Type	Input or Output	Size
clk	wire	Input	1 bit
rst	wire	Input	1 bit
clk_div	reg	Output	1 bit

The goal is to get clk_div to flip to 1 at a rate of 1Hz (F2), given the 10KHz (F1) input frequency signal. To create this clock, we can see that, the relationship can be roughly modeled using the equation F1/k = F2, where k represents the number of cycles of F1 that correspond to 1 cycle of F2. In this case, since F1 is 10KHz and F2 is 1Hz, we get k = 10000. Therefore, F2 will need to flip its bit from 0 to 1 after k/2, or 5000 cycles. Therefore, if we create a counter that counts from 0 to 4999, we should be able to simulate this idea fairly accurately. Within this module, internally, it will be important to create a counter register than can increment from 0 to 4999 and then reset it back to 0 after that. We can divide this whole idea into 3 parts:

1. If reset is 1, set the counter to 0 and clk_div signal to 0.
2. If counter is 4999, reset counter to 0 and flip clk_div signal: clk_div <= ~clk_div
3. Otherwise, simply increment counter for every posedge trigger of the clock.

This results in the following schematic diagrams:

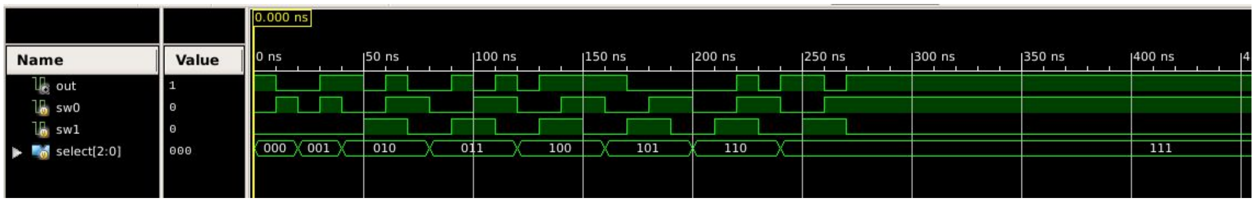



clockdivider:1
Madd_counter[12]_GND_1_o_add_2_OUT1
Mmux_counter[12]_GND_1_o_mux_3_OUT1
fdc
inv
clk_div_INV_3_o1
fdce
Madd_counter[12]_GND_1_o_add_2_OUT1
Mmux_counter[12]_GND_1_o_mux_3_OUT1
clk_div
gnd
XST_GND
and4
GND_1_o_GND_1_o_equal_2_o<12>_imp
GND_1_o_GND_1_o_equal_2_o<12>1
GND_1_o_GND_1_o_equal_2_o<12>_imp
and4b1
GND_1_o_GND_1_o_equal_2_o<12>2
clockdivider

Implementation for the 10KHz clock can be seen in the testbench module for this project.

Simulation Documentation

8:1 Multiplexer



Name	Value
out	1
sw0	0
sw1	0
select[2:0]	000

For the multiplexer, these are the simulation waveforms. In particular, all combinations and permutations were tested:

Test: Not; sw0=0, sw1=0, sel=000, out=1 Test: Not; sw0=1, sw1=0, sel=000, out=0	Test: Buf; sw0=0, sw1=0, sel=001, out=0 Test: Buf; sw0=1, sw1=0, sel=001, out=1
Test: XNOR; sw0=0, sw1=0, sel=010, out=1 Test: XNOR; sw0=0, sw1=1, sel=010, out=0 Test: XNOR; sw0=1, sw1=1, sel=010, out=1 Test: XNOR; sw0=1, sw1=0, sel=010, out=0	Test: XOR; sw0=0, sw1=0, sel=011, out=0 Test: XOR; sw0=0, sw1=1, sel=011, out=1 Test: XOR; sw0=1, sw1=1, sel=011, out=0 Test: XOR; sw0=1, sw1=0, sel=011, out=1
Test: NOR; sw0=0, sw1=0, sel=101, out=1 Test: NOR; sw0=0, sw1=1, sel=101, out=0 Test: NOR; sw0=1, sw1=1, sel=101, out=0 Test: NOR; sw0=1, sw1=0, sel=101, out=0	Test: OR; sw0=0, sw1=0, sel=100, out=0 Test: OR; sw0=0, sw1=1, sel=100, out=1 Test: OR; sw0=1, sw1=1, sel=100, out=1 Test: OR; sw0=1, sw1=0, sel=100, out=1
Test: NAND; sw0=0, sw1=0, sel=111, out=1 Test: NAND; sw0=0, sw1=1, sel=111, out=1	Test: AND; sw0=0, sw1=0, sel=110, out=0 Test: AND; sw0=0, sw1=1, sel=110, out=0

Test: NAND; sw0=1, sw1=1, sel=111, out=0 Test: NAND; sw0=1, sw1=0, sel=111, out=1	Test: AND; sw0=1, sw1=1, sel=110, out=1 Test: AND; sw0=1, sw1=0, sel=110, out=0

Based on the waveforms from simulation and output from the testbench, it appears that there are no obvious bugs that can be seen from the simulation.

/// Synthesis Report

```
Release 14.7 - xst P.20131013 (lin64)
Copyright (c) 1995-2013 Xilinx, Inc.  All rights reserved.
-->
Parameter TMPDIR set to xst/projnav.tmp


Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.05 secs

-->
Parameter xsthdpdir set to xst


Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.05 secs

-->
Reading design: mux.prj

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            8.4.4) Timing Details
            8.4.5) Cross Clock Domains Report


=========================================================================
*                      Synthesis Options Summary                        *
=========================================================================
---- Source Parameters
Input File Name                    : "mux.prj"
Ignore Synthesis Constraint File   : NO

---- Target Parameters
Output File Name                   : "mux"
Output Format                      : NGC
Target Device                      : xc7a100t-3-csg324

---- Source Options
Top Module Name                    : mux
Automatic FSM Extraction           : YES
FSM Encoding Algorithm             : Auto
Safe Implementation                : No
FSM Style                          : LUT
RAM Extraction                     : Yes
RAM Style                          : Auto
ROM Extraction                     : Yes
Shift Register Extraction          : YES
ROM Style                          : Auto
Resource Sharing                   : YES
Asynchronous To Synchronous        : NO
Shift Register Minimum Size        : 2
Use DSP Block                      : Auto
Automatic Register Balancing       : No

---- Target Options
LUT Combining                      : Auto
Reduce Control Sets                : Auto
Add IO Buffers                     : YES
Global Maximum Fanout              : 100000
Add Generic Clock Buffer(BUFG)     : 32
Register Duplication               : YES
Optimize Instantiated Primitives   : NO
Use Clock Enable                   : Auto
Use Synchronous Set                : Auto
Use Synchronous Reset              : Auto
Pack IO Registers into IOBs        : Auto
Equivalent register Removal        : YES

---- General Options
Optimization Goal                  : Speed
Optimization Effort                : 1
Power Reduction                    : NO
Keep Hierarchy                     : No
Netlist Hierarchy                  : As_Optimized
RTL Output                         : Yes
Global Optimization                : AllClockNets
Read Cores                         : YES
Write Timing Constraints           : NO
Cross Clock Analysis               : NO
Hierarchy Separator                : /
Bus Delimiter                      : <>
Case Specifier                     : Maintain
Slice Utilization Ratio            : 100
BRAM Utilization Ratio             : 100
DSP48 Utilization Ratio            : 100
Auto BRAM Packing                  : NO
Slice Utilization Ratio Delta      : 5

=========================================================================


=========================================================================
*                          HDL Parsing                                  *
=========================================================================
Analyzing Verilog file "/home/ise/Project1/mux.v" into library work
Parsing module <mux>.

=========================================================================
*                            HDL Elaboration                            *
=========================================================================

Elaborating module <mux>.
WARNING:HDLCompiler:91 - "/home/ise/Project1/mux.v" Line 50: Signal <w0>
missing in the sensitivity list is added for synthesis purposes. HDL and
post-synthesis simulations may differ as a result.
WARNING:HDLCompiler:91 - "/home/ise/Project1/mux.v" Line 51: Signal <w1>
missing in the sensitivity list is added for synthesis purposes. HDL and
post-synthesis simulations may differ as a result.
WARNING:HDLCompiler:91 - "/home/ise/Project1/mux.v" Line 52: Signal <w2>
missing in the sensitivity list is added for synthesis purposes. HDL and
post-synthesis simulations may differ as a result.
WARNING:HDLCompiler:91 - "/home/ise/Project1/mux.v" Line 53: Signal <w3>
missing in the sensitivity list is added for synthesis purposes. HDL and
post-synthesis simulations may differ as a result.
WARNING:HDLCompiler:91 - "/home/ise/Project1/mux.v" Line 54: Signal <w4>
missing in the sensitivity list is added for synthesis purposes. HDL and
post-synthesis simulations may differ as a result.
```

```
WARNING:HDLCompiler:91 - "/home/ise/Project1/mux.v" Line 55: Signal <w5>
missing in the sensitivity list is added for synthesis purposes. HDL and
post-synthesis simulations may differ as a result.
WARNING:HDLCompiler:91 - "/home/ise/Project1/mux.v" Line 56: Signal <w6>
missing in the sensitivity list is added for synthesis purposes. HDL and
post-synthesis simulations may differ as a result.
WARNING:HDLCompiler:91 - "/home/ise/Project1/mux.v" Line 57: Signal <w7>
missing in the sensitivity list is added for synthesis purposes. HDL and
post-synthesis simulations may differ as a result.
WARNING:HDLCompiler:91 - "/home/ise/Project1/mux.v" Line 58: Signal <out>
missing in the sensitivity list is added for synthesis purposes. HDL and
post-synthesis simulations may differ as a result.

=========================================================================
*                           HDL Synthesis                               *
=========================================================================

Synthesizing Unit <mux>.
    Related source file is "/home/ise/Project1/mux.v".
    Found 1-bit 8-to-1 multiplexer for signal <out> created at line 49.
    Summary:
      inferred   1 Multiplexer(s).
Unit <mux> synthesized.

=========================================================================
HDL Synthesis Report

Macro Statistics
# Multiplexers                                         : 1
 1-bit 8-to-1 multiplexer                              : 1
# Xors                                                 : 2
 1-bit xor2                                            : 2

=========================================================================

=========================================================================
*                       Advanced HDL Synthesis                          *
=========================================================================


=========================================================================
Advanced HDL Synthesis Report

Macro Statistics
# Multiplexers                                         : 1
 1-bit 8-to-1 multiplexer                              : 1
# Xors                                                 : 2
 1-bit xor2                                            : 2
```

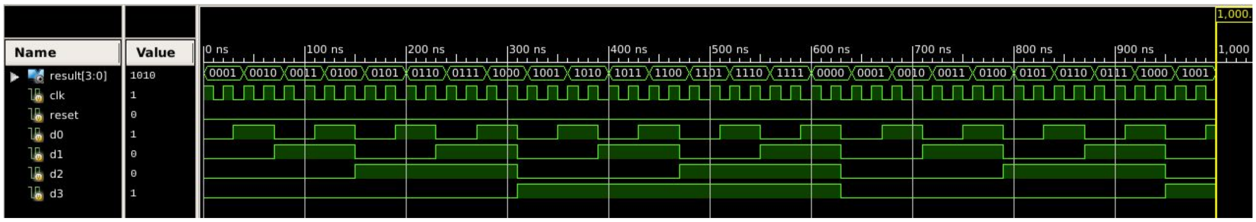
```
=========================================================================

=========================================================================
*                          Low Level Synthesis                          *
=========================================================================

Optimizing unit <mux> ...

Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block mux, actual ratio is 0.

Final Macro Processing ...

=========================================================================
Final Register Report

Found no macro
=========================================================================

=========================================================================
*                            Partition Report                           *
=========================================================================

Partition Implementation Status
-------------------------------

  No Partitions were found in this design.

-------------------------------

=========================================================================
*                             Design Summary                            *
=========================================================================

Top Level Output File Name         : mux.ngc

Primitive and Black Box Usage:
------------------------------
# BELS                             : 1
#      LUT5                        : 1
# IO Buffers                       : 6
#      IBUF                        : 5
#      OBUF                        : 1

Device utilization summary:
---------------------------
```

```
Selected Device : 7a100tcsg324-3


Slice Logic Utilization:
 Number of Slice LUTs:                    1  out of  63400     0%
    Number used as Logic:                 1  out of  63400     0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:      1
   Number with an unused Flip Flop:       1  out of      1   100%
   Number with an unused LUT:             0  out of      1     0%
   Number of fully used LUT-FF pairs:     0  out of      1     0%
   Number of unique control sets:         0

IO Utilization:
 Number of IOs:                           6
 Number of bonded IOBs:                   6  out of    210     2%

Specific Feature Utilization:

---------------------------
Partition Resource Summary:
---------------------------

  No Partitions were found in this design.

---------------------------



=========================================================================
Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
No clock signals found in this design

Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design

Timing Summary:
---------------
Speed Grade: -3
```

```
   Minimum period: No path found
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: No path found
   Maximum combinational path delay: 1.061ns

Timing Details:
---------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 5 / 1
-------------------------------------------------------------------------
Delay:               1.061ns (Levels of Logic = 3)
  Source:            select<1> (PAD)
  Destination:       out (PAD)

  Data Path: select<1> to out
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             1   0.001   0.683  select_1_IBUF (select_1_IBUF)
     LUT5:I0->O            1   0.097   0.279  Mmux_out_2_f7 (out_OBUF)
     OBUF:I->O                 0.000          out_OBUF (out)
    ----------------------------------------
    Total                      1.061ns (0.098ns logic, 0.963ns route)
                                       (9.2% logic, 90.8% route)

=========================================================================

Cross Clock Domains Report:
--------------------------

=========================================================================


Total REAL time to Xst completion: 8.00 secs
Total CPU time to Xst completion: 7.78 secs

-->


Total memory usage is 592624 kilobytes

Number of errors   :    0 (   0 filtered)
Number of warnings :    9 (   0 filtered)
Number of infos    :    0 (   0 filtered)
```

///

4-bit counter using the schematic



These are the waveforms observed for the 4-bit counter with gates and D flip-flops. It is evident from these waveforms that the counter is being incremented correctly, and in equal intervals. The counter was always reset to 0000 before starting, and the reset signal was passed in between to see if it would correctly restart from 0000. Here is some of the output from the simulation console log:

```
Counter=0000
Counter=0001
Counter=0010
Counter=0011
Counter=0100
    ……
Counter=1101
Counter=1110
Counter=1111
Counter=0000
```

There were no obvious bugs seen during execution, and the module appeared to work correctly from both pieces of supporting evidence.

/// Synthesis Report

```
Release 14.7 - xst P.20131013 (lin64)
Copyright (c) 1995-2013 Xilinx, Inc.  All rights reserved.
-->
Parameter TMPDIR set to xst/projnav.tmp


Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.04 secs

-->
Parameter xsthdpdir set to xst
```

```
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.04 secs

-->
Reading design: schematic_counter.prj

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            8.4.3) Timing Summary
            8.4.4) Timing Details
            8.4.5) Cross Clock Domains Report


=========================================================================
*                      Synthesis Options Summary                        *
=========================================================================
---- Source Parameters
Input File Name                    : "schematic_counter.prj"
Ignore Synthesis Constraint File   : NO

---- Target Parameters
Output File Name                   : "schematic_counter"
Output Format                      : NGC
Target Device                      : xc7a100t-3-csg324

---- Source Options
Top Module Name                    : schematic_counter
Automatic FSM Extraction           : YES
FSM Encoding Algorithm             : Auto
Safe Implementation                : No
FSM Style                          : LUT
RAM Extraction                     : Yes
RAM Style                          : Auto
ROM Extraction                     : Yes
Shift Register Extraction          : YES
ROM Style                          : Auto
Resource Sharing                   : YES
Asynchronous To Synchronous        : NO
```

```
Shift Register Minimum Size        : 2
Use DSP Block                      : Auto
Automatic Register Balancing       : No

---- Target Options
LUT Combining                      : Auto
Reduce Control Sets                : Auto
Add IO Buffers                     : YES
Global Maximum Fanout              : 100000
Add Generic Clock Buffer(BUFG)     : 32
Register Duplication               : YES
Optimize Instantiated Primitives   : NO
Use Clock Enable                   : Auto
Use Synchronous Set                : Auto
Use Synchronous Reset              : Auto
Pack IO Registers into IOBs        : Auto
Equivalent register Removal        : YES

---- General Options
Optimization Goal                  : Speed
Optimization Effort                : 1
Power Reduction                    : NO
Keep Hierarchy                     : No
Netlist Hierarchy                  : As_Optimized
RTL Output                         : Yes
Global Optimization                : AllClockNets
Read Cores                         : YES
Write Timing Constraints           : NO
Cross Clock Analysis               : NO
Hierarchy Separator                : /
Bus Delimiter                      : <>
Case Specifier                     : Maintain
Slice Utilization Ratio            : 100
BRAM Utilization Ratio             : 100
DSP48 Utilization Ratio            : 100
Auto BRAM Packing                  : NO
Slice Utilization Ratio Delta      : 5

==========================================================================


==========================================================================
*                          HDL Parsing                                   *
==========================================================================
Analyzing Verilog file "/home/ise/Project1-schemecounter/d_ff.v" into library
work
Parsing module <d_ff>.
Analyzing Verilog file "/home/ise/Project1-schemecounter/schematic-counter.v"
into library work
Parsing module <schematic_counter>.

==========================================================================
*                            HDL Elaboration                             *
==========================================================================
Elaborating module <schematic_counter>.

Elaborating module <d_ff>.

=========================================================================
*                           HDL Synthesis                               *
=========================================================================

Synthesizing Unit <schematic_counter>.
    Related source file is
"/home/ise/Project1-schemecounter/schematic-counter.v".
    Summary:
      inferred   1 Multiplexer(s).
Unit <schematic_counter> synthesized.

Synthesizing Unit <d_ff>.
    Related source file is "/home/ise/Project1-schemecounter/d_ff.v".
    Found 1-bit register for signal <q>.
    Summary:
      inferred   1 D-type flip-flop(s).
Unit <d_ff> synthesized.

=========================================================================
HDL Synthesis Report

Macro Statistics
# Registers                                            : 4
 1-bit register                                        : 4
# Multiplexers                                         : 1
 4-bit 2-to-1 multiplexer                              : 1
# Xors                                                 : 1
 1-bit xor2                                            : 1

=========================================================================

=========================================================================
*                       Advanced HDL Synthesis                          *
=========================================================================


=========================================================================
Advanced HDL Synthesis Report

Macro Statistics
# Registers                                            : 4
 Flip-Flops                                            : 4
# Multiplexers                                         : 1
 4-bit 2-to-1 multiplexer                              : 1
# Xors                                                 : 1
 1-bit xor2                                            : 1

=========================================================================
=========================================================================
*                          Low Level Synthesis                          *
=========================================================================

Optimizing unit <schematic_counter> ...

Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block schematic_counter, actual
ratio is 0.

Final Macro Processing ...

=========================================================================
Final Register Report

Macro Statistics
# Registers                                            : 4
 Flip-Flops                                            : 4

=========================================================================

=========================================================================
*                            Partition Report                           *
=========================================================================

Partition Implementation Status
-------------------------------

  No Partitions were found in this design.

-------------------------------

=========================================================================
*                             Design Summary                            *
=========================================================================

Top Level Output File Name         : schematic_counter.ngc

Primitive and Black Box Usage:
------------------------------
# BELS                             : 4
#      LUT2                        : 2
#      LUT3                        : 1
#      LUT4                        : 1
# FlipFlops/Latches                : 4
#      FDC                         : 4
# Clock Buffers                    : 1
#      BUFGP                       : 1
# IO Buffers                       : 9
#      IBUF                        : 5
#      OBUF                        : 4

Device utilization summary:
```

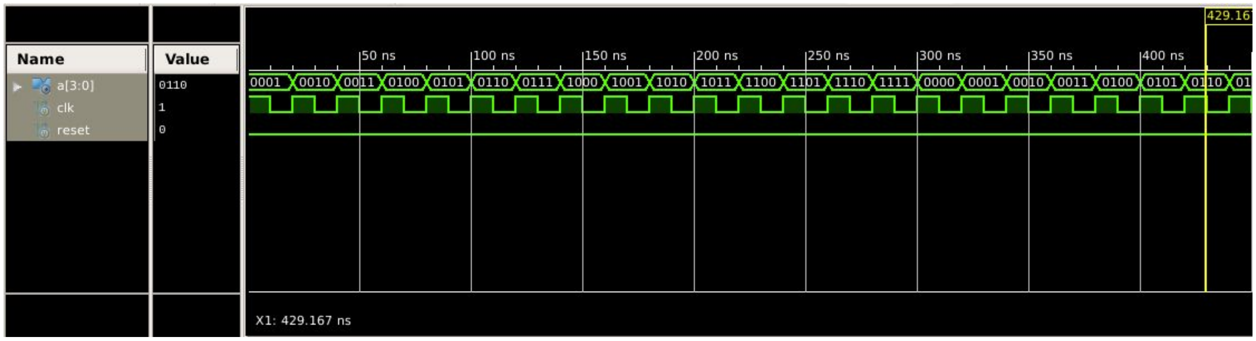
```
---------------------------

Selected Device : 7a100tcsg324-3


Slice Logic Utilization:
 Number of Slice LUTs:                    4  out of  63400     0%
    Number used as Logic:                 4  out of  63400     0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:      4
   Number with an unused Flip Flop:       4  out of      4   100%
   Number with an unused LUT:             0  out of      4     0%
   Number of fully used LUT-FF pairs:     0  out of      4     0%
   Number of unique control sets:         1

IO Utilization:
 Number of IOs:                          10
 Number of bonded IOBs:                  10  out of    210     4%
    IOB Flip Flops/Latches:               4

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:                1  out of     32     3%

---------------------------
Partition Resource Summary:
---------------------------

  No Partitions were found in this design.

---------------------------


=========================================================================
Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
-----------------------------------+------------------------+-------+
Clock Signal                       | Clock buffer(FF name)  | Load  |
-----------------------------------+------------------------+-------+
clk                                | BUFGP                  | 4     |
-----------------------------------+------------------------+-------+

Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design

Timing Summary:
---------------
```

```
Speed Grade: -3

   Minimum period: No path found
   Minimum input arrival time before clock: 0.648ns
   Maximum output required time after clock: 1.294ns
   Maximum combinational path delay: 0.775ns

Timing Details:
---------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'
  Total number of paths / destination ports: 8 / 8
-------------------------------------------------------------------------
Offset:              0.648ns (Levels of Logic = 1)
  Source:            reset (PAD)
  Destination:       f3/q (FF)
  Destination Clock: clk rising

  Data Path: reset to f3/q
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             5   0.001   0.298  reset_IBUF (reset_IBUF)
     FDC:CLR                   0.349          f3/q
    ----------------------------------------
    Total                      0.648ns (0.350ns logic, 0.298ns route)
                                       (54.0% logic, 46.0% route)

=========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'
  Total number of paths / destination ports: 10 / 4
-------------------------------------------------------------------------
Offset:              1.294ns (Levels of Logic = 2)
  Source:            f3/q (FF)
  Destination:       result<3> (PAD)
  Source Clock:      clk rising

  Data Path: f3/q to result<3>
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDC:C->Q              1   0.361   0.556  f3/q (f3/q)
     LUT4:I0->O            1   0.097   0.279  result<3>1 (result_3_OBUF)
     OBUF:I->O                 0.000          result_3_OBUF (result<3>)
    ----------------------------------------
    Total                      1.294ns (0.458ns logic, 0.836ns route)
                                       (35.4% logic, 64.6% route)

=========================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 1 / 1
-------------------------------------------------------------------------
```

```
Delay:               0.775ns (Levels of Logic = 3)
  Source:            reset (PAD)
  Destination:       result<0> (PAD)

  Data Path: reset to result<0>
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             5   0.001   0.398  reset_IBUF (reset_IBUF)
     LUT2:I0->O            1   0.097   0.279  Mmux_result11 (result_0_OBUF)
     OBUF:I->O                 0.000          result_0_OBUF (result<0>)
    ----------------------------------------
    Total                      0.775ns (0.098ns logic, 0.677ns route)
                                       (12.6% logic, 87.4% route)

=========================================================================

Cross Clock Domains Report:
--------------------------

=========================================================================


Total REAL time to Xst completion: 8.00 secs
Total CPU time to Xst completion: 7.68 secs

-->


Total memory usage is 601492 kilobytes

Number of errors   :    0 (   0 filtered)
Number of warnings :    0 (   0 filtered)
Number of infos    :    0 (   0 filtered)
```

///

4-bit counter using higher-level abstraction



These are the waveforms observed for the 4-bit counter with the modern design. It is evident from these waveforms that the counter is being incremented correctly, and in equal intervals.

The counter was always reset to 0000 before starting, and the reset signal was passed in between to see if it would correctly restart from 0000. Here is some of the output from the simulation console log:

```
Counter=0000
Counter=0001
Counter=0010
Counter=0011
Counter=0100
     ……
Counter=1101
Counter=1110
Counter=1111
Counter=0000
```

/// Synthesis Report

```
Release 14.7 - xst P.20131013 (lin64)
Copyright (c) 1995-2013 Xilinx, Inc.  All rights reserved.
-->
Parameter TMPDIR set to xst/projnav.tmp


Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.06 secs

-->
Parameter xsthdpdir set to xst


Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.07 secs

-->
Reading design: modern_counter.prj

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       8.3) Partition Resource Summary
       8.4) Timing Report
```

```
=========================================================================
*                      Synthesis Options Summary                        *
=========================================================================
---- Source Parameters
Input File Name                    : "modern_counter.prj"
Ignore Synthesis Constraint File   : NO

---- Target Parameters
Output File Name                   : "modern_counter"
Output Format                      : NGC
Target Device                      : xc7a100t-3-csg324

---- Source Options
Top Module Name                    : modern_counter
Automatic FSM Extraction           : YES
FSM Encoding Algorithm             : Auto
Safe Implementation                : No
FSM Style                          : LUT
RAM Extraction                     : Yes
RAM Style                          : Auto
ROM Extraction                     : Yes
Shift Register Extraction          : YES
ROM Style                          : Auto
Resource Sharing                   : YES
Asynchronous To Synchronous        : NO
Shift Register Minimum Size        : 2
Use DSP Block                      : Auto
Automatic Register Balancing       : No

---- Target Options
LUT Combining                      : Auto
Reduce Control Sets                : Auto
Add IO Buffers                     : YES
Global Maximum Fanout              : 100000
Add Generic Clock Buffer(BUFG)     : 32
Register Duplication               : YES
Optimize Instantiated Primitives   : NO
Use Clock Enable                   : Auto
Use Synchronous Set                : Auto
Use Synchronous Reset              : Auto
Pack IO Registers into IOBs        : Auto
Equivalent register Removal        : YES

---- General Options
Optimization Goal                  : Speed
Optimization Effort                : 1
Power Reduction                    : NO
```

```
Keep Hierarchy                     : No
Netlist Hierarchy                  : As_Optimized
RTL Output                         : Yes
Global Optimization                : AllClockNets
Read Cores                         : YES
Write Timing Constraints           : NO
Cross Clock Analysis               : NO
Hierarchy Separator                : /
Bus Delimiter                      : <>
Case Specifier                     : Maintain
Slice Utilization Ratio            : 100
BRAM Utilization Ratio             : 100
DSP48 Utilization Ratio            : 100
Auto BRAM Packing                  : NO
Slice Utilization Ratio Delta      : 5

=========================================================================


=========================================================================
*                          HDL Parsing                                  *
=========================================================================
Analyzing Verilog file "/home/ise/Project1-moderncounter/modern_counter.v" into
library work
Parsing module <modern_counter>.

=========================================================================
*                            HDL Elaboration                            *
=========================================================================

Elaborating module <modern_counter>.

=========================================================================
*                           HDL Synthesis                               *
=========================================================================

Synthesizing Unit <modern_counter>.
    Related source file is "/home/ise/Project1-moderncounter/modern_counter.v".
    Found 4-bit register for signal <a>.
    Found 4-bit adder for signal <a[3]_GND_1_o_add_0_OUT> created at line 42.
    Summary:
      inferred   1 Adder/Subtractor(s).
      inferred   4 D-type flip-flop(s).
Unit <modern_counter> synthesized.

=========================================================================
HDL Synthesis Report

Macro Statistics
# Adders/Subtractors                                   : 1
 4-bit adder                                           : 1
# Registers                                            : 1
 4-bit register                                        : 1
```

```
=========================================================================

=========================================================================
*                       Advanced HDL Synthesis                          *
=========================================================================


Synthesizing (advanced) Unit <modern_counter>.
The following registers are absorbed into counter <a>: 1 register on signal
<a>.
Unit <modern_counter> synthesized (advanced).

=========================================================================
Advanced HDL Synthesis Report

Macro Statistics
# Counters                                             : 1
 4-bit up counter                                      : 1

=========================================================================

=========================================================================
*                         Low Level Synthesis                           *
=========================================================================

Optimizing unit <modern_counter> ...

Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block modern_counter, actual ratio
is 0.

Final Macro Processing ...

=========================================================================
Final Register Report

Macro Statistics
# Registers                                            : 4
 Flip-Flops                                            : 4

=========================================================================

=========================================================================
*                           Partition Report                            *
=========================================================================

Partition Implementation Status
-------------------------------

  No Partitions were found in this design.

-------------------------------
```

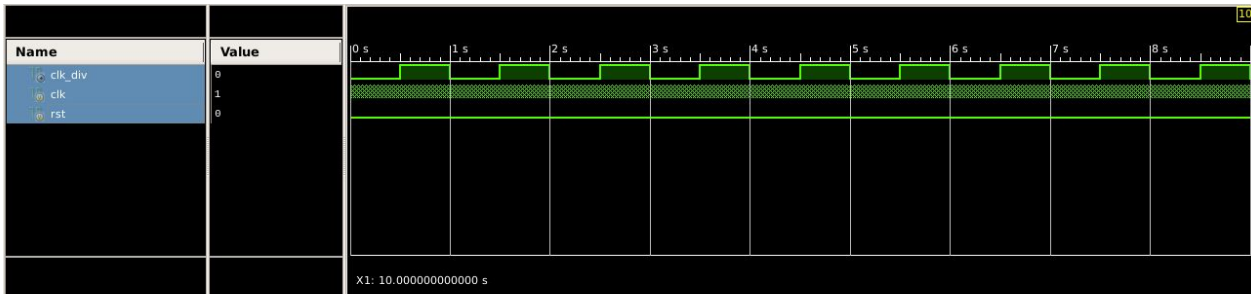
```
=========================================================================
*                            Design Summary                             *
=========================================================================

Top Level Output File Name         : modern_counter.ngc

Primitive and Black Box Usage:
------------------------------
# BELS                             : 4
#      INV                         : 1
#      LUT2                        : 1
#      LUT3                        : 1
#      LUT4                        : 1
# FlipFlops/Latches                : 4
#      FDC                         : 4
# Clock Buffers                    : 1
#      BUFGP                       : 1
# IO Buffers                       : 5
#      IBUF                        : 1
#      OBUF                        : 4

Device utilization summary:
---------------------------

Selected Device : 7a100tcsg324-3


Slice Logic Utilization:
 Number of Slice Registers:               4  out of  126800     0%
 Number of Slice LUTs:                    4  out of  63400     0%
    Number used as Logic:                 4  out of  63400     0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:      8
   Number with an unused Flip Flop:       4  out of      8    50%
   Number with an unused LUT:             4  out of      8    50%
   Number of fully used LUT-FF pairs:     0  out of      8     0%
   Number of unique control sets:         1

IO Utilization:
 Number of IOs:                           6
 Number of bonded IOBs:                   6  out of    210     2%

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:                1  out of     32     3%

---------------------------
Partition Resource Summary:
---------------------------

  No Partitions were found in this design.

---------------------------
```

```
=========================================================================
Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
-----------------------------------+------------------------+-------+
Clock Signal                       | Clock buffer(FF name)  | Load  |
-----------------------------------+------------------------+-------+
clk                                | BUFGP                  | 4     |
-----------------------------------+------------------------+-------+

Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design

Timing Summary:
---------------
Speed Grade: -3

   Minimum period: 1.059ns (Maximum Frequency: 943.842MHz)
   Minimum input arrival time before clock: 0.643ns
   Maximum output required time after clock: 0.659ns
   Maximum combinational path delay: No path found

Timing Details:
---------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'clk'
  Clock period: 1.059ns (frequency: 943.842MHz)
  Total number of paths / destination ports: 10 / 4
-------------------------------------------------------------------------
Delay:               1.059ns (Levels of Logic = 1)
  Source:            a_0 (FF)
  Destination:       a_0 (FF)
  Source Clock:      clk rising
  Destination Clock: clk rising

  Data Path: a_0 to a_0
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDC:C->Q              5   0.361   0.298  a_0 (a_0)
     INV:I->O              1   0.113   0.279  Mcount_a_xor<0>11_INV_0
(Result<0>)
     FDC:D                     0.008          a_0
    ----------------------------------------
    Total                      1.059ns (0.482ns logic, 0.577ns route)
```

```
                                       (45.5% logic, 54.5% route)

========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'
  Total number of paths / destination ports: 4 / 4
------------------------------------------------------------------------
Offset:              0.643ns (Levels of Logic = 1)
  Source:            reset (PAD)
  Destination:       a_0 (FF)
  Destination Clock: clk rising

  Data Path: reset to a_0
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             4   0.001   0.293  reset_IBUF (reset_IBUF)
     FDC:CLR                   0.349          a_0
    ----------------------------------------
    Total                      0.643ns (0.350ns logic, 0.293ns route)
                                       (54.4% logic, 45.6% route)

========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'
  Total number of paths / destination ports: 4 / 4
------------------------------------------------------------------------
Offset:              0.659ns (Levels of Logic = 1)
  Source:            a_0 (FF)
  Destination:       a<0> (PAD)
  Source Clock:      clk rising

  Data Path: a_0 to a<0>
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDC:C->Q              5   0.361   0.298  a_0 (a_0)
     OBUF:I->O                 0.000          a_0_OBUF (a<0>)
    ----------------------------------------
    Total                      0.659ns (0.361ns logic, 0.298ns route)
                                       (54.8% logic, 45.2% route)

========================================================================

Cross Clock Domains Report:
--------------------------

Clock to Setup on destination clock clk
---------------+---------+---------+---------+---------+
               | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock   |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------+---------+---------+---------+---------+
clk            |    1.059|         |         |         |
---------------+---------+---------+---------+---------+

========================================================================
Total REAL time to Xst completion: 8.00 secs
Total CPU time to Xst completion: 7.51 secs

-->


Total memory usage is 600752 kilobytes

Number of errors   :    0 (   0 filtered)
Number of warnings :    0 (   0 filtered)
Number of infos    :    0 (   0 filtered)
```

///

Clock-divider



As can be seen from this waveform, we're able to simulate/create a 1Hz clock (represented by clk_div). To do this, the timescale was set to 100000ns / 100ns and the total simulation time was changed to 10s. The time in between each clk edge signal is #0.5. Reset is set to 1 at the beginning to set the counter to 0 and then back to 0 before the main simulation actually starts.

/// Synthesis Report

```
Release 14.7 - xst P.20131013 (lin64)
Copyright (c) 1995-2013 Xilinx, Inc.  All rights reserved.
-->
Parameter TMPDIR set to xst/projnav.tmp


Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.04 secs

-->
Parameter xsthdpdir set to xst


Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.05 secs
```

```
-->
Reading design: clockdivider.prj

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            8.4.4) Timing Details
            8.4.5) Cross Clock Domains Report


=========================================================================
*                      Synthesis Options Summary                        *
=========================================================================
---- Source Parameters
Input File Name                    : "clockdivider.prj"
Ignore Synthesis Constraint File   : NO

---- Target Parameters
Output File Name                   : "clockdivider"
Output Format                      : NGC
Target Device                      : xc7a100t-3-csg324

---- Source Options
Top Module Name                    : clockdivider
Automatic FSM Extraction           : YES
FSM Encoding Algorithm             : Auto
Safe Implementation                : No
FSM Style                          : LUT
RAM Extraction                     : Yes
RAM Style                          : Auto
ROM Extraction                     : Yes
Shift Register Extraction          : YES
ROM Style                          : Auto
Resource Sharing                   : YES
Asynchronous To Synchronous        : NO
Shift Register Minimum Size        : 2
Use DSP Block                      : Auto
Automatic Register Balancing       : No
```

```
---- Target Options
LUT Combining                      : Auto
Reduce Control Sets                : Auto
Add IO Buffers                     : YES
Global Maximum Fanout              : 100000
Add Generic Clock Buffer(BUFG)     : 32
Register Duplication               : YES
Optimize Instantiated Primitives   : NO
Use Clock Enable                   : Auto
Use Synchronous Set                : Auto
Use Synchronous Reset              : Auto
Pack IO Registers into IOBs        : Auto
Equivalent register Removal        : YES

---- General Options
Optimization Goal                  : Speed
Optimization Effort                : 1
Power Reduction                    : NO
Keep Hierarchy                     : No
Netlist Hierarchy                  : As_Optimized
RTL Output                         : Yes
Global Optimization                : AllClockNets
Read Cores                         : YES
Write Timing Constraints           : NO
Cross Clock Analysis               : NO
Hierarchy Separator                : /
Bus Delimiter                      : <>
Case Specifier                     : Maintain
Slice Utilization Ratio            : 100
BRAM Utilization Ratio             : 100
DSP48 Utilization Ratio            : 100
Auto BRAM Packing                  : NO
Slice Utilization Ratio Delta      : 5

=========================================================================


=========================================================================
*                          HDL Parsing                                  *
=========================================================================
Analyzing Verilog file "/home/ise/project1clockdidiver/clockdivider.v" into
library work
Parsing module <clockdivider>.

=========================================================================
*                            HDL Elaboration                            *
=========================================================================

Elaborating module <clockdivider>.
WARNING:HDLCompiler:413 - "/home/ise/project1clockdidiver/clockdivider.v" Line
53: Result of 14-bit expression is truncated to fit in 13-bit target.

=========================================================================
*                           HDL Synthesis                               *
```

```
=========================================================================

Synthesizing Unit <clockdivider>.
    Related source file is "/home/ise/project1clockdidiver/clockdivider.v".
    Found 13-bit register for signal <counter>.
    Found 1-bit register for signal <clk_div>.
    Found 13-bit adder for signal <counter[12]_GND_1_o_add_2_OUT> created at
line 53.
    Summary:
      inferred   1 Adder/Subtractor(s).
      inferred  14 D-type flip-flop(s).
      inferred   1 Multiplexer(s).
Unit <clockdivider> synthesized.

=========================================================================
HDL Synthesis Report

Macro Statistics
# Adders/Subtractors                                   : 1
 13-bit adder                                          : 1
# Registers                                            : 2
 1-bit register                                        : 1
 13-bit register                                       : 1
# Multiplexers                                         : 1
 13-bit 2-to-1 multiplexer                             : 1

=========================================================================

=========================================================================
*                       Advanced HDL Synthesis                          *
=========================================================================


Synthesizing (advanced) Unit <clockdivider>.
The following registers are absorbed into counter <counter>: 1 register on
signal <counter>.
Unit <clockdivider> synthesized (advanced).

=========================================================================
Advanced HDL Synthesis Report

Macro Statistics
# Counters                                             : 1
 13-bit up counter                                     : 1
# Registers                                            : 1
 Flip-Flops                                            : 1

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=========================================================================
*                         Low Level Synthesis                           *
=========================================================================

Optimizing unit <clockdivider> ...
```

```
Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block clockdivider, actual ratio is
0.

Final Macro Processing ...

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Final Register Report

Macro Statistics
# Registers                                            : 14
 Flip-Flops                                            : 14

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=========================================================================
*                            Partition Report                           *
=========================================================================

Partition Implementation Status
-------------------------------

  No Partitions were found in this design.

-------------------------------

=========================================================================
*                             Design Summary                            *
=========================================================================

Top Level Output File Name         : clockdivider.ngc

Primitive and Black Box Usage:
------------------------------
# BELS                             : 57
#      GND                         : 1
#      INV                         : 2
#      LUT1                        : 12
#      LUT4                        : 1
#      LUT5                        : 14
#      LUT6                        : 1
#      MUXCY                       : 12
#      VCC                         : 1
#      XORCY                       : 13
# FlipFlops/Latches                : 14
#      FDC                         : 13
#      FDCE                        : 1
# Clock Buffers                    : 1
#      BUFGP                       : 1
# IO Buffers                       : 2
#      IBUF                        : 1
#      OBUF                        : 1
```

```
Device utilization summary:
---------------------------

Selected Device : 7a100tcsg324-3


Slice Logic Utilization:
 Number of Slice Registers:              14  out of  126800     0%
 Number of Slice LUTs:                   30  out of  63400     0%
    Number used as Logic:                30  out of  63400     0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:     30
   Number with an unused Flip Flop:      16  out of     30    53%
   Number with an unused LUT:             0  out of     30     0%
   Number of fully used LUT-FF pairs:    14  out of     30    46%
   Number of unique control sets:         2

IO Utilization:
 Number of IOs:                           3
 Number of bonded IOBs:                   3  out of    210     1%

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:                1  out of     32     3%

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Partition Resource Summary:
---------------------------

  No Partitions were found in this design.

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=========================================================================
Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
-----------------------------------+------------------------+-------+
Clock Signal                       | Clock buffer(FF name)  | Load  |
-----------------------------------+------------------------+-------+
clk                                | BUFGP                  | 14    |
-----------------------------------+------------------------+-------+

Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design
```

```
Timing Summary:
---------------
Speed Grade: -3

   Minimum period: 2.194ns (Maximum Frequency: 455.789MHz)
   Minimum input arrival time before clock: 0.689ns
   Maximum output required time after clock: 0.645ns
   Maximum combinational path delay: No path found

Timing Details:
---------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'clk'
  Clock period: 2.194ns (frequency: 455.789MHz)
  Total number of paths / destination ports: 274 / 15
-------------------------------------------------------------------------
Delay:               2.194ns (Levels of Logic = 15)
  Source:            counter_0 (FF)
  Destination:       counter_12 (FF)
  Source Clock:      clk rising
  Destination Clock: clk rising

  Data Path: counter_0 to counter_12
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDC:C->Q             15   0.361   0.344  counter_0 (counter_0)
     INV:I->O              1   0.113   0.000  Mcount_counter_lut<0>_INV_0
(Mcount_counter_lut<0>)
     MUXCY:S->O            1   0.353   0.000  Mcount_counter_cy<0>
(Mcount_counter_cy<0>)
     MUXCY:CI->O           1   0.023   0.000  Mcount_counter_cy<1>
(Mcount_counter_cy<1>)
     MUXCY:CI->O           1   0.023   0.000  Mcount_counter_cy<2>
(Mcount_counter_cy<2>)
     MUXCY:CI->O           1   0.023   0.000  Mcount_counter_cy<3>
(Mcount_counter_cy<3>)
     MUXCY:CI->O           1   0.023   0.000  Mcount_counter_cy<4>
(Mcount_counter_cy<4>)
     MUXCY:CI->O           1   0.023   0.000  Mcount_counter_cy<5>
(Mcount_counter_cy<5>)
     MUXCY:CI->O           1   0.023   0.000  Mcount_counter_cy<6>
(Mcount_counter_cy<6>)
     MUXCY:CI->O           1   0.023   0.000  Mcount_counter_cy<7>
(Mcount_counter_cy<7>)
     MUXCY:CI->O           1   0.023   0.000  Mcount_counter_cy<8>
(Mcount_counter_cy<8>)
     MUXCY:CI->O           1   0.023   0.000  Mcount_counter_cy<9>
(Mcount_counter_cy<9>)
     MUXCY:CI->O           1   0.023   0.000  Mcount_counter_cy<10>
(Mcount_counter_cy<10>)
```

```
     MUXCY:CI->O           0   0.023   0.000  Mcount_counter_cy<11>
(Mcount_counter_cy<11>)
     XORCY:CI->O           1   0.370   0.295  Mcount_counter_xor<12>
(Result<12>)
     LUT5:I4->O            1   0.097   0.000  Mcount_counter_eqn_121
(Mcount_counter_eqn_12)
     FDC:D                     0.008          counter_12
    ----------------------------------------
    Total                      2.194ns (1.555ns logic, 0.639ns route)
                                       (70.9% logic, 29.1% route)

=========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'
  Total number of paths / destination ports: 14 / 14
-------------------------------------------------------------------------
Offset:              0.689ns (Levels of Logic = 1)
  Source:            rst (PAD)
  Destination:       clk_div (FF)
  Destination Clock: clk rising

  Data Path: rst to clk_div
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O            14   0.001   0.339  rst_IBUF (rst_IBUF)
     FDCE:CLR                  0.349          clk_div
    ----------------------------------------
    Total                      0.689ns (0.350ns logic, 0.339ns route)
                                       (50.8% logic, 49.2% route)

=========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'
  Total number of paths / destination ports: 1 / 1
-------------------------------------------------------------------------
Offset:              0.645ns (Levels of Logic = 1)
  Source:            clk_div (FF)
  Destination:       clk_div (PAD)
  Source Clock:      clk rising

  Data Path: clk_div to clk_div
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDCE:C->Q             2   0.361   0.283  clk_div (clk_div_OBUF)
     OBUF:I->O                 0.000          clk_div_OBUF (clk_div)
    ----------------------------------------
    Total                      0.645ns (0.361ns logic, 0.283ns route)
                                       (56.0% logic, 44.0% route)

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Cross Clock Domains Report:
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```

```
Clock to Setup on destination clock clk
---------------+---------+---------+---------+---------+
               | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock   |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------+---------+---------+---------+---------+
clk            |    2.194|         |         |         |
---------------+---------+---------+---------+---------+

=========================================================================


Total REAL time to Xst completion: 12.00 secs
Total CPU time to Xst completion: 11.02 secs

-->


Total memory usage is 601096 kilobytes

Number of errors   :    0 (   0 filtered)
Number of warnings :    1 (   0 filtered)
Number of infos    :    0 (   0 filtered)
```

///

Conclusion

Overall, all four parts of this lab were challenging and exposed me to a new part of VHDL and working with Xilinx. Four modules were created: an 8:1 Mux, 4-bit counter with gates and flip-flops, a modern 4-bit counter, and a clock-divider. Each module has been explained above in-depth but allowed us to explore both combinational and sequential circuits and the timescale aspect of the test bench.

In this lab, it took me a while to understand some of the Verilog syntax properly. I found designing the 4-bit counter using D flip-flops and gates pretty challenging since there was a lot of room for error. The same goes for the clock-divider module, where it had a two-pronged challenge in terms of setting us the 1Hz signal and tweaking the test bench to actually create the 10KHz clock. It took some trial and error to get it right. The only improvement I can suggest is that it would have been helpful if we went over how to actually manipulate the timescale in the test bench.

Another part I struggled with was with the test bench for part 4 of this lab. I kept thinking my test bench was incorrect but didn’t realize that we can change the total simulation time from the default of 1000ns to anything we like. Because of this, I spent 3 hours inspecting my module and test bench which was a very frustrating experience. I wish I had known earlier that we could change the default simulation time.

Answers to questions:

1. What is a ".ucf" file? How would you use it for Nexys3 in an actual setting on a real board to connect the inputs of the combinational circuitry to the switches on the FPGA?

   ucf stands for User Constraints File (UCF). A .ucf file helps map variables in the defined module to actual ports on the FPGA board, which in our case, would be on the Nexys3 board. More specifically, the .ucf is needed when using the Implement Design step on Xilinx. The Map step actually performs the required mapping from module inputs/outputs to board input/outputs.

   For the combinational circuit in the first part of this lab, we have 3 inputs (which are switches), and the output (which is an LED). Therefore, the UCF file would look something like this:

```
NET sw0 LOC = T10 | IOSTANDARD = LVCMOS33;
NET sw1 LOC = T9 | IOSTANDARD = LVCMOS33;
NET select<0> LOC = V9 | IOSTANDARD = LVCMOS33;
NET select<1> LOC = M8 | IOSTANDARD = LVCMOS33;
NET select<2> LOC = N8| IOSTANDARD = LVCMOS33;
NET out LOC = U16 | IOSTANDARD = LVCMOS33;
```