CS M152A - Introduction to Digital Design Lab

Project 5: Finite State Machine Design - Parking Meter

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Introduction and Background

This lab primarily focuses on creating and implementing an FSM for a parking meter. This FSM simulates coins being added and displays the appropriate time remaining. The inputs primarily represent a variety of different buttons that can add different increments of time to the timer. The output is displayed via a seven-segment LED display before the timer expires. In particular, the parking meter behaves differently for different durations and lights up the LED in two different formats based on this criteria. Once a button is pushed, time is immediately added. The output is modeled as 4 seven segment displays which display the time remaining.

Binary-Coded Decimal:
The basic principle behind BCD is that a binary number can be expressed as a set of individual decimal numbers. For eg. we can represent 110010 (50 in binary) as 0101 0000, where each digit is represented using its own output. The basic algorithm to convert binary to BCD is as follows (assume an 8-bit binary input). The maximum number that can be represented is 256, so the BCD representation will have 3 values.

Algorithm:

1. If any column (100's, 10's, 1's, etc.) is 5 or greater, add 3 to that column.
2. Shift all #'s to the left 1 position.
3. If 8 shifts have been performed, it's done! Evaluate each column for the BCD values.
4. Go to step 1.

The pseudocode looks as follows:

```
for(i=0; i<8; i++) {
	//check all columns for >= 5
	for each column {
		if (column >= 5)
			column += 3;

	//shift all binary digits left 1
	Hundreds <<= 1;
	Hundreds[0] = Tens[3];
	Tens << = 1;
	Tens[0] = Ones[3];
	Ones << = 1;
	Ones[0] = Binary[7];
	Binary <<= 1;
}
```

Further description of the module itself is provided in the design description. A design summary report and overall synthesis report is attached at the end.

Design Description

For this module, the table below lists the set of inputs provided.

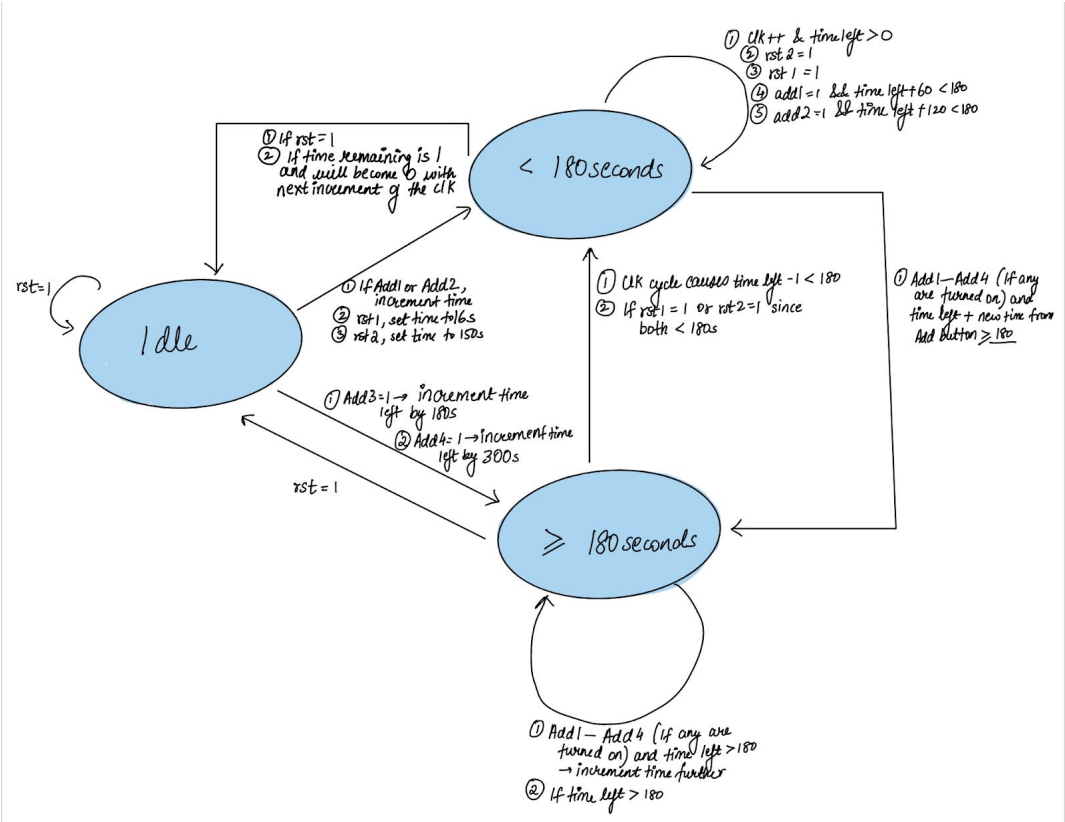
Inputs	Function
add1	add 60 seconds
add2	add 120 seconds
add3	add 180 seconds
add4	add 300 seconds
rst1	reset time to 16 seconds
rst2	reset time to 150 seconds
clk	frequency of 100 Hz
rst	resets to the initial state

Additionally, the following outputs were set:

```
output reg [6:0] led_seg,
output reg [3:0] val1,
output reg [3:0] val2,
output reg [3:0] val3,
output reg [3:0] val4,
output reg a1,
output reg a2,
output reg a3,
output reg a4
```

Here, led_seg is a 7-bit bus representing the 7 different cathodes of the LED, a1-a4 represent the 4 different anodes for each of the digits, and val1 - val4 represent BCD outputs for each of the LED digits.

FSM Diagram for Parking Meter



Very broadly, the about FSM diagram explains how this parking meter works. It consists of 3 states - Idle (the initial state), ABOVE_3_MIN, and BELOW_3_MIN. Each of these states handles the LED segment and BCD outputs separately. If add1 or add2 are passed in from IDLE, we transition to BELOW_3_MIN. The counter decrements once every 50% duty cycle of the global clock. From here, if the counter runs out to 0, then we move back to the IDLE state. Otherwise, we continue in this state. If add3 or add4 are passed, then the time remaining is greater than 180, so we transition to ABOVE_3_MIN. Likewise, if the time remaining reaches < 180 seconds, then we transition from ABOVE_3_MIN to BELOW_3_MIN. Once we're in ABOVE_3_MIN, all different time increments (add1-add4) are handled gracefully since the only upper bound is 9999s, which is the value we latch onto. If a global rst = 1 at any point, then all outputs are set to 0, time remaining is set to 0 and we transition back to the IDLE state.

To implement a lot of this logic, a bunch of internal variables were created.

```
// Constant states
   parameter IDLE        = 3'b001;
   parameter ABOVE_3_MIN = 3'b010;
   parameter BELOW_3_MIN = 3'b100;
```

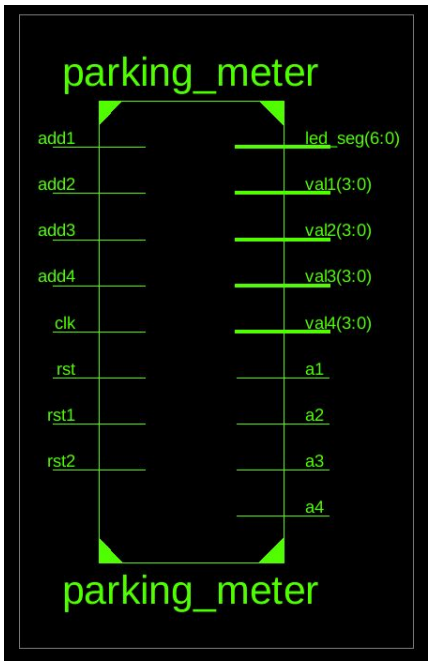
```
// Internal variables
reg [2:0] current_state, next_state;

// Used for binary to BCD conversion
reg [3:0] digit1  = 4'b0000;
reg [3:0] digit2  = 4'b0000;
reg [3:0] digit3  = 4'b0000;
reg [3:0] digit4  = 4'b0000;
integer k;

// time remaining
reg [6:0] clk_counter     = 7'b0;
reg [13:0] time_remaining = 14'b0;

// used for clock divider
reg internal_clk;
```

The overall program itself is divided into 3 blocks:

1. Always block for combination circuit to set next state
    a. First component is a clock divider that flips an internal clock bit every 50 podedge cycles of the external/global clock.
    b. Second just checks rst1 and rst2 and sets current state to the BELOW_3_MIN if either of these are turned on. Otherwise, it sets current state to next state.
2. Always block for a sequential circuit to set the current state
    a. Here, we check if add1-add4 is passed in and increment the time remaining accordingly. If the internal clock is set to 1, we decrement time remaining by 1. Finally, if time remaining is 9999, we latch it onto that. And if time remaining is between [0,180), we move to BELOW_3_MIN, and if greater than or equal to 180, we go to ABOVE_3_MIN.
3. Always block to update output. This does several things:
    a. First, it initializes the 4 anodes representing each of the digits in the LED display.
    b. It converts our binary time to BCD outputs using 4 digits, and sets val1-val4 to these values. The algorithm for converting to BCD was described above.
    c. It initializes the LED segment itself.
    d. It sets the LED segment bits. This is done using a case statement. The basic idea is that all the cathodes that need to be turned on must be set to low, and all the cathodes that we want turned off must be set to high:

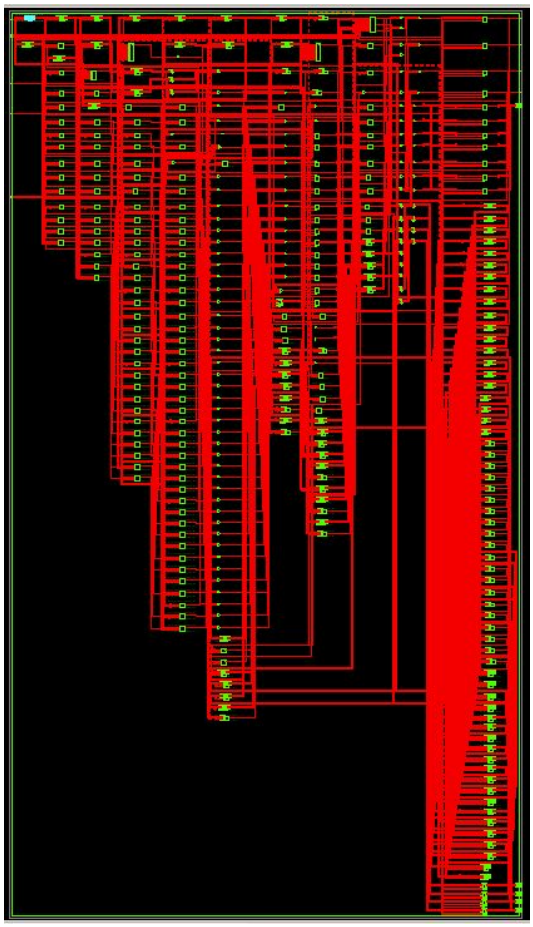
```
case(val2)
    0: led_seg = 7'b1111110;
    1: led_seg = 7'b1001111;
    2: led_seg = 7'b0010010;
    3: led_seg = 7'b0000110;
    4: led_seg = 7'b1001100;
    5: led_seg = 7'b0100100;
    6: led_seg = 7'b0100000;
    7: led_seg = 7'b0001111;
    8: led_seg = 7'b0000000;
    9: led_seg = 7'b0001100;
    default: led_seg = 7'b1111110;
endcase;
```

e. Finally, it turns anodes on and off in a cycle, since only one LED can be turned on at a time (this is the required design).



High Level Schematic Diagram

The overall high-level schematic shows the inputs and outputs described for this FSM in this design requirement section. val1-val4 are all 4-bit buses, while the led segment has 7 bits, where each bit represents each of the 7 cathodes. a1-a4 are used to indicate which anode to turn on, which in turn indicates which LED digit to light up.



Overall Schematic

The actual overall schematic is quite dense and complex. This makes sense given we had a wide array of individual buses and counters, including the main time remaining counter that is 14 bits. A lot of these blocks also representing a large number of if conditions throughout the program. The complexity also comes from the way the binary to BCD converter works, which is a for loop with lots of left shits that are clearly represented by the right side of the schematic with the large red solid portion.

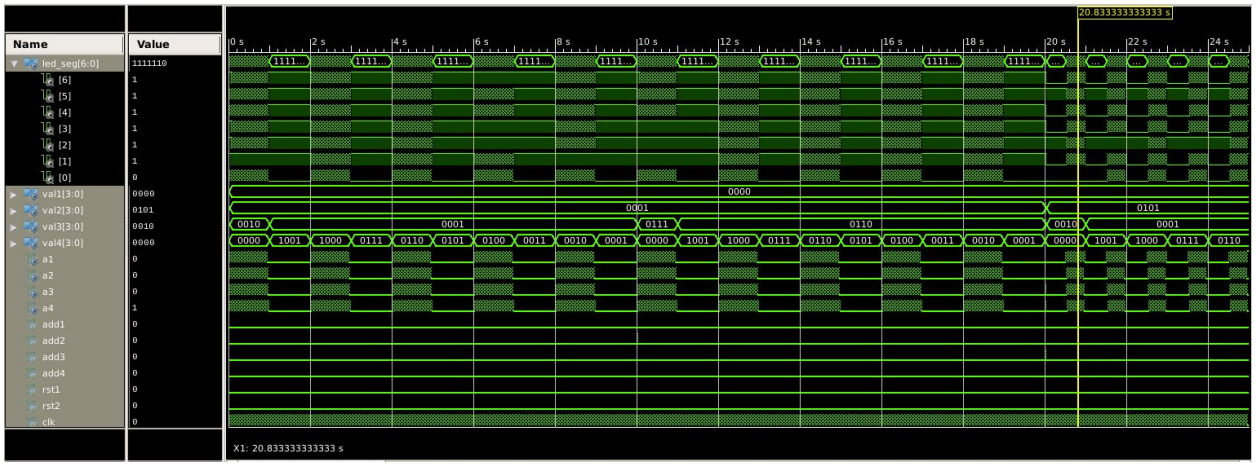
Simulation

The test bench I wrote uses a timescale of 100000ns/1ps, so 50ns represents a 1s full cycle. The main goal was to see different BCD changes when trying all different inputs. That is, seeing BCD increments when add1-add4 are passes, seeing time remaining changing when rst1 and rst2 are passed, and seeing BCD actually decrement between these. Here's the test sequence.

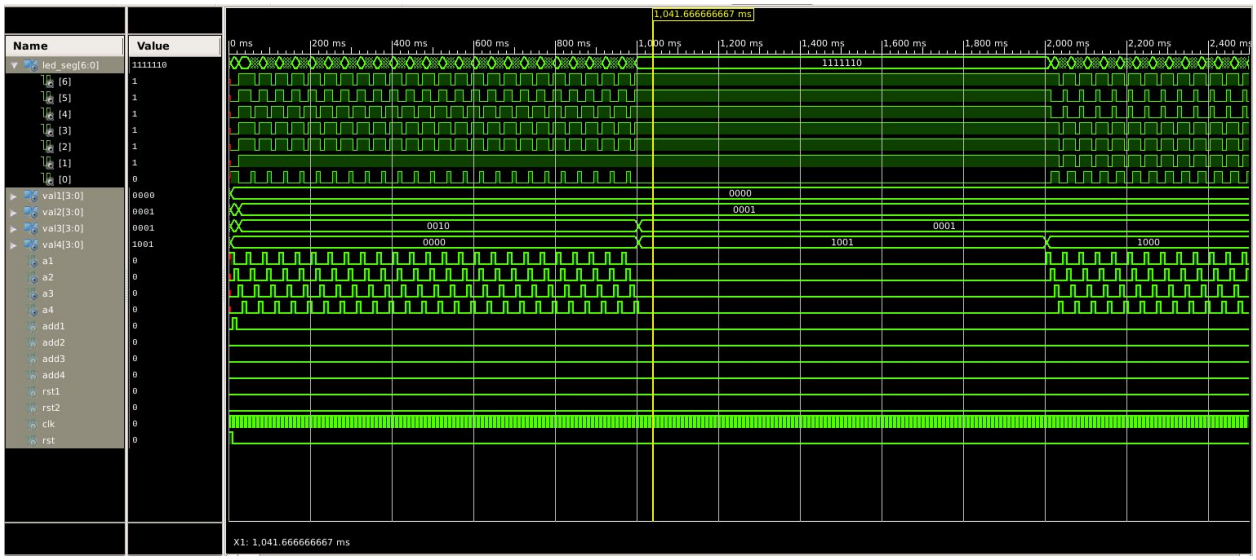
```
initial begin
            forever #50 clk = ~clk;
        end
```

```
    initial begin
    // Initialize Inputs
    clk = 0;
    rst = 1;
    add1 = 0;
    add2 = 0;
    add3 = 0;
    add4 = 0;
    rst1 = 0;
    rst2 = 0;

    // Wait for entire clock cycle for all outputs to initialize
    #100;
  rst = 0;

    $monitor("remaining time=%d %d %d %d", val1, val2, val3, val4);

   add1 = 1;
    #100;
    add1 = 0;
    #100000;
    add2 = 1;
    #100;
    add2 = 0;
    #100000;
    add3 = 1;
    #100;
    add3 = 0;
  #100000;
    rst1 = 1;
  #100;
  rst1 = 0;
    #50000;
    add4 = 1;
    #100;
    add4 = 0;
    #100000;
```

```
        rst2 = 1;
        #100;
        rst2 = 0;
        #100000;
    end
```



This is a very high-level waveform output for the testbench I wrote.It illustrates the required clock changes, both internal and external, as well as a 50% duty cycle. Additionally, val1-val4 are changing correctly as well. What also supports this is the fact that one changes very often, the second twice as slow, the third twice as slow as the second, and the 4th twice as slow as the third, which is what we would expect. Additionally, the LED bits light up correctly. I've explained this further in my video demo, where for the number 1, only 2/7 cathodes go low, and for the number 2, 5/7 cathodes go low.



A deeper/more zoomed-in look into the waveforms also reveals the same thing, that is, the anodes and cathodes change as expected, and that val1-val4 are updating at the right time and roughly as frequently as you would expect. I've described this further in my video.

Below, ive attached a snapshot of my console log. It specifically showcases the BCD output as well as the counter counting down. At 601s, rst2 is set to 1 so the time gets changed to 150s and it continues decrementing from that point on. To get this to work, I had to change my overall simulation time from 1000ns to 60s.

```
remaining time= 0 6 0 9
remaining time= 0 6 0 8
remaining time= 0 6 0 7
remaining time= 0 6 0 6
remaining time= 0 6 0 5
remaining time= 0 6 0 4
remaining time= 0 6 0 3
remaining time= 0 6 0 2
remaining time= 0 6 0 1
remaining time= 0 1 5 0
remaining time= 0 1 4 9
remaining time= 0 1 4 8
remaining time= 0 1 4 7
remaining time= 0 1 4 6
remaining time= 0 1 4 5
remaining time= 0 1 4 4
remaining time= 0 1 4 3
remaining time= 0 1 4 2
remaining time= 0 1 4 1
remaining time= 0 1 4 0
```

Conclusion

Overall, this lab works correctly as far as I know. It was challenging, especially to get BCD to work since it requires a for loop which feels extremely unintuitive for an HDL. However, it is interesting to see the amount of precision required in timing while making something as simple as a parking meter. I found the way the 7-segment LED board to work pretty interesting, and the way the anodes and cathodes control each of the 4 digits interesting. Even more so, I thought the fact that they actually light up once at a time and not all together even more interesting since high frequencies can clearly create optics that are not very obvious.

Additionally, I believe that the parts that were truly challenging were synchronizing all the outputs correctly and making sure that the anode update loop was created so all LEDs could take turns lighting up. I also found that the schematic was so complex for something that's conceptually not that complex, which I found particularly striking. It's also cool to visualize parts of your design implementation as a schemeatic, and actually be able to recognize what parts each might be despite the schematic being so complex.

Design Summary

```
================================================================================
*                              Design Summary                                  *
```

```
=========================================================================

Top Level Output File Name         : parking_meter.ngc

Primitive and Black Box Usage:
------------------------------
# BELS                             : 416
#      GND                         : 1
#      INV                         : 14
#      LUT1                        : 1
#      LUT2                        : 11
#      LUT3                        : 12
#      LUT4                        : 30
#      LUT5                        : 86
#      LUT6                        : 161
#      MUXCY                       : 46
#      MUXF7                       : 3
#      VCC                         : 1
#      XORCY                       : 50
# FlipFlops/Latches                : 51
#      FD                          : 1
#      FDR                         : 34
#      FDS                         : 2
#      LDC                         : 6
#      LDP                         : 8
# Clock Buffers                    : 1
#      BUFGP                       : 1
# IO Buffers                       : 34
#      IBUF                        : 7
#      OBUF                        : 27

Device utilization summary:
---------------------------

Selected Device : 7a100tcsg324-3


Slice Logic Utilization:
 Number of Slice Registers:              51  out of  126800     0%
 Number of Slice LUTs:                  315  out of  63400     0%
    Number used as Logic:               315  out of  63400     0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:    317
   Number with an unused Flip Flop:     266  out of    317    83%
   Number with an unused LUT:             2  out of    317     0%
   Number of fully used LUT-FF pairs:    49  out of    317    15%
   Number of unique control sets:         4

IO Utilization:
 Number of IOs:                         35
 Number of bonded IOBs:                 35  out of    210    16%

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:               1  out of     32     3%

---------------------------
```

```
Partition Resource Summary:
---------------------------

  No Partitions were found in this design.

---------------------------


================================================================================
```

Full Synthesis Report

```
Release 14.7 - xst P.20131013 (lin64)
Copyright (c) 1995-2013 Xilinx, Inc.  All rights reserved.
-->
Parameter TMPDIR set to xst/projnav.tmp


Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.05 secs

-->
Parameter xsthdpdir set to xst


Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.05 secs

-->
Reading design: parking_meter.prj

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================================================================================
*                      Synthesis Options Summary                         *
================================================================================
---- Source Parameters
```

```
Input File Name                    : "parking_meter.prj"
Ignore Synthesis Constraint File   : NO

---- Target Parameters
Output File Name                   : "parking_meter"
Output Format                      : NGC
Target Device                      : xc7a100t-3-csg324

---- Source Options
Top Module Name                    : parking_meter
Automatic FSM Extraction           : YES
FSM Encoding Algorithm             : Auto
Safe Implementation                : No
FSM Style                          : LUT
RAM Extraction                     : Yes
RAM Style                          : Auto
ROM Extraction                     : Yes
Shift Register Extraction          : YES
ROM Style                          : Auto
Resource Sharing                   : YES
Asynchronous To Synchronous        : NO
Shift Register Minimum Size        : 2
Use DSP Block                      : Auto
Automatic Register Balancing       : No

---- Target Options
LUT Combining                      : Auto
Reduce Control Sets                : Auto
Add IO Buffers                     : YES
Global Maximum Fanout              : 100000
Add Generic Clock Buffer(BUFG)     : 32
Register Duplication               : YES
Optimize Instantiated Primitives   : NO
Use Clock Enable                   : Auto
Use Synchronous Set                : Auto
Use Synchronous Reset              : Auto
Pack IO Registers into IOBs        : Auto
Equivalent register Removal        : YES

---- General Options
Optimization Goal                  : Speed
Optimization Effort                : 1
Power Reduction                    : NO
Keep Hierarchy                     : No
Netlist Hierarchy                  : As_Optimized
RTL Output                         : Yes
Global Optimization                : AllClockNets
Read Cores                         : YES
Write Timing Constraints           : NO
Cross Clock Analysis               : NO
Hierarchy Separator                : /
Bus Delimiter                      : <>
Case Specifier                     : Maintain
Slice Utilization Ratio            : 100
BRAM Utilization Ratio             : 100
DSP48 Utilization Ratio            : 100
Auto BRAM Packing                  : NO
```

```
Slice Utilization Ratio Delta      : 5

=========================================================================


=========================================================================
*                           HDL Parsing                                 *
=========================================================================
Analyzing Verilog file "/home/ise/Project5/parking_meter.v" into library work
Parsing module <parking_meter>.

=========================================================================
*                            HDL Elaboration                            *
=========================================================================

Elaborating module <parking_meter>.
WARNING:HDLCompiler:91 - "/home/ise/Project5/parking_meter.v" Line 110: Signal
<time_remaining> missing in the sensitivity list is added for synthesis purposes. HDL and
post-synthesis simulations may differ as a result.
WARNING:HDLCompiler:91 - "/home/ise/Project5/parking_meter.v" Line 111: Signal
<time_remaining> missing in the sensitivity list is added for synthesis purposes. HDL and
post-synthesis simulations may differ as a result.

=========================================================================
*                            HDL Synthesis                              *
=========================================================================

Synthesizing Unit <parking_meter>.
    Related source file is "/home/ise/Project5/parking_meter.v".
        IDLE = 3'b001
        ABOVE_3_MIN = 3'b010
        BELOW_3_MIN = 3'b100
    Found 3-bit register for signal <current_state>.
    Found 1-bit register for signal <internal_clk>.
    Found 1-bit register for signal <a1>.
    Found 1-bit register for signal <a2>.
    Found 1-bit register for signal <a3>.
    Found 1-bit register for signal <a4>.
    Found 4-bit register for signal <val1>.
    Found 4-bit register for signal <val2>.
    Found 4-bit register for signal <val3>.
    Found 4-bit register for signal <val4>.
    Found 7-bit register for signal <led_seg>.
    Found 7-bit register for signal <clk_counter>.
    Found finite state machine <FSM_0> for signal <current_state>.
    -----------------------------------------------------------------------
    | States             | 3                                              |
    | Transitions        | 24                                             |
    | Inputs             | 10                                             |
    | Outputs            | 3                                              |
    | Clock              | clk (rising_edge)                              |
    | Reset              | rst (positive)                                 |
    | Reset type         | synchronous                                    |
    | Reset State        | 001                                            |
    | Encoding           | auto                                           |
    | Implementation     | LUT                                            |
    -----------------------------------------------------------------------
```

```
    Found 14-bit subtractor for signal <time_remaining[13]_GND_1_o_sub_15_OUT> created at line
111.
    Found 7-bit adder for signal <clk_counter[6]_GND_1_o_add_8_OUT> created at line 98.
    Found 14-bit adder for signal <time_remaining[13]_GND_1_o_add_26_OUT> created at line 136.
    Found 14-bit adder for signal <time_remaining[13]_GND_1_o_add_28_OUT> created at line 142.
    Found 14-bit adder for signal <time_remaining[13]_GND_1_o_add_30_OUT> created at line 148.
    Found 14-bit adder for signal <time_remaining[13]_GND_1_o_add_67_OUT> created at line 216.
    Found 4-bit adder for signal <n0487> created at line 327.
    Found 4-bit adder for signal <GND_1_o_GND_1_o_add_130_OUT> created at line 327.
    Found 4-bit adder for signal <GND_1_o_GND_1_o_add_133_OUT> created at line 327.
    Found 4-bit adder for signal <n0497> created at line 325.
    Found 4-bit adder for signal <GND_1_o_GND_1_o_add_139_OUT> created at line 327.
    Found 4-bit adder for signal <GND_1_o_GND_1_o_add_142_OUT> created at line 325.
    Found 4-bit adder for signal <GND_1_o_GND_1_o_add_145_OUT> created at line 327.
    Found 4-bit adder for signal <GND_1_o_GND_1_o_add_148_OUT> created at line 325.
    Found 4-bit adder for signal <GND_1_o_GND_1_o_add_151_OUT> created at line 327.
    Found 4-bit adder for signal <n0516> created at line 323.
    Found 4-bit adder for signal <GND_1_o_GND_1_o_add_157_OUT> created at line 325.
    Found 4-bit adder for signal <GND_1_o_GND_1_o_add_160_OUT> created at line 327.
    Found 4-bit adder for signal <GND_1_o_GND_1_o_add_163_OUT> created at line 323.
    Found 4-bit adder for signal <GND_1_o_GND_1_o_add_166_OUT> created at line 325.
    Found 4-bit adder for signal <GND_1_o_GND_1_o_add_169_OUT> created at line 327.
    Found 4-bit adder for signal <GND_1_o_GND_1_o_add_172_OUT> created at line 323.
    Found 4-bit adder for signal <GND_1_o_GND_1_o_add_175_OUT> created at line 325.
    Found 4-bit adder for signal <GND_1_o_GND_1_o_add_178_OUT> created at line 327.
    Found 4-bit adder for signal <n0544> created at line 321.
    Found 4-bit adder for signal <GND_1_o_GND_1_o_add_184_OUT> created at line 323.
    Found 4-bit adder for signal <GND_1_o_GND_1_o_add_187_OUT> created at line 325.
    Found 4-bit adder for signal <GND_1_o_GND_1_o_add_190_OUT> created at line 327.
    Found 4-bit adder for signal <GND_1_o_GND_1_o_add_193_OUT> created at line 321.
    Found 4-bit adder for signal <GND_1_o_GND_1_o_add_196_OUT> created at line 323.
    Found 4-bit adder for signal <GND_1_o_GND_1_o_add_199_OUT> created at line 325.
    Found 4-bit adder for signal <GND_1_o_GND_1_o_add_202_OUT> created at line 327.
    Found 16x7-bit Read Only RAM for signal <val2[3]_PWR_1_o_wide_mux_205_OUT>
    Found 16x7-bit Read Only RAM for signal <val3[3]_PWR_1_o_wide_mux_207_OUT>
    Found 16x7-bit Read Only RAM for signal <val4[3]_PWR_1_o_wide_mux_209_OUT>
    Found 16x7-bit Read Only RAM for signal <val1[3]_PWR_1_o_wide_mux_212_OUT>
WARNING:Xst:737 - Found 1-bit latch for signal <time_remaining<12>>. Latches may be generated
from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD
designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <time_remaining<11>>. Latches may be generated
from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD
designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <time_remaining<10>>. Latches may be generated
from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD
designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <time_remaining<9>>. Latches may be generated
from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD
designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <time_remaining<8>>. Latches may be generated
from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD
designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <time_remaining<7>>. Latches may be generated
from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD
designs, as they may lead to timing problems.
```

```
WARNING:Xst:737 - Found 1-bit latch for signal <time_remaining<6>>. Latches may be generated
from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD
designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <time_remaining<5>>. Latches may be generated
from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD
designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <time_remaining<4>>. Latches may be generated
from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD
designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <time_remaining<3>>. Latches may be generated
from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD
designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <time_remaining<2>>. Latches may be generated
from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD
designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <time_remaining<1>>. Latches may be generated
from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD
designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <time_remaining<0>>. Latches may be generated
from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD
designs, as they may lead to timing problems.
WARNING:Xst:737 - Found 1-bit latch for signal <time_remaining<13>>. Latches may be generated
from incomplete case or if statements. We do not recommend the use of latches in FPGA/CPLD
designs, as they may lead to timing problems.
    Found 14-bit comparator greater for signal <n0026> created at line 153
    Found 14-bit comparator greater for signal <GND_1_o_time_remaining[13]_LessThan_34_o>
created at line 156
    Found 14-bit comparator greater for signal <time_remaining[13]_GND_1_o_LessThan_69_o>
created at line 217
    Found 14-bit comparator greater for signal <PWR_1_o_current_state[2]_LessThan_91_o>
created at line 245
    Found 3-bit comparator greater for signal <PWR_1_o_time_remaining[13]_LessThan_127_o>
created at line 326
    Found 4-bit comparator greater for signal <GND_1_o_GND_1_o_LessThan_130_o> created at line
326
    Found 4-bit comparator greater for signal <GND_1_o_GND_1_o_LessThan_133_o> created at line
326
    Found 3-bit comparator greater for signal <PWR_1_o_GND_1_o_LessThan_136_o> created at line
324
    Found 4-bit comparator greater for signal <GND_1_o_GND_1_o_LessThan_139_o> created at line
326
    Found 4-bit comparator greater for signal <GND_1_o_GND_1_o_LessThan_142_o> created at line
324
    Found 4-bit comparator greater for signal <GND_1_o_GND_1_o_LessThan_145_o> created at line
326
    Found 4-bit comparator greater for signal <GND_1_o_GND_1_o_LessThan_148_o> created at line
324
    Found 4-bit comparator greater for signal <GND_1_o_GND_1_o_LessThan_151_o> created at line
326
    Found 3-bit comparator greater for signal <PWR_1_o_GND_1_o_LessThan_154_o> created at line
322
    Found 4-bit comparator greater for signal <GND_1_o_GND_1_o_LessThan_157_o> created at line
324
    Found 4-bit comparator greater for signal <GND_1_o_GND_1_o_LessThan_160_o> created at line
326
    Found 4-bit comparator greater for signal <GND_1_o_GND_1_o_LessThan_163_o> created at line
322
```

```
    Found 4-bit comparator greater for signal <GND_1_o_GND_1_o_LessThan_166_o> created at line
324
    Found 4-bit comparator greater for signal <GND_1_o_GND_1_o_LessThan_169_o> created at line
326
    Found 4-bit comparator greater for signal <GND_1_o_GND_1_o_LessThan_172_o> created at line
322
    Found 4-bit comparator greater for signal <GND_1_o_GND_1_o_LessThan_175_o> created at line
324
    Found 4-bit comparator greater for signal <GND_1_o_GND_1_o_LessThan_178_o> created at line
326
    Found 3-bit comparator greater for signal <PWR_1_o_GND_1_o_LessThan_181_o> created at line
320
    Found 4-bit comparator greater for signal <GND_1_o_GND_1_o_LessThan_184_o> created at line
322
    Found 4-bit comparator greater for signal <GND_1_o_GND_1_o_LessThan_187_o> created at line
324
    Found 4-bit comparator greater for signal <GND_1_o_GND_1_o_LessThan_190_o> created at line
326
    Found 4-bit comparator greater for signal <GND_1_o_GND_1_o_LessThan_193_o> created at line
320
    Found 4-bit comparator greater for signal <GND_1_o_GND_1_o_LessThan_196_o> created at line
322
    Found 4-bit comparator greater for signal <GND_1_o_GND_1_o_LessThan_199_o> created at line
324
    Found 4-bit comparator greater for signal <GND_1_o_GND_1_o_LessThan_202_o> created at line
326
    Found 7-bit comparator lessequal for signal <n0320> created at line 588
    Summary:
       inferred   4 RAM(s).
       inferred  32 Adder/Subtractor(s).
       inferred  35 D-type flip-flop(s).
       inferred  14 Latch(s).
       inferred  31 Comparator(s).
       inferred 168 Multiplexer(s).
       inferred   1 Finite State Machine(s).
Unit <parking_meter> synthesized.

=========================================================================
HDL Synthesis Report

Macro Statistics
# RAMs                                                 : 4
 16x7-bit single-port Read Only RAM                    : 4
# Adders/Subtractors                                   : 32
 14-bit adder                                          : 4
 14-bit subtractor                                     : 1
 4-bit adder                                           : 26
 7-bit adder                                           : 1
# Registers                                            : 11
 1-bit register                                        : 5
 4-bit register                                        : 4
 7-bit register                                        : 2
# Latches                                              : 14
 1-bit latch                                           : 14
# Comparators                                          : 31
 14-bit comparator greater                             : 4
 3-bit comparator greater                              : 4
```

```
 4-bit comparator greater                              : 22
 7-bit comparator lessequal                            : 1
# Multiplexers                                         : 168
 1-bit 2-to-1 multiplexer                              : 124
 14-bit 2-to-1 multiplexer                             : 11
 4-bit 2-to-1 multiplexer                              : 26
 7-bit 2-to-1 multiplexer                              : 7
# FSMs                                                 : 1

=========================================================================

=========================================================================
*                        Advanced HDL Synthesis                         *
=========================================================================


Synthesizing (advanced) Unit <parking_meter>.
The following registers are absorbed into counter <clk_counter>: 1 register on signal
<clk_counter>.
INFO:Xst:3231 - The small RAM <Mram_val1[3]_PWR_1_o_wide_mux_212_OUT> will be implemented on
LUTs in order to maximize performance and save block RAM resources. If you want to force its
implementation on block, use option/constraint ram_style.
    -----------------------------------------------------------------------
    | ram_type           | Distributed                         |          |
    -----------------------------------------------------------------------
    | Port A                                                               |
    |     aspect ratio   | 16-word x 7-bit                     |          |
    |     weA            | connected to signal <GND>           | high     |
    |     addrA          | connected to signal <val1>          |          |
    |     diA            | connected to signal <GND>           |          |
    |     doA            | connected to internal node          |          |
    -----------------------------------------------------------------------
INFO:Xst:3231 - The small RAM <Mram_val2[3]_PWR_1_o_wide_mux_205_OUT> will be implemented on
LUTs in order to maximize performance and save block RAM resources. If you want to force its
implementation on block, use option/constraint ram_style.
    -----------------------------------------------------------------------
    | ram_type           | Distributed                         |          |
    -----------------------------------------------------------------------
    | Port A                                                               |
    |     aspect ratio   | 16-word x 7-bit                     |          |
    |     weA            | connected to signal <GND>           | high     |
    |     addrA          | connected to signal <val2>          |          |
    |     diA            | connected to signal <GND>           |          |
    |     doA            | connected to internal node          |          |
    -----------------------------------------------------------------------
INFO:Xst:3231 - The small RAM <Mram_val3[3]_PWR_1_o_wide_mux_207_OUT> will be implemented on
LUTs in order to maximize performance and save block RAM resources. If you want to force its
implementation on block, use option/constraint ram_style.
    -----------------------------------------------------------------------
    | ram_type           | Distributed                         |          |
    -----------------------------------------------------------------------
    | Port A                                                               |
    |     aspect ratio   | 16-word x 7-bit                     |          |
    |     weA            | connected to signal <GND>           | high     |
    |     addrA          | connected to signal <val3>          |          |
    |     diA            | connected to signal <GND>           |          |
    |     doA            | connected to internal node          |          |
```

```
    ----------------------------------------------------------------------
INFO:Xst:3231 - The small RAM <Mram_val4[3]_PWR_1_o_wide_mux_209_OUT> will be implemented on
LUTs in order to maximize performance and save block RAM resources. If you want to force its
implementation on block, use option/constraint ram_style.
    ----------------------------------------------------------------------
    | ram_type           | Distributed                          |          |
    ----------------------------------------------------------------------
    | Port A                                                    |          |
    |     aspect ratio   | 16-word x 7-bit                      |          |
    |     weA            | connected to signal <GND>            | high     |
    |     addrA          | connected to signal <val4>           |          |
    |     diA            | connected to signal <GND>            |          |
    |     doA            | connected to internal node           |          |
    ----------------------------------------------------------------------
Unit <parking_meter> synthesized (advanced).

=========================================================================
Advanced HDL Synthesis Report

Macro Statistics
# RAMs                                                 : 4
 16x7-bit single-port distributed Read Only RAM        : 4
# Adders/Subtractors                                   : 31
 14-bit adder                                          : 4
 14-bit subtractor                                     : 1
 4-bit adder                                           : 26
# Counters                                             : 1
 7-bit up counter                                      : 1
# Registers                                            : 28
 Flip-Flops                                            : 28
# Comparators                                          : 31
 14-bit comparator greater                             : 4
 3-bit comparator greater                              : 4
 4-bit comparator greater                              : 22
 7-bit comparator lessequal                            : 1
# Multiplexers                                         : 168
 1-bit 2-to-1 multiplexer                              : 124
 14-bit 2-to-1 multiplexer                             : 11
 4-bit 2-to-1 multiplexer                              : 26
 7-bit 2-to-1 multiplexer                              : 7
# FSMs                                                 : 1

=========================================================================

=========================================================================
*                        Low Level Synthesis                            *
=========================================================================
Analyzing FSM <MFsm> for best encoding.
Optimizing FSM <FSM_0> on signal <current_state[1:2]> with gray encoding.
-------------------
 State | Encoding
-------------------
 001   | 00
 010   | 01
 100   | 11
-------------------
```

```
Optimizing unit <parking_meter> ...

Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block parking_meter, actual ratio is 0.

Final Macro Processing ...

=========================================================================
Final Register Report

Macro Statistics
# Registers                                          : 37
 Flip-Flops                                          : 37

=========================================================================

=========================================================================
*                           Partition Report                            *
=========================================================================

Partition Implementation Status
-------------------------------

  No Partitions were found in this design.

-------------------------------

=========================================================================
*                            Design Summary                             *
=========================================================================

Top Level Output File Name         : parking_meter.ngc

Primitive and Black Box Usage:
------------------------------
# BELS                             : 416
#      GND                         : 1
#      INV                         : 14
#      LUT1                        : 1
#      LUT2                        : 11
#      LUT3                        : 12
#      LUT4                        : 30
#      LUT5                        : 86
#      LUT6                        : 161
#      MUXCY                       : 46
#      MUXF7                       : 3
#      VCC                         : 1
#      XORCY                       : 50
# FlipFlops/Latches                : 51
#      FD                          : 1
#      FDR                         : 34
#      FDS                         : 2
#      LDC                         : 6
#      LDP                         : 8
# Clock Buffers                    : 1
#      BUFGP                       : 1
```

```
# IO Buffers                        : 34
#      IBUF                         : 7
#      OBUF                         : 27

Device utilization summary:
---------------------------

Selected Device : 7a100tcsg324-3


Slice Logic Utilization:
 Number of Slice Registers:              51  out of  126800     0%
 Number of Slice LUTs:                  315  out of  63400     0%
    Number used as Logic:               315  out of  63400     0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:    317
   Number with an unused Flip Flop:     266  out of    317    83%
   Number with an unused LUT:             2  out of    317     0%
   Number of fully used LUT-FF pairs:    49  out of    317    15%
   Number of unique control sets:         4

IO Utilization:
 Number of IOs:                         35
 Number of bonded IOBs:                 35  out of    210    16%

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:               1  out of     32     3%

---------------------------
Partition Resource Summary:
---------------------------

  No Partitions were found in this design.

---------------------------


=================================================================================
Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
----------------------------------------+----------------------------+-------+
Clock Signal                            | Clock buffer(FF name)      | Load  |
----------------------------------------+----------------------------+-------+
clk                                     | BUFGP                      | 37    |
add1_add2_OR_60_o(add1_add2_OR_60_o1:O)| NONE(*)(time_remaining_12)| 14    |
----------------------------------------+----------------------------+-------+
(*) This 1 clock signal(s) are generated by combinatorial logic,
and XST is not able to identify which are the primary clock signals.
Please use the CLOCK_SIGNAL constraint to specify the clock signal(s) generated by
combinatorial logic.
```

```
INFO:Xst:2169 - HDL ADVISOR - Some clock signals were not automatically buffered by XST with
BUFG/BUFR resources. Please use the buffer_type constraint in order to insert these buffers to
the clock signals to help prevent skew problems.

Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design

Timing Summary:
---------------
Speed Grade: -3

   Minimum period: 5.897ns (Maximum Frequency: 169.564MHz)
   Minimum input arrival time before clock: 5.160ns
   Maximum output required time after clock: 0.709ns
   Maximum combinational path delay: No path found

Timing Details:
---------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'clk'
  Clock period: 4.488ns (frequency: 222.817MHz)
  Total number of paths / destination ports: 694 / 44
-------------------------------------------------------------------------
Delay:               4.488ns (Levels of Logic = 10)
  Source:            internal_clk (FF)
  Destination:       current_state_FSM_FFd1 (FF)
  Source Clock:      clk rising
  Destination Clock: clk rising

  Data Path: internal_clk to current_state_FSM_FFd1
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FD:C->Q              70   0.361   0.624  internal_clk (internal_clk)
     LUT3:I0->O            5   0.097   0.575  Mmux_n05781221 (Mmux_n0578122)
     LUT6:I2->O            1   0.097   0.000
Madd_time_remaining[13]_GND_1_o_add_67_OUT_lut<2>
(Madd_time_remaining[13]_GND_1_o_add_67_OUT_lut<2>)
     MUXCY:S->O            1   0.353   0.000  Madd_time_remaining[13]_GND_1_o_add_67_OUT_cy<2>
(Madd_time_remaining[13]_GND_1_o_add_67_OUT_cy<2>)
     MUXCY:CI->O           1   0.023   0.000  Madd_time_remaining[13]_GND_1_o_add_67_OUT_cy<3>
(Madd_time_remaining[13]_GND_1_o_add_67_OUT_cy<3>)
     MUXCY:CI->O           1   0.023   0.000  Madd_time_remaining[13]_GND_1_o_add_67_OUT_cy<4>
(Madd_time_remaining[13]_GND_1_o_add_67_OUT_cy<4>)
     MUXCY:CI->O           1   0.023   0.000  Madd_time_remaining[13]_GND_1_o_add_67_OUT_cy<5>
(Madd_time_remaining[13]_GND_1_o_add_67_OUT_cy<5>)
     XORCY:CI->O           4   0.370   0.707
Madd_time_remaining[13]_GND_1_o_add_67_OUT_xor<6> (time_remaining[13]_GND_1_o_add_67_OUT<6>)
     LUT6:I0->O            1   0.097   0.556  current_state_FSM_FFd1-In2
(current_state_FSM_FFd1-In2)
     LUT6:I2->O            1   0.097   0.379  current_state_FSM_FFd1-In3
(current_state_FSM_FFd1-In3)
     LUT6:I4->O            1   0.097   0.000  current_state_FSM_FFd1-In6
(current_state_FSM_FFd1-In)
```

```
     FDR:D                     0.008          current_state_FSM_FFd1
    ----------------------------------------
    Total                      4.488ns (1.646ns logic, 2.842ns route)
                                       (36.7% logic, 63.3% route)

=========================================================================
Timing constraint: Default period analysis for Clock 'add1_add2_OR_60_o'
  Clock period: 5.897ns (frequency: 169.564MHz)
  Total number of paths / destination ports: 134508 / 28
-------------------------------------------------------------------------
Delay:               5.897ns (Levels of Logic = 8)
  Source:            time_remaining_1 (LATCH)
  Destination:       time_remaining_12 (LATCH)
  Source Clock:      add1_add2_OR_60_o falling
  Destination Clock: add1_add2_OR_60_o falling

  Data Path: time_remaining_1 to time_remaining_12
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     LDP:G->Q              9   0.472   0.720  time_remaining_1 (time_remaining_1)
     LUT6:I1->O           15   0.097   0.444  time_remaining[13]_GND_1_o_not_equal_13_o2
(time_remaining[13]_GND_1_o_not_equal_13_o2)
     LUT4:I2->O           51   0.097   0.405  time_remaining[13]_GND_1_o_not_equal_13_o3
(time_remaining[13]_GND_1_o_not_equal_13_o)
     LUT5:I4->O           10   0.097   0.725  Mmux_n0578111 (n0578<6>)
     LUT5:I0->O            3   0.097   0.305  PWR_1_o_current_state[2]_LessThan_91_o16
(PWR_1_o_current_state[2]_LessThan_91_o16)
     LUT4:I3->O            1   0.097   0.556  PWR_1_o_current_state[2]_LessThan_91_o17_SW0_SW0
(N97)
     LUT6:I2->O            1   0.097   0.511  PWR_1_o_current_state[2]_LessThan_91_o17
(PWR_1_o_current_state[2]_LessThan_91_o17)
     LUT6:I3->O            1   0.097   0.295  PWR_1_o_current_state[2]_LessThan_91_o113
(PWR_1_o_current_state[2]_LessThan_91_o112)
     LUT5:I4->O           14   0.097   0.339  PWR_1_o_current_state[2]_LessThan_91_o114
(PWR_1_o_current_state[2]_LessThan_91_o)
     LDC:CLR                   0.349          time_remaining_12
    ----------------------------------------
    Total                      5.897ns (1.597ns logic, 4.300ns route)
                                       (27.1% logic, 72.9% route)

=========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'
  Total number of paths / destination ports: 535 / 31
-------------------------------------------------------------------------
Offset:              4.235ns (Levels of Logic = 10)
  Source:            rst (PAD)
  Destination:       current_state_FSM_FFd1 (FF)
  Destination Clock: clk rising

  Data Path: rst to current_state_FSM_FFd1
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O            40   0.001   0.664  rst_IBUF (rst_IBUF)
     LUT4:I0->O           41   0.097   0.664  Mmux_n05781141 (Mmux_n0578114)
```

```
     LUT5:I1->O            1   0.097   0.000
Madd_time_remaining[13]_GND_1_o_add_67_OUT_lut<3>
(Madd_time_remaining[13]_GND_1_o_add_67_OUT_lut<3>)
     MUXCY:S->O            1   0.353   0.000  Madd_time_remaining[13]_GND_1_o_add_67_OUT_cy<3>
(Madd_time_remaining[13]_GND_1_o_add_67_OUT_cy<3>)
     MUXCY:CI->O           1   0.023   0.000  Madd_time_remaining[13]_GND_1_o_add_67_OUT_cy<4>
(Madd_time_remaining[13]_GND_1_o_add_67_OUT_cy<4>)
     MUXCY:CI->O           1   0.023   0.000  Madd_time_remaining[13]_GND_1_o_add_67_OUT_cy<5>
(Madd_time_remaining[13]_GND_1_o_add_67_OUT_cy<5>)
     XORCY:CI->O           4   0.370   0.707
Madd_time_remaining[13]_GND_1_o_add_67_OUT_xor<6> (time_remaining[13]_GND_1_o_add_67_OUT<6>)
     LUT6:I0->O            1   0.097   0.556  current_state_FSM_FFd1-In2
(current_state_FSM_FFd1-In2)
     LUT6:I2->O            1   0.097   0.379  current_state_FSM_FFd1-In3
(current_state_FSM_FFd1-In3)
     LUT6:I4->O            1   0.097   0.000  current_state_FSM_FFd1-In6
(current_state_FSM_FFd1-In)
     FDR:D                 0.008          current_state_FSM_FFd1
    ----------------------------------------
    Total                  4.235ns (1.263ns logic, 2.972ns route)
                                   (29.8% logic, 70.2% route)

=========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'add1_add2_OR_60_o'
  Total number of paths / destination ports: 19974 / 28
-------------------------------------------------------------------------
Offset:              5.160ns (Levels of Logic = 13)
  Source:            rst (PAD)
  Destination:       time_remaining_12 (LATCH)
  Destination Clock: add1_add2_OR_60_o falling

  Data Path: rst to time_remaining_12
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O            40   0.001   0.664  rst_IBUF (rst_IBUF)
     LUT4:I0->O           41   0.097   0.791  Mmux_n05781141 (Mmux_n0578114)
     LUT5:I0->O            1   0.097   0.000
Madd_time_remaining[13]_GND_1_o_add_30_OUT_lut<3>
(Madd_time_remaining[13]_GND_1_o_add_30_OUT_lut<3>)
     MUXCY:S->O            1   0.353   0.000  Madd_time_remaining[13]_GND_1_o_add_30_OUT_cy<3>
(Madd_time_remaining[13]_GND_1_o_add_30_OUT_cy<3>)
     MUXCY:CI->O           1   0.023   0.000  Madd_time_remaining[13]_GND_1_o_add_30_OUT_cy<4>
(Madd_time_remaining[13]_GND_1_o_add_30_OUT_cy<4>)
     MUXCY:CI->O           1   0.023   0.000  Madd_time_remaining[13]_GND_1_o_add_30_OUT_cy<5>
(Madd_time_remaining[13]_GND_1_o_add_30_OUT_cy<5>)
     MUXCY:CI->O           1   0.023   0.000  Madd_time_remaining[13]_GND_1_o_add_30_OUT_cy<6>
(Madd_time_remaining[13]_GND_1_o_add_30_OUT_cy<6>)
     MUXCY:CI->O           1   0.023   0.000  Madd_time_remaining[13]_GND_1_o_add_30_OUT_cy<7>
(Madd_time_remaining[13]_GND_1_o_add_30_OUT_cy<7>)
     XORCY:CI->O           2   0.370   0.383
Madd_time_remaining[13]_GND_1_o_add_30_OUT_xor<8> (time_remaining[13]_GND_1_o_add_30_OUT<8>)
     LUT6:I4->O            2   0.097   0.561  SF06 (SF06)
     LUT6:I2->O            1   0.097   0.295  SF07 (SF0)
     LUT6:I5->O            1   0.097   0.379  PWR_1_o_current_state[2]_LessThan_91_o11
(PWR_1_o_current_state[2]_LessThan_91_o1)
```

```
     LUT5:I3->O           14   0.097   0.339  PWR_1_o_current_state[2]_LessThan_91_o114
(PWR_1_o_current_state[2]_LessThan_91_o)
     LDC:CLR                   0.349          time_remaining_12
    ----------------------------------------
    Total                      5.160ns (1.747ns logic, 3.413ns route)
                                       (33.9% logic, 66.1% route)

==========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'
  Total number of paths / destination ports: 27 / 27
--------------------------------------------------------------------------
Offset:              0.709ns (Levels of Logic = 1)
  Source:            a1 (FF)
  Destination:       a1 (PAD)
  Source Clock:      clk rising

  Data Path: a1 to a1
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDS:C->Q             16   0.361   0.348  a1 (a1_OBUF)
     OBUF:I->O                 0.000          a1_OBUF (a1)
    ----------------------------------------
    Total                      0.709ns (0.361ns logic, 0.348ns route)
                                       (50.9% logic, 49.1% route)

==========================================================================

Cross Clock Domains Report:
--------------------------

Clock to Setup on destination clock add1_add2_OR_60_o
-----------------+---------+---------+---------+---------+
                 | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock     |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
-----------------+---------+---------+---------+---------+
add1_add2_OR_60_o|         |         |    5.897|         |
clk              |         |         |    5.286|         |
-----------------+---------+---------+---------+---------+

Clock to Setup on destination clock clk
-----------------+---------+---------+---------+---------+
                 | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock     |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
-----------------+---------+---------+---------+---------+
add1_add2_OR_60_o|         |    8.895|         |         |
clk              |    4.488|         |         |         |
-----------------+---------+---------+---------+---------+

==========================================================================


Total REAL time to Xst completion: 12.00 secs
Total CPU time to Xst completion: 11.56 secs

-->
```

```
Total memory usage is 604056 kilobytes

Number of errors   :    0 (   0 filtered)
Number of warnings :   16 (   0 filtered)
Number of infos    :    5 (   0 filtered)
```