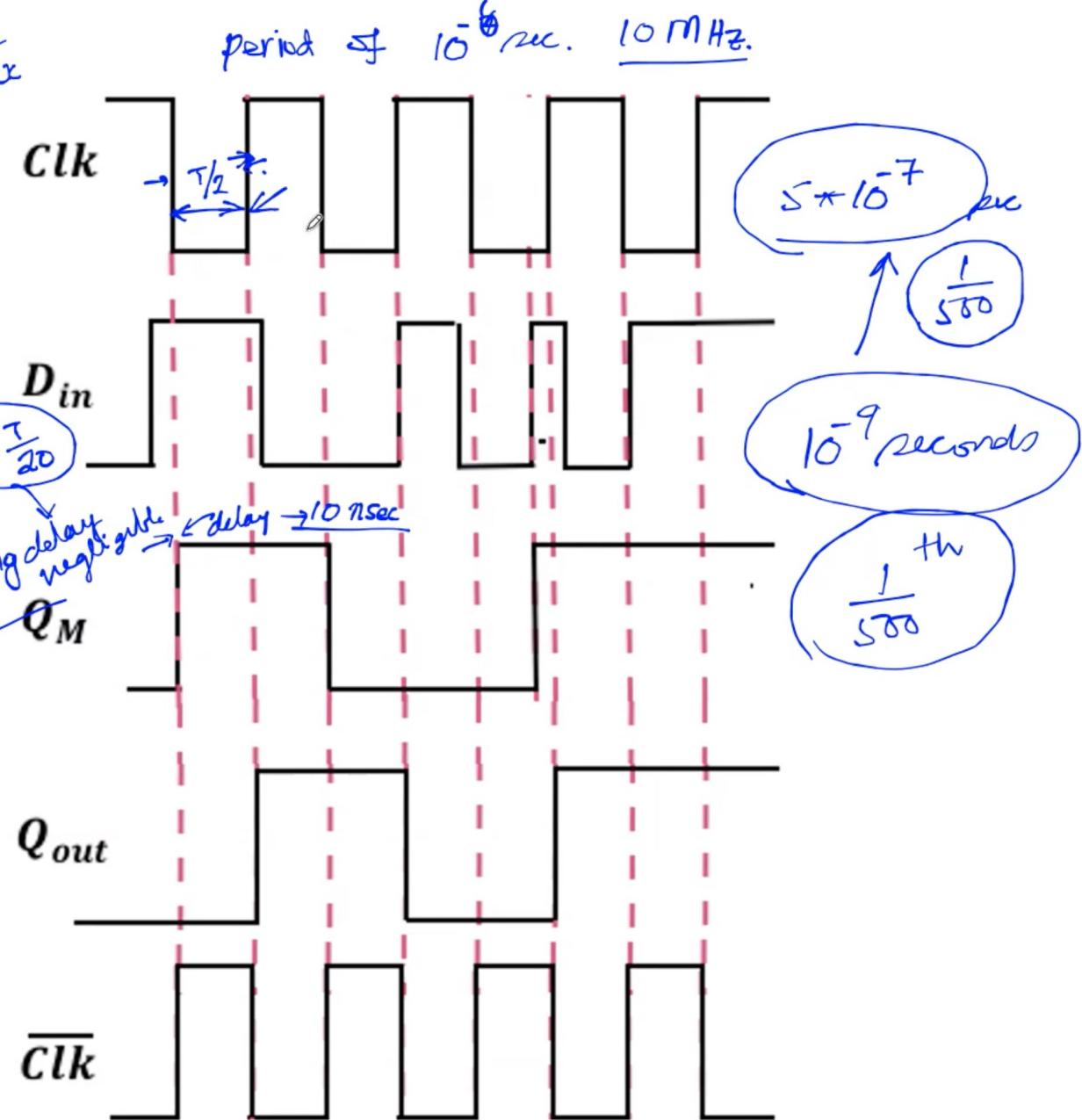
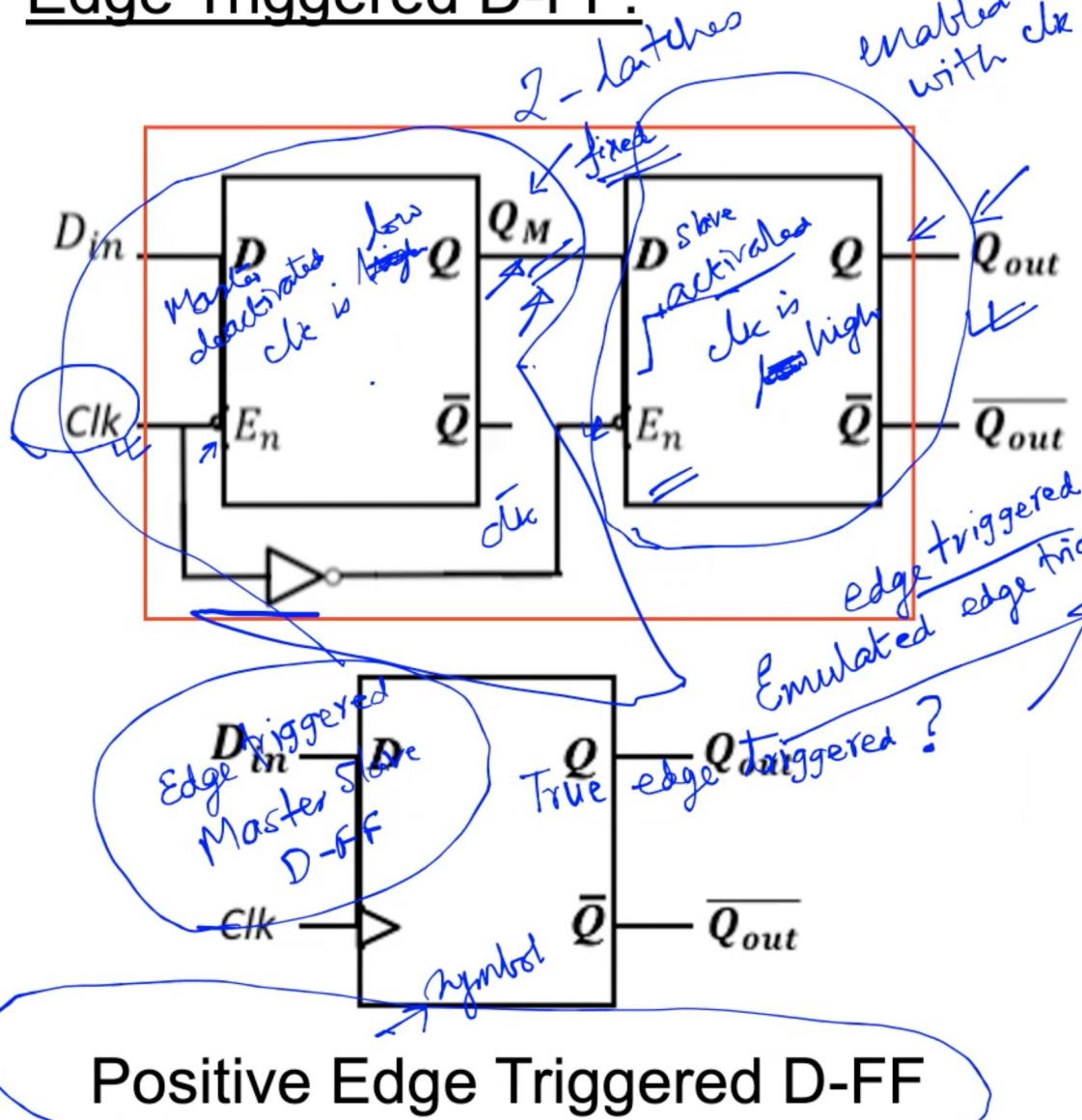


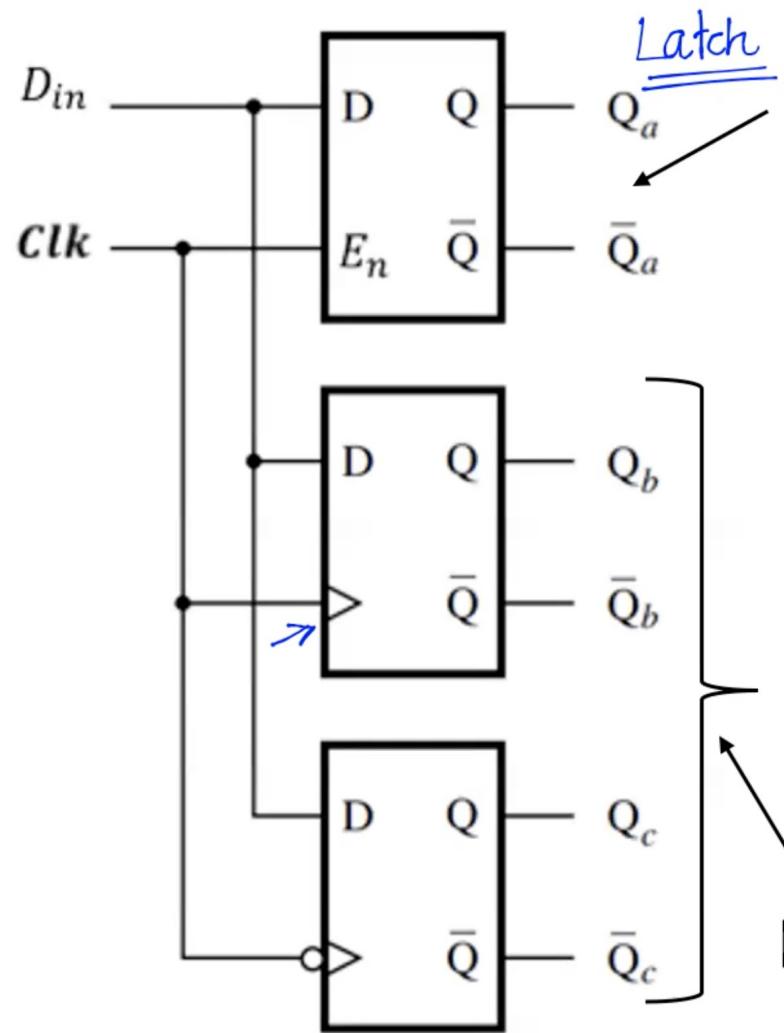


## Edge Triggered D-FF:

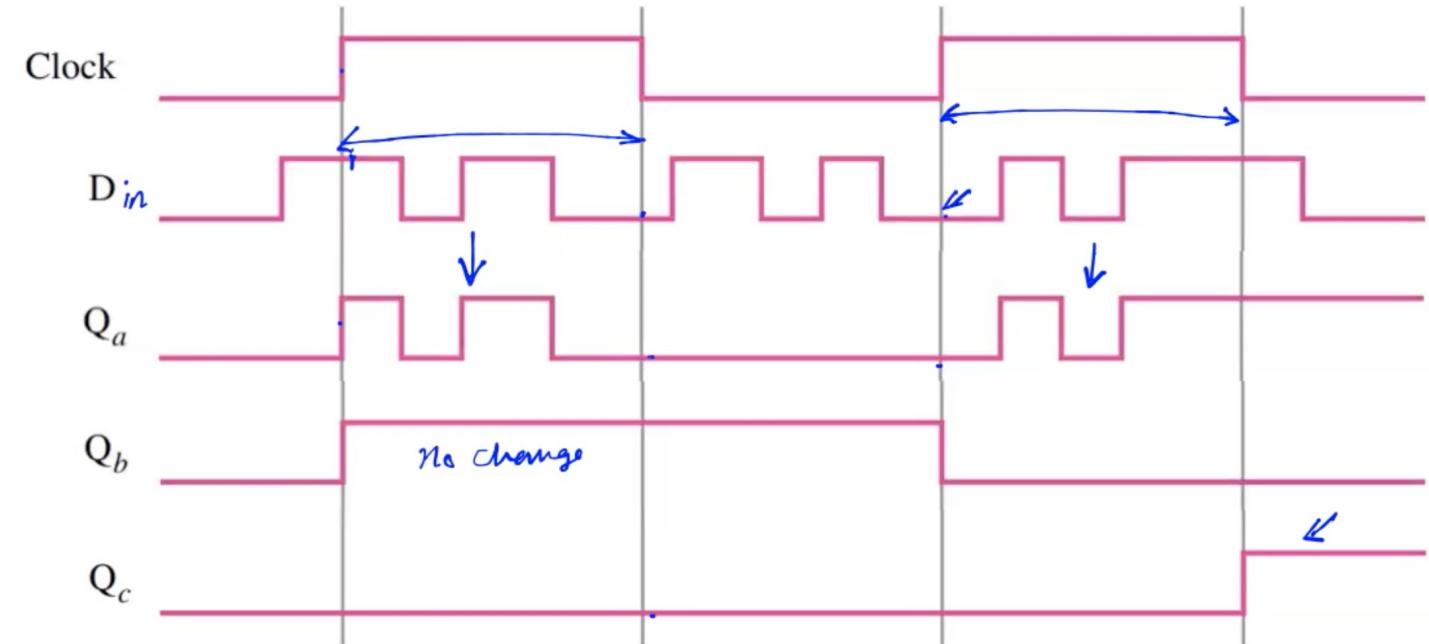


Positive Edge Triggered D-FF

# Level and Edge Triggered D-FFs:

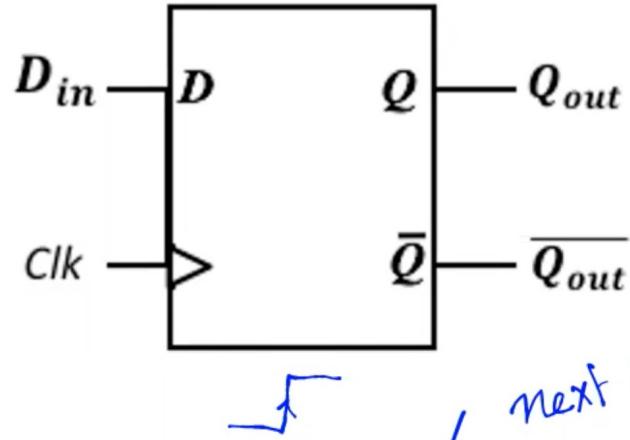


Level Triggered Latch



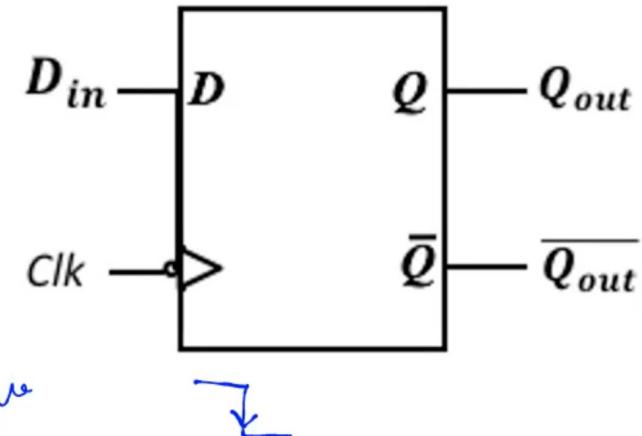
Edge Triggered Latch - An emulated property.  
FF

## Truth Table for Edge Triggered D-FF:



D	Clk	Q <sub>n</sub>	Q̄ <sub>n</sub>
0	↑	0	1
1	↑	1	0

next value of Q  
Q<sub>n-1</sub> → immediate previous value or present value  
Q<sub>p</sub>

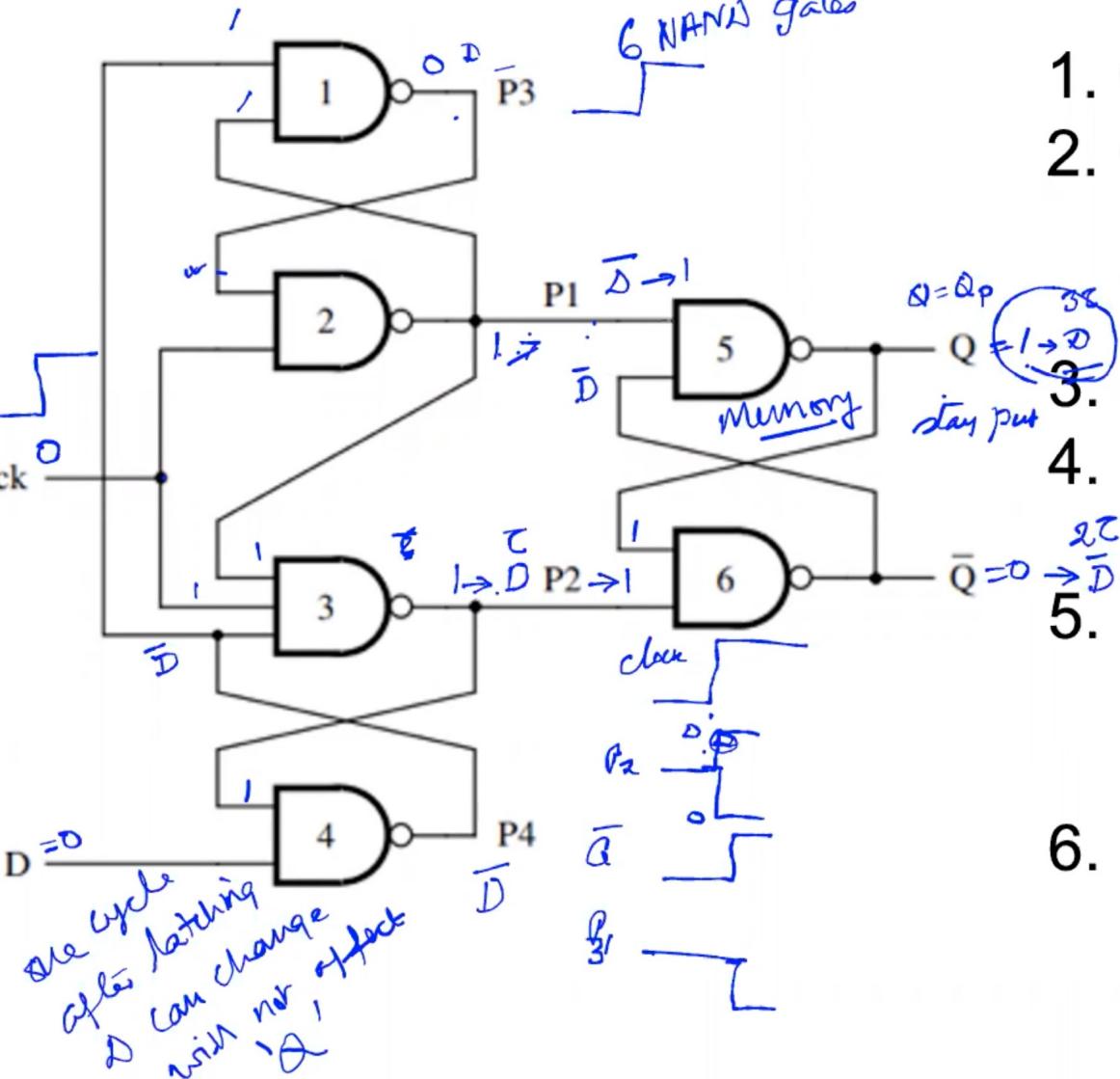


D	Clk	Q <sub>n</sub>	Q̄ <sub>n</sub>
0	↓ <sup>-&gt; edge</sup>	0	1
1	↓	1	0

# Edge Triggered D-FF Using 6 NAND Gates:

$$8+1=9 \text{ NAND gates}$$

NAND galés

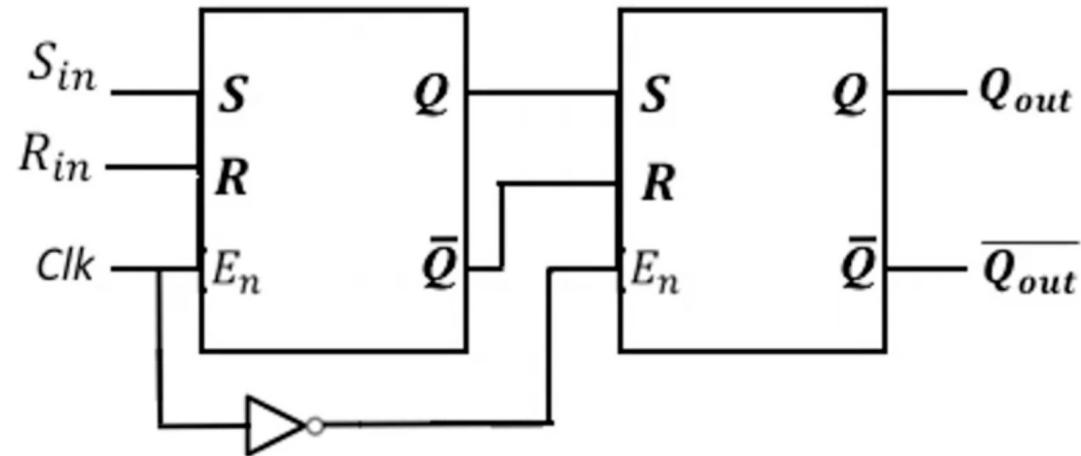


5. finite delay of each gate

1. Clock = 0;  $P_2 = P_1 = 1$  and  $P_4 = \bar{D}$ . let  $Q = \underline{\underline{1}}$
  2. Clock transits from 0 to 1  
 $P_4 = \bar{D}$ ;  $P_2 = D$  and  $\bar{Q} = \bar{D}$  and  $Q = D$ ,  $P_3 = \underline{\underline{P_4}} = D$  and  $P_1 = \bar{D}$ .
  3. Clock = 1;  $P_1 = \bar{D}$ ;  $P_2 = \underline{\underline{D}}$  hence  $Q = D$
  4. Clock ~~transits~~ from 1 to 0  
 $P_1 = P_2 = 1$  and  $Q = \underline{\underline{D}}$   $\bar{Q} = \bar{D}$
  5. Clock = 0,  $P_1 = P_2 = 1$  and the output remains unchanged, and the circuit is in memory state.
  6. If  $D$  changes while the clock is stable at 0 or 1, the output will remain unaffected.

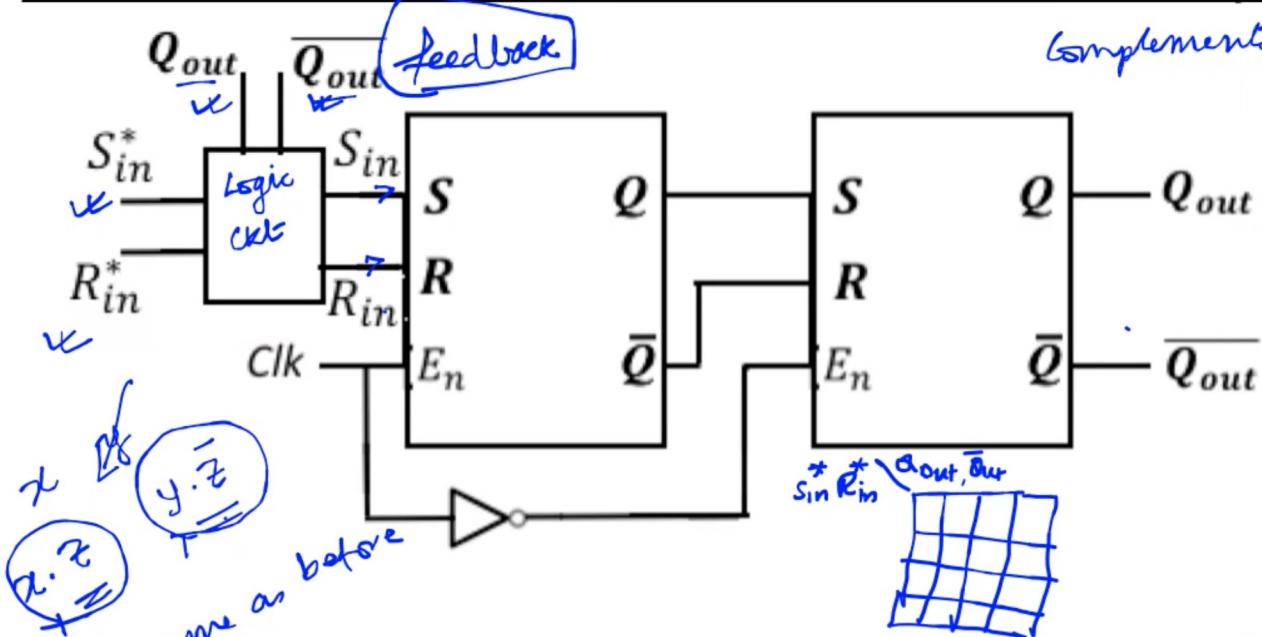
## Edge Triggered Master Slave S-R Flip Flop:

~~Wrote~~  ~~$S_{in} = R_{in} = 1$~~   $R_{in} = \bar{S}_{in} \rightarrow \underline{\underline{D-FF}}$



$S_{in}$	$R_{in}$	$Clk$	$Q_n$	$\bar{Q}_n$
0	0	↓	$Q_{n-1}$	$\bar{Q}_{n-1}$
0	1	↓	0	1
1	0	↓	1	0
1	1		Forbidden	

## Provisions to use 1-1 combination at the input of an Edge Triggered S-R Flip Flop:



$$S_{in} = S_{in}^* \overline{Q_{n-1}}$$

$$R_{in} = R_{in}^* Q_{n-1}$$

Complements

$S_{in}^*$	$R_{in}^*$	$Clk$	$Q_n$	$\bar{Q}_n$
0	0	↓	$Q_{n-1}$	$\bar{Q}_{n-1}$
0	1	↓	0	1
1	0	↓	1	0
1	1	↓	$\bar{Q}_{n-1}$	$Q_{n-1}$

available  
demand ↪

$S_{in}^*$	$R_{in}^*$	00	01	11	10
00	φ	0	φ	0	0
01	φ	0	φ	0	0
11	φ	1	φ	0	0
10	φ	1	φ	0	φ

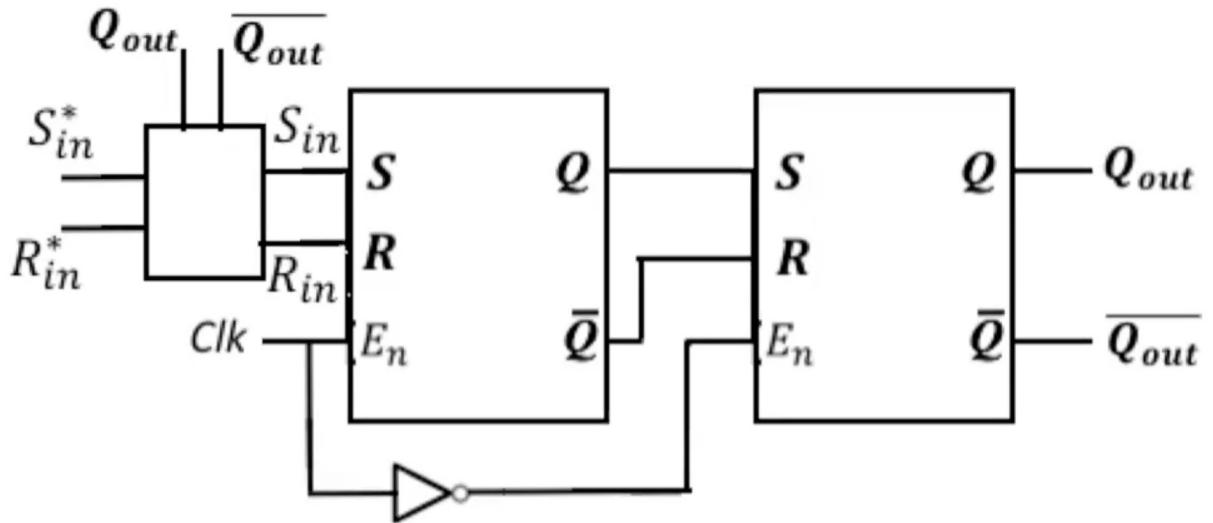
K-Map for  $S_{in}$

IIITD ECE 111 Section A

$S_{in}^*$	$R_{in}^*$	00	01	11	10
00	φ	0	φ	0	0
01	φ	φ	φ	1	0
11	φ	0	φ	1	0
10	φ	0	φ	0	0

K-Map for  $R_{in}$

$S_{in}^*$	$R_{in}^*$	$Q_{n-1}$	S	R	$Clk$	$Q_n$
0	0	0	0	0	↓	0
0	0	1	1	0	↓	1
0	1	0	0	0	↓	0
0	1	1	0	1	↓	0
1	0	0	1	0	↓	1
1	0	1	0	0	↓	1
1	1	0	1	0	↓	1
1	1	1	0	1	↓	0

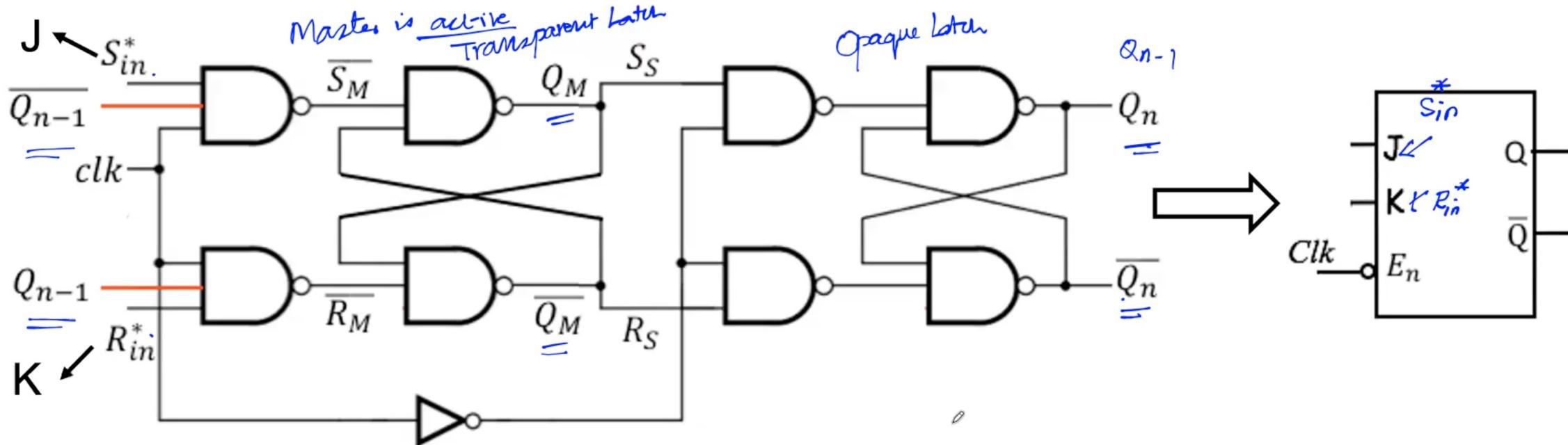


I got

$$S_{in} = S_{in}^* \overline{Q_{n-1}}$$

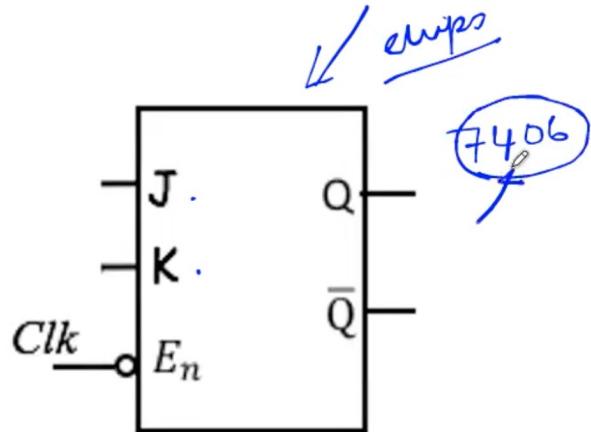
$$R_{in} = R_{in}^* Q_{n-1}$$

## NAND based Master-Slave (Edge Triggered) Flip Flop:



clk	clk	$Q_{n-1}$	$\bar{Q}_{n-1}$	$S_{in}^*$	$R_{in}^*$	$S_{in}$	$R_{in}$	$Q_M$	$\bar{Q}_M$	$S$	$R$	$Q_n$	$\bar{Q}_n$
1	1	0	1	1	1	0	1	1	0	1	1	0	1
↓	0	0	1	1	1	1	1	1	0	0	1	1	0
1	1	1	0	1	1	1	0	0	1	1	1	1	0
↓	0	1	0	1	1	1	1	0	1	1	0	0	1
1	1	0	1	1	1	0	1	1	0	1	1	0	1
↓	0	0	1	1	1	1	1	1	0	0	1	1	0

## J K Flip Flop:



$J$	$K$	$Clk$	$Q_n$	$\bar{Q}_n$
0	0	$\downarrow$	$Q_{n-1}$	$\bar{Q}_{n-1}$
0	1	$\downarrow$	0	1
1	0	$\downarrow$	1	0
1	1	$\downarrow$	$\bar{Q}_{n-1}$	$Q_{n-1}$

Integrated circuits  
calculators

Casio  
pioneers

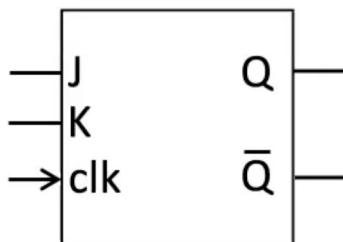
TI  
HP

Named after the first person to make an integrated circuit while working with Texas Instruments, **Jack Kilby**. He later obtained Physics Nobel Prize in 2000.

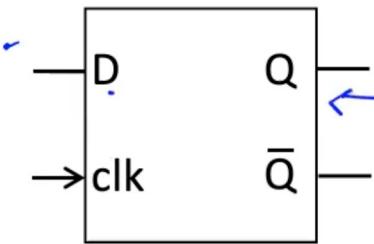
## J-K FF, D-FF and T-FF:

$J$	$K$	$Q_n$	$\bar{Q}_n$
0	0	$Q_{n-1}$	$\bar{Q}_{n-1}$
0	1	0	1
1	0	1	0
1	1	$\bar{Q}_{n-1}$	$Q_{n-1}$

Toggles



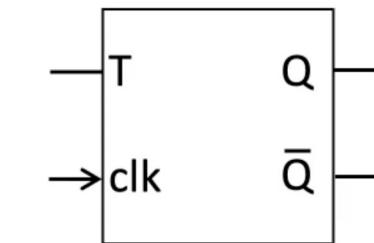
$$\begin{array}{l} K = \bar{J} \\ \underline{D = J = \bar{K}} \end{array}$$



$D$	$Q_n$	$\bar{Q}_n$
0	0	1
1	1	0

$D$ -FF  $\rightarrow$  Data FF  
delay FF

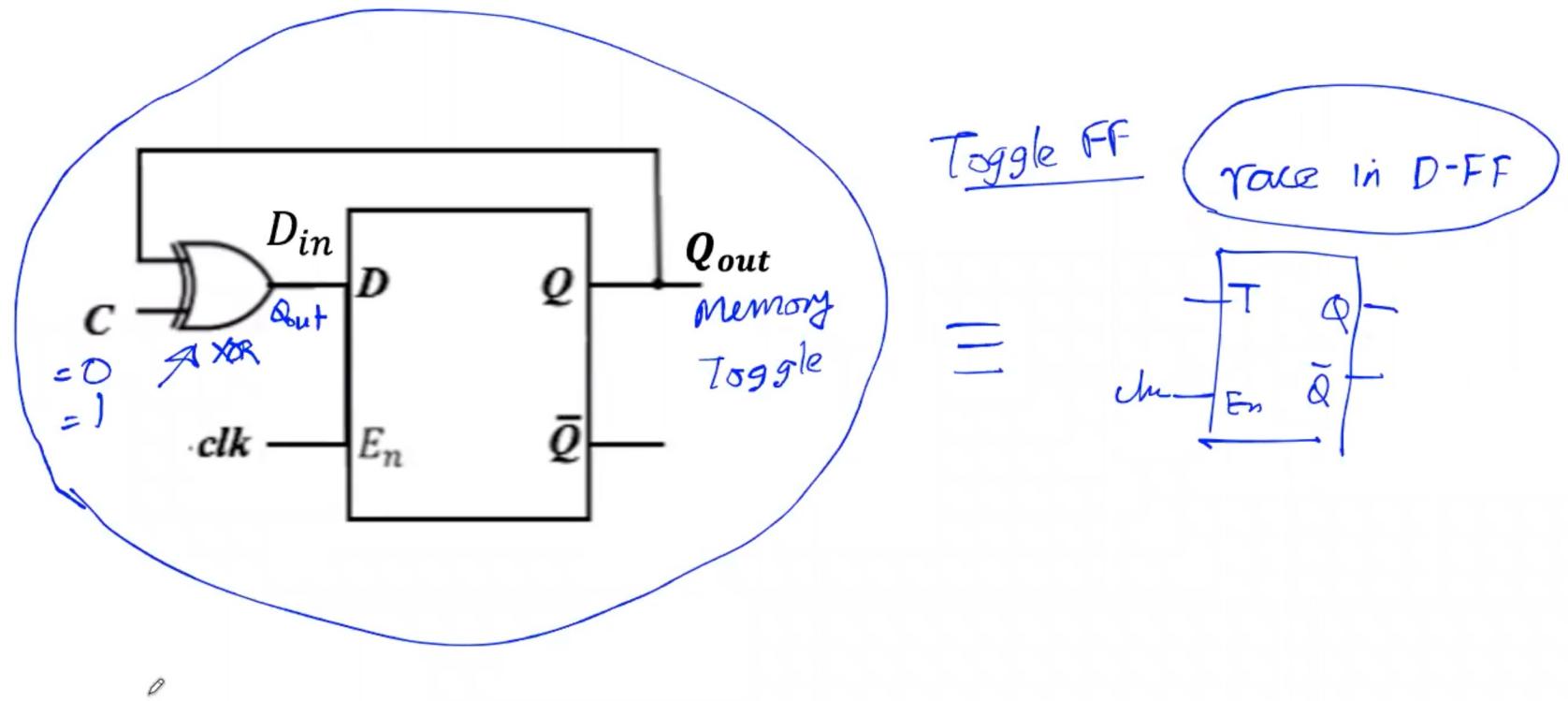
$$T = J = K$$



Toggle FF

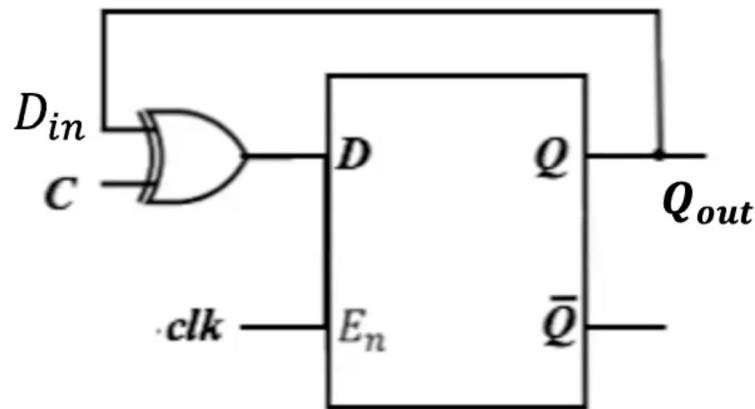
$T$	$Q_n$	$\bar{Q}_n$
0	$Q_{n-1}$	$\bar{Q}_{n-1}$
1	$\bar{Q}_{n-1}$	$Q_{n-1}$

Identify the nature of this FF and the normal designation of the input C:

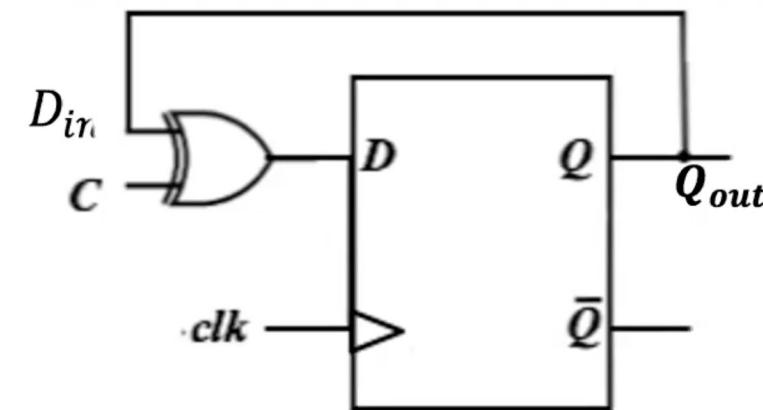


Identify the nature of this FF and the normal designation of the input C:

*You can understand*



T-FF with Race



T-FF without Race