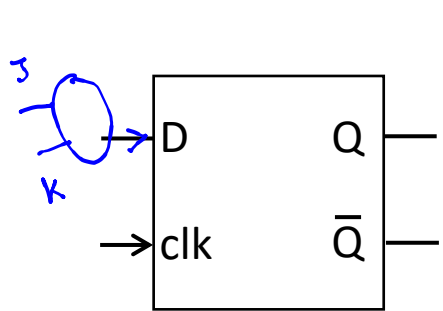


J-K FF Using D-FF

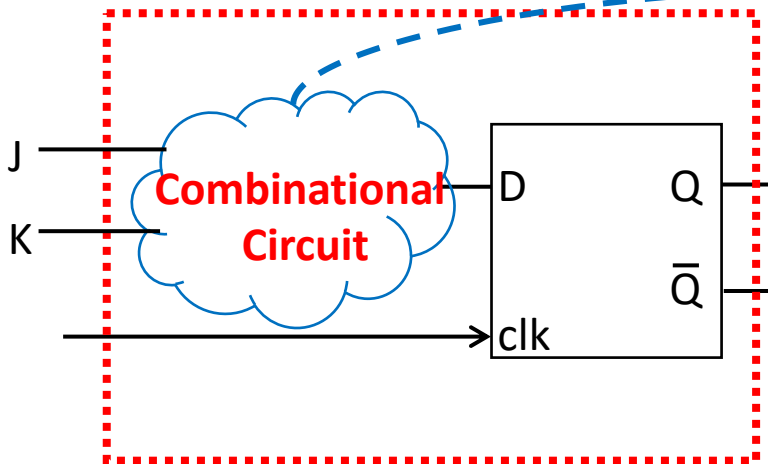
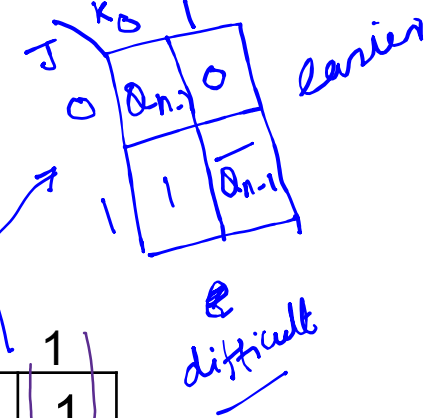
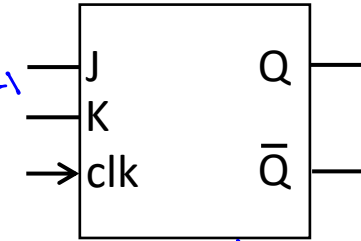


D	Q_n	\bar{Q}_n
0	0	1
1	1	0

Handwritten blue annotations: A circle around the '1' in the D column of the second row, and arrows pointing from the '0' and '1' in the Q_n column to the '0' and '1' in the D column respectively.

J	K	Q_n	\bar{Q}_n
0	0	Q_{n-1}	\bar{Q}_{n-1}
0	1	0	1
1	0	1	0
1	1	\bar{Q}_{n-1}	Q_{n-1}

Handwritten blue annotations: A circle around Q_{n-1} in the first row. Arrows and notes: $D = Q_{n-1}$ (with an arrow from Q_{n-1} to D), $D = 0$ (with an arrow from 0 to D), $D = 1$ (with an arrow from 1 to D), and $D = \bar{Q}_{n-1}$ (with an arrow from \bar{Q}_{n-1} to D).



$$D = f(J, K, Q_{n-1}, \bar{Q}_{n-1})$$

J	K	D
0	0	Q_{n-1}
0	1	0
1	0	1
1	1	\bar{Q}_{n-1}

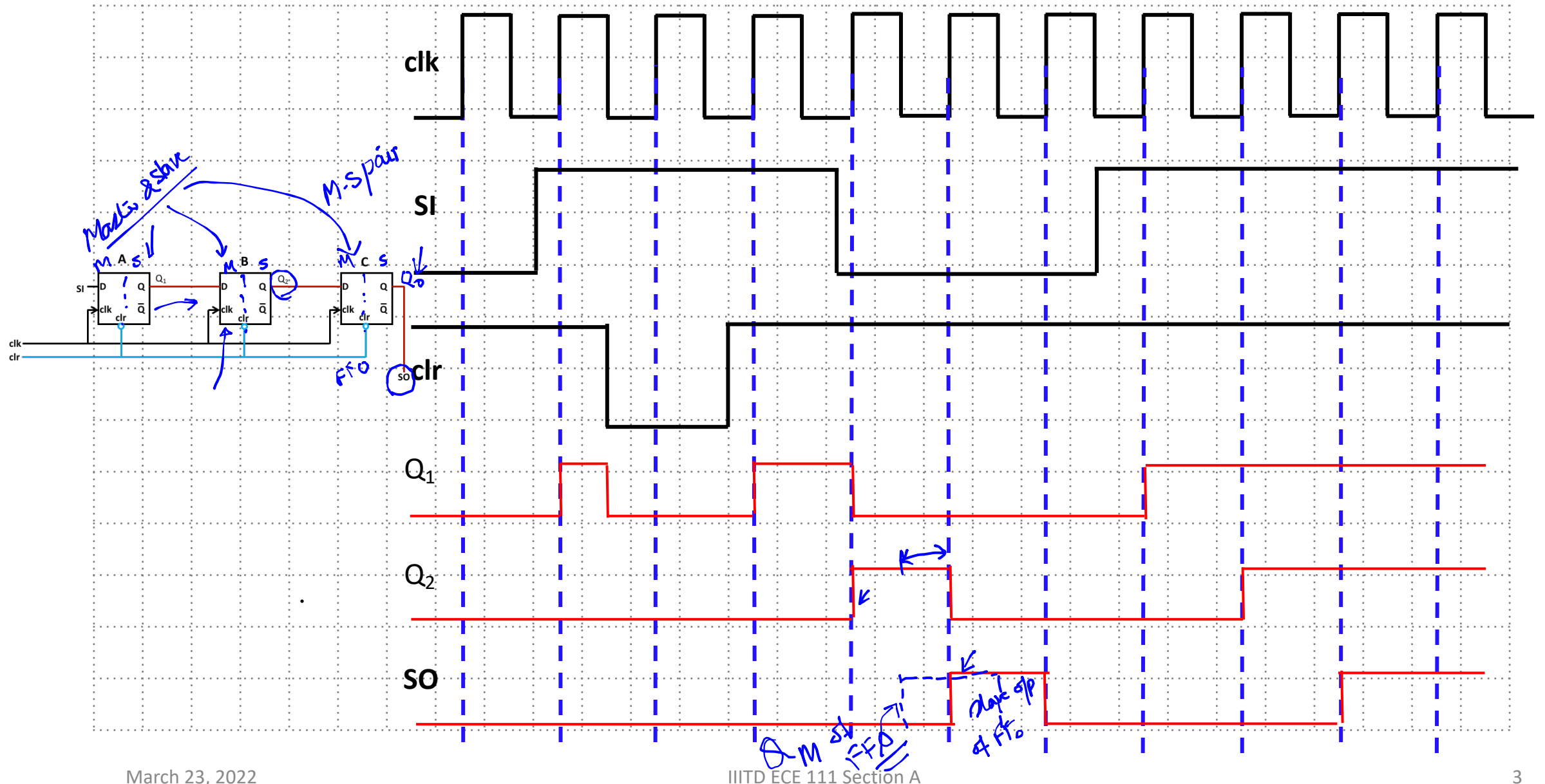
JK	Q_{n-1} 0	Q_{n-1} 1
00	0	1
01	0	0
11	1	0
10	1	1

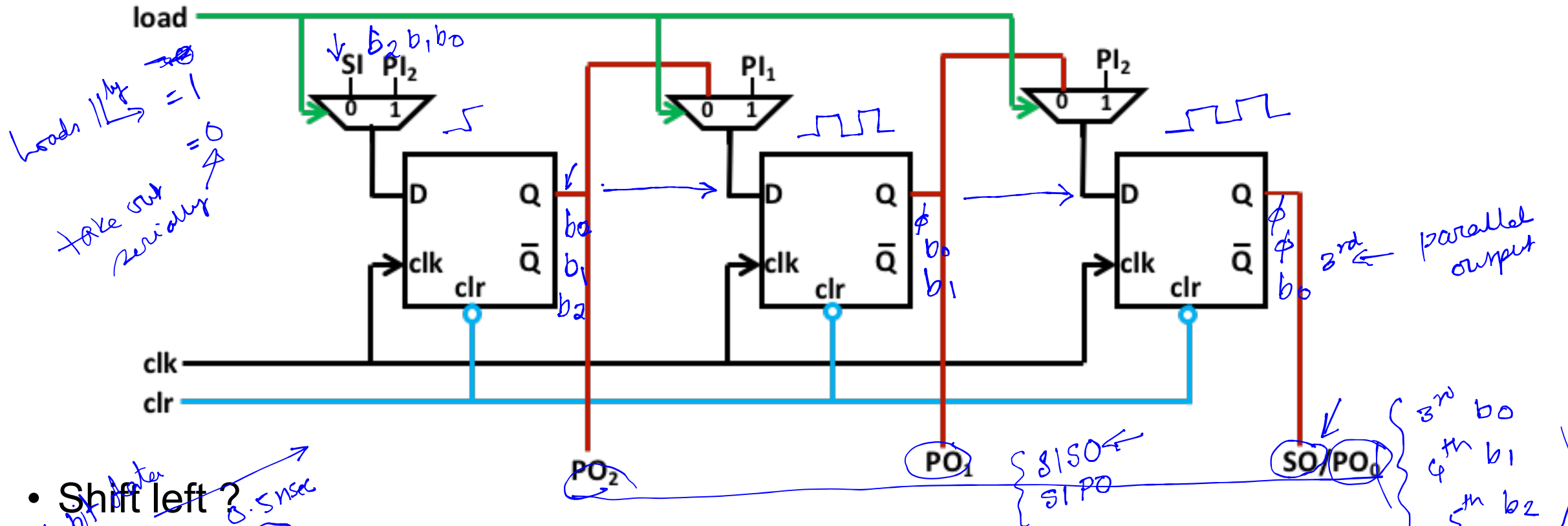
Handwritten blue annotations: Circles around the '1' in the top-right cell (00, 1) and the '1' in the bottom-left cell (10, 0). An arrow points from the '1' in the top-right cell to the '1' in the bottom-left cell.

$$D = J\bar{Q}_{n-1} + \bar{K}Q_{n-1}$$

Similarly realize T-FF using D-FF and D-FF using T-FF

Shift Register (SISO):

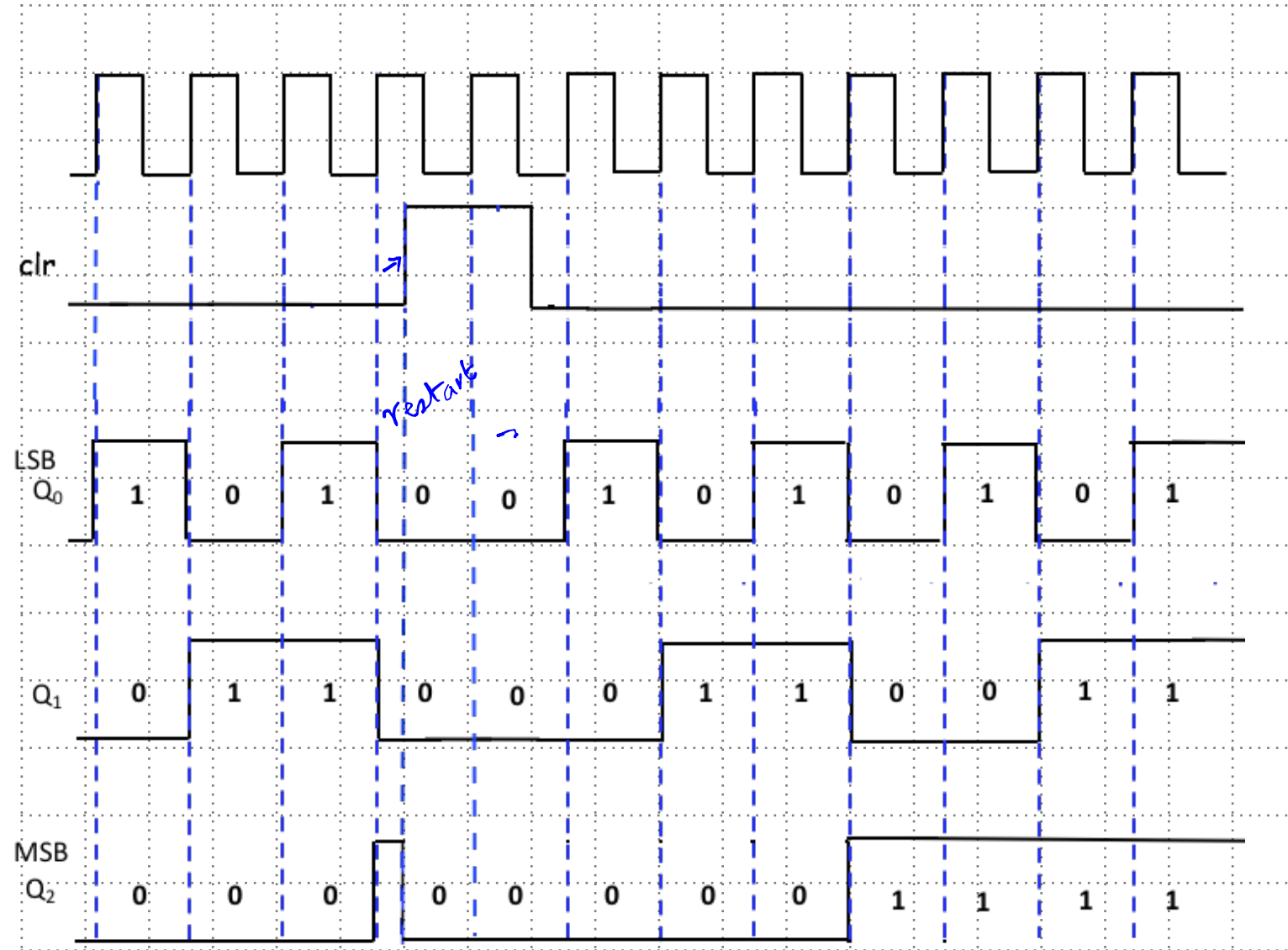
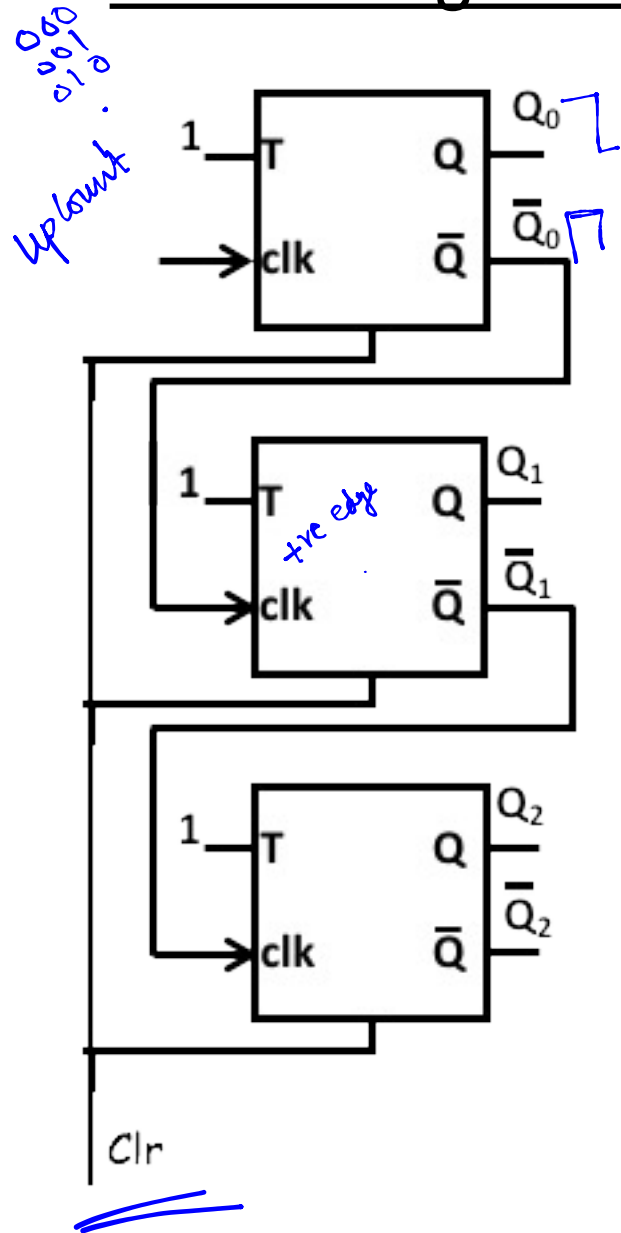




- Shift left ?
- Shift right ?
- Memory

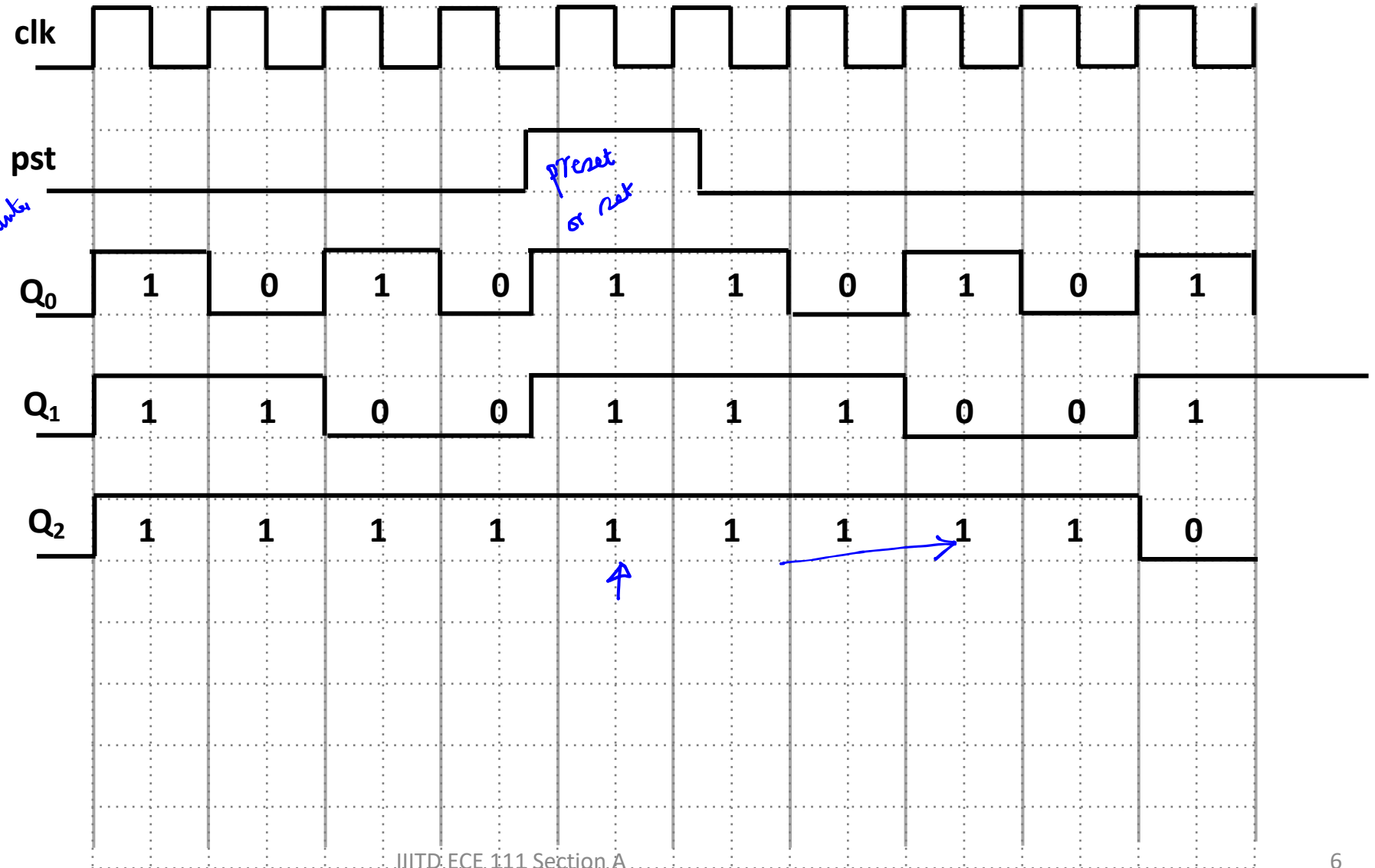
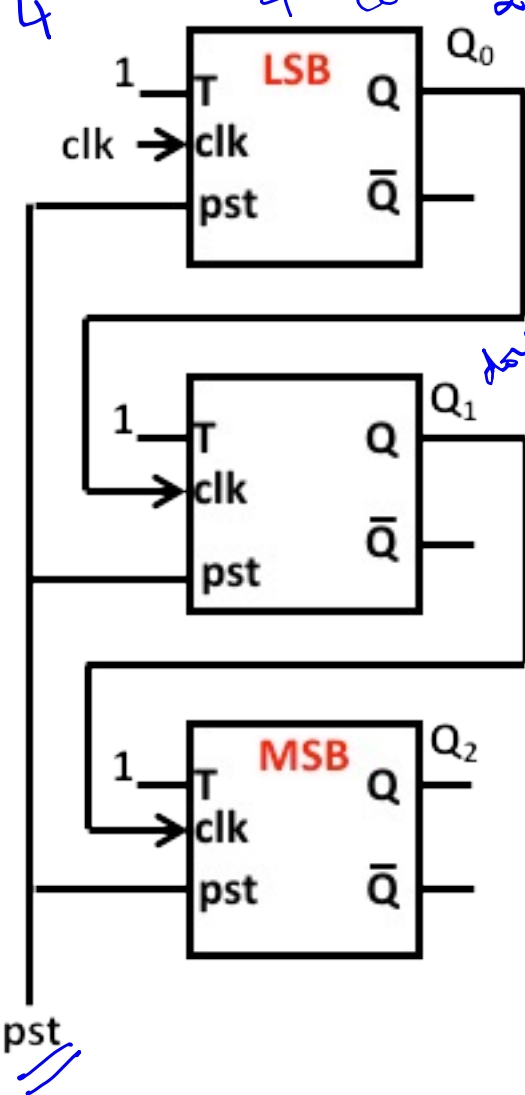
Shift Register (SISO, PISO, PIPO, SIPO, Shift Right)

3-Bit Unsigned Binary UP Counter with Clear:



3-Bit Unsigned Binary Down Counter with Preset:

4 TFF
4-bit counter $2^N \rightarrow N$ counter



Binary Counter with Clear and Preset– Count length not a power of 2:

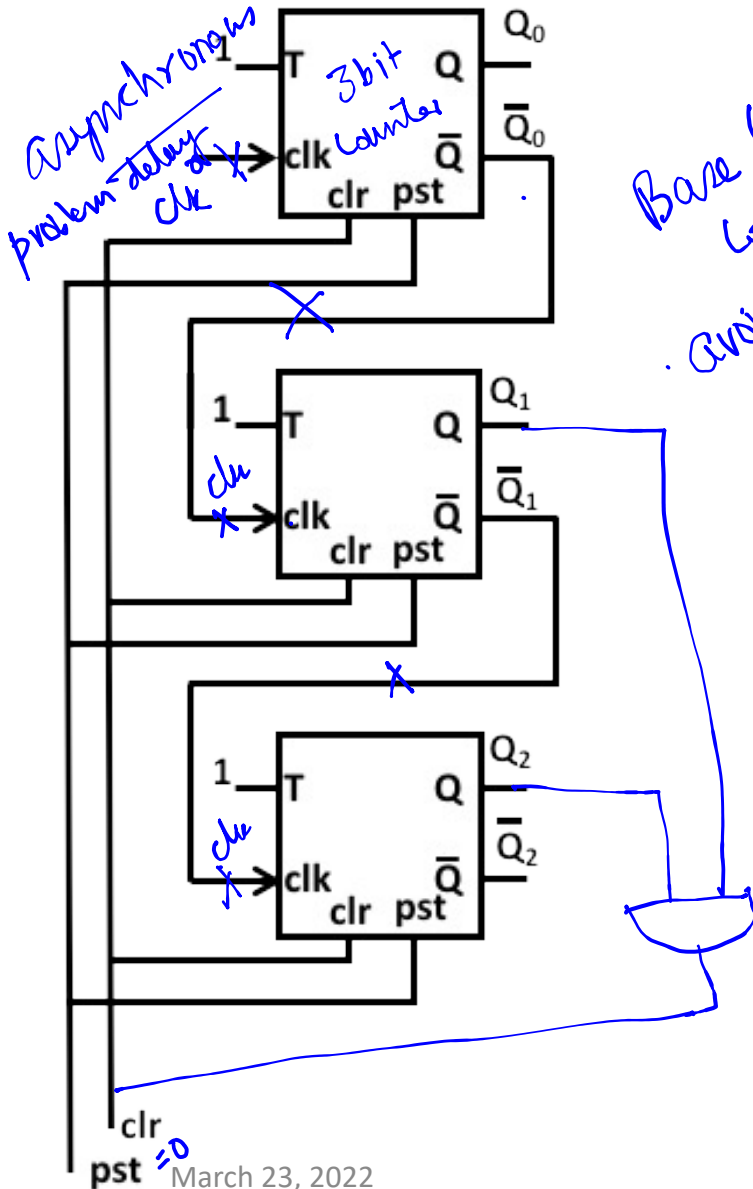
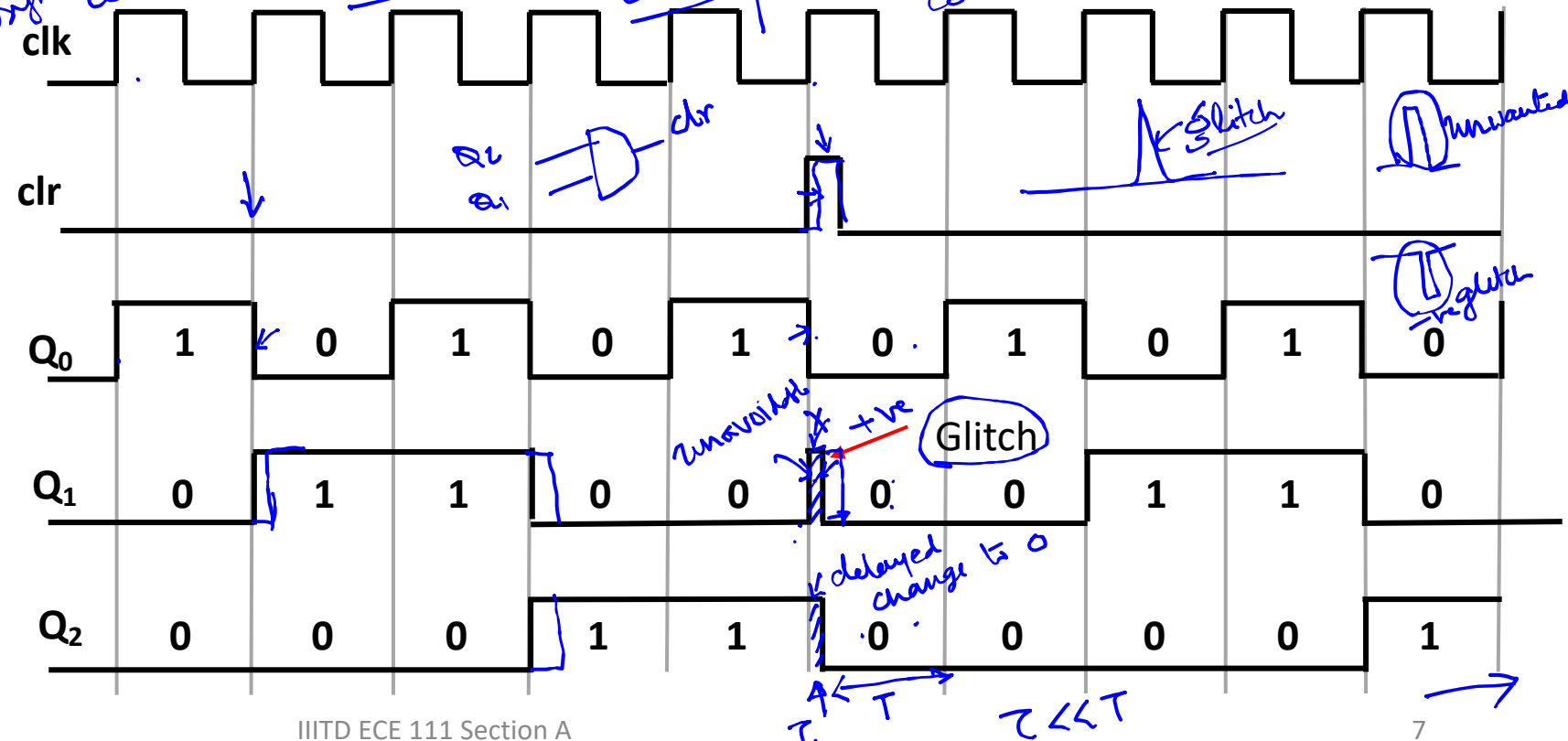
- Modulo 6 counter:** $0 \rightarrow 1 \rightarrow 2 \rightarrow 3 \rightarrow 4 \rightarrow 5 \rightarrow 0 \rightarrow 1 \dots$

$000 \rightarrow 001 \rightarrow 010 \rightarrow 011 \rightarrow 100 \rightarrow 101 \rightarrow 000 \rightarrow 001 \dots$

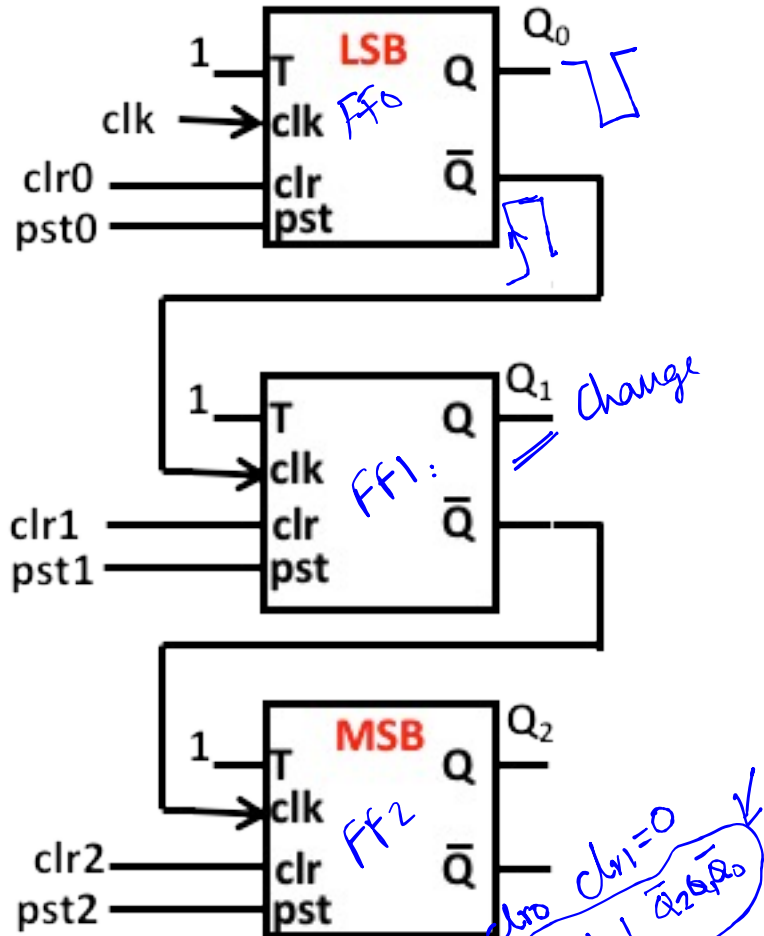
$$\text{clr} = Q_2 \cdot Q_1$$

all FFs have the same clock

clear is rth
back here
short period
asynchronous control.
110
000
111
 $\text{clr} = Q_2 \cdot Q_1$



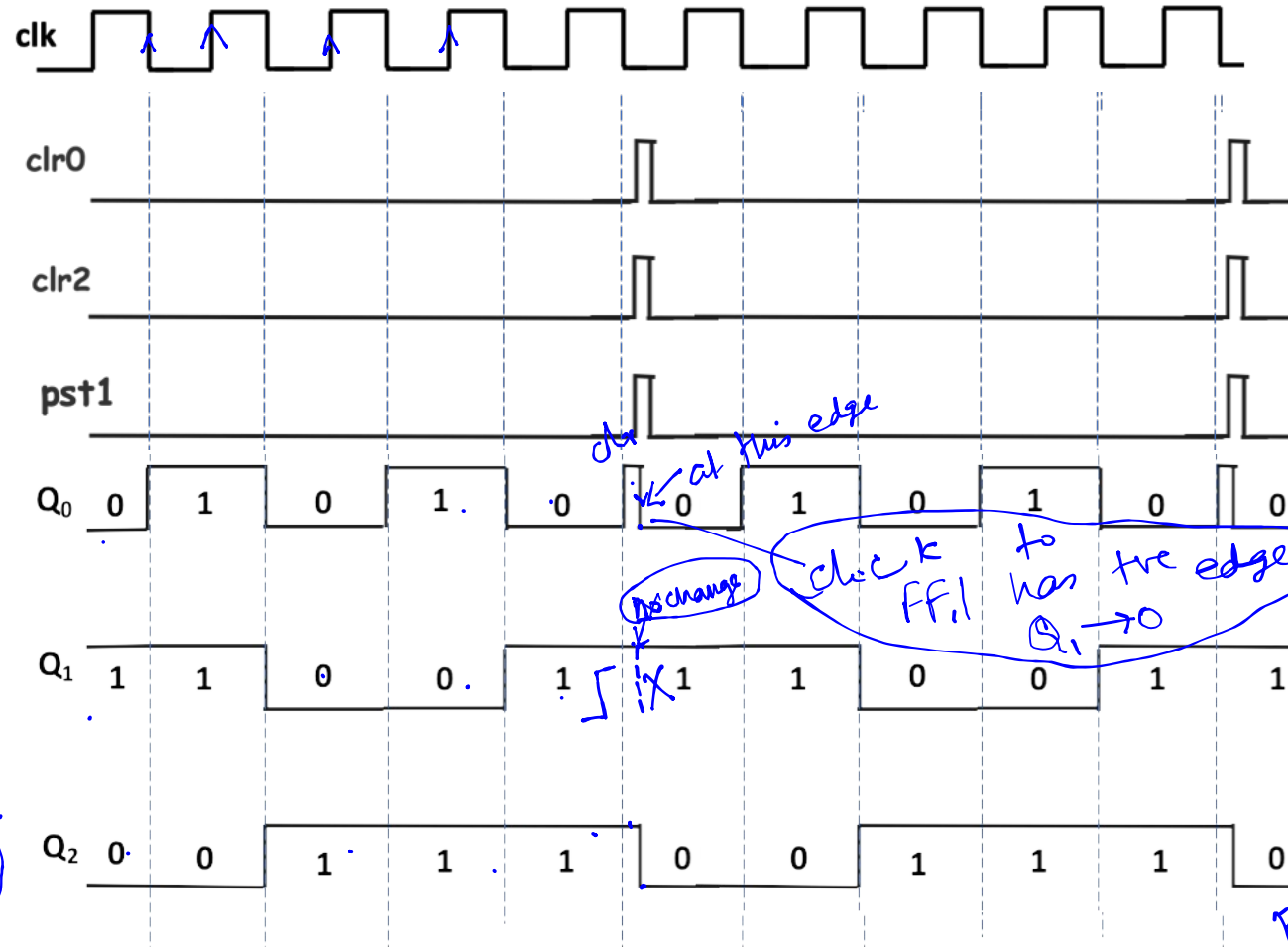
Binary Counter with Clear and Preset:



- **Counter:** 2->3->4->5-> 6->2->3->4->5-> 6->2-----

3 bits

010 011 100 101 110



cut this edge

No change

check to the edge
FF.1 has the edge
① → 0

éviter
↓
prévenir

$$125t = 1$$

0
p_{st}1 = dr0 = dr2

$$clr0 = clr2 = pst1 = Q_2 \cdot Q_1 \cdot Q_0 ; \quad clr1 = pst0 = pst2 = 0$$

March 23, 2022

HW:

1. Design the counter with sequence as 4-5-6-7-8-9-4.... Using active low clear and active low preset
2. Assume that you have an oscillator which provides clock signal with frequency 8 Hz. Design modulo-6 counter which increments its output count every second.
period $\rightarrow \frac{1}{8}$ sec $\rightarrow 128$ \rightarrow
3. Decade BCD counter.

Definition of some important characteristics with Digital Circuits:

Combinational Circuits:

