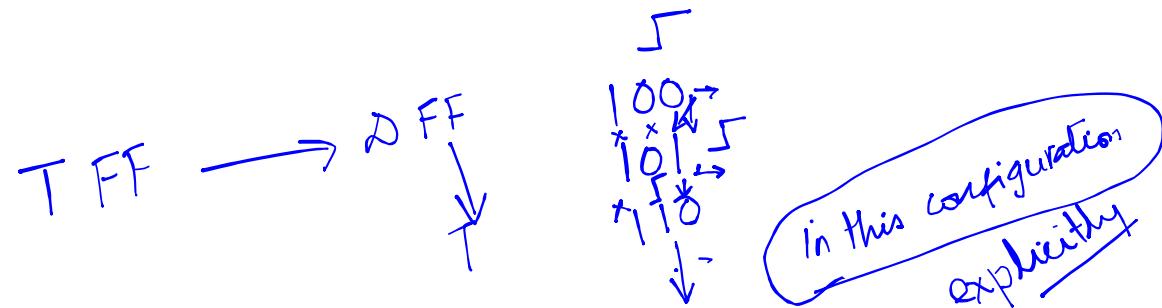


SR latch made with basic logic gates have different functionality??

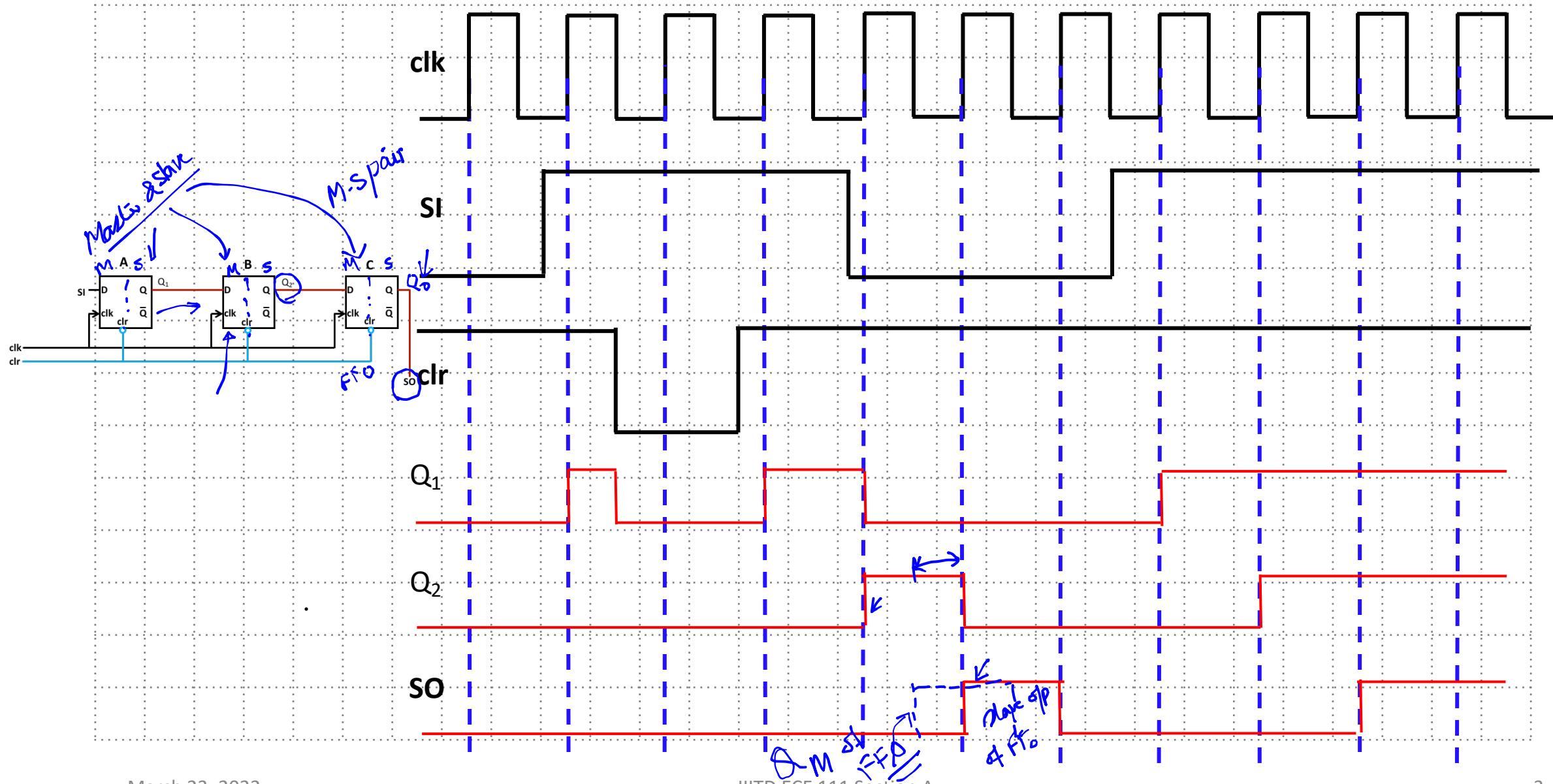
HW:

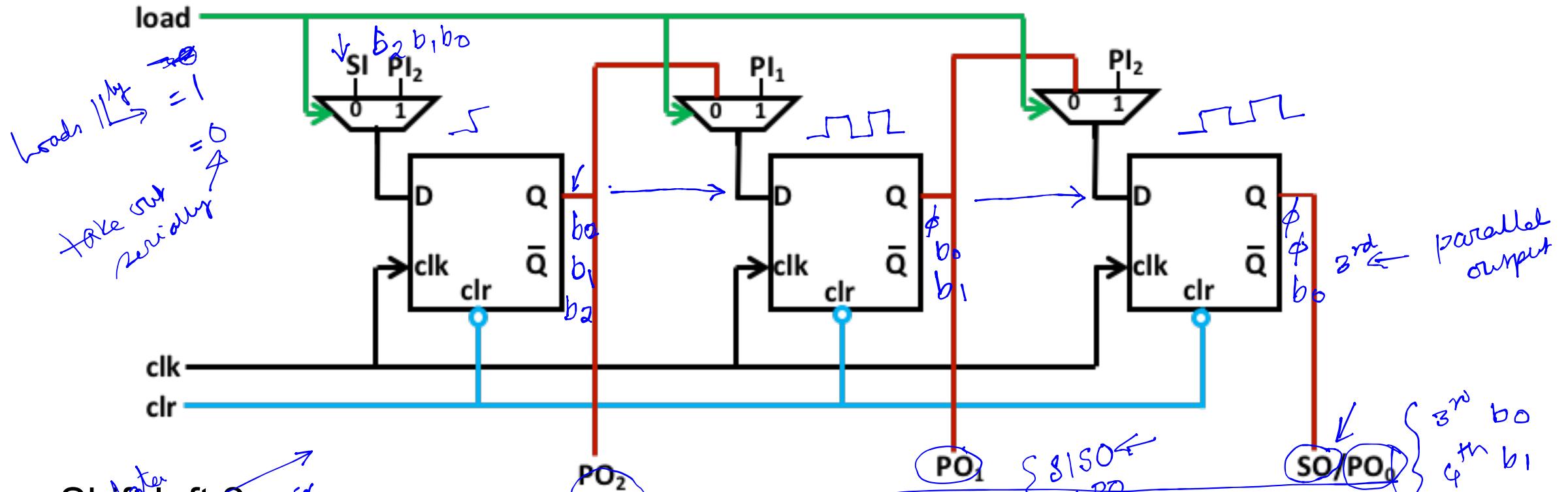


Design the counter with sequence as 4-5-6-7-8-9-4.... Using active low clear and active low preset

Assume that you have an oscillator which provides clock signal with frequency 8 Hz. Design modulo-6 counter which increments its output count every second.

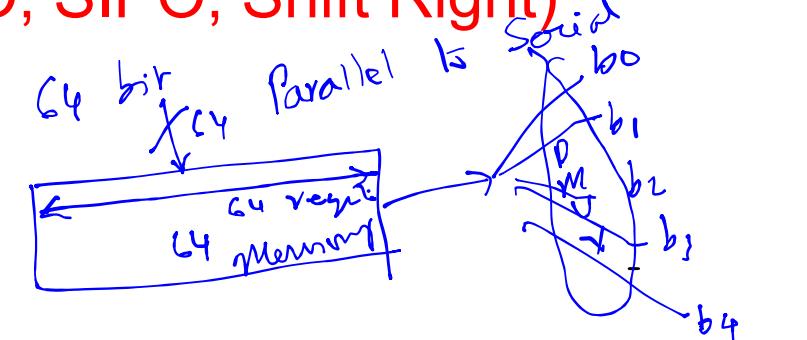
# Shift Register (SISO):





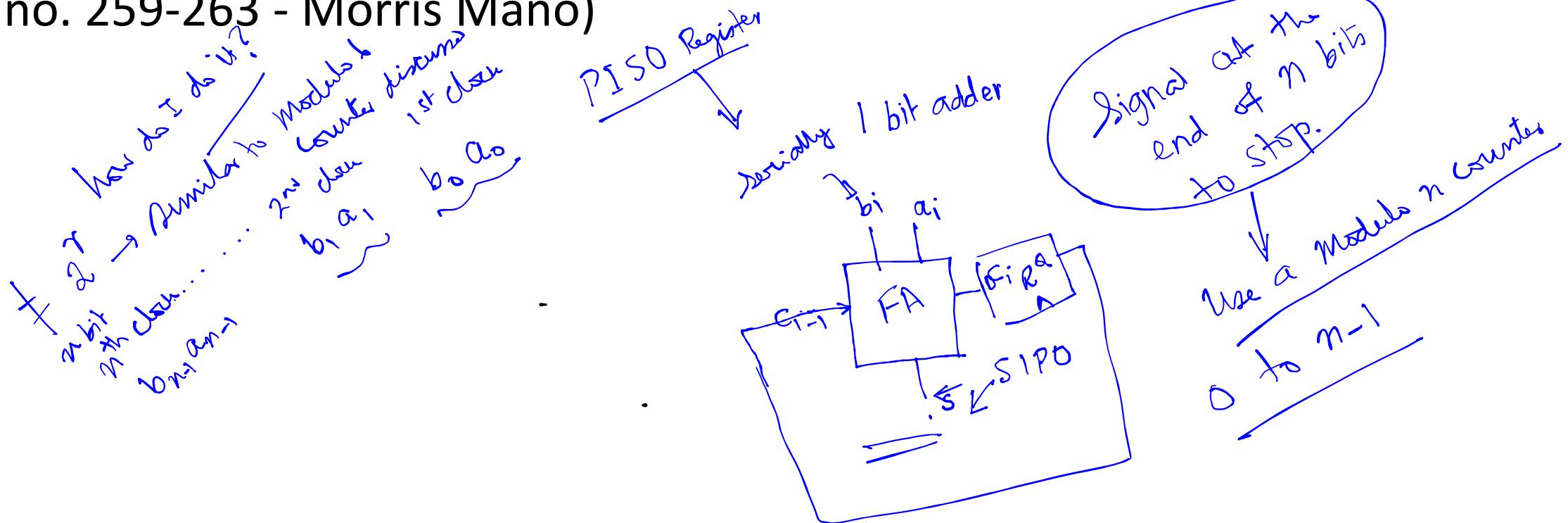
- Shift left ?
  - Shift right ?
  - Memory
- $b_{64}$  bit  
32 nsec  
 $b_{64}$  bit  
64 bit  
Wireless  
analog  
digital  
antenna  
radio receiver  
hear it

## Shift Register (SISO, PISO, PIPO, SIPO, Shift Right)

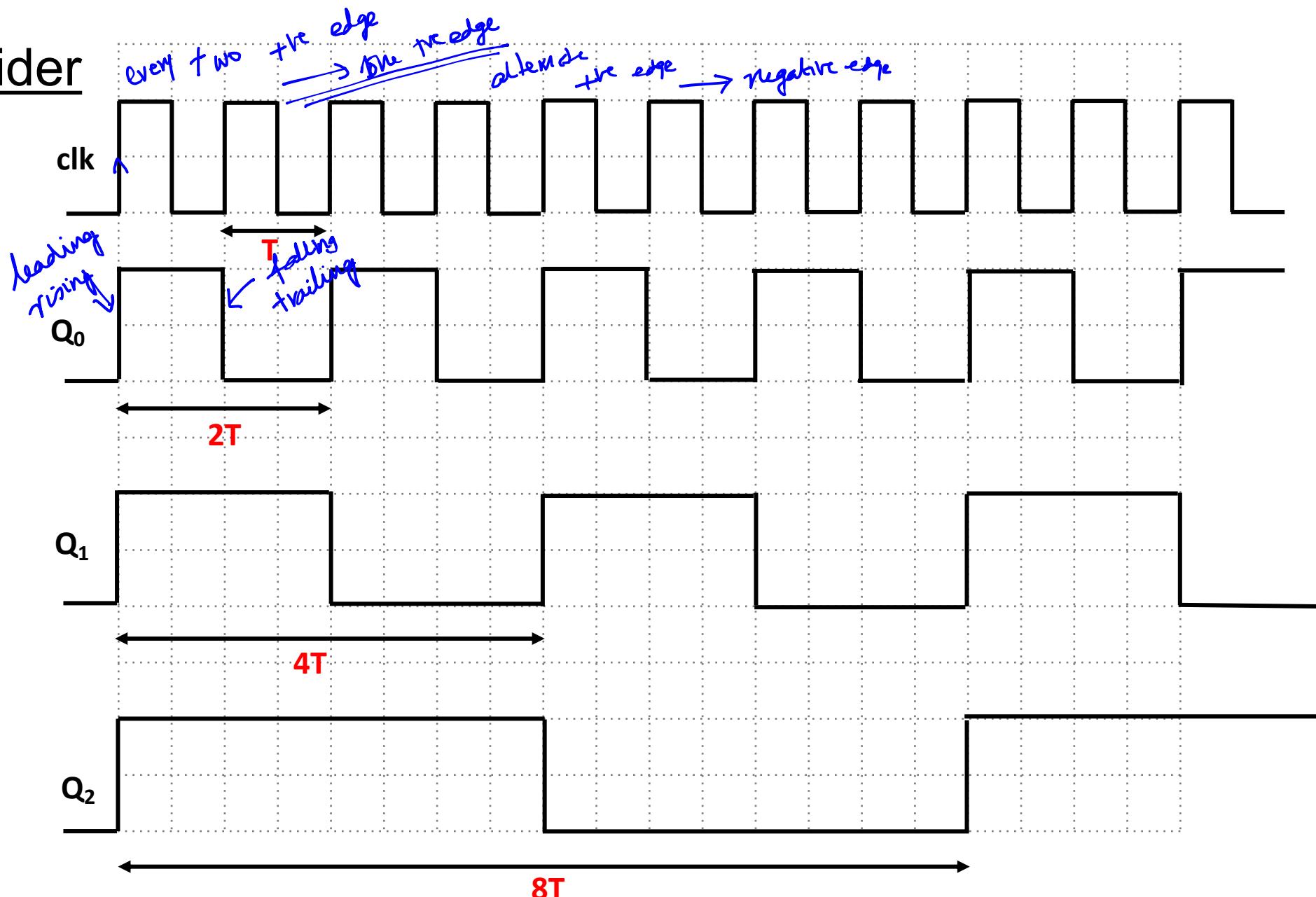
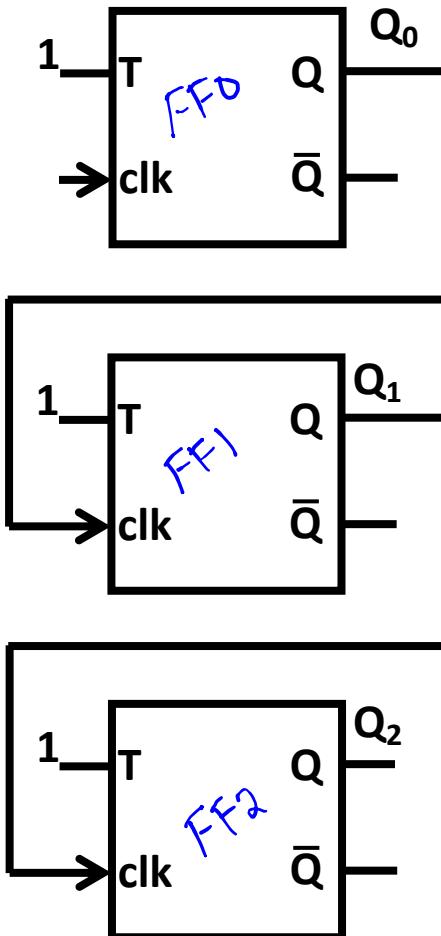


# Universal Shift Register (HW):

- Design serial n-bit adder using 1-bit adder and shift registers (Page no. 259-263 - Morris Mano)

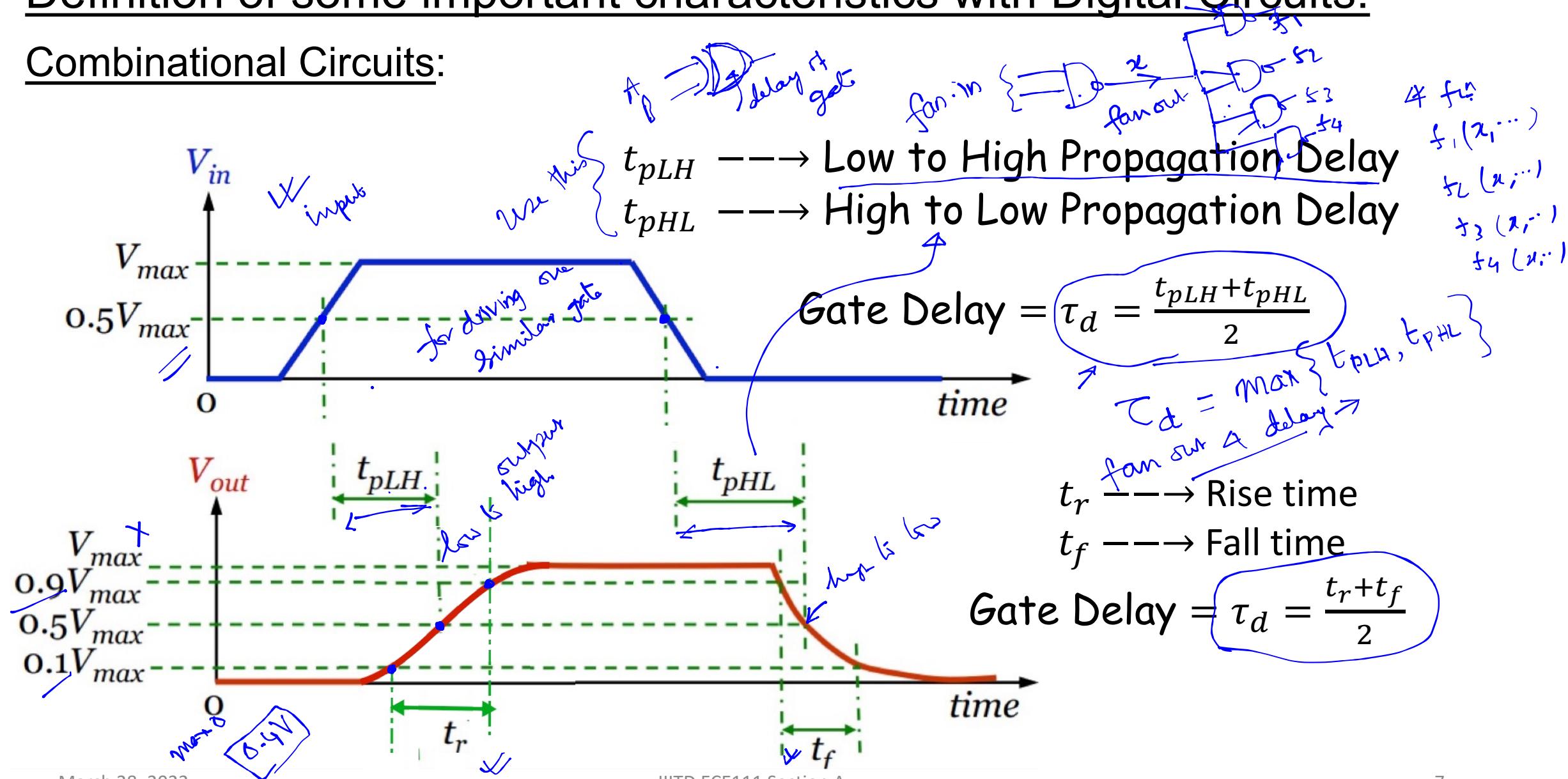


# Frequency Divider



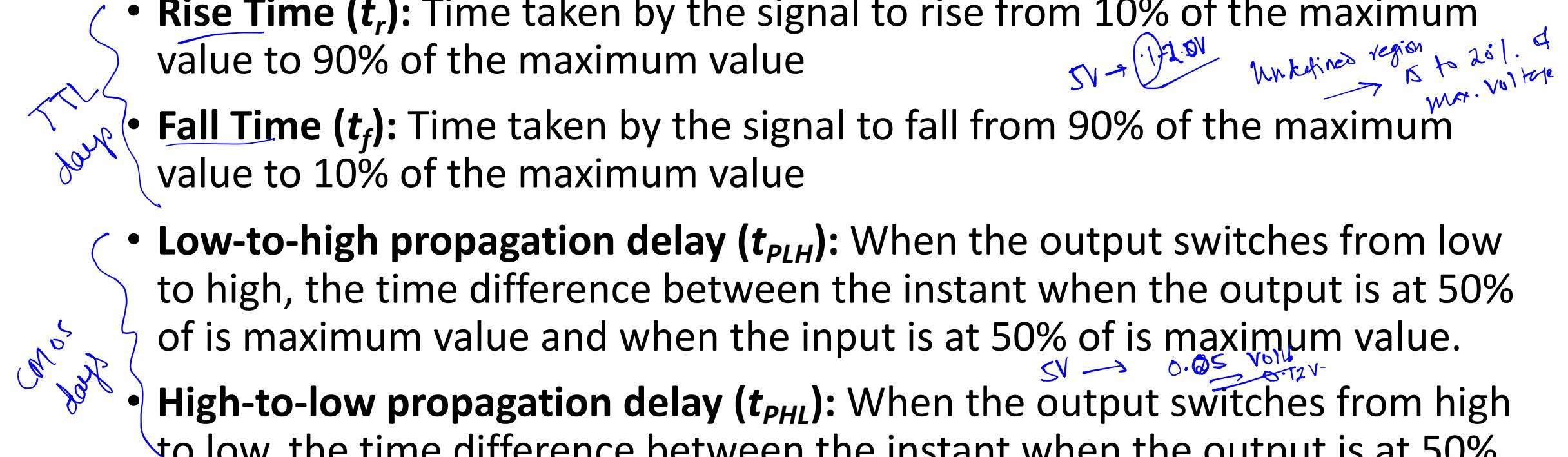
# Definition of some important characteristics with Digital Circuits:

## Combinational Circuits:

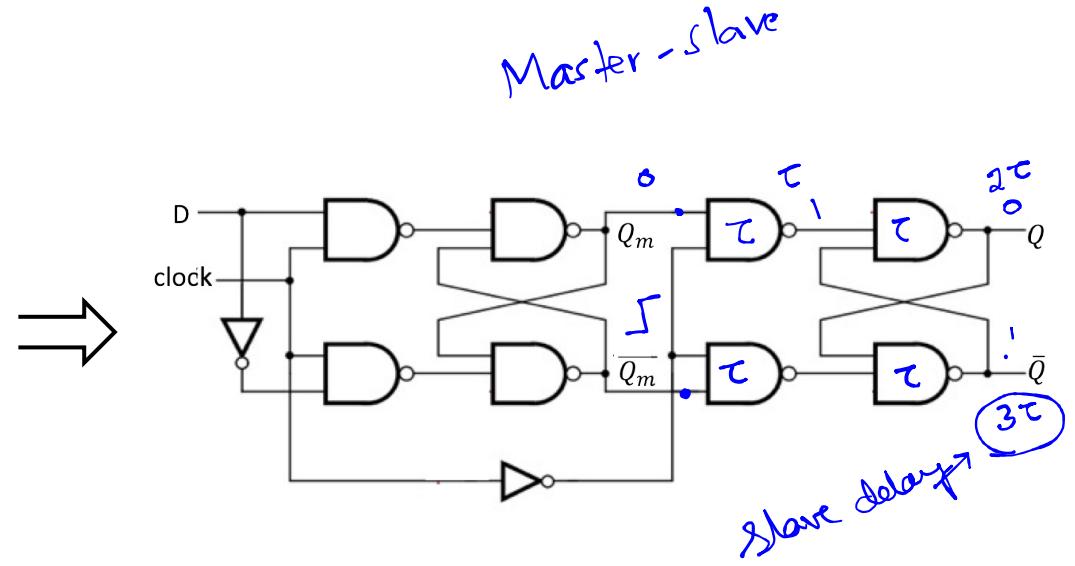
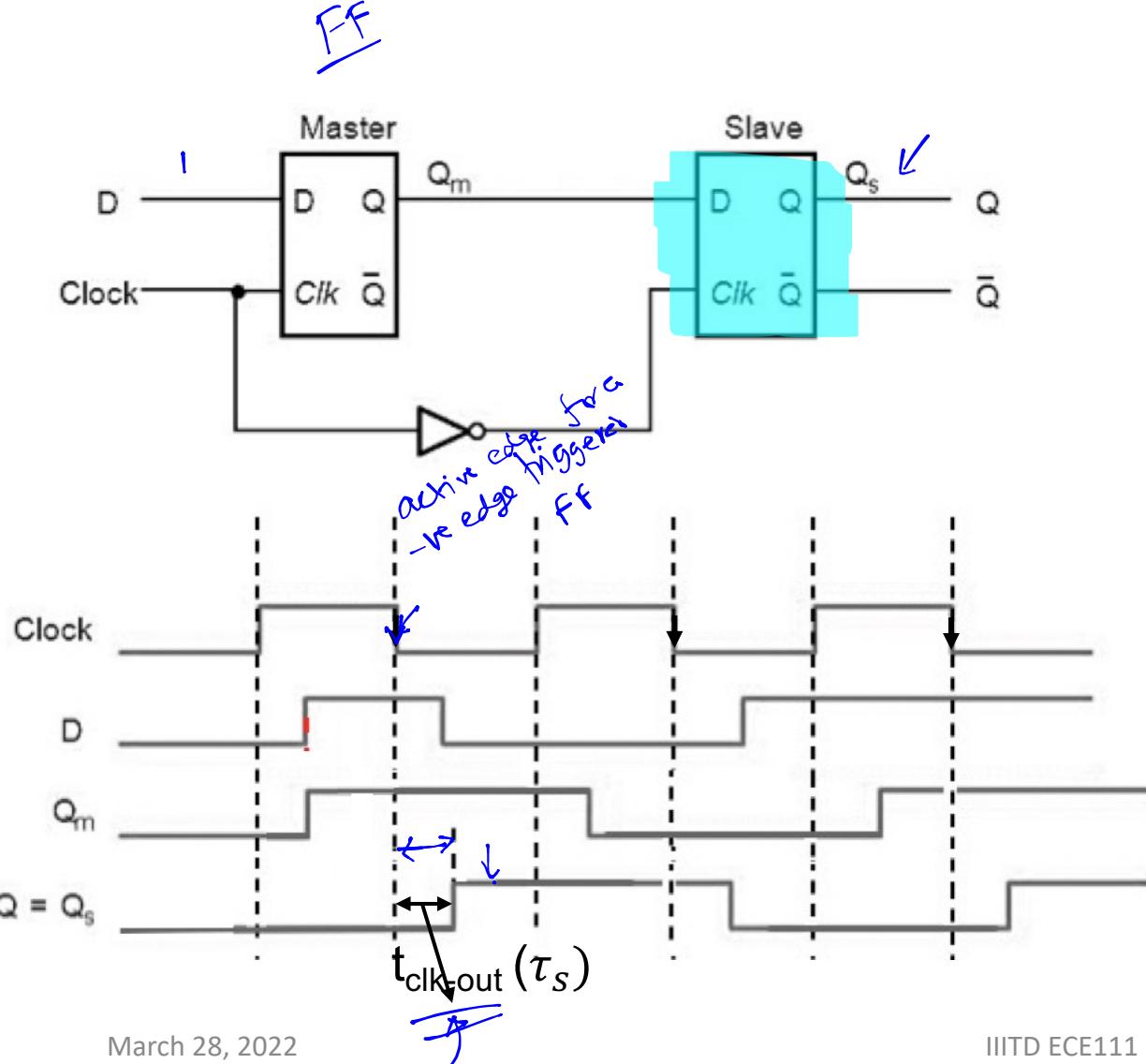


# Timing: Combinational Circuits

- **Rise Time ( $t_r$ )**: Time taken by the signal to rise from 10% of the maximum value to 90% of the maximum value
- **Fall Time ( $t_f$ )**: Time taken by the signal to fall from 90% of the maximum value to 10% of the maximum value
- **Low-to-high propagation delay ( $t_{PLH}$ )**: When the output switches from low to high, the time difference between the instant when the output is at 50% of its maximum value and when the input is at 50% of its maximum value.
- **High-to-low propagation delay ( $t_{PHL}$ )**: When the output switches from high to low, the time difference between the instant when the output is at 50% of its maximum value and when the input is at 50% of its maximum value.

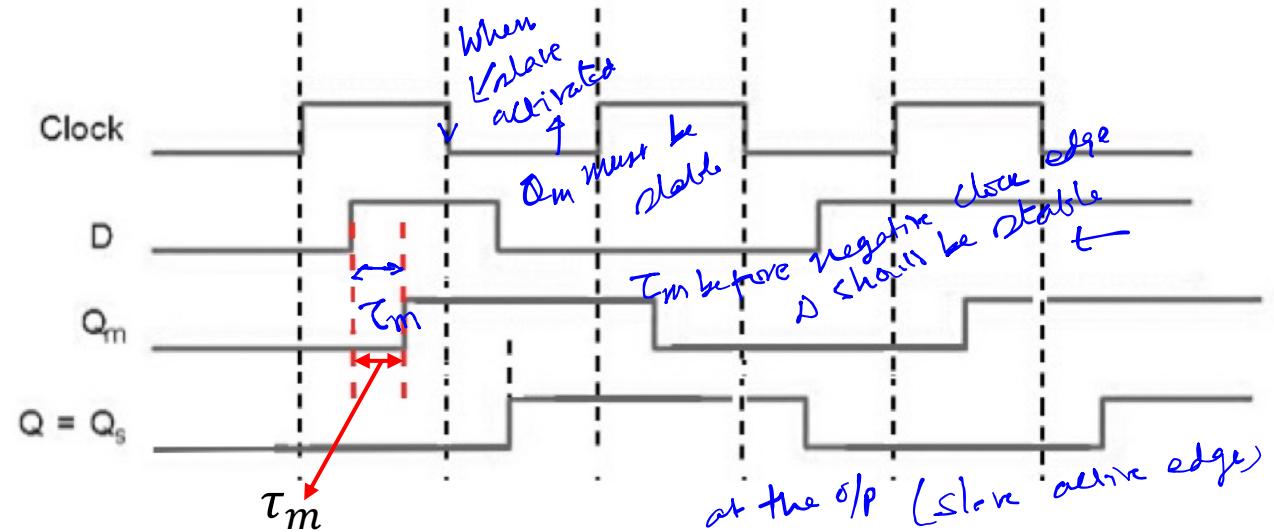
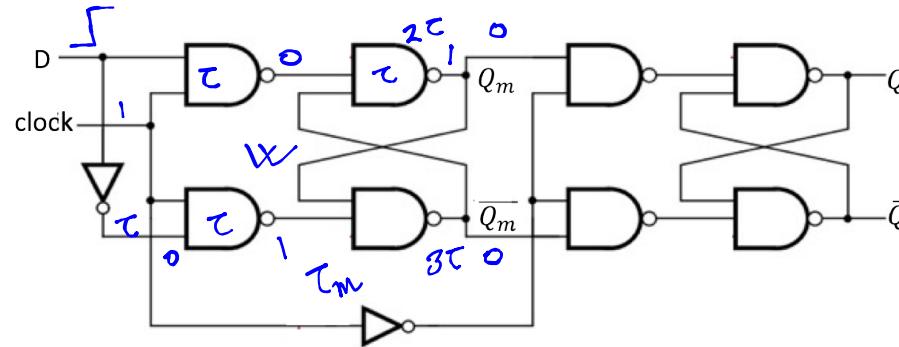


## Timing: Sequential Circuits: $t_{clk-out}$



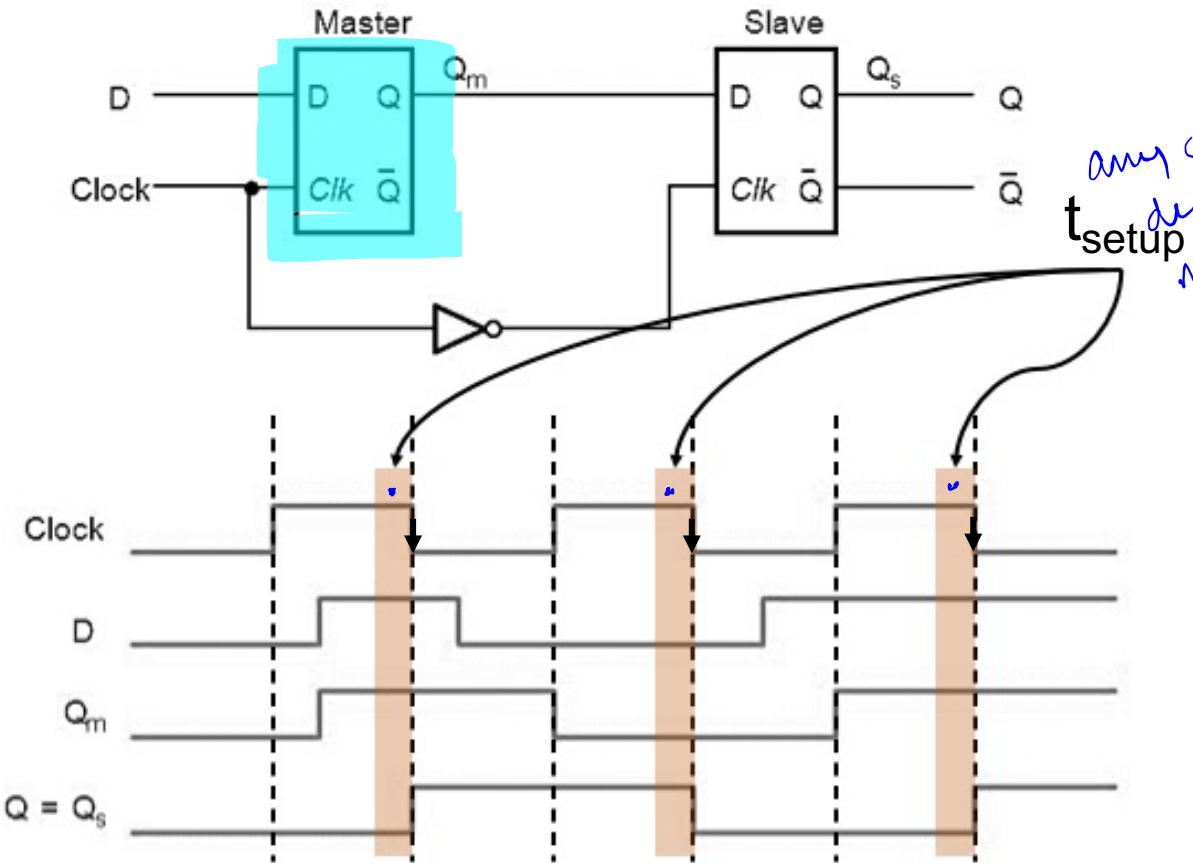
- The time it takes to see the change in the output of the flip-flop after the active clock edge is called the  $t_{clk-out} = t_{FF}$  FF delay
- It is approximately equal to the propagation delay,  $\tau_s$ , of the slave latch

## X Setup Time ( $t_{\text{setup}}$ ):



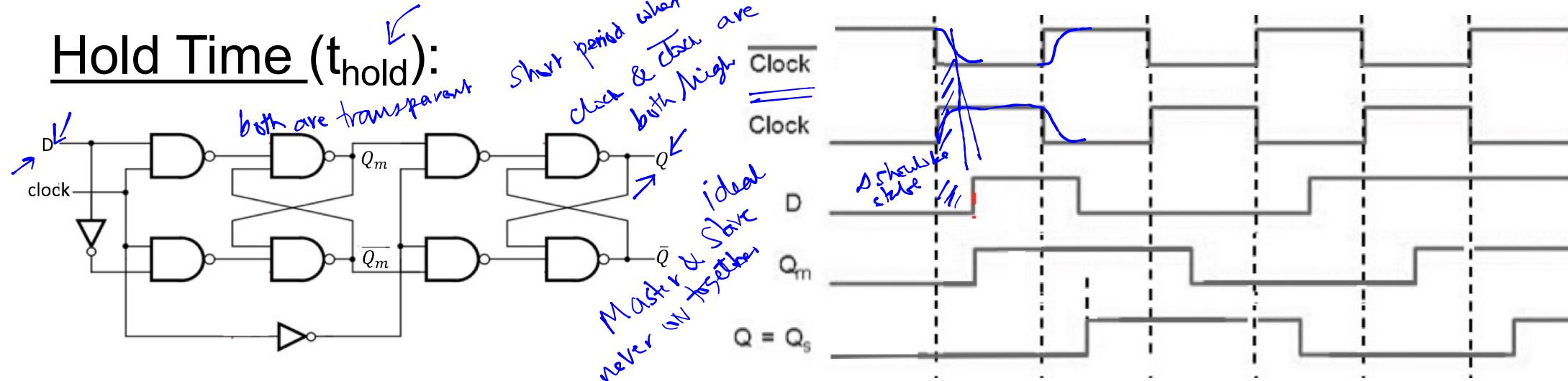
- It defines the time period before the active clock edge during which input must not change. ←
- Time taken by an input to propagate through master latch in order to be read correctly by slave latch
- It is approximately equal to the propagation delay,  $\tau_m$ , of the master latch
- If the input is changed during this time, the output of the slave latch becomes unpredictable.  
*Completed transition*  $t_{\text{setup}}$

## Setup Time ( $t_{\text{setup}}$ ):



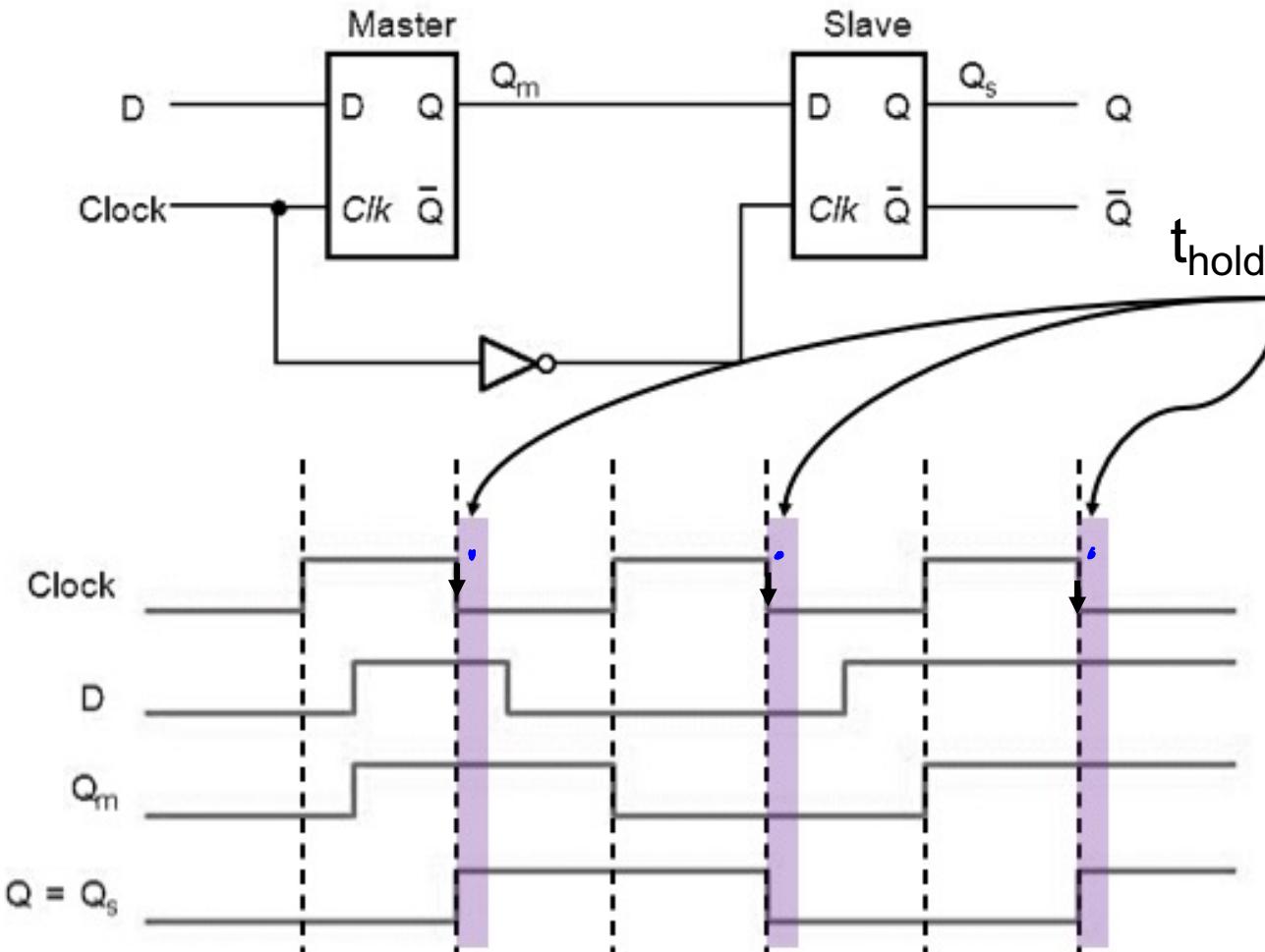
- Input should not change during this period.  
*If the input changes during the period, we are not sure whether output corresponds to current or previous value of the input (ambiguous output)*

## Hold Time ( $t_{hold}$ ):



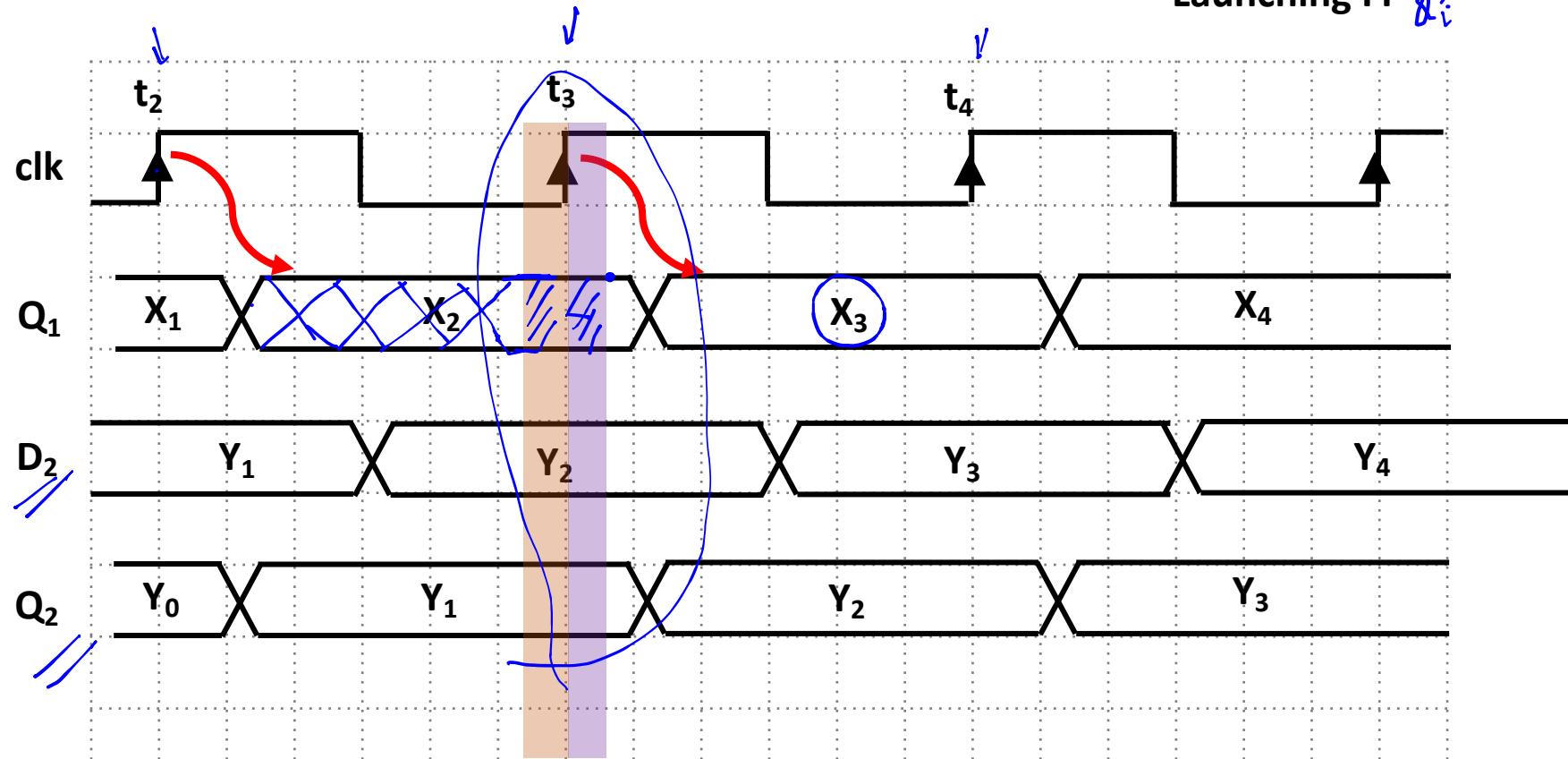
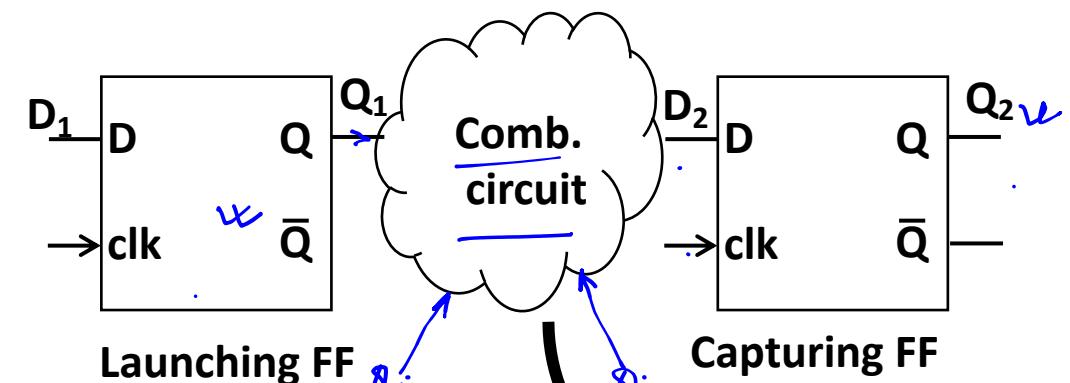
- When clock goes from high to low (for -ve edge triggered FF), master latch is in memory state and slave latch is enabled (in ideal world)
- BUT...due to rise time of the clock signal, both latches are ON at the same time for a short while.
- If the input changes during this time, we don't know whether output corresponds to previous input or present input (unpredictable).
- This is called **hold time**: Time after the active clock edge (-ve edge for -ve edge triggered FF) during which the input must be stable.

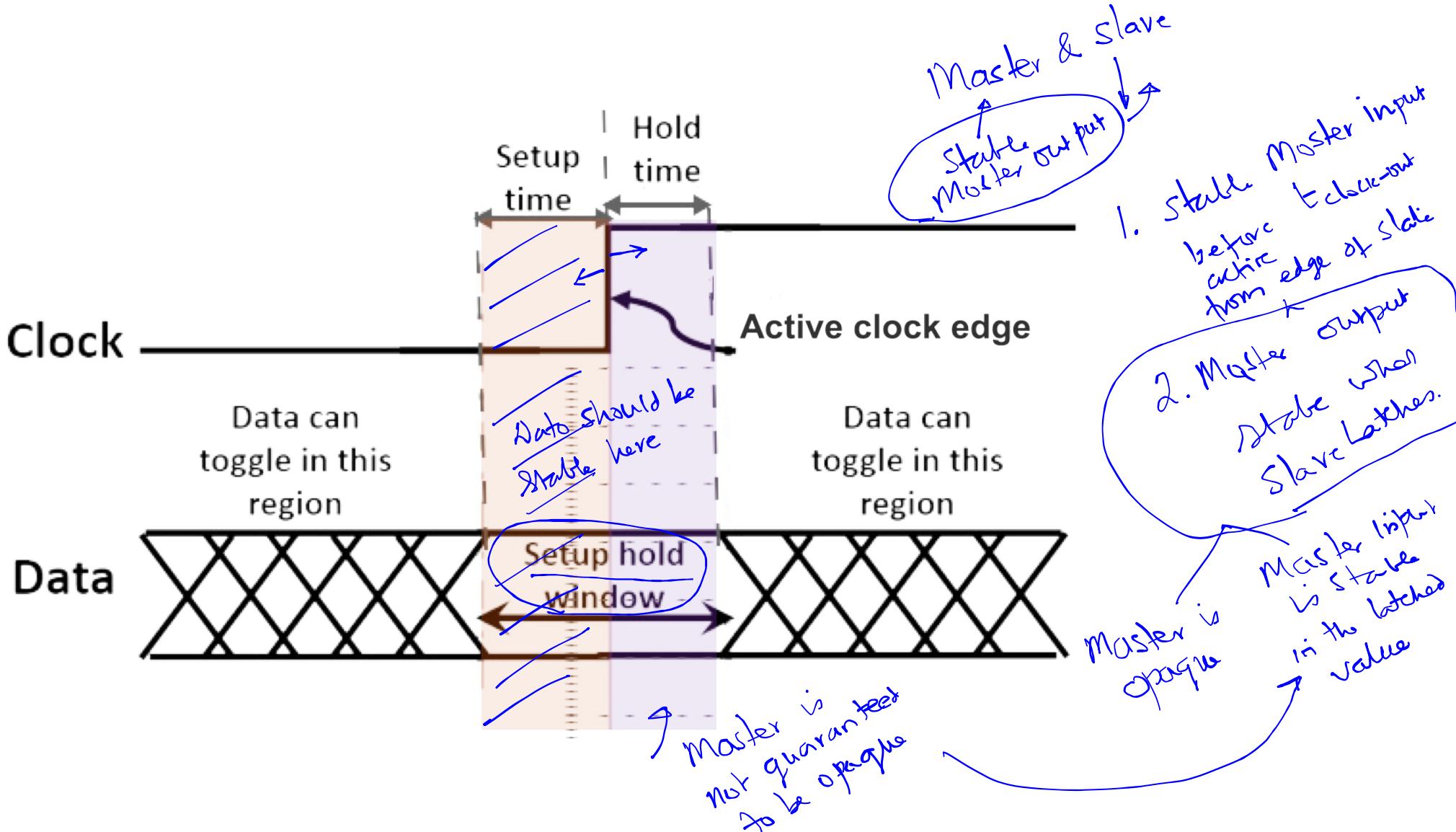
## Hold Time ( $t_{hold}$ ):



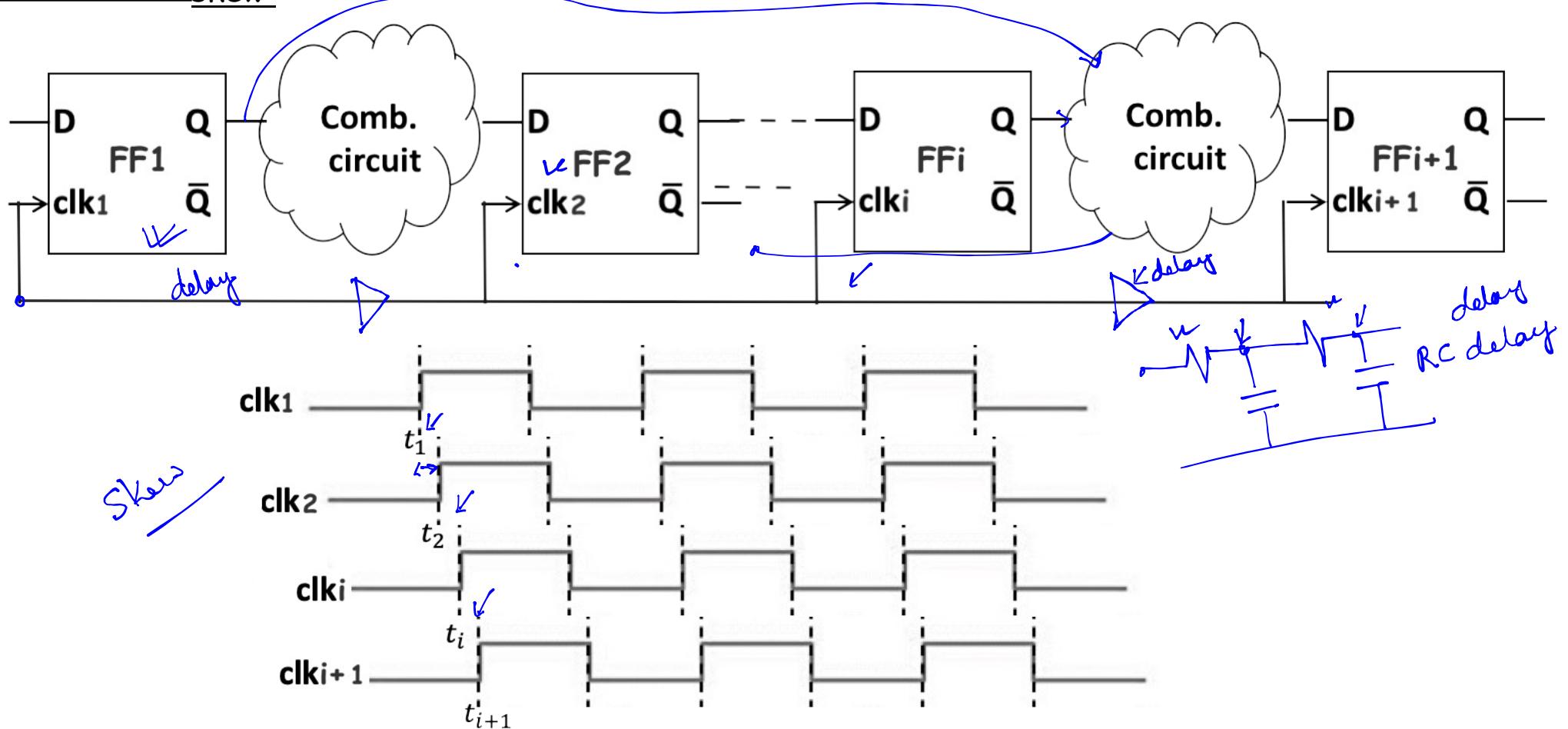
- Input should not change during this period.
- If the input changes during the period, we are not sure whether output corresponds to current or previous value of the input (ambiguous output)

## FF Timing Constraints:





## Clock Skew $t_{skew}$ :



The clock to FF1 goes high at time  $t_1$  whereas that for FF2 goes high at time  $t_2$ , we then say that there is a clock skew of  $t_{skew} = t_2 - t_1$  between FF1 and FF2.