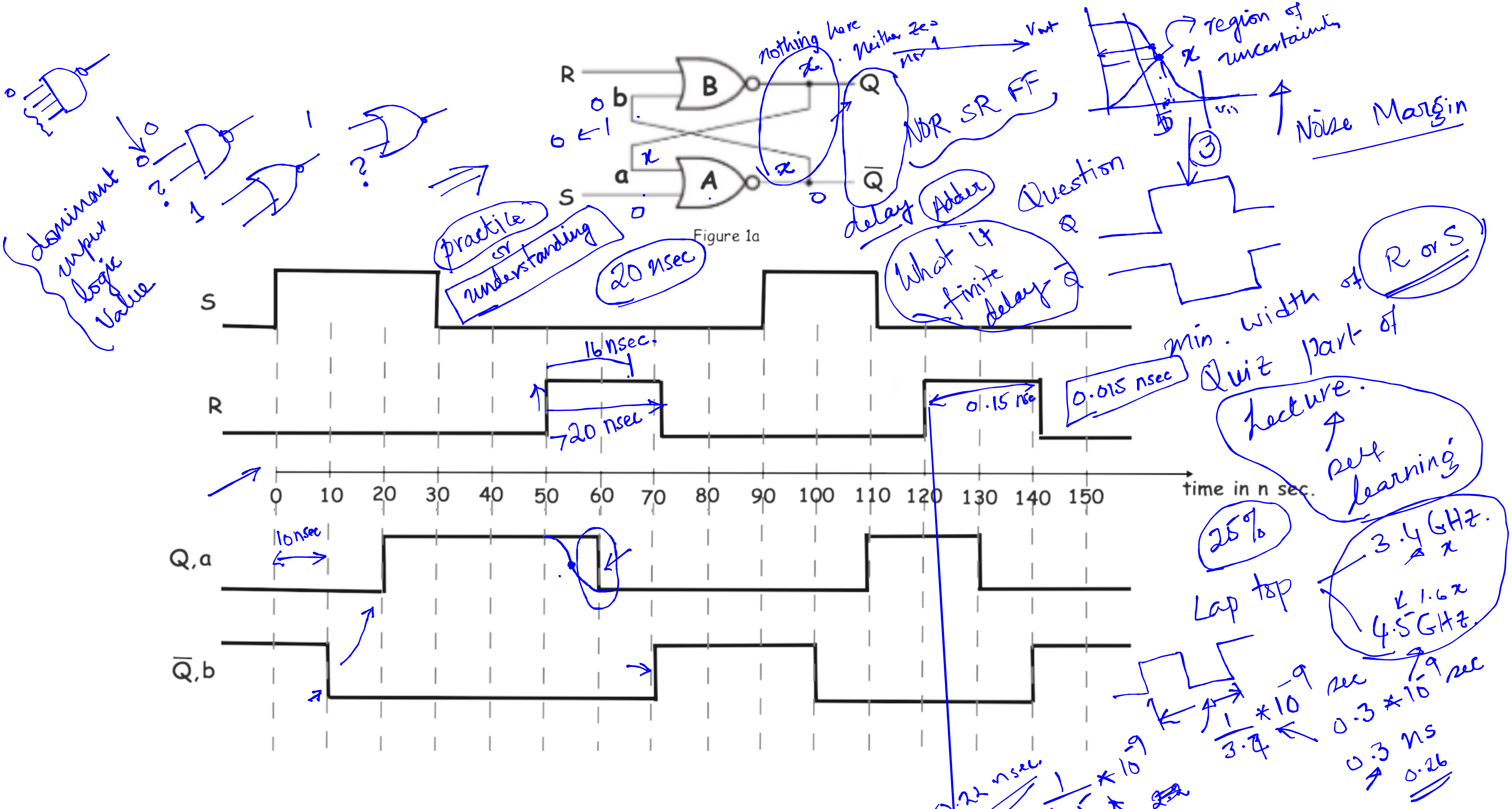
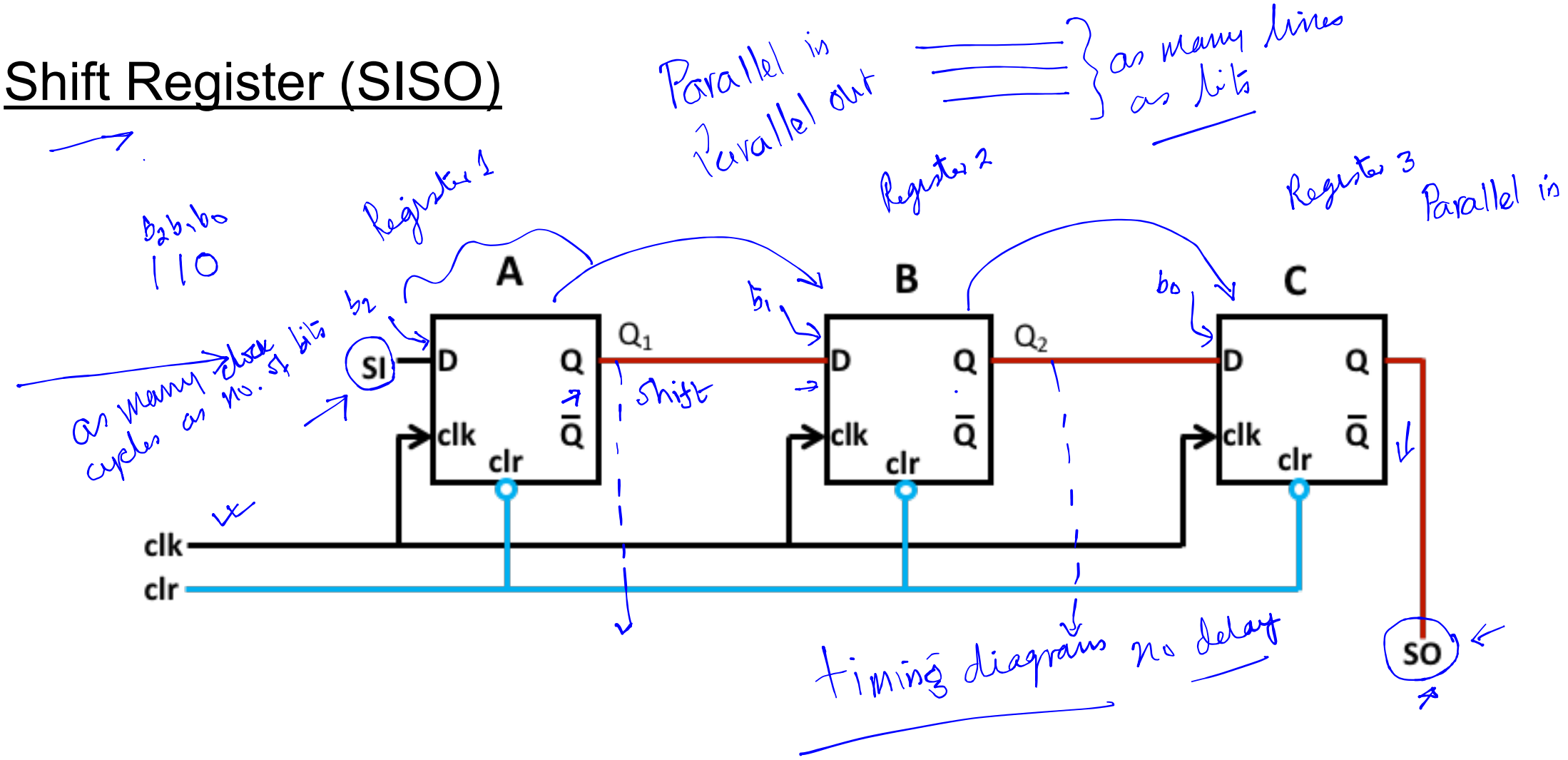
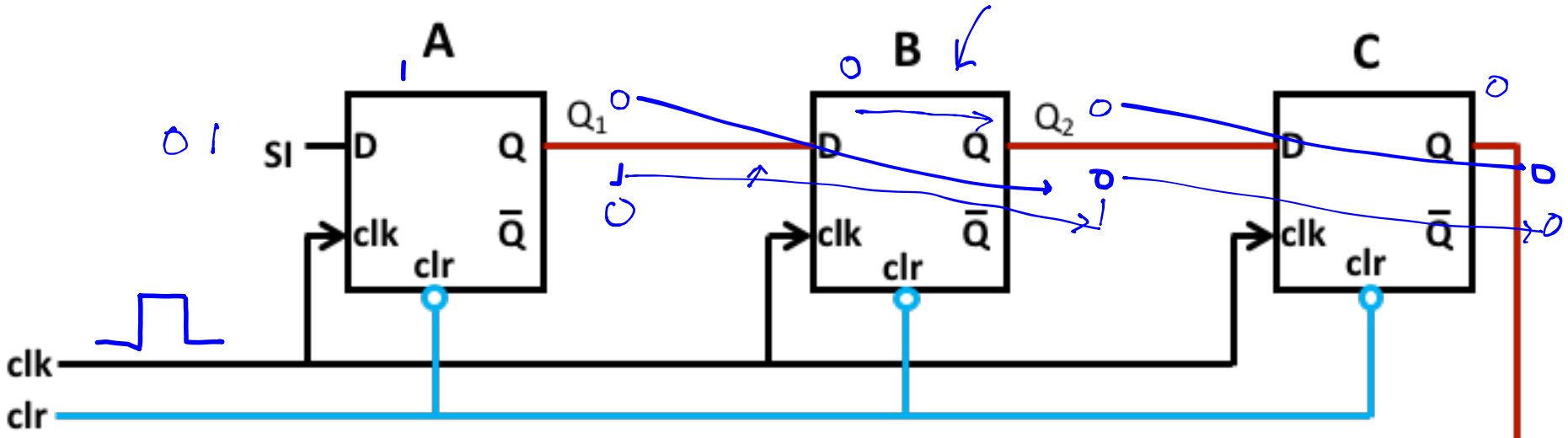
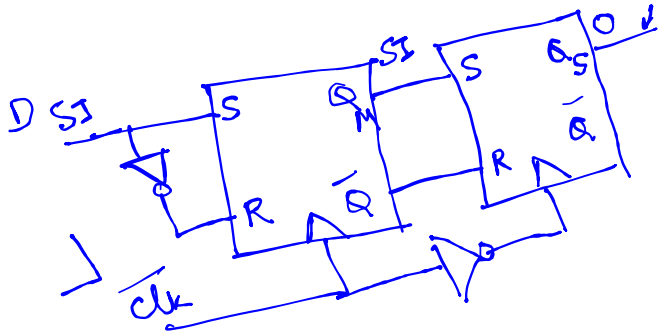

R
S
B
A
b
a
Q
Q̄
S
R
Q,a
Q̄,b
0 10 20 30 40 50 60 70 80 90 100 110 120 130 140 150
time in n sec.

Figure 1a

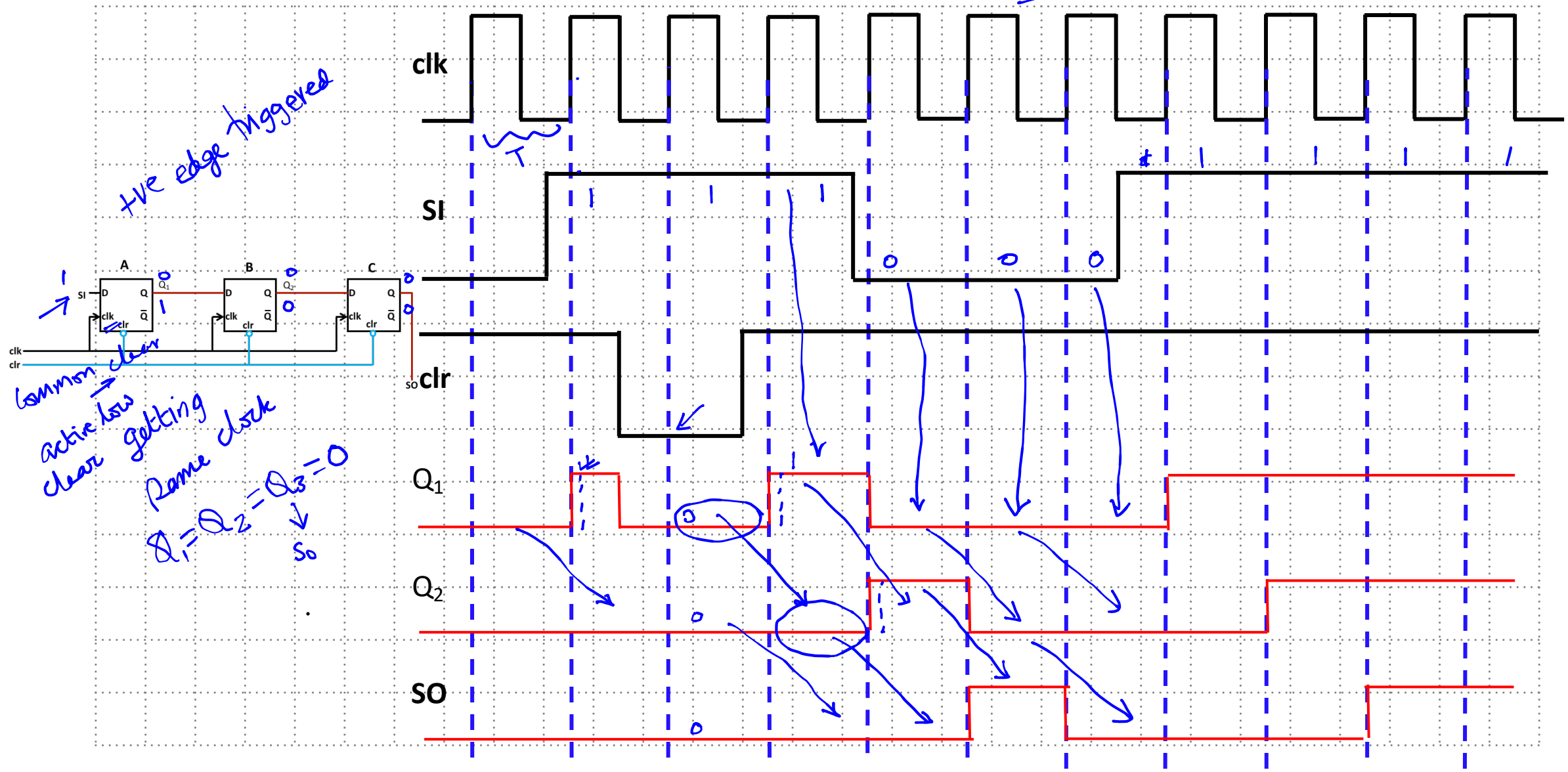
Shift Register (SISO)

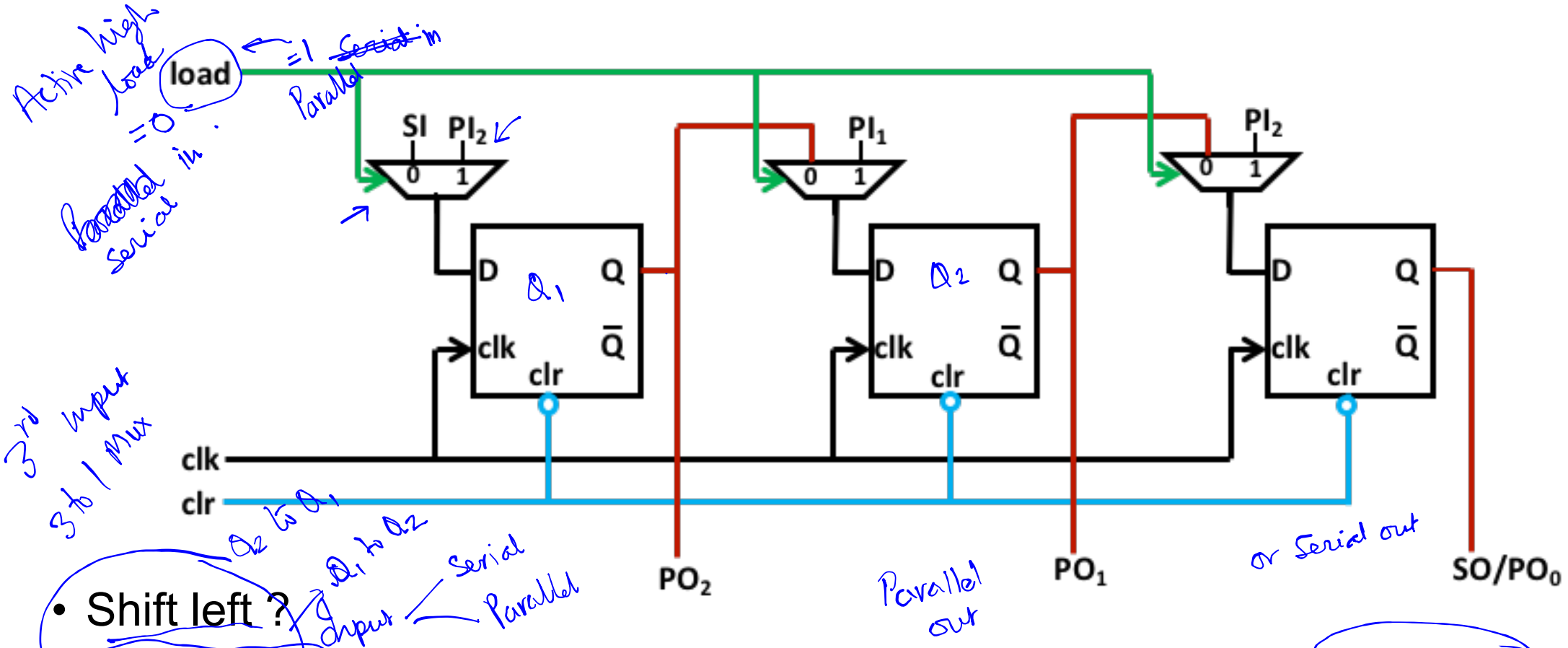



A
B
C
SI
D
Q
clk
clr
Q_1
Q_2
clk
clr
SO


S
R
clk

Shift Register (SISO):

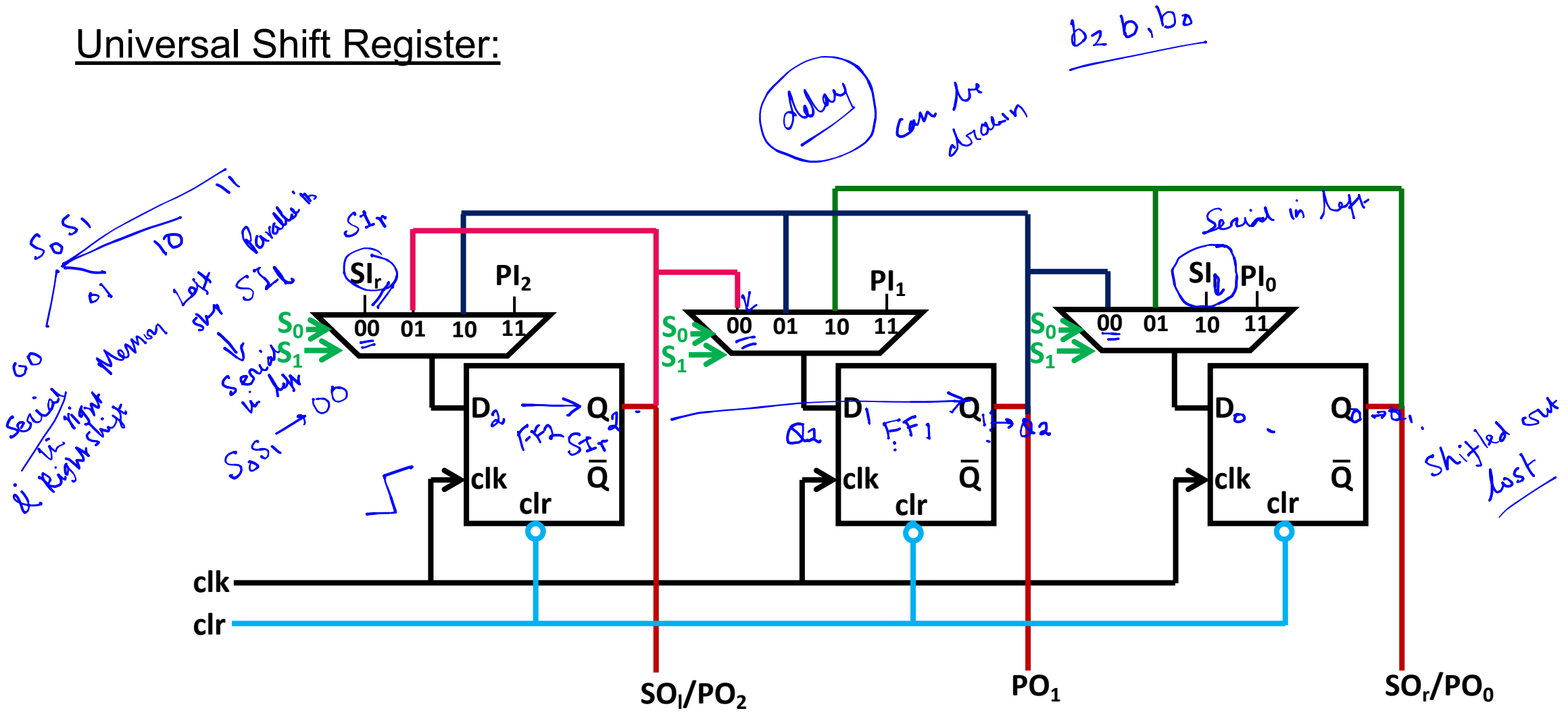




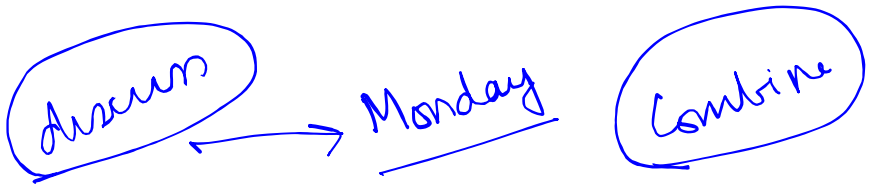
- Shift left ?
- Shift right ?
- Memory

Shift Register (SISO, PISO, PIPO, SIPO, Shift Right)

Universal Shift Register:

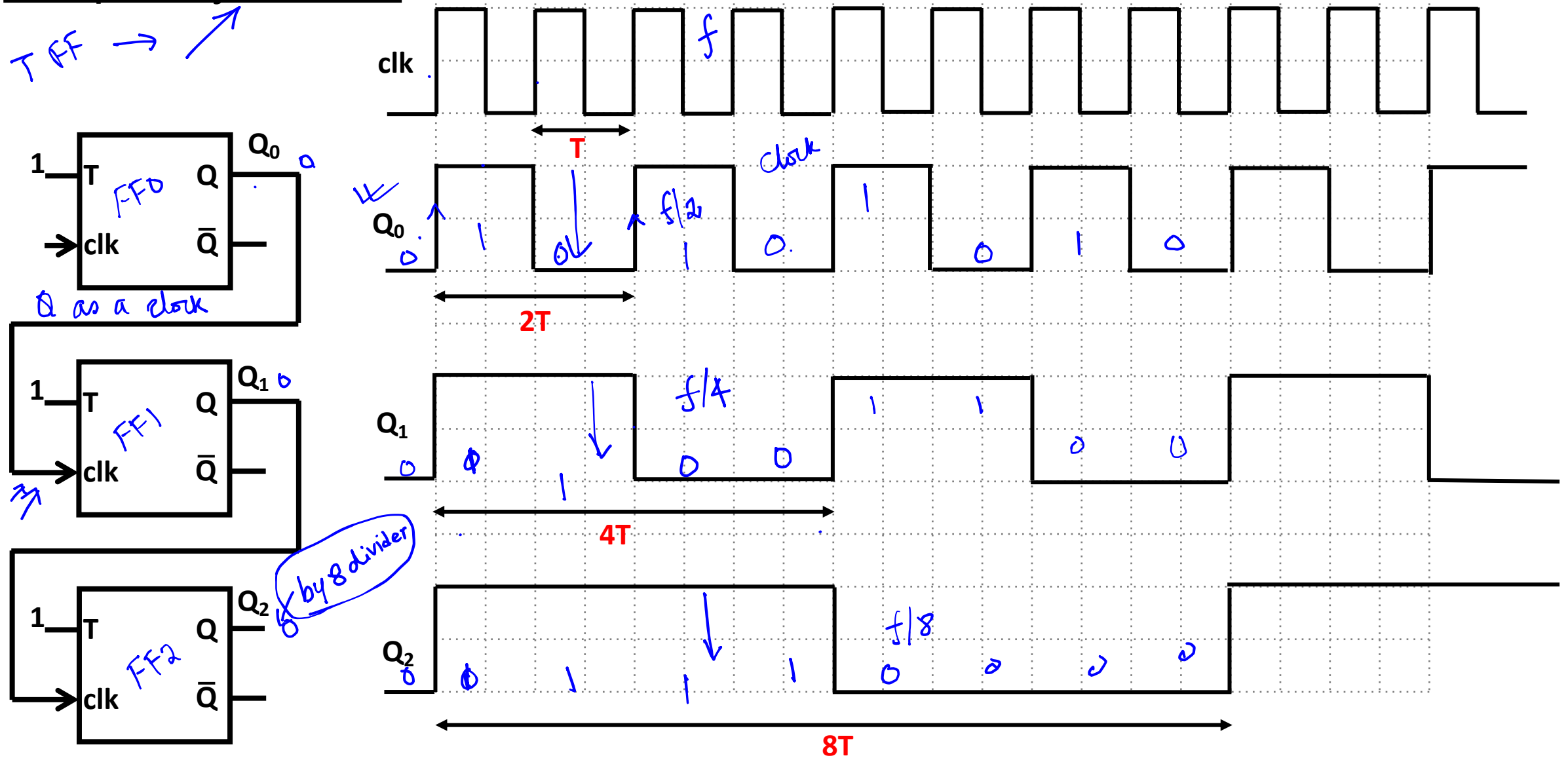


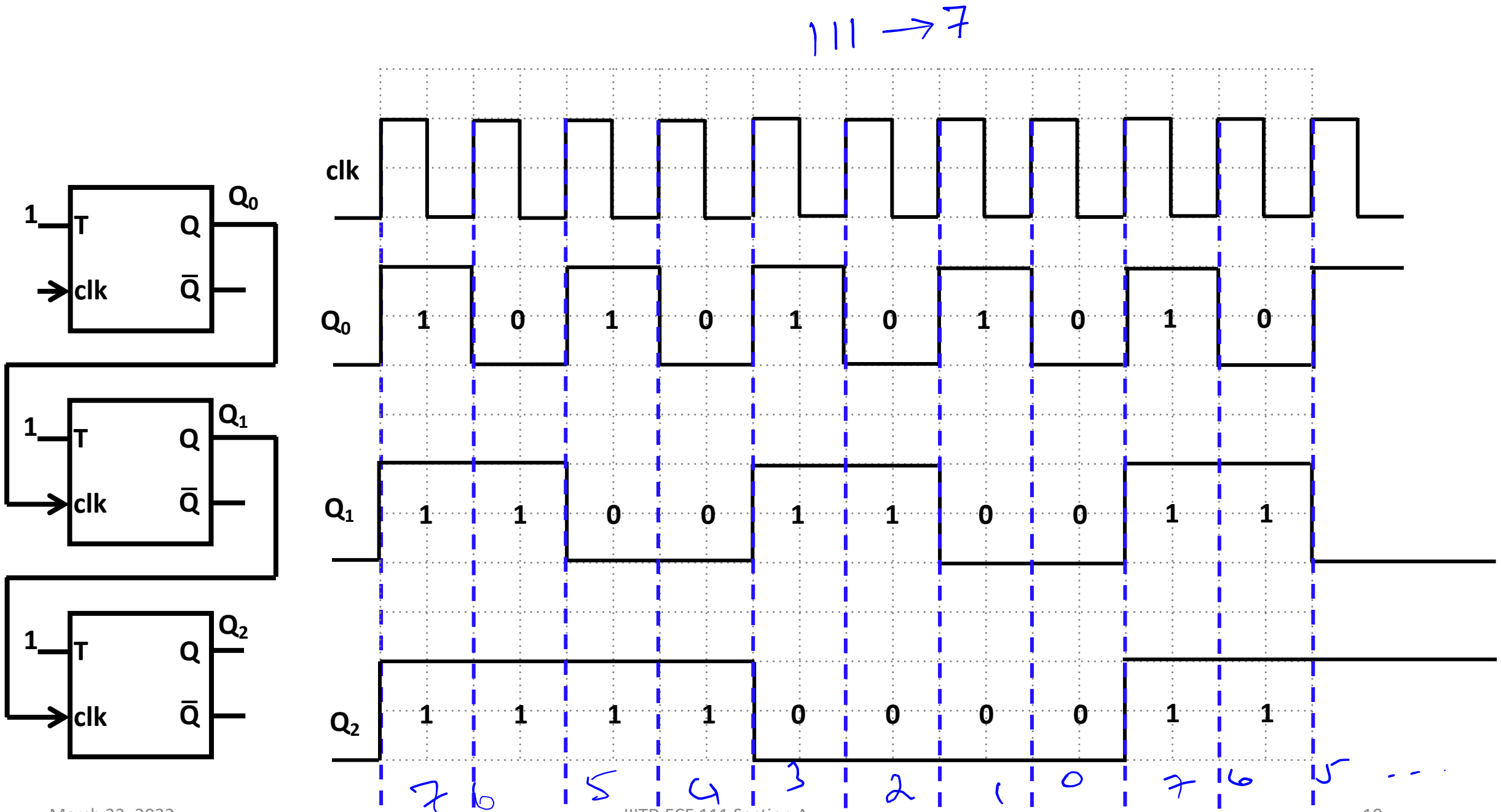
Universal Shift Register (HW):



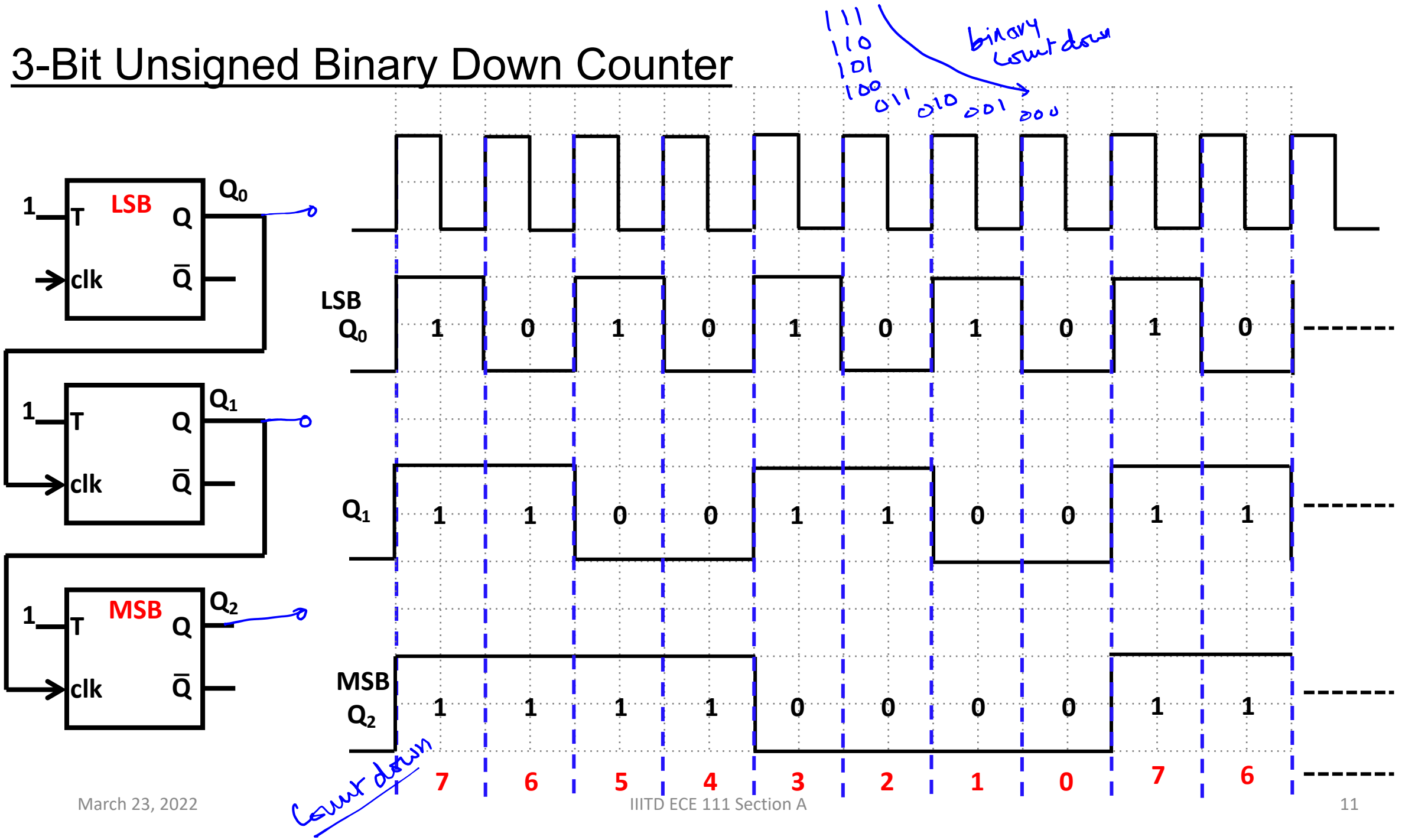
- Design serial n-bit adder using 1-bit adder and shift registers (Page no. 259-263 - Morris Mano)

Frequency Divider

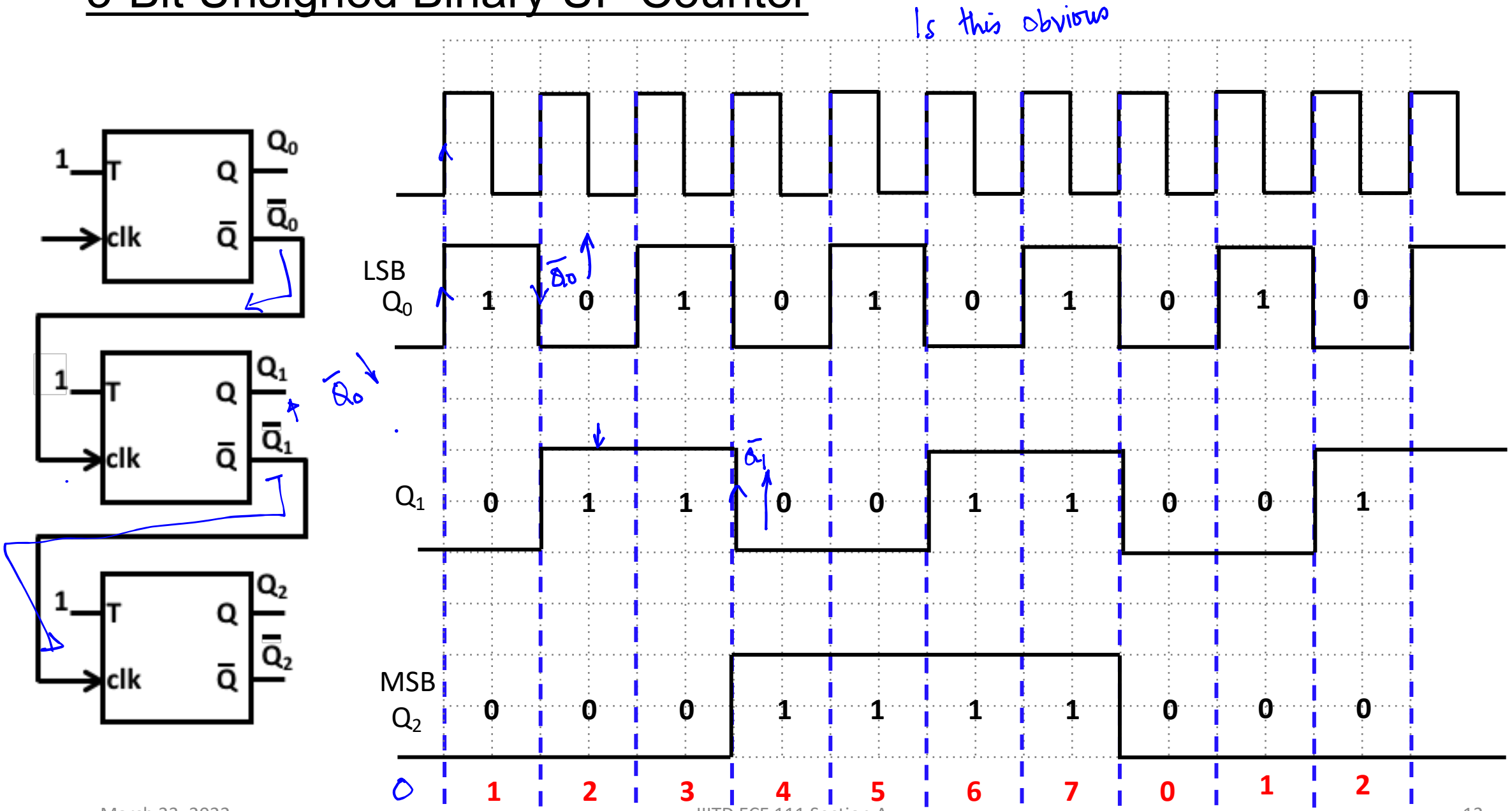



111 → 7
1
T
Q
clk
$\bar{Q}$
Q_0
Q_1
Q_2
clk
Q_0
Q_1
Q_2
1 0 1 0 1 0 1 0 1 0
1 1 0 0 1 1 0 0 1 1
1 1 1 1 0 0 0 0 1 1
7 6 5 4 3 2 1 0 7 6 5 ...

3-Bit Unsigned Binary Down Counter



3-Bit Unsigned Binary UP Counter



3-Bit Unsigned Binary UP Counter with Clear: