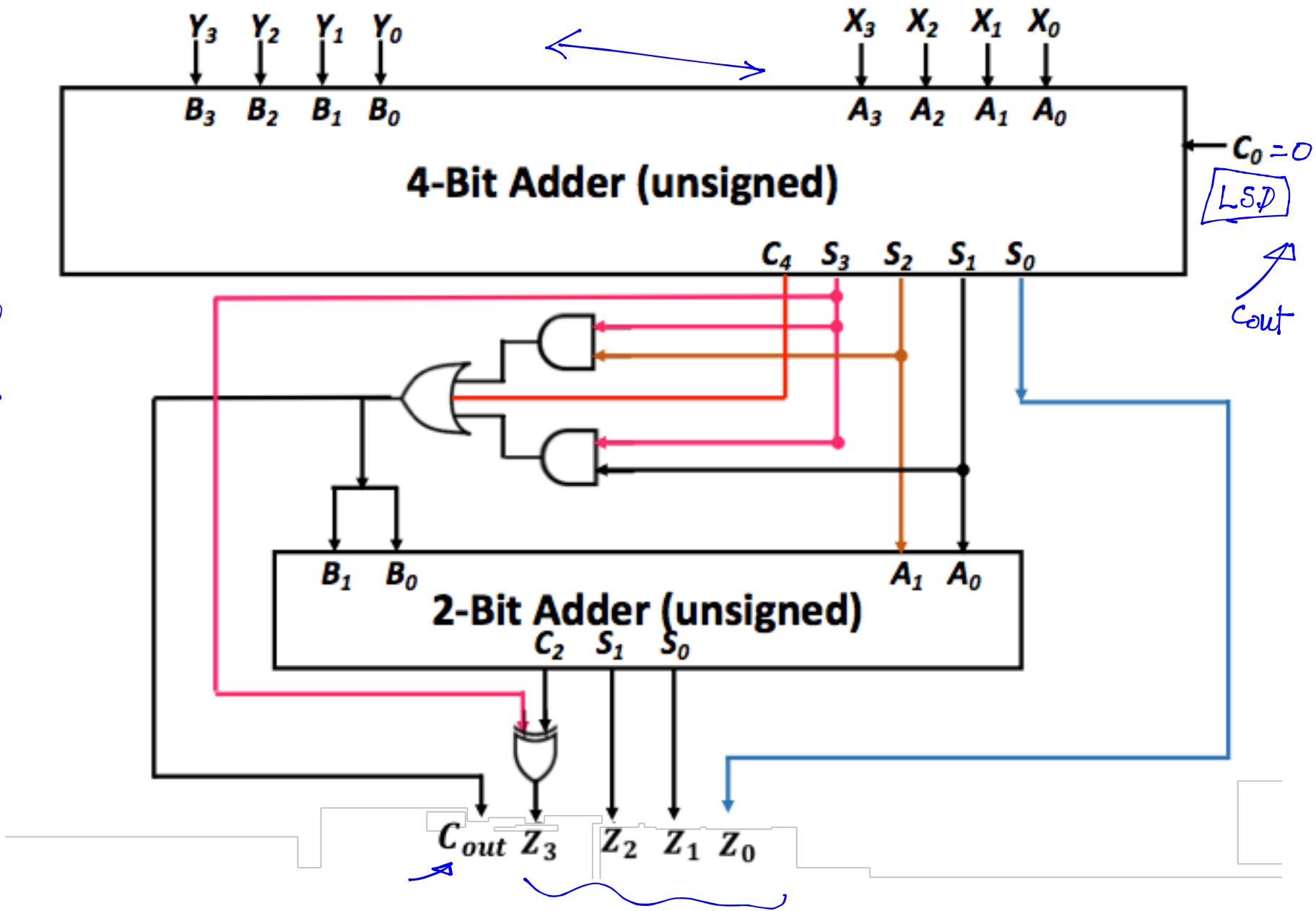
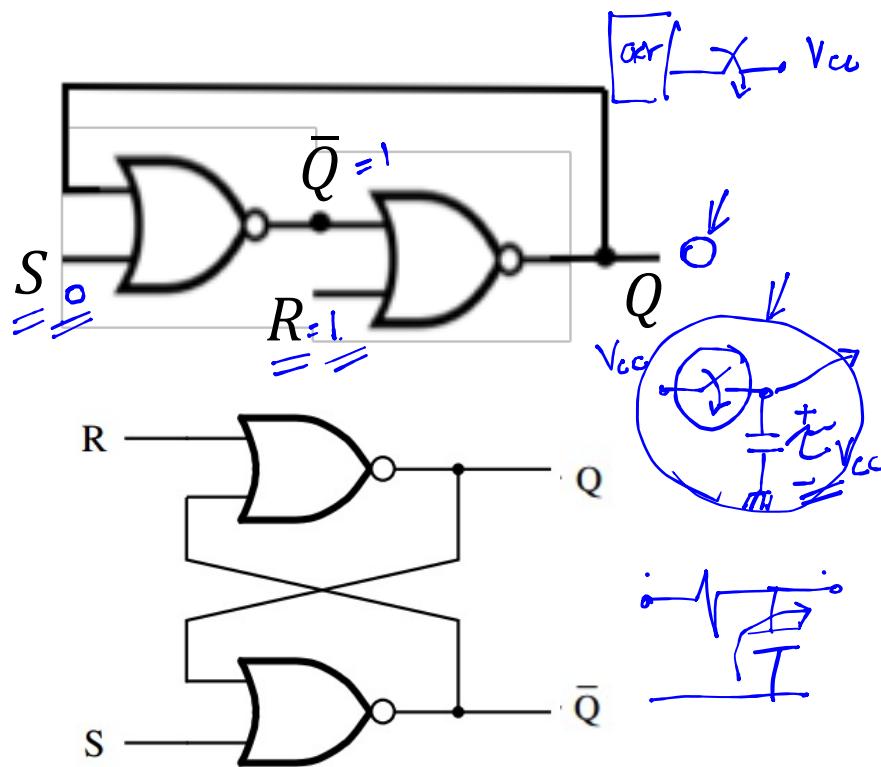


1 Digit BCD Adder:

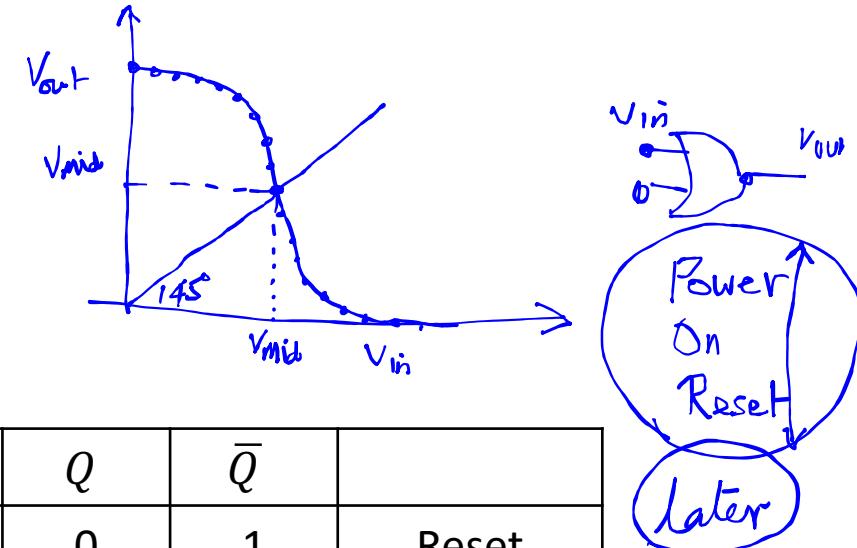
3 digit
 digit 3
 digit 2
 digit 1
 $d_1 d_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0$
 $d_2 e_2 e_1 e_0$
 Comt
 $s_1 s_2 s_1 s_0$



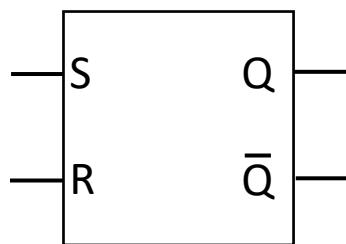
Latch: S-R Latch Using NOR Gate



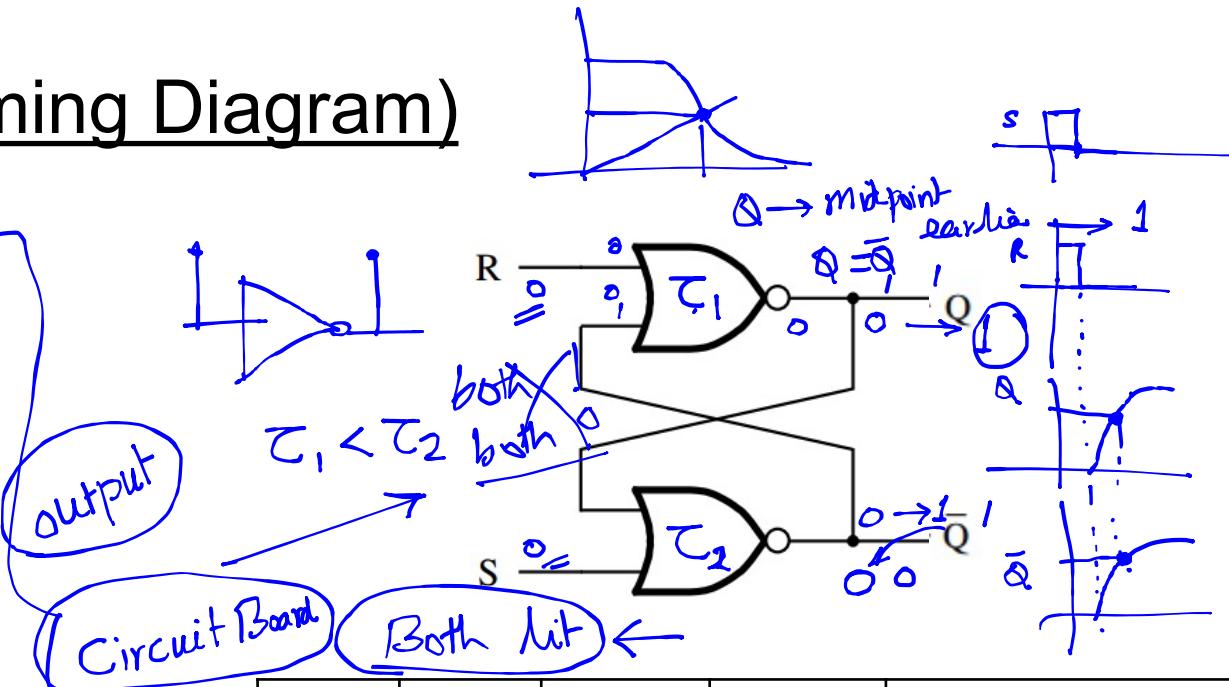
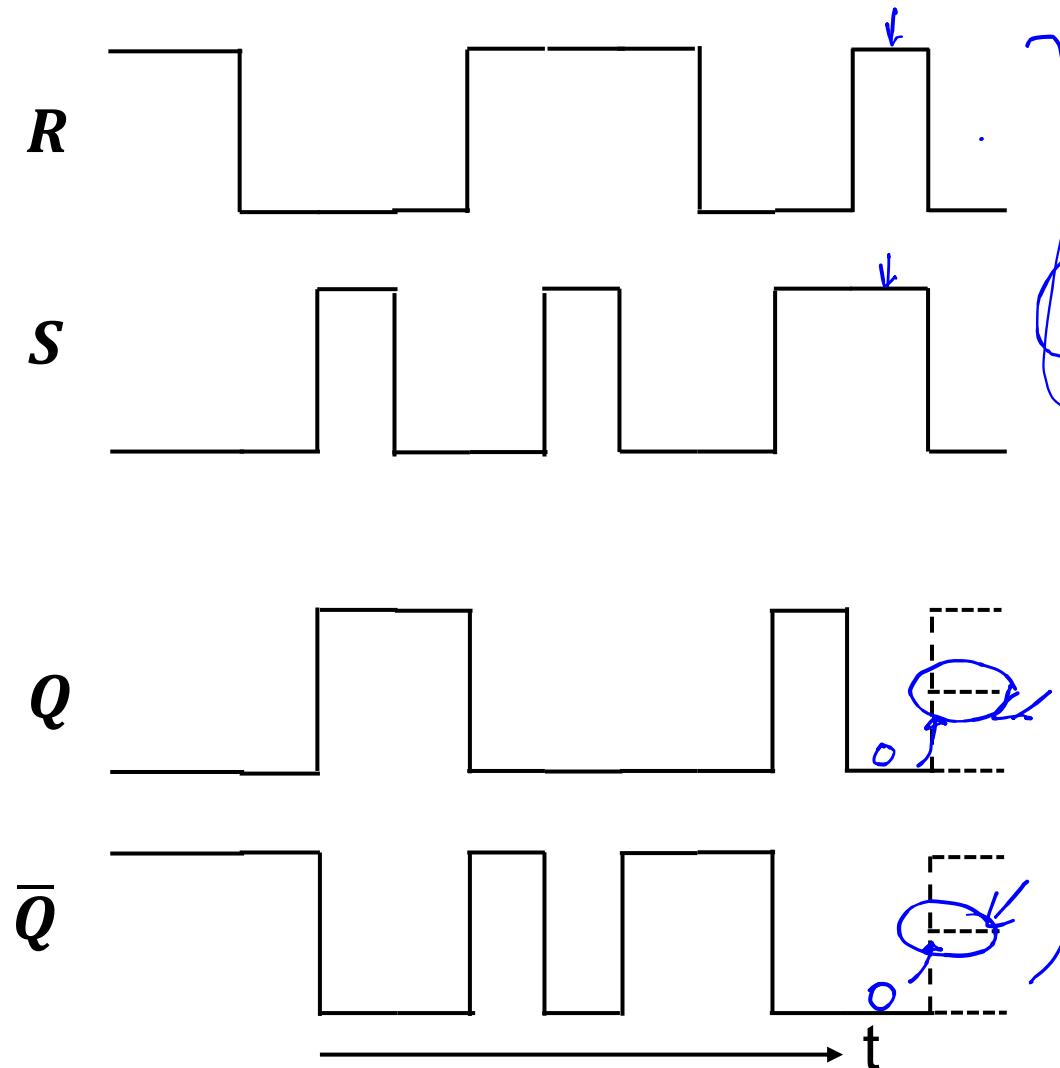
Q can take any value
Initially Reset



T	S	R	Q	\bar{Q}	
1	0	1	0	1	Reset
2	0	0	0	1	Memory
3	1	0	1	0	Set
4	0	0	1	0	Memory
5	1	1	0	0	forbidden

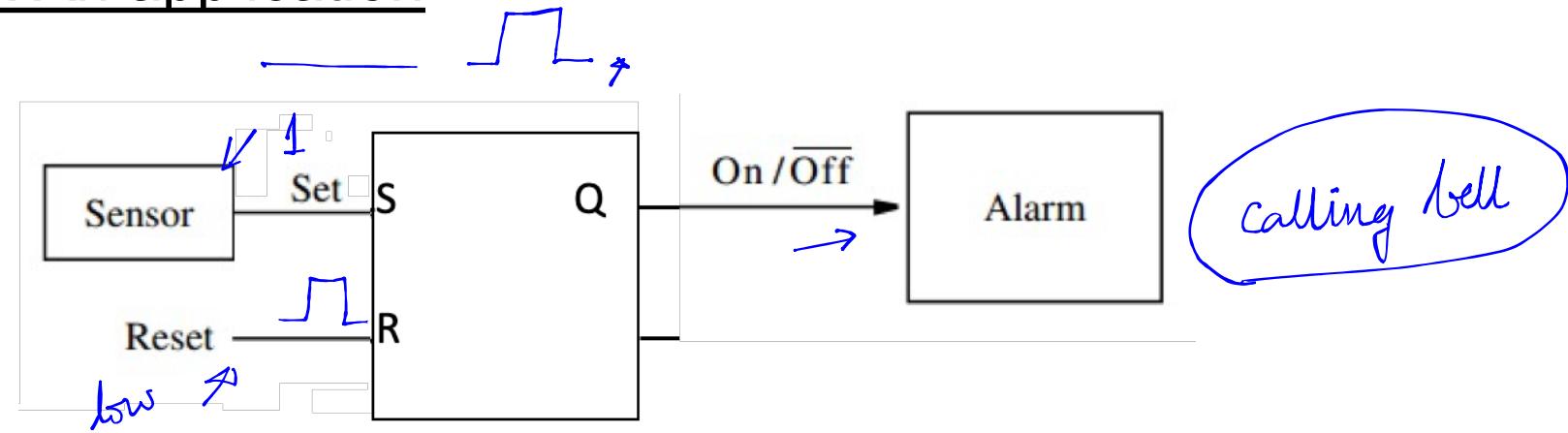


S-R Latch Using NOR Gate (Timing Diagram)



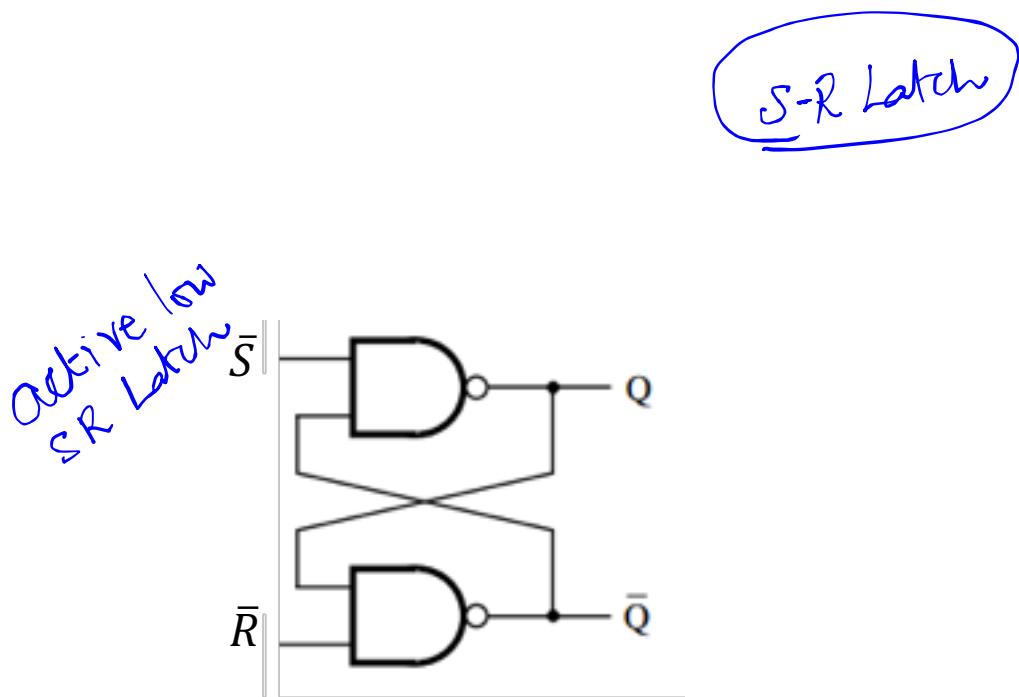
S	R	Q_n	\bar{Q}_n	State
0	0	Q_{n-1}	\bar{Q}_{n-1}	Memory
1	0	1	0	Set
0	1	0	1	Reset
1	1	?	?	Forbidden

Latch: S-R Latch: An application



- When sensor output goes high, $S=1$. Then, $Q=1$ assuming $R=0$.
- Therefore, ALARM goes ON. Even if S becomes LOW, Q remains high due to memory state.
- When Reset goes high, Q goes LOW and the alarm turns OFF

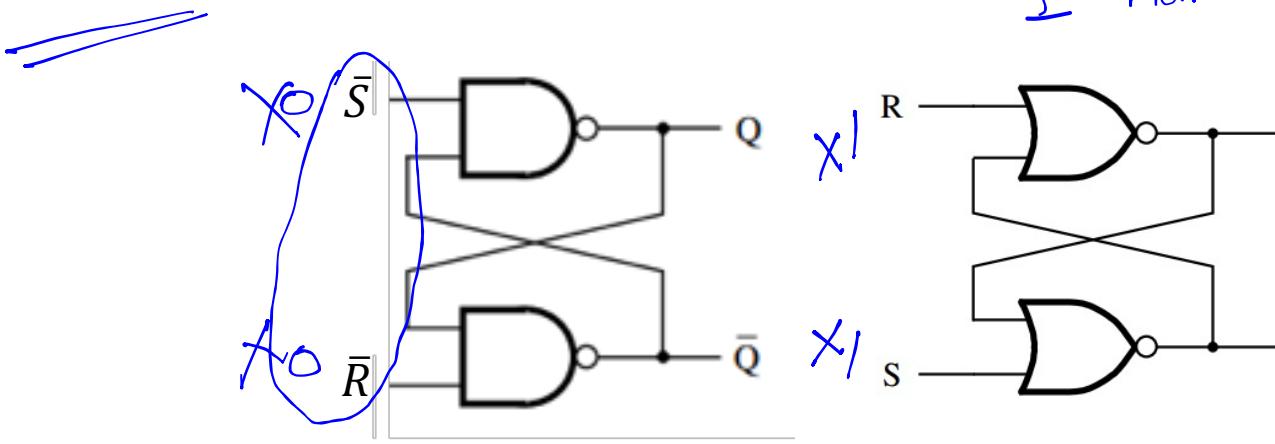
Latch: S-R Latch with NAND Gates:



This is called an $\bar{S}\bar{R}$ Latch

\bar{S}	\bar{R}	Q_n	\bar{Q}_n
1	1	Q_{n-1}	\bar{Q}_{n-1}
0	1	1	0
1	0	0	1
0	0	Forbidden	

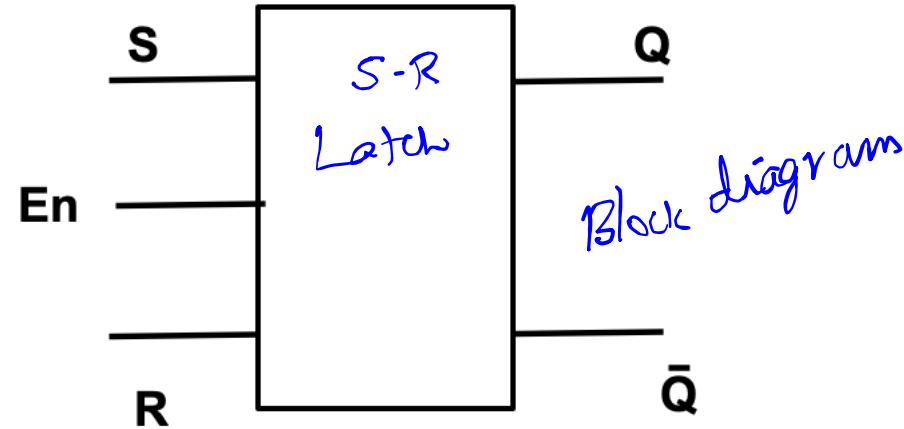
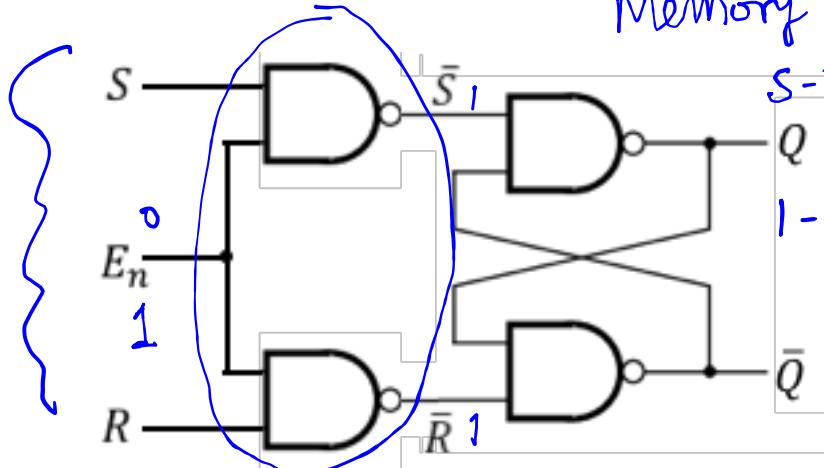
Latch: S-R Latch -> Issues



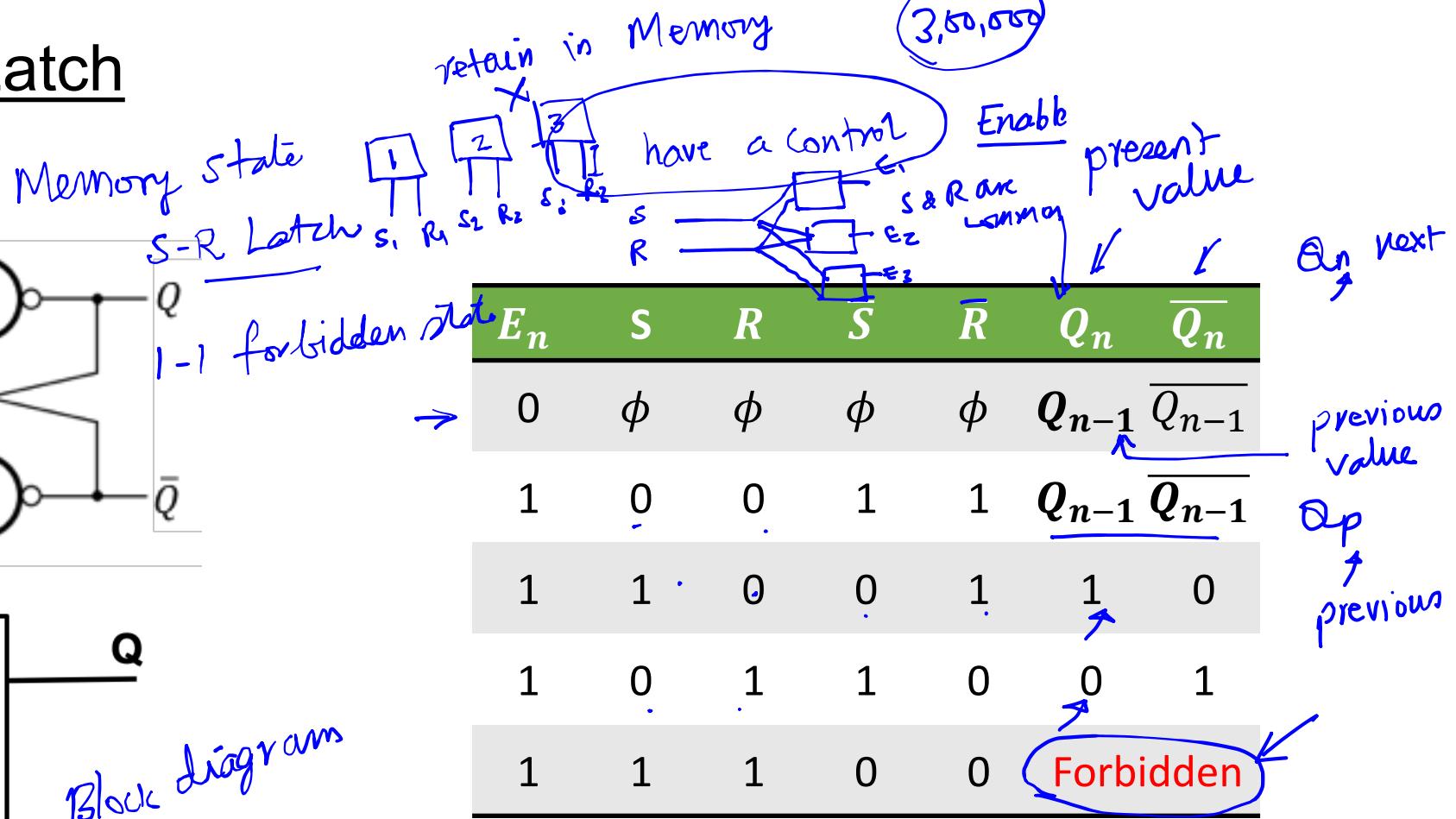
I have no control
Either both exclusive
or inclusive
Zero if inclusive
Decoder, Encoder
↓ Enable controlled the o/p

- We must avoid forbidden state. Some glitches may lead to input going to 11/00 at the same time. *avoid $S=R=1$*
- We don't have any control (remember enable signal) over latch.
- We need two inputs to store 1-bit of data $\boxed{R \& S} \rightarrow Q$ *introduce an enable provision*
- For $\bar{S}\bar{R}$ NAND latch, modify it to SR latch (not a major issue)

Latch: Gated S-R Latch



Symbol

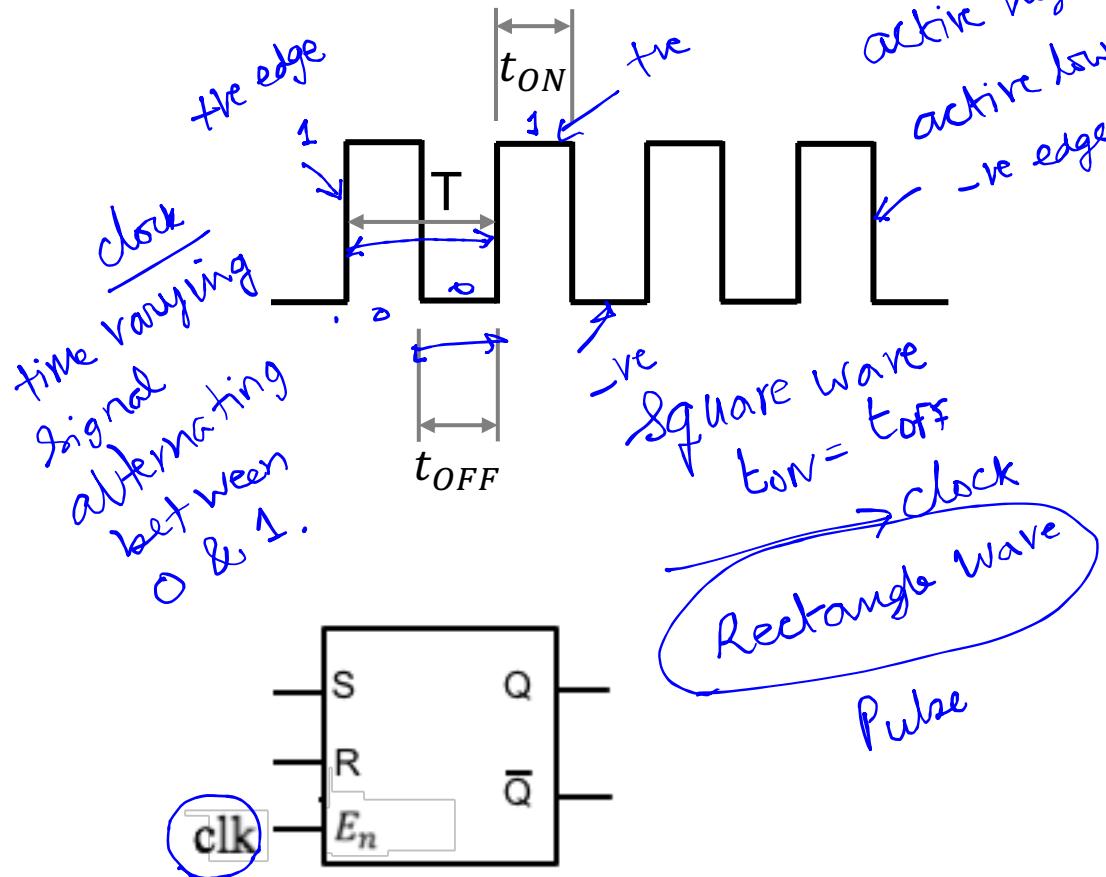


Latch: Gated S-R Latch (HW)

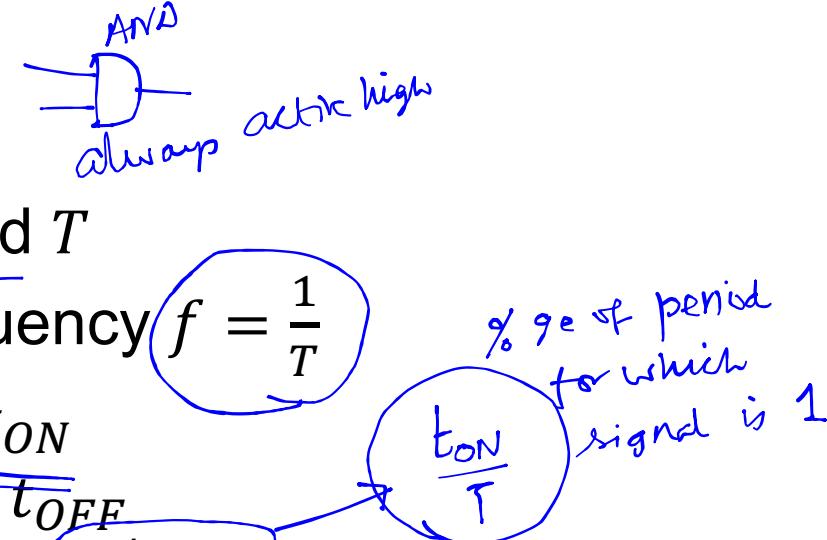
- Design gated SR latch with enabled signal using NOR gate
- Consider active high as well as active low enable signal



Clock Instead of Enable Signal:

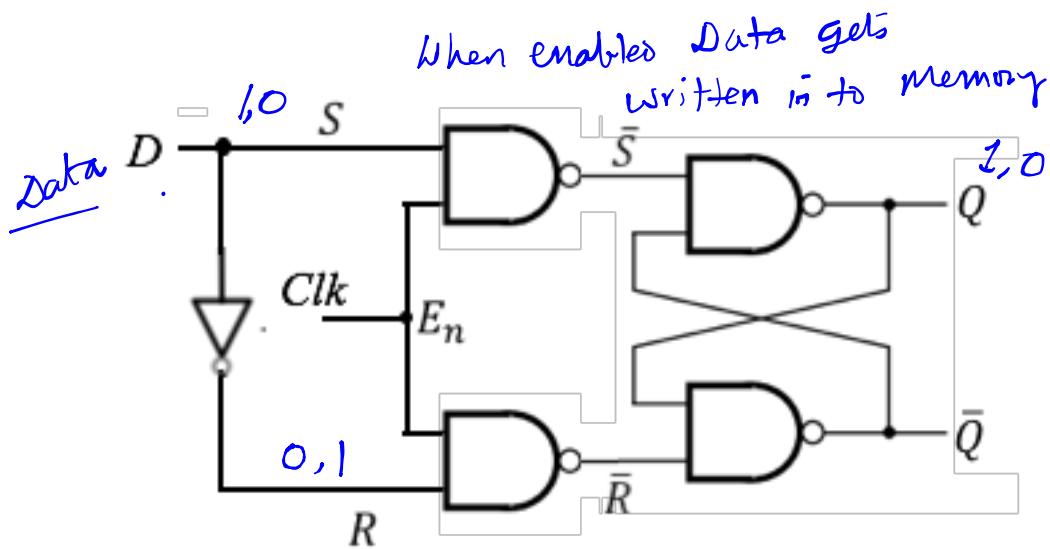
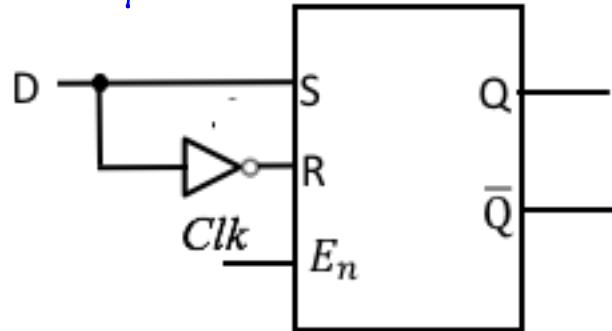


- Clock Period T
- Clock Frequency $f = \frac{1}{T}$
- ON time = t_{ON}
- OFF time = t_{OFF}
- Duty Cycle = $\frac{t_{ON}}{t_{OFF} + t_{ON}} = \frac{1}{2}$ for clocks
<1/2 for pulses.

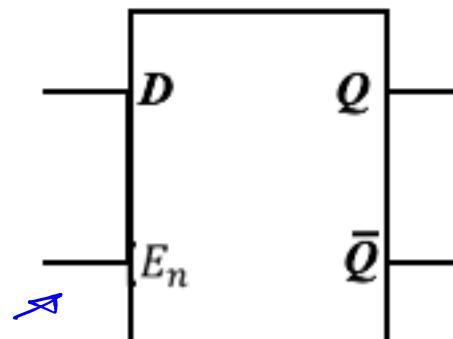


Gated/Clocked D Latch: Positive Level or Active High

Data latch *forbidden state is avoided* $S = \bar{R}$ or $R = \bar{S}$ ensures $S \neq R \neq 1, 0$

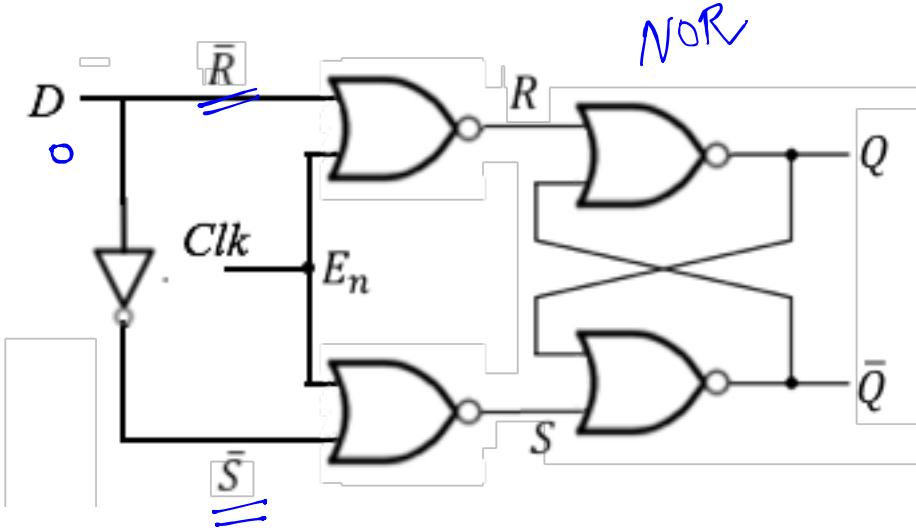


D	Clk	Q_n	\bar{Q}_n	Function
ϕ	0	Q_{n-1}	\bar{Q}_{n-1}	Memory
0	1	0 <small>Set or Clear</small>	1	Set/Preset
1	1	1 <small>Preset</small>	0	Reset/Clear

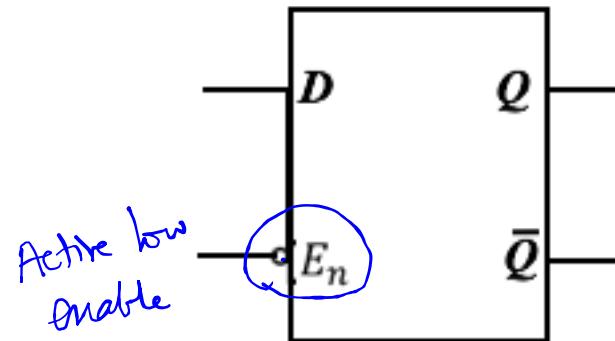
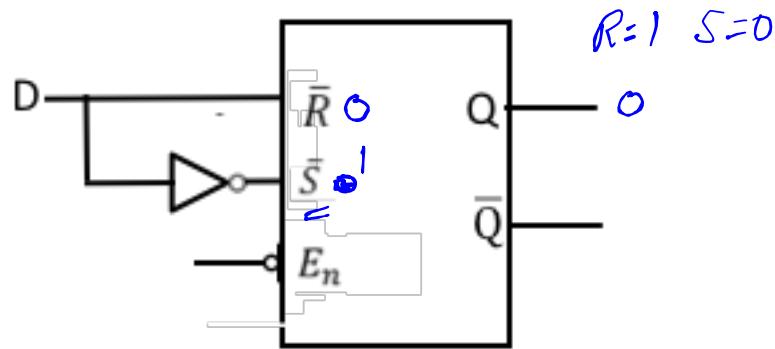


clocked D - Latch
Symbol of a D - Latch

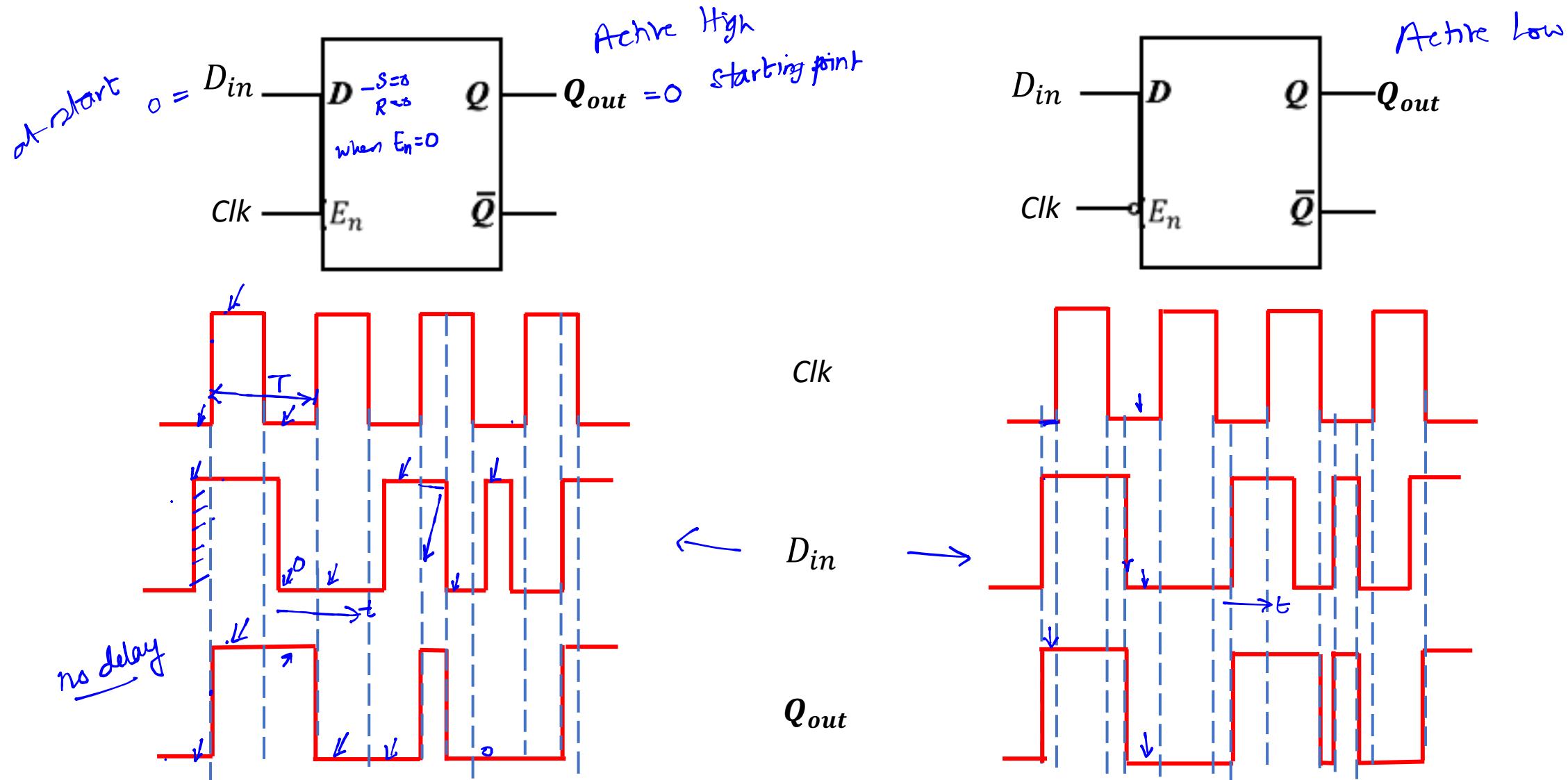
Gated/Clocked D Latch: Negative Level or Active Low



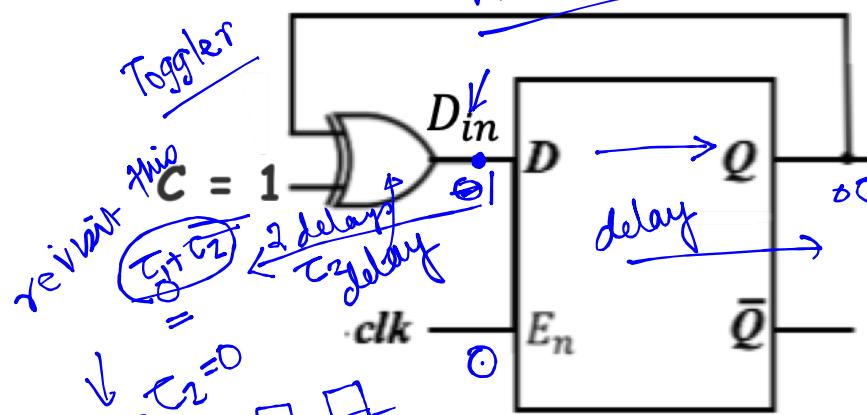
D	Clk	Q_n	\bar{Q}_n	Function
ϕ	1	Q_{n-1}	\bar{Q}_{n-1}	Memory
0	0	0	1	Set/Preset
1	0	1	0	Reset/Clear



Gated D-Latch (Timing Diagram)

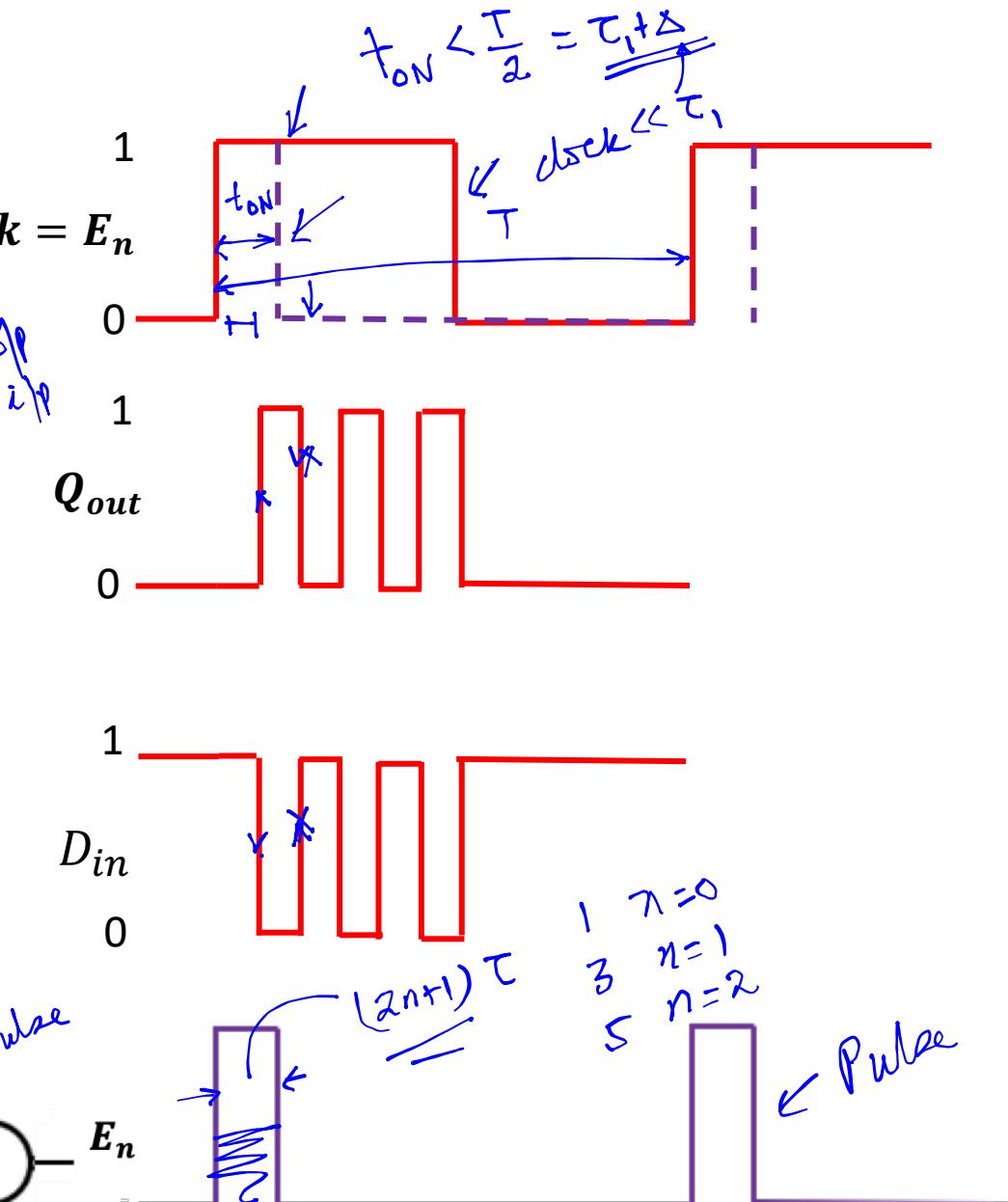
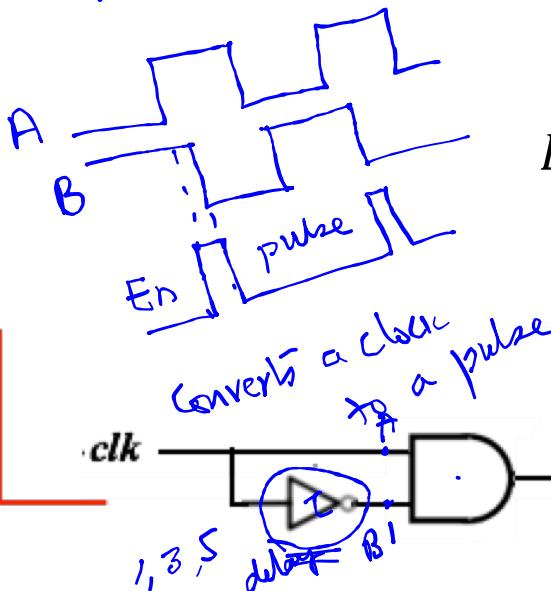


Racing in D-Latch:

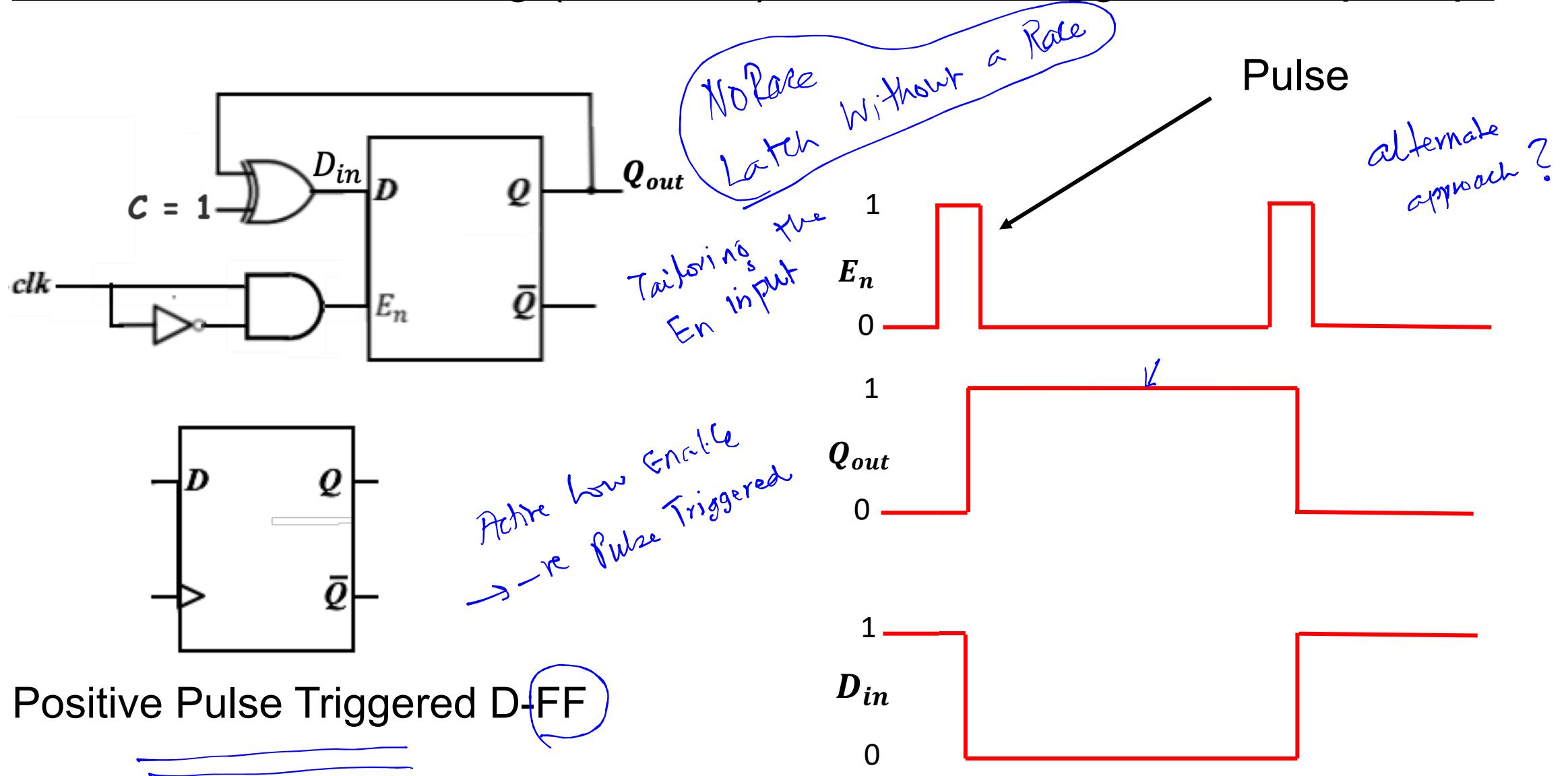


if there is a delay
2 intelligent
 $D_{in} = \bar{Q}_{out}$

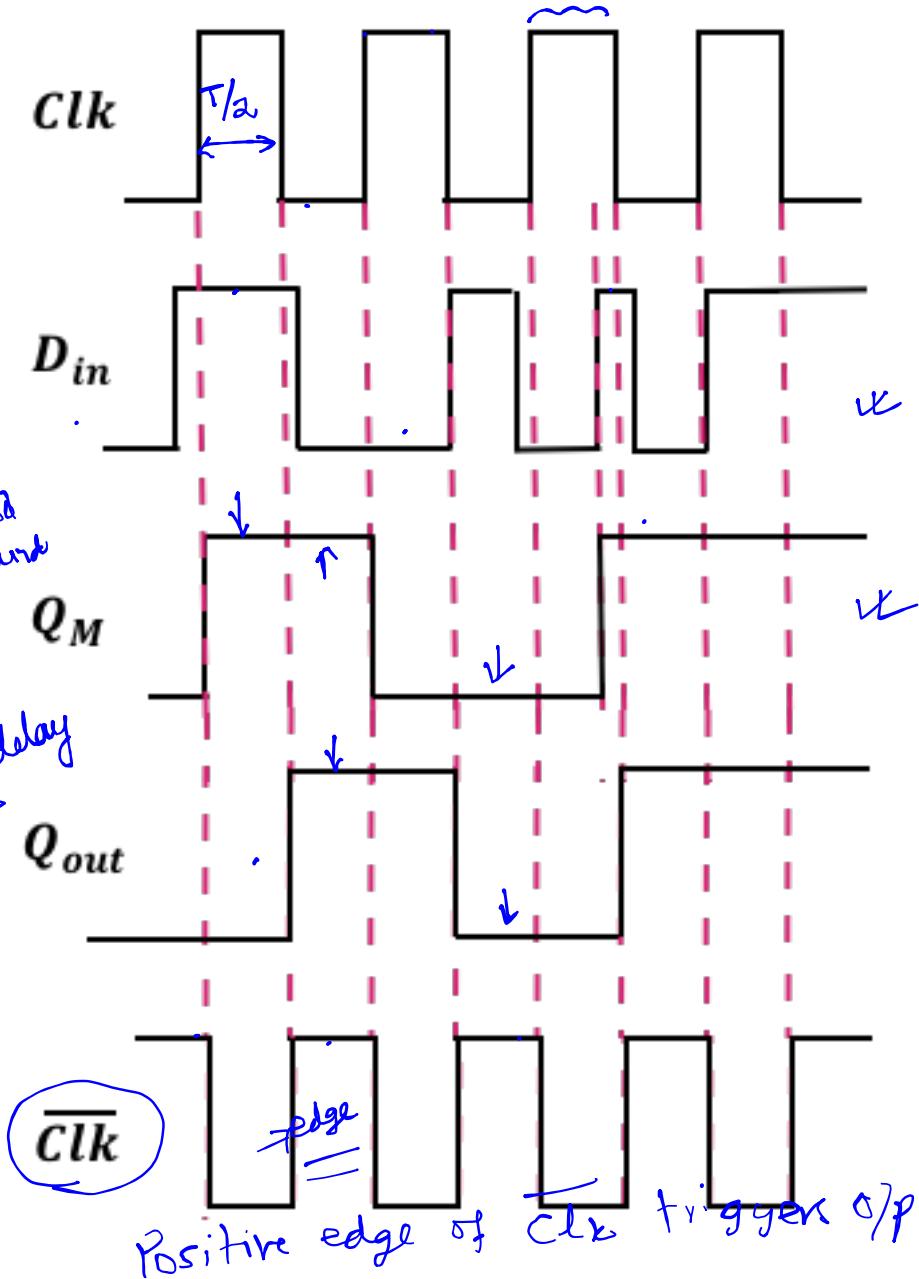
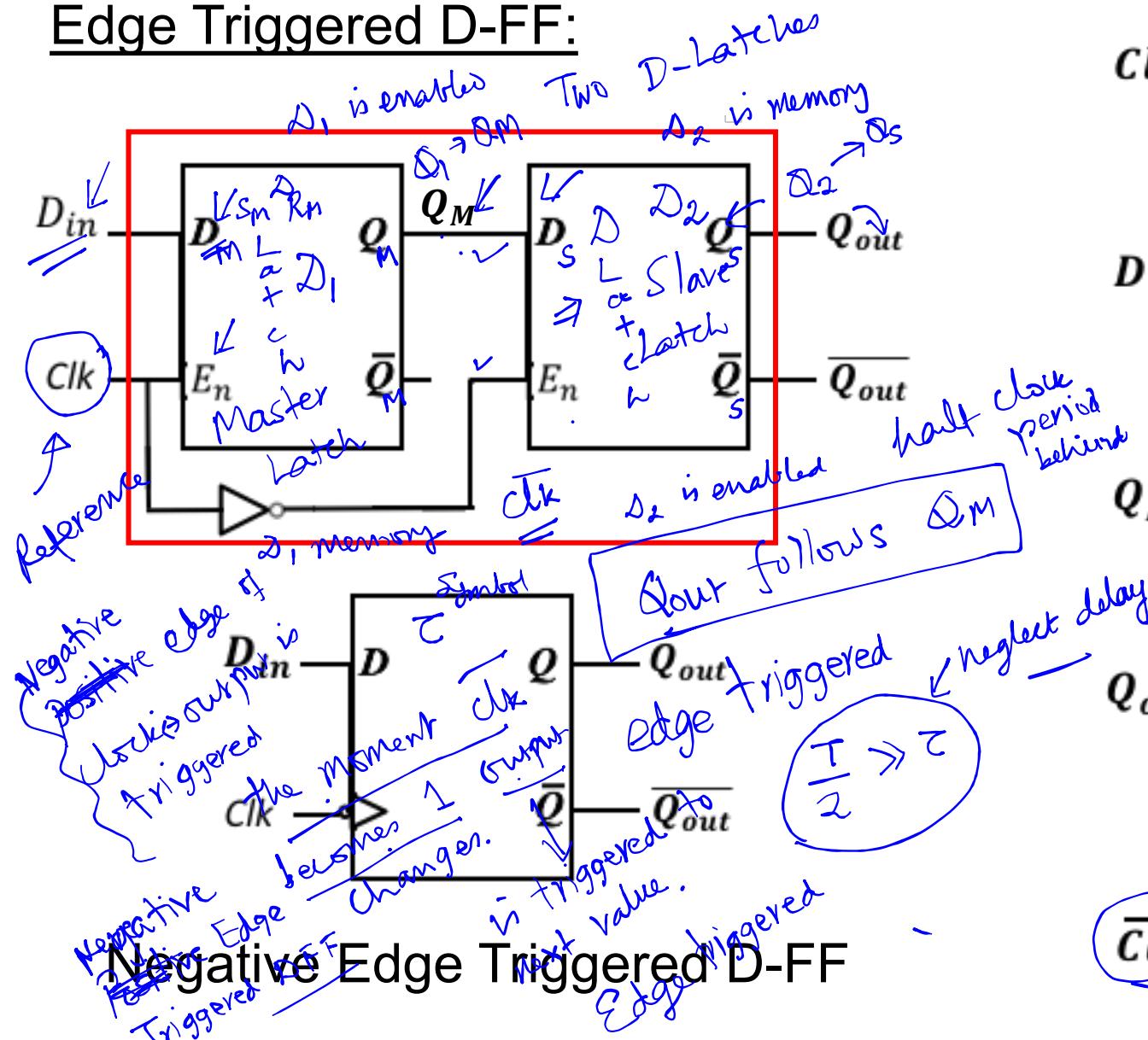
Racing



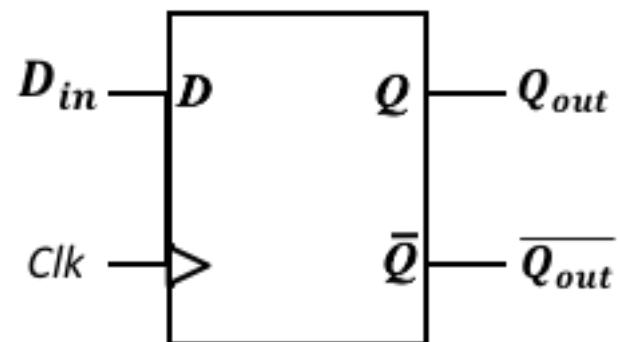
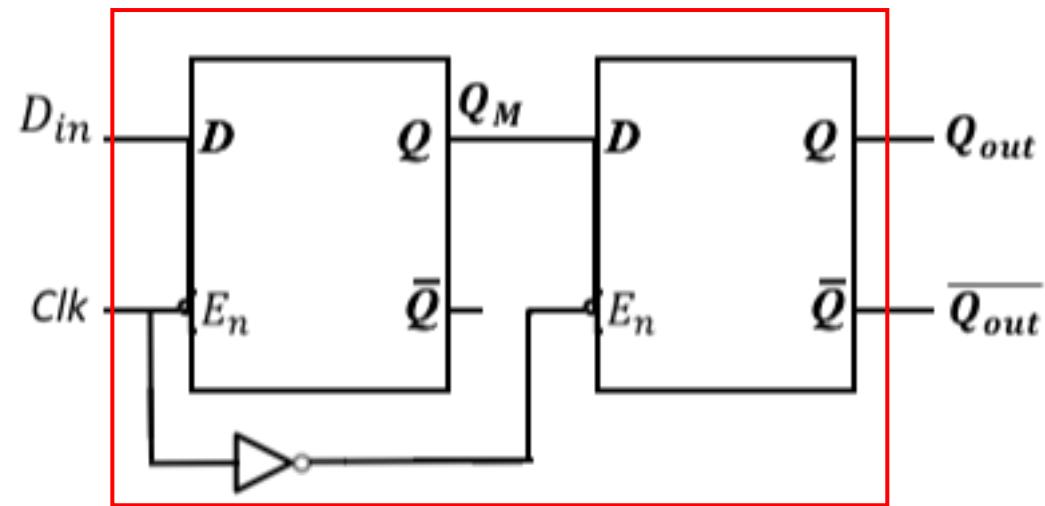
Latches without Racing (D- Latch) ---- Pulse Triggered D-Flip Flop:



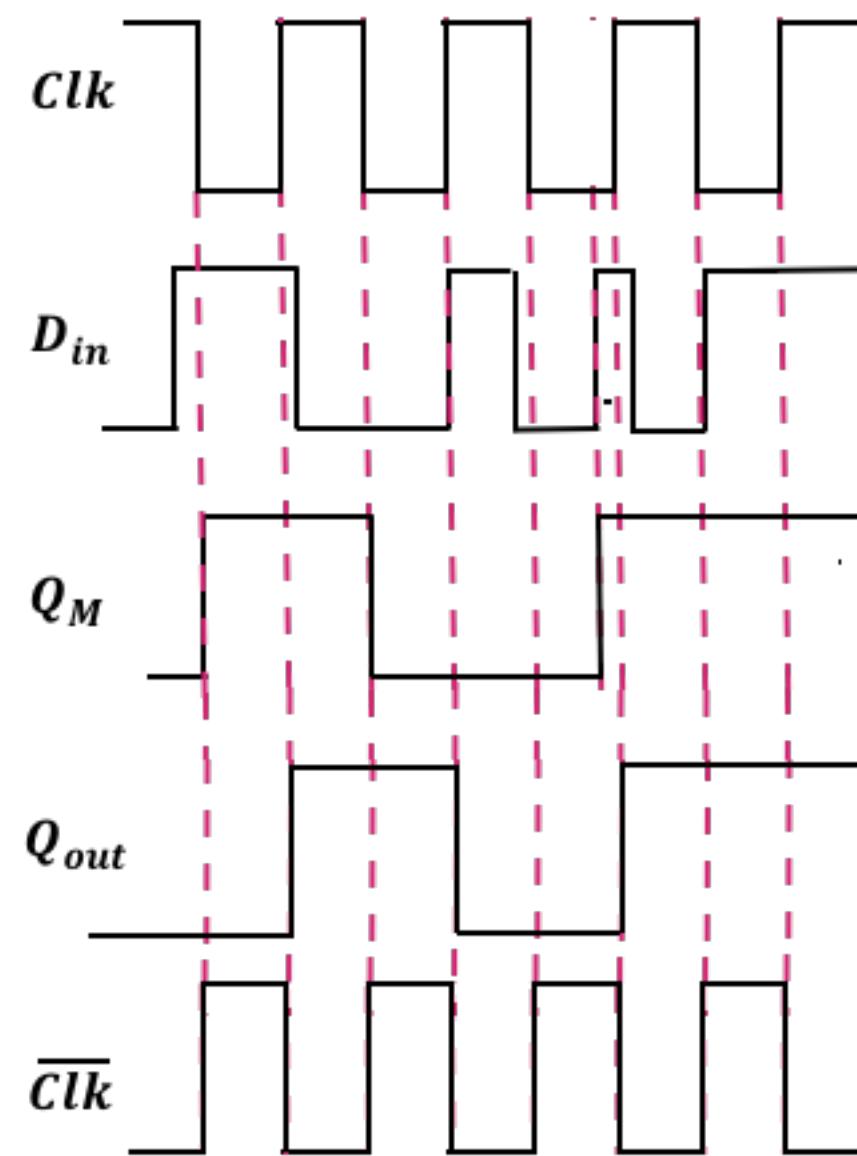
Edge Triggered D-FF:



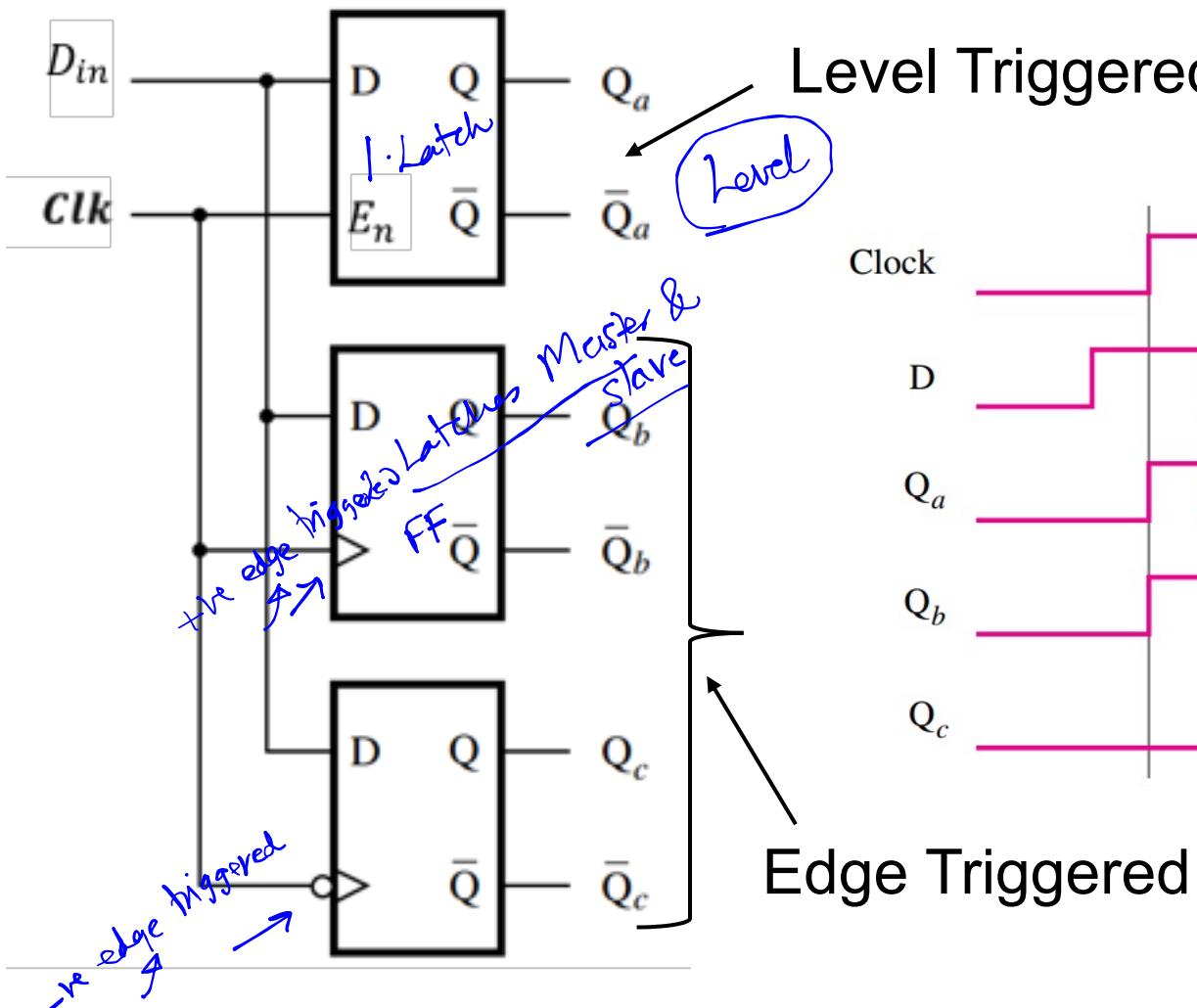
Edge Triggered D-FF:



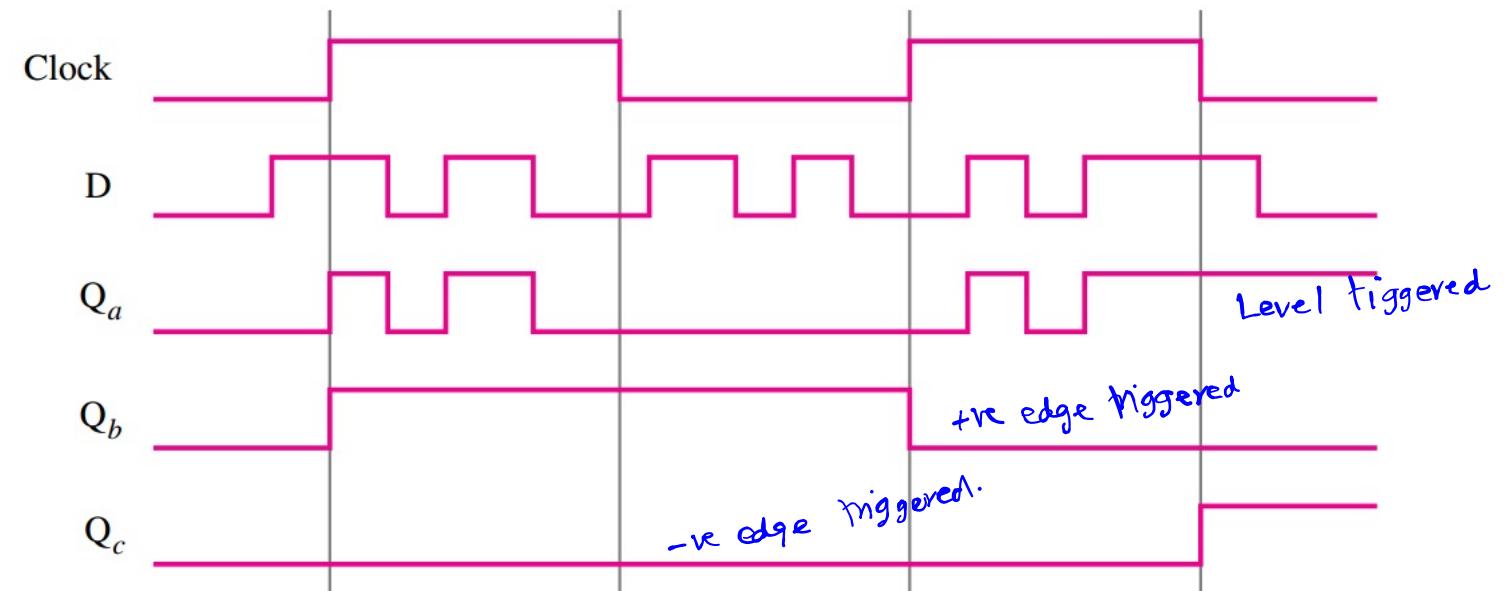
Positive Edge Triggered D-FF



Edge Triggered D-FF



Latch → a storage triggered on Level
FF → a storage triggered on edge



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