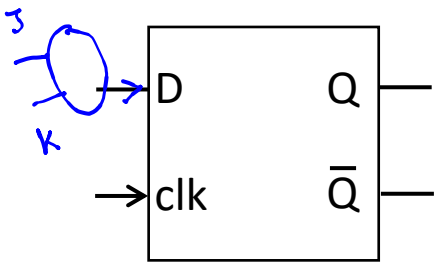
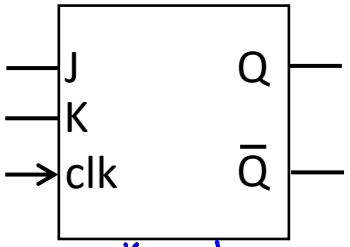
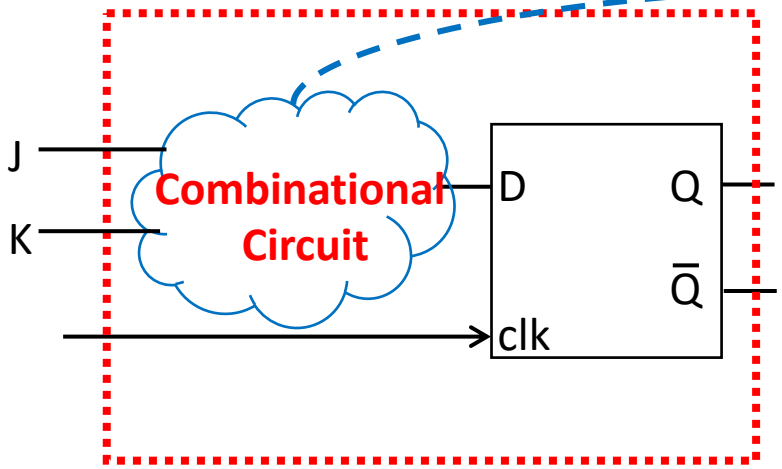
J-K FF Using D-FF



D	Q_n	$\overline{Q_n}$
0	0	1
1	1	0

J	K	Q_n	$\overline{Q_n}$
0	0	Q_{n-1}	$\overline{Q_{n-1}}$
0	1	0	1
1	0	1	0
1	1	$\overline{Q_{n-1}}$	Q_{n-1}





$$D = f(J, K, Q_{n-1}, \bar{Q}_{n-1})$$

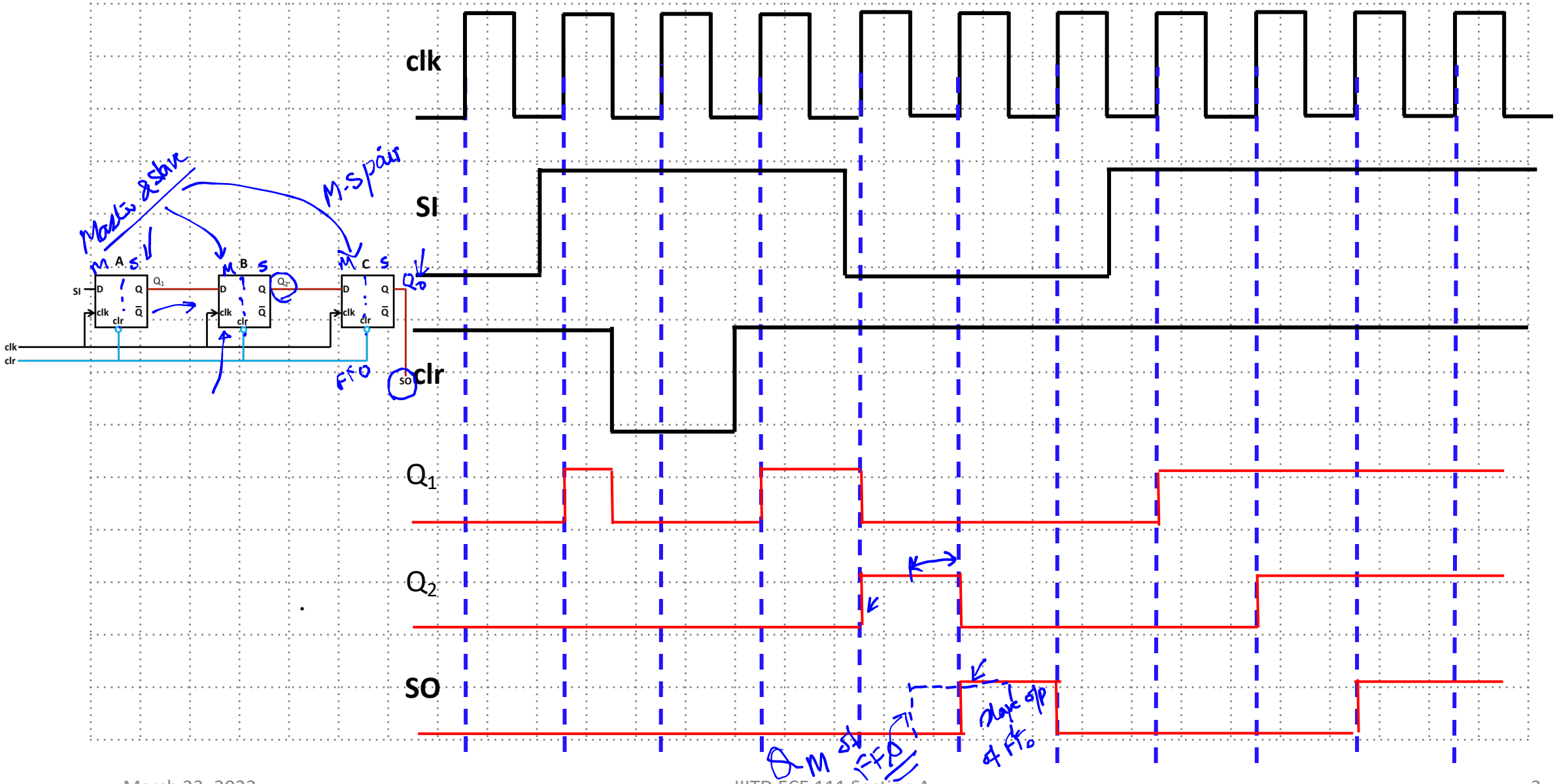
J	K	D
0	0	Q_{n-1}
0	1	0
1	0	1
1	1	$\overline{Q_{n-1}}$

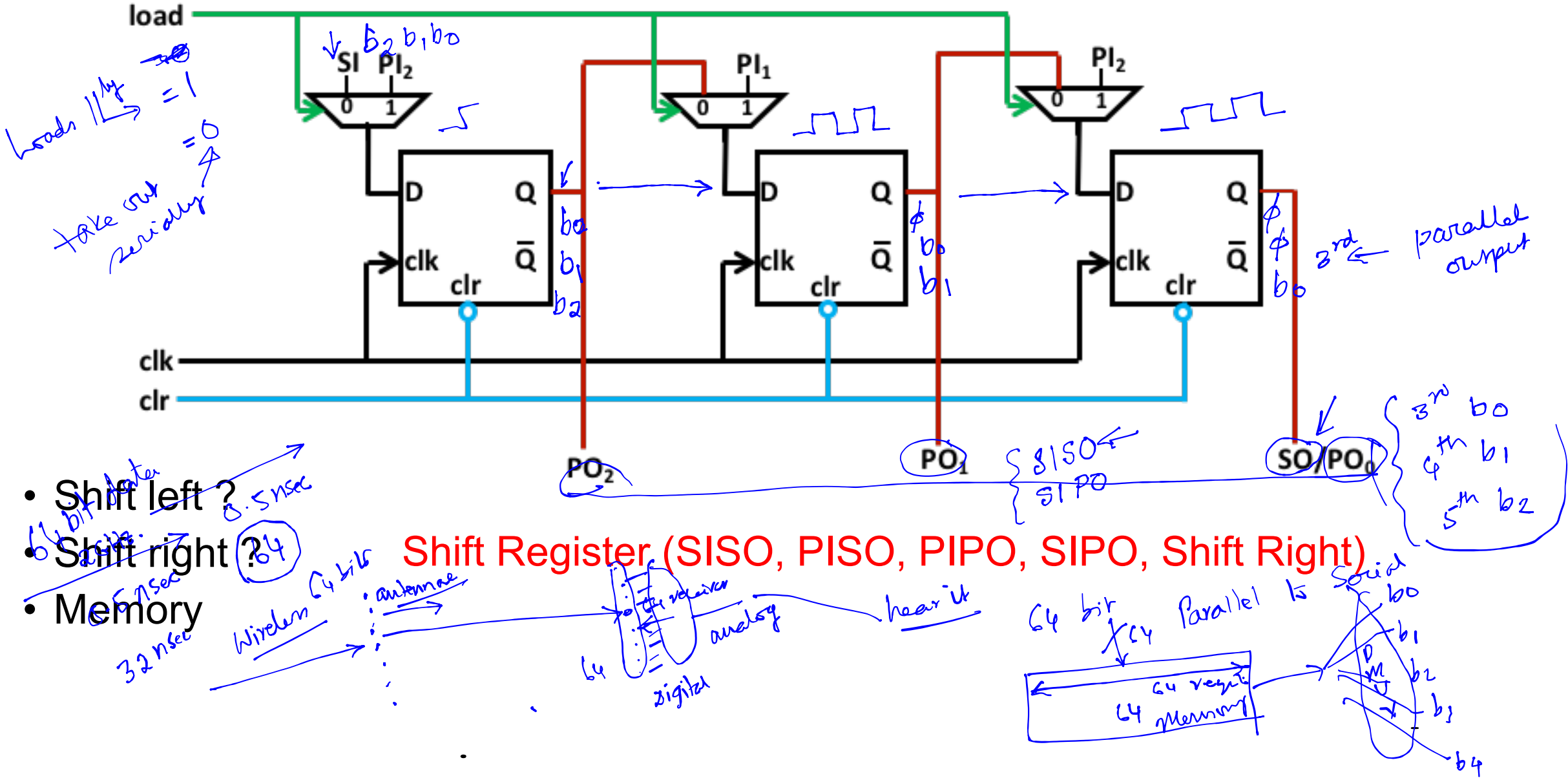
JK \ Q_{n-1}	0	1
00	0	1
01	0	0
11	1	0
10	1	1

$$D = J\overline{Q_{n-1}} + \overline{K}Q_{n-1}$$

Similarly realize T-FF using D-FF and D-FF using T-FF

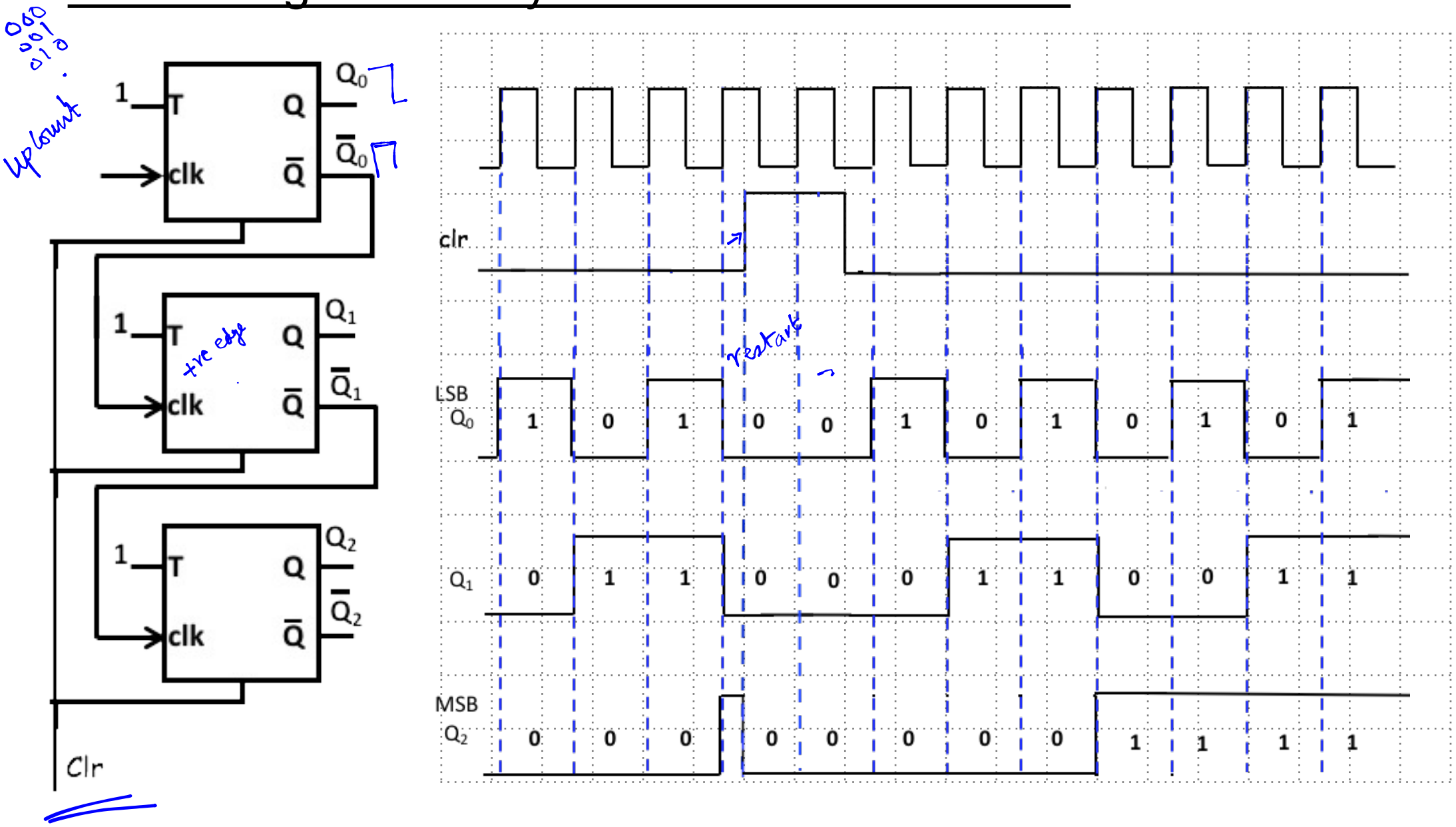
Shift Register (SISO):



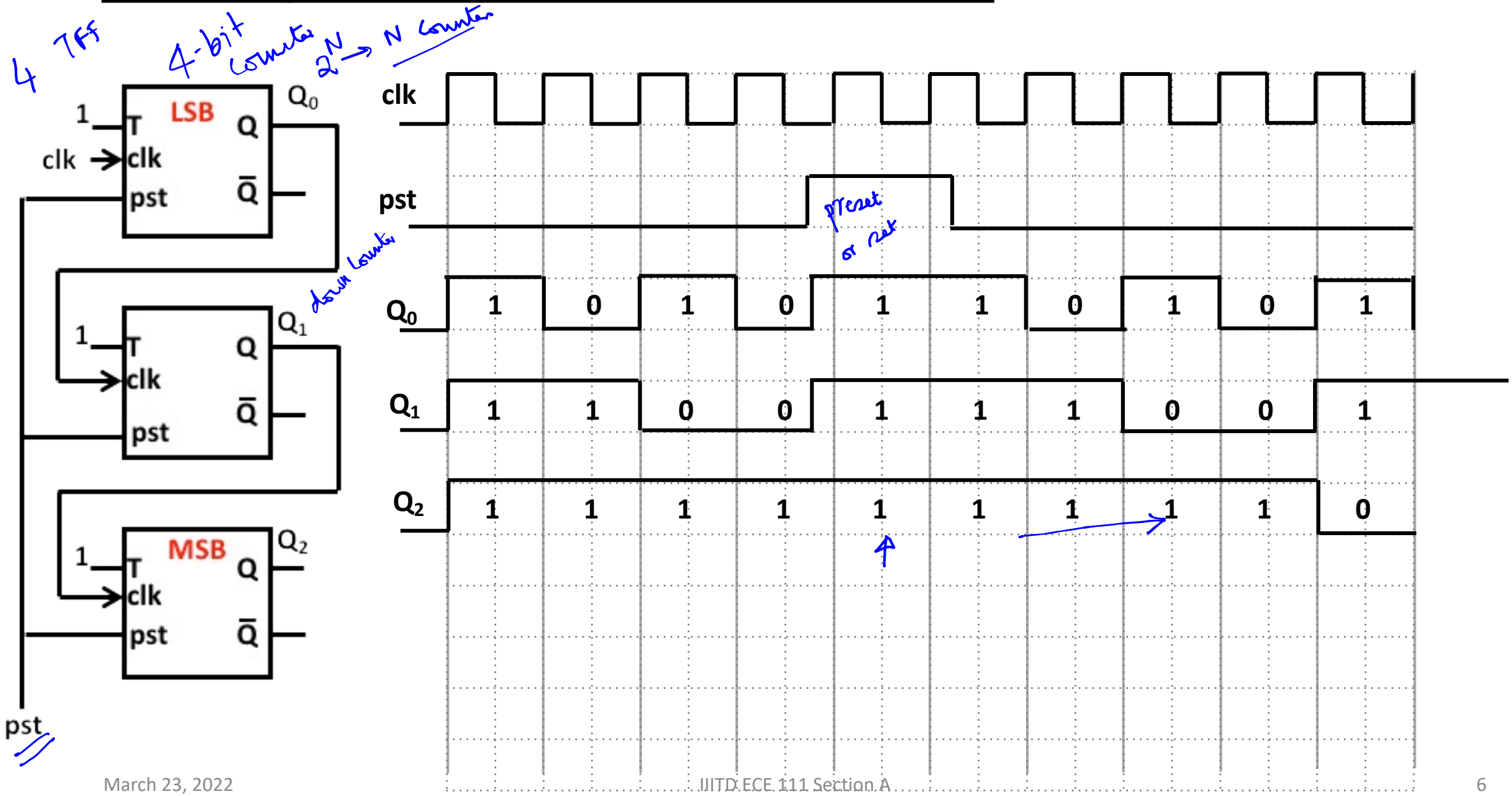


- Shift left ?
- Shift right ?
- Memory

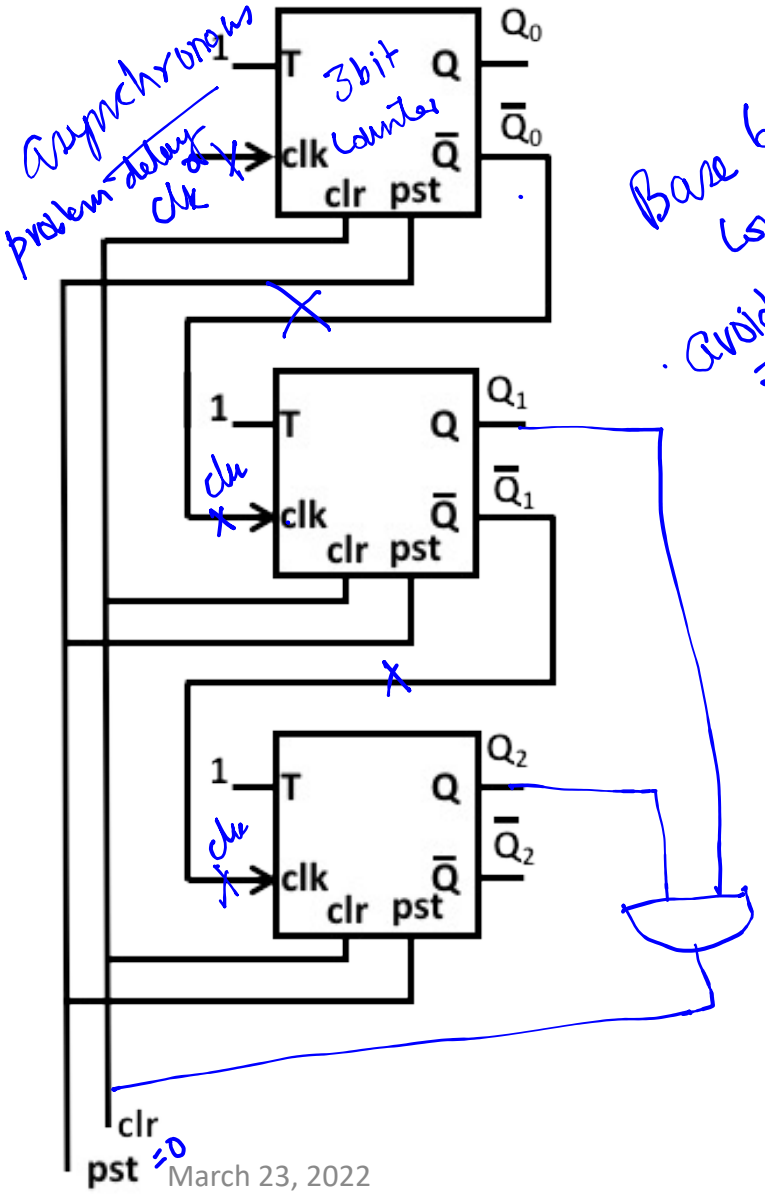
3-Bit Unsigned Binary UP Counter with Clear:



3-Bit Unsigned Binary Down Counter with Preset:



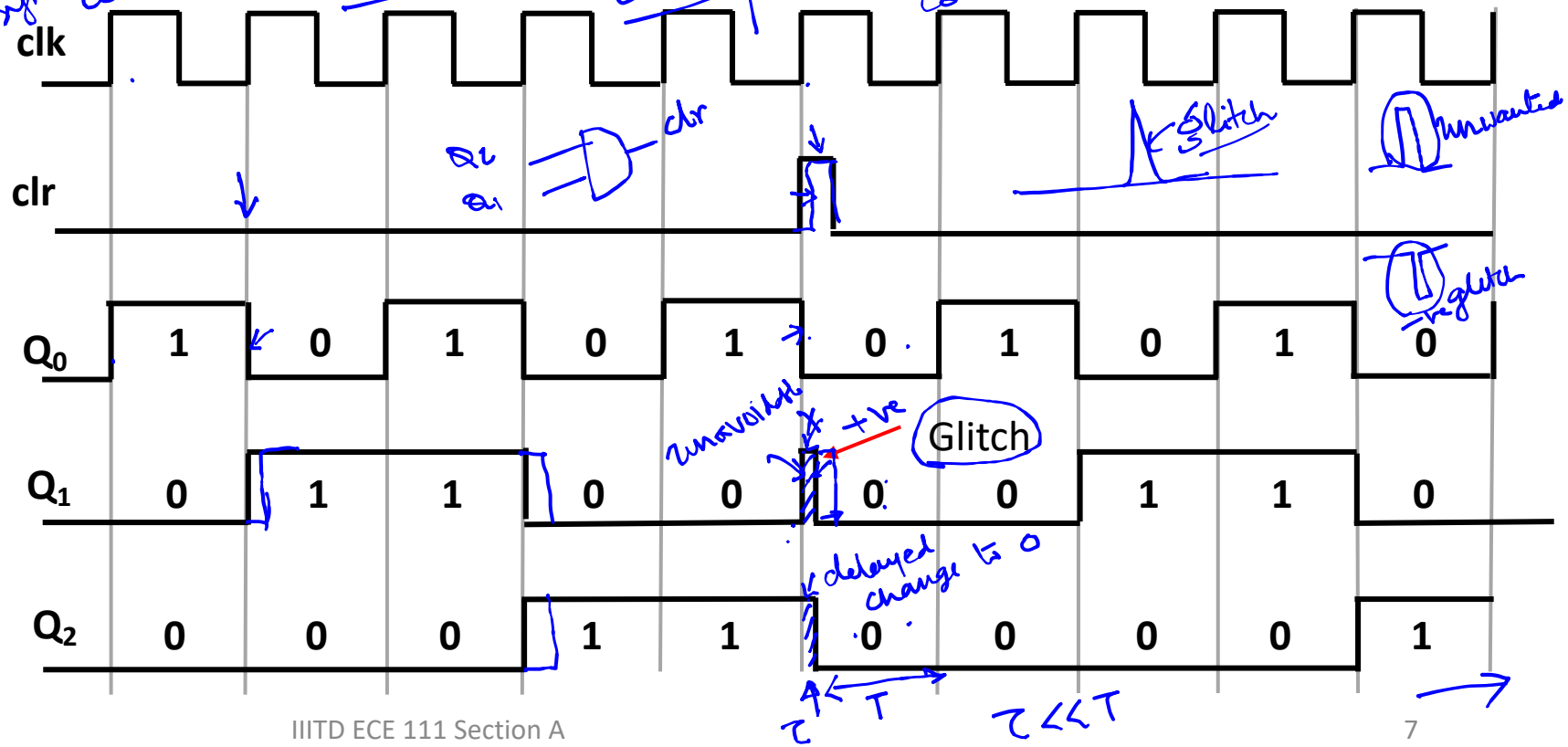
Binary Counter with Clear and Preset– Count length not a power of 2:



- **Modulo 6 counter**: $0 \rightarrow 1 \rightarrow 2 \rightarrow 3 \rightarrow 4 \rightarrow 5 \rightarrow 0 \rightarrow 1 \ldots$

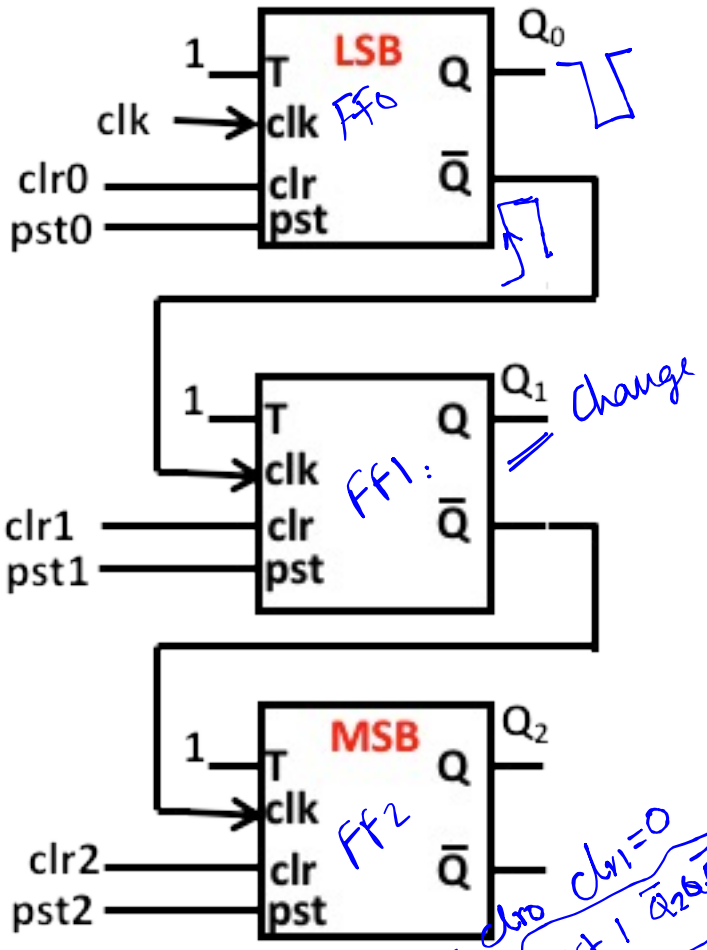
$000 \rightarrow 001 \rightarrow 010 \rightarrow 011 \rightarrow 100 \rightarrow 101 \rightarrow 000 \rightarrow 001 \ldots$

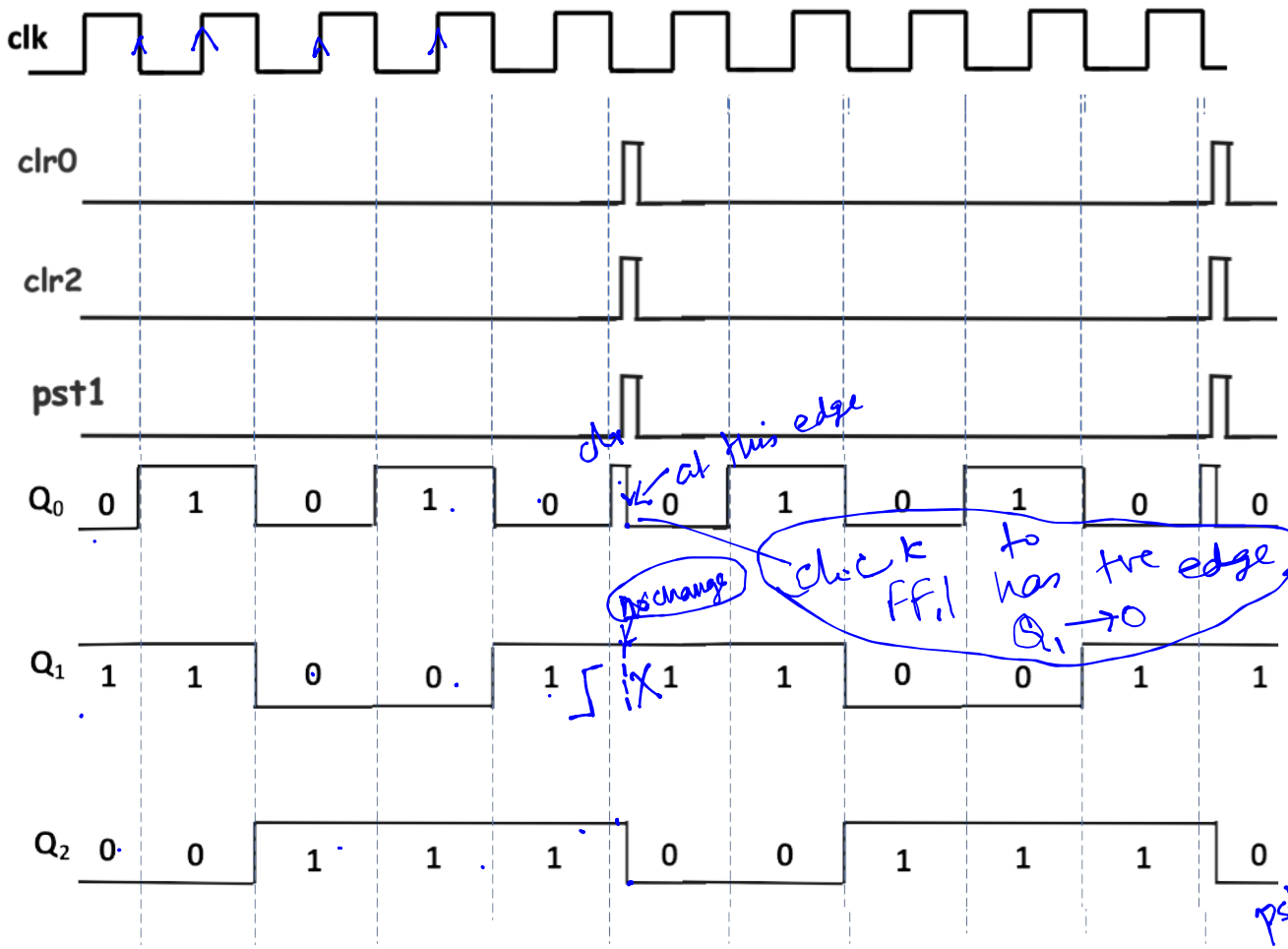
$$clr = Q_2 \cdot Q_1$$



Binary Counter with Clear and Preset:

- **Counter**: 2->3->4->5-> 6->2->3->4->5-> 6->2-----





$$clr0 = clr2 = pst1 = \overline{Q_2} \cdot Q_1 \cdot Q_0 \;;\; clr1 = pst0 = pst2 = 0$$

HW:

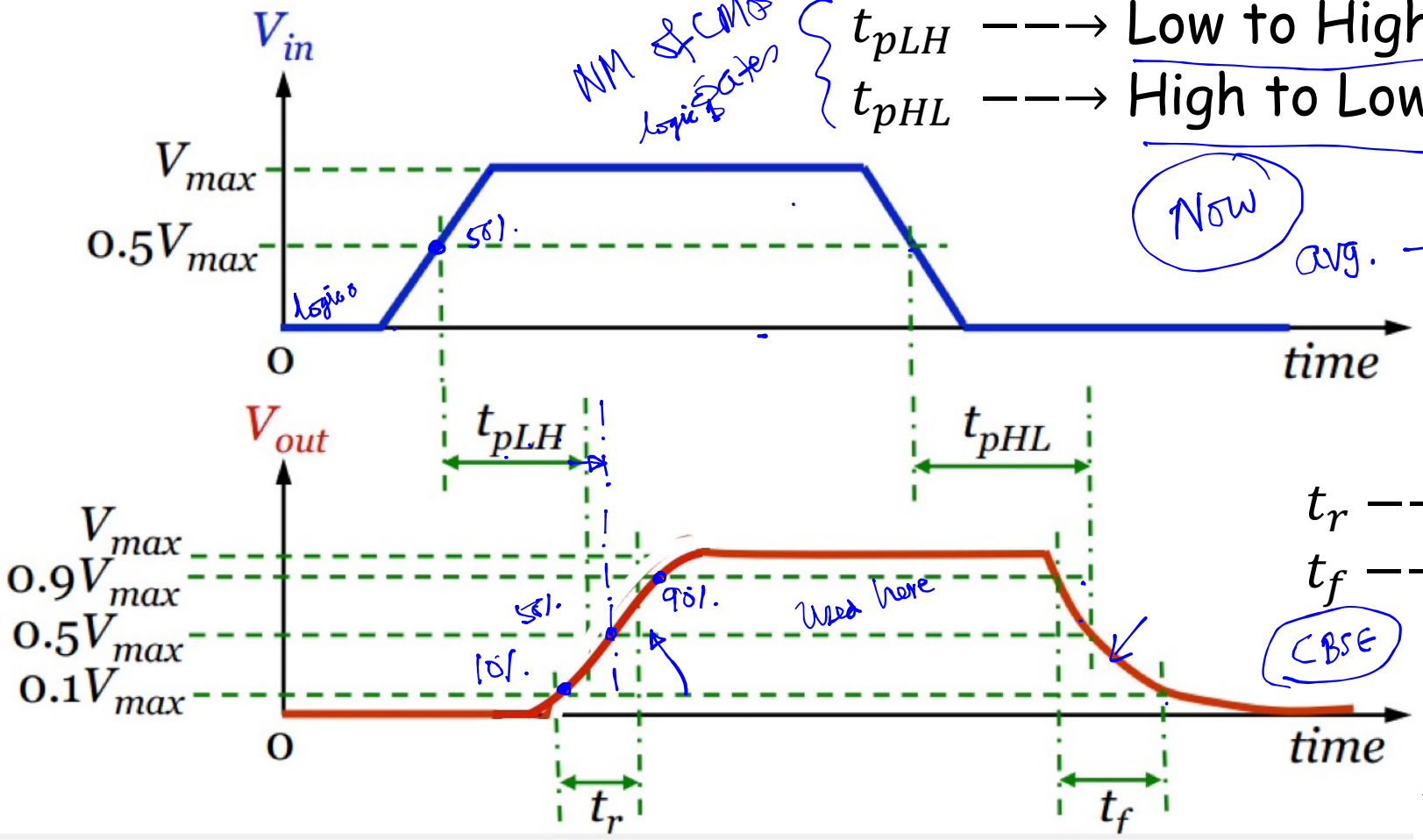
1. Design the counter with sequence as 4-5-6-7-8-9-4…. Using active low clear and active low preset
2. Assume that you have an oscillator which provides clock signal with frequency 8 Hz. Design modulo-6 counter which increments its output count every second.

period → $\frac{1}{8}$ sec → 1 Hz.

3. Decade BCD counter.

Definition of some important characteristics with Digital Circuits:

Combinational Circuits:



t_{pLH} ⟶ Low to High Propagation Delay

t_{pHL} ⟶ High to Low Propagation Delay

t_r ⟶ Rise time

t_f ⟶ Fall time