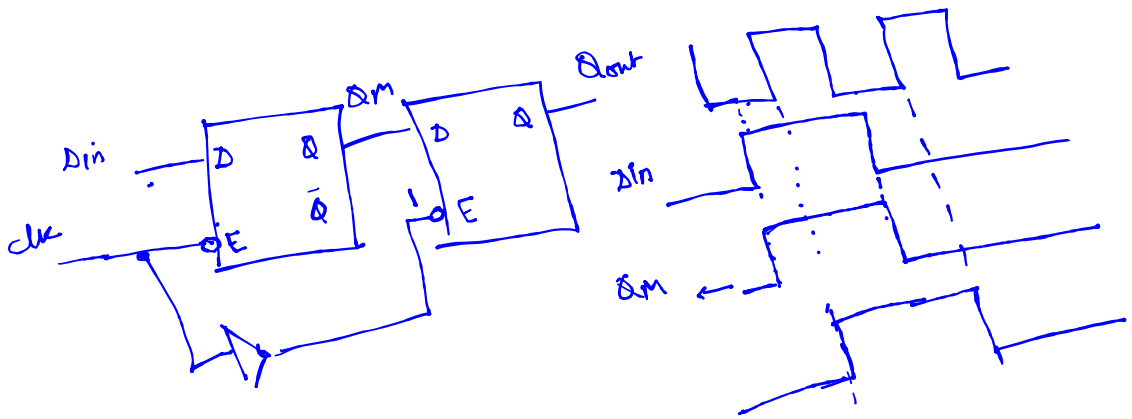
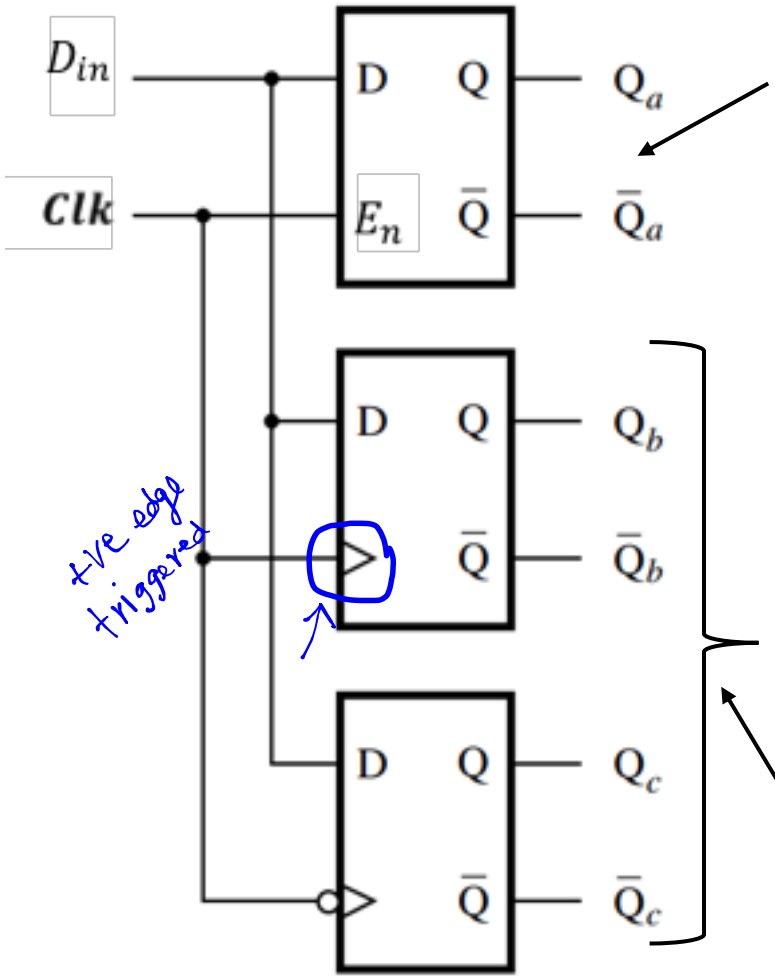
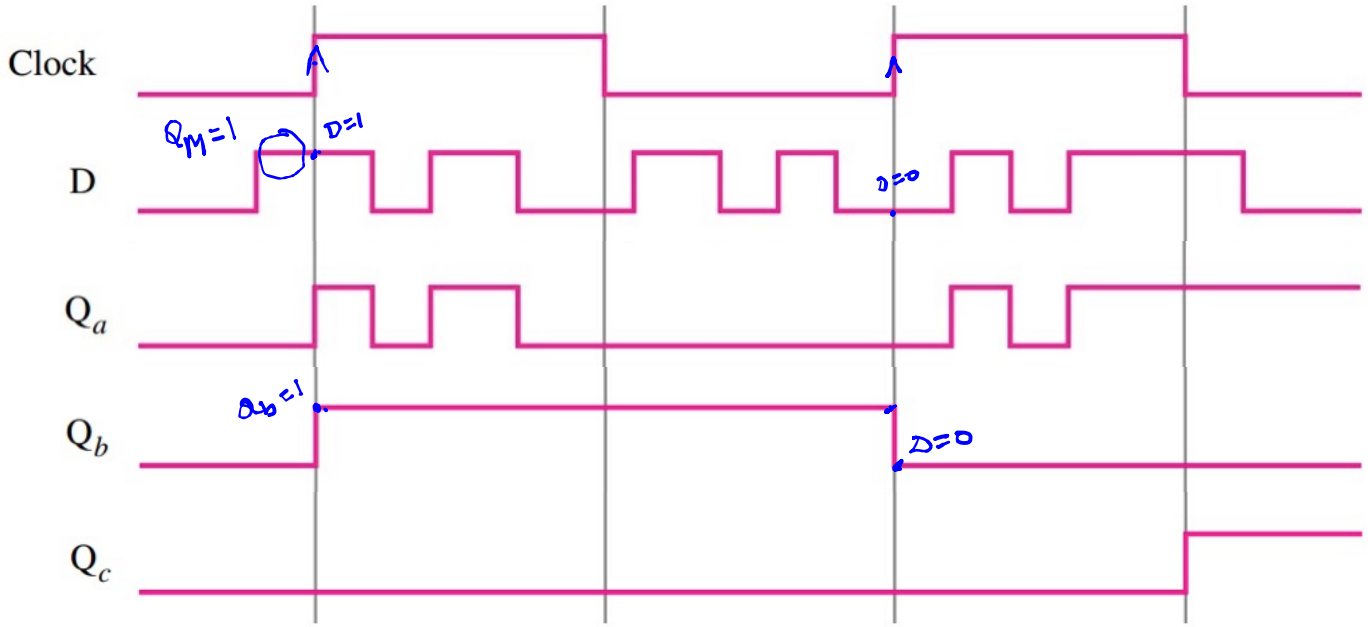

Din
clk
D
Q
Q̄
E
Dm
D
Q
E
Qout
Din
Dm

Level and Edge Triggered D-FFs:



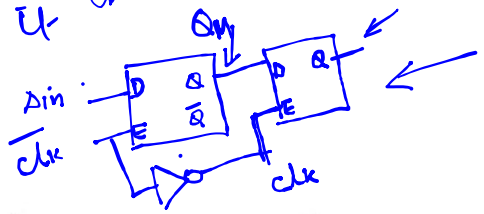
Level Triggered



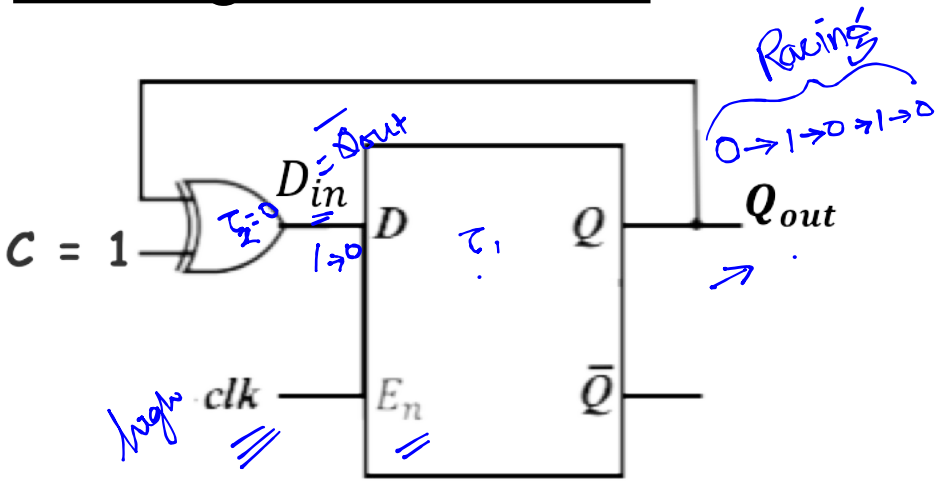
Edge Triggered ---- An emulated property.

Flip Flop

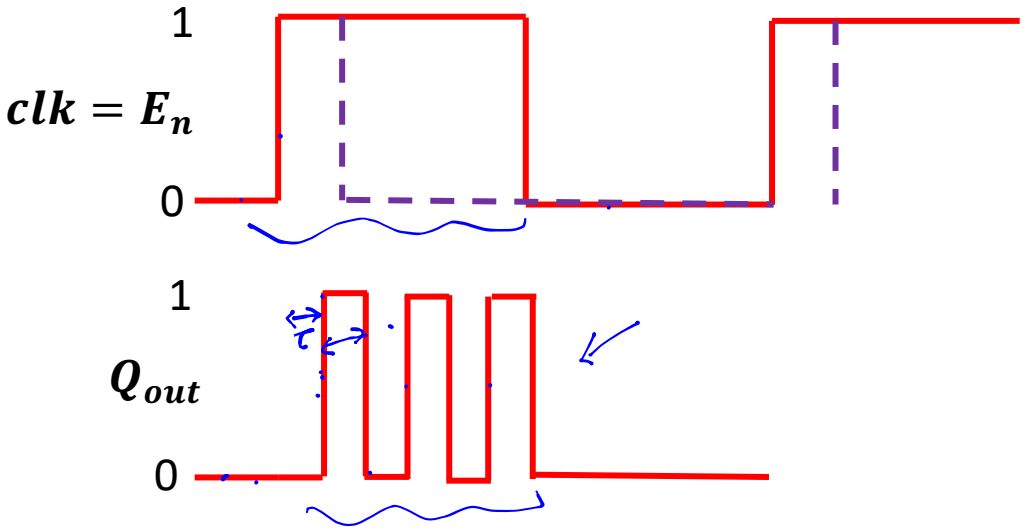
Latch will change state o/p if i/p changes & is in active

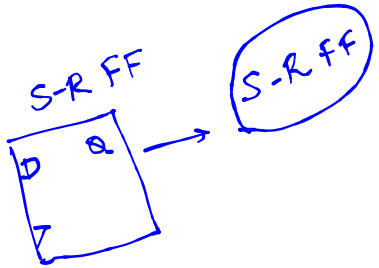


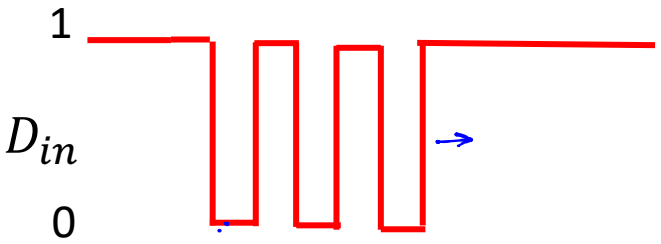
Racing in D- Latch:

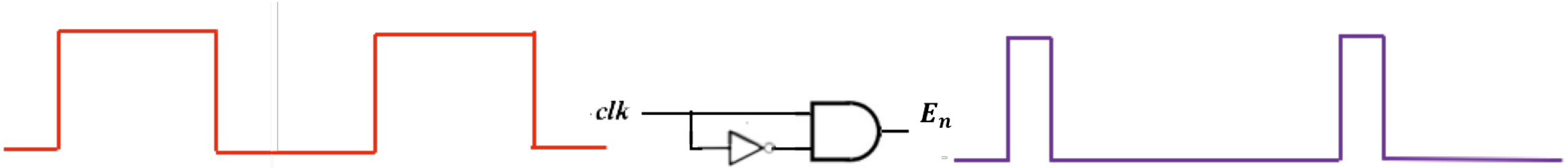


$$D_{in} = \overline{Q_{out}}$$

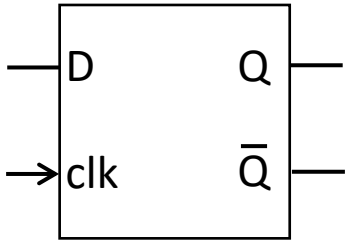






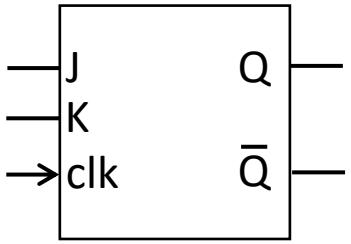


J-K FF Using D-FF



D	Q_n	$\overline{Q_n}$
0	0	1
1	1	0

J	K	Q_n	$\overline{Q_n}$
0	0	Q_{n-1}	$\overline{Q_{n-1}}$
0	1	0	1
1	0	1	0
1	1	$\overline{Q_{n-1}}$	Q_{n-1}

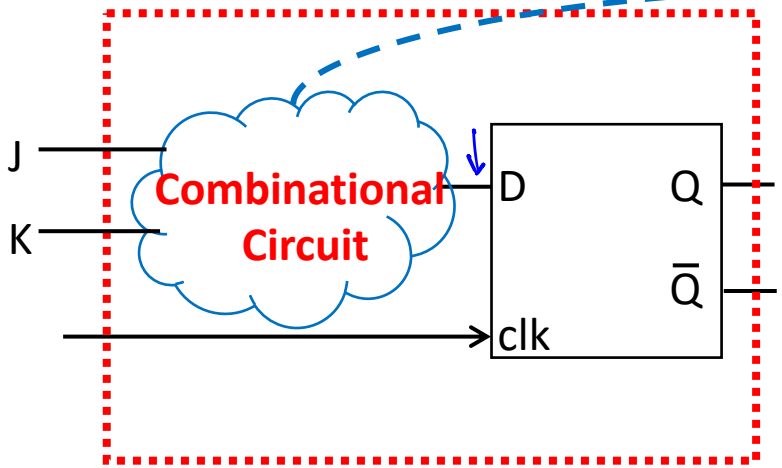


Truth Table for J-K

Characteristic eqn of J-K FF

$Q_n = J\overline{Q_{n-1}} + \overline{K}Q_{n-1}$

$$D = f(J, K, Q_{n-1}, \bar{Q}_{n-1})$$



J	K	D
0	0	Q_{n-1}
0	1	0
1	0	1
1	1	$\overline{Q_{n-1}}$

JK \ Q_{n-1}	0	1
00	0	1
01	0	0
11	1	0
10	1	1

In today's tech. CMOS we design on chip. We use/design only D FF

Counting down
present
restart
100
0
0 → 100
restart
clear
stop watch

J → Q

$$D = J\overline{Q_{n-1}} + \overline{K}Q_{n-1}$$

Similarly realize T-FF using D-FF and D-FF using T-FF

Preset and Clear:

D, clk

→ clear & preset

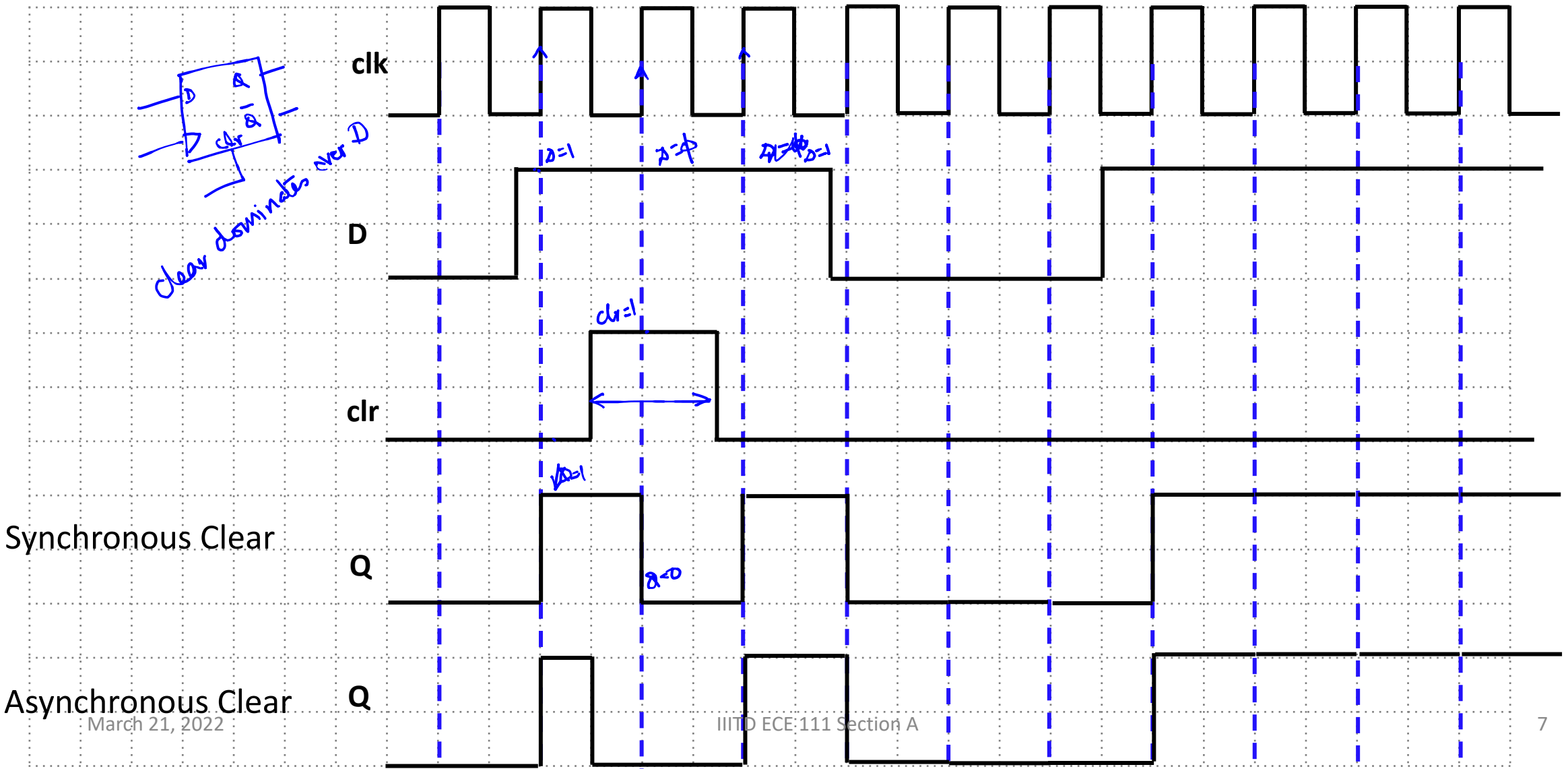
cl pr

Q $\bar{Q}$

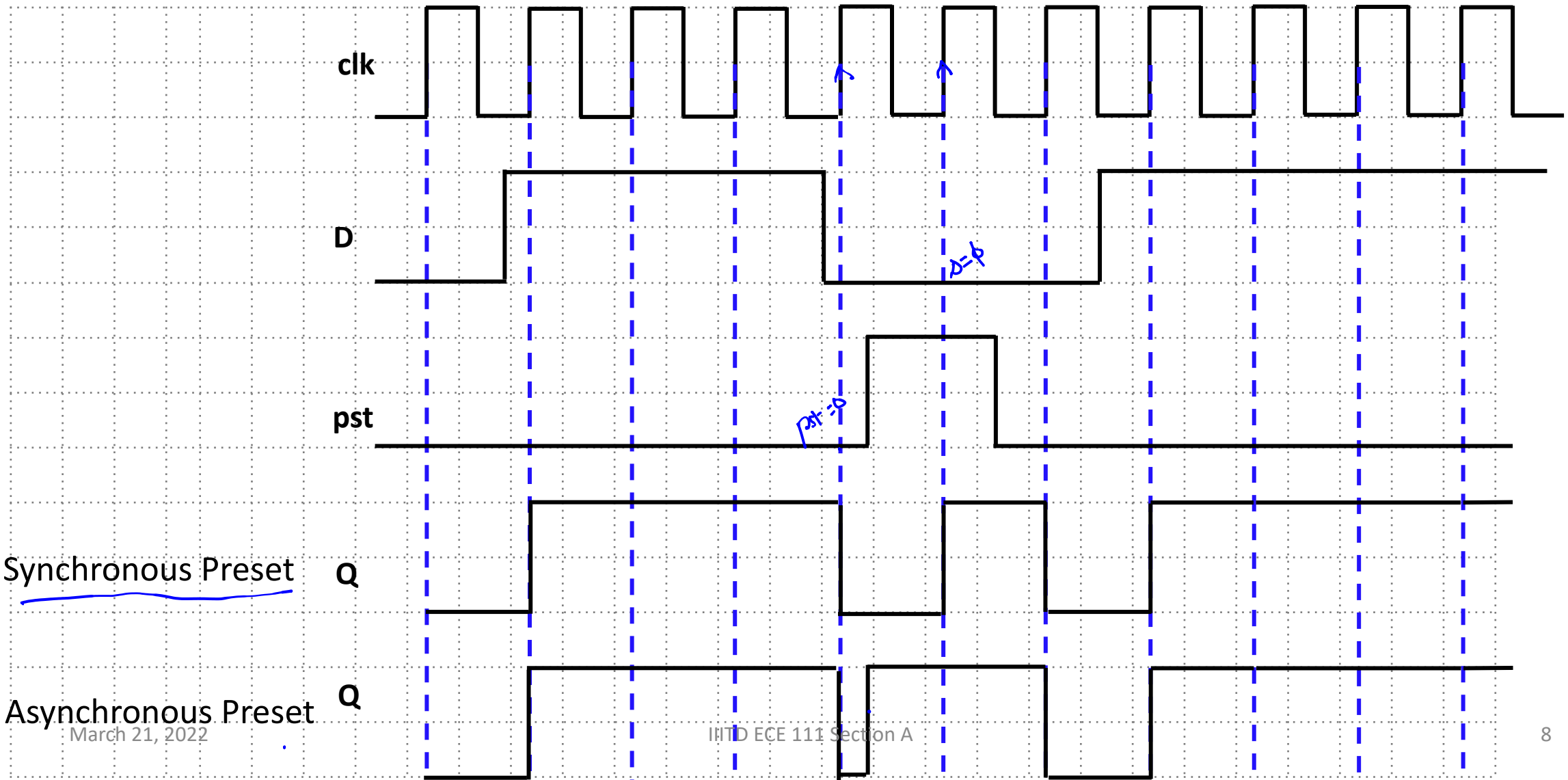
- Active low clear
- Active high clear
- Active low preset
- Active high preset

Synchronous vs Asynchronous Clear for a +ve Edge Triggered FF (Timing Diagram)

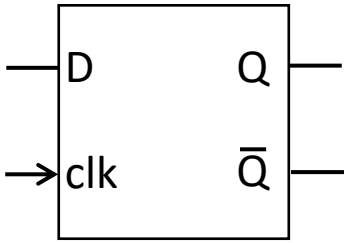
+ve edge triggered — clear/preset only on +ve edge

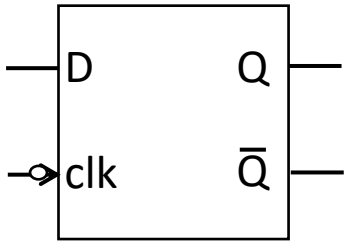


Synchronous vs Asynchronous Preset for a +ve Edge Triggered FF (Timing Diagram)



D-FF with Synchronous Clear and Preset:





changes are made at the i/p

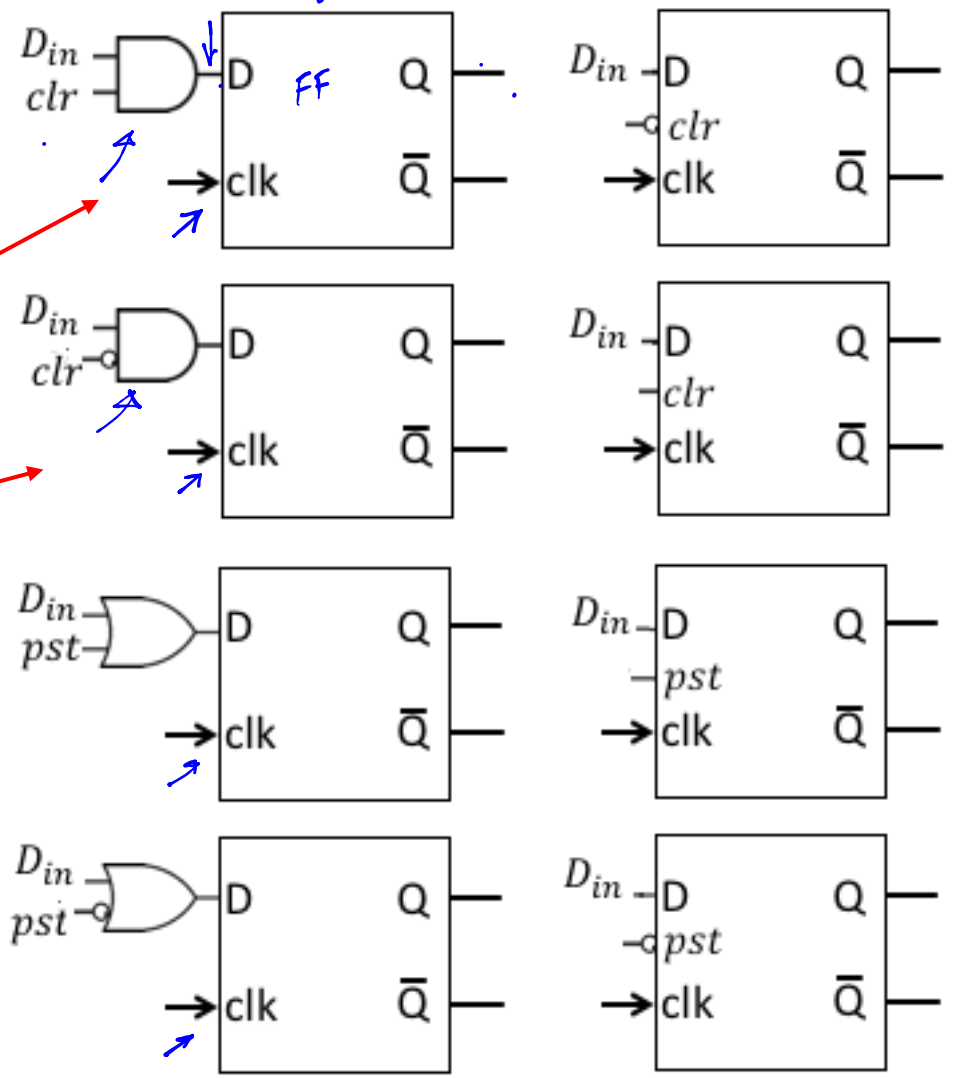
FF basic structure is untouched.

$Active\ low\ clear \rightarrow D = clr\ AND\ D_{in}$

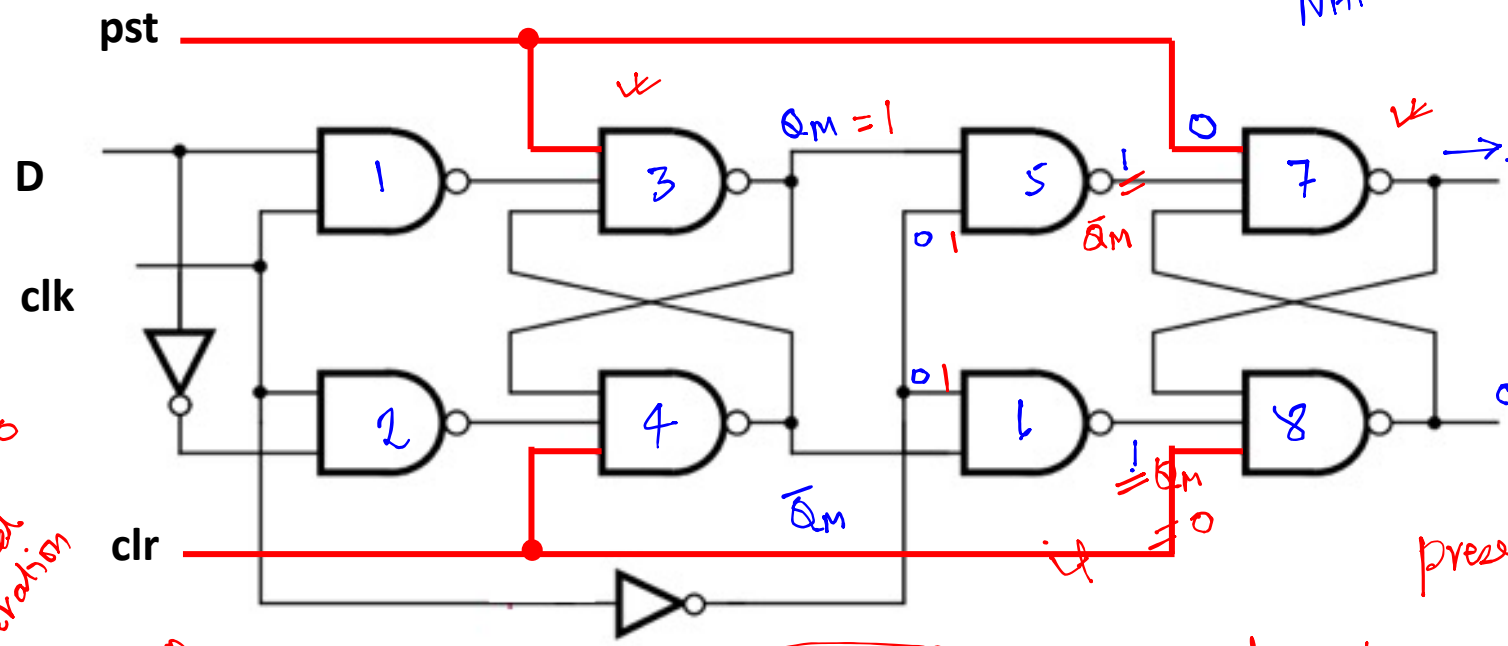
$Active\ high\ clear \rightarrow D = \overline{clr}\ AND\ D_{in}$

$Active\ high\ preset \rightarrow D = pst\ OR\ D_{in}$

$Active\ low\ preset \rightarrow D = \overline{pst}\ OR\ D_{in}$



D-FF with Asynchronous Active Low Clear and Active Low Preset:



NAND based D-FF

NAND $\rightarrow$ pst dominated by zero

preset $\rightarrow$ Q=1 assume clk = 1 what if clk = 0 forbidden over come this

preset both Master & Slave

preset { pst = 0, clr = 1

clear { pst = 1, clr = 0

pst = 1, clr = 1 } Normal operation

pst = 0, clr = 0 } forbidden

1. pst & clr
2. clr
3. pst

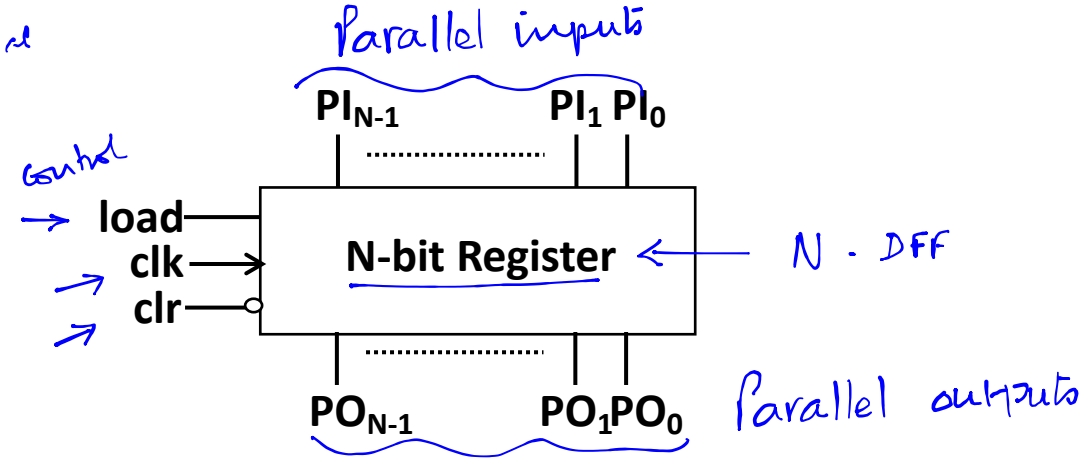
designs with clear —

D-FF have only clr

D-FF have only pst

D-FF have both clr & pst.

Register:



is a simple D-FF with additional provisions.

1-bit

Memory

N-FF

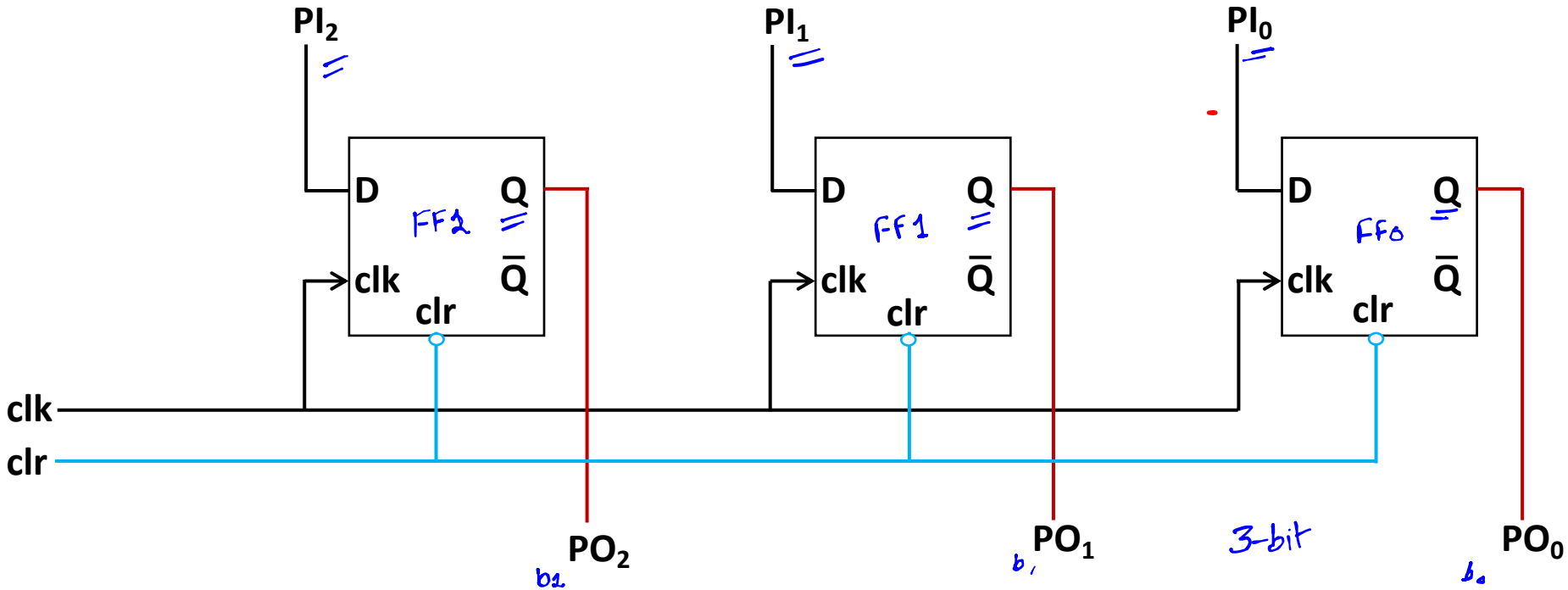
- N-bit Register -> Can store N-bit data
- Consists of N D-FFs
- Clear (clr) is asynchronous. It can be synchronous as well.
- When load is 1, inputs are stored in the D-FFs at the next positive clock edge. When load is zero, inputs are ignored and FFs retain their values.
- FF outputs are available in parallel.
- Parallel in parallel out

Memory write mode

Memory Read mode

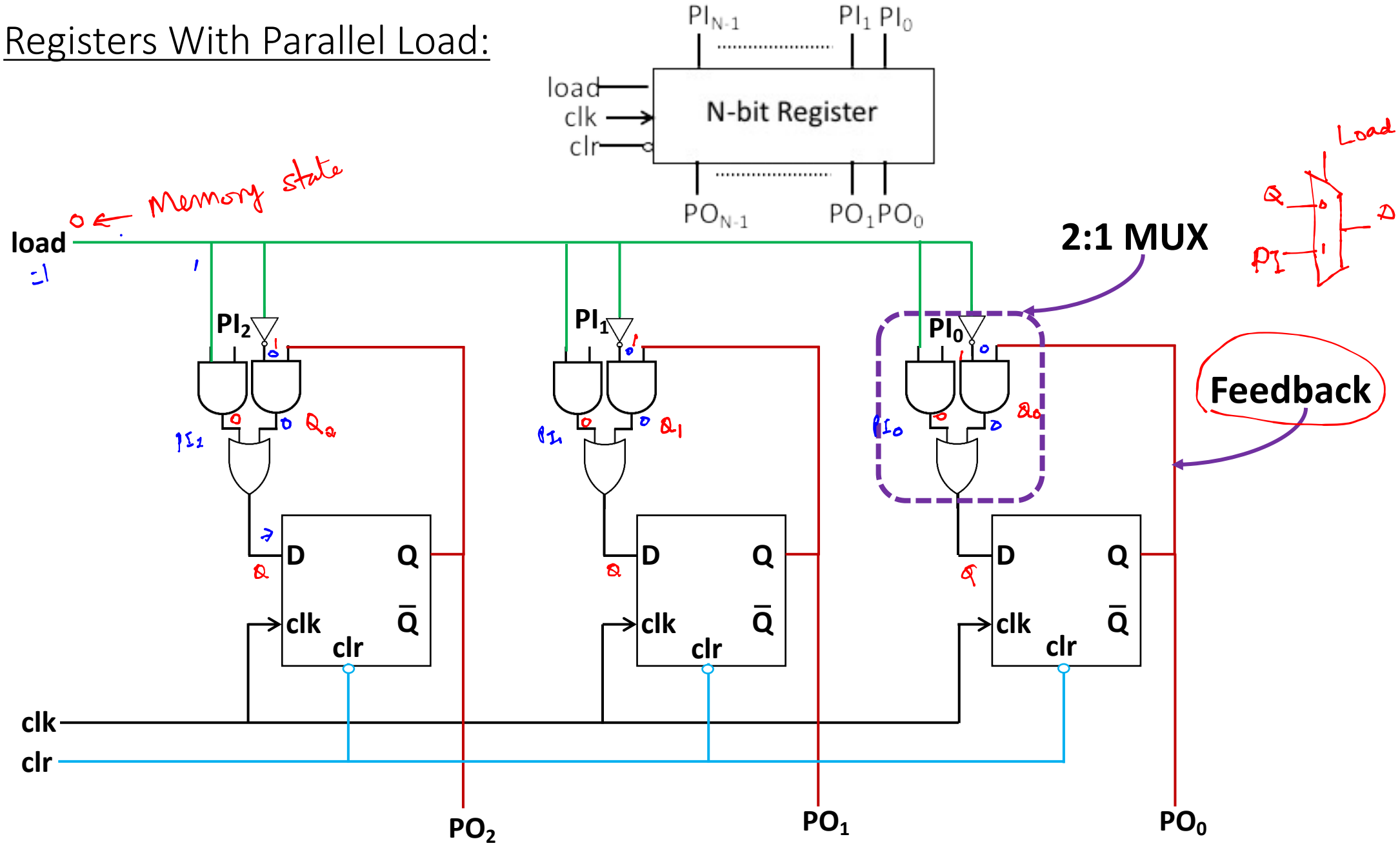
Register

Registers:

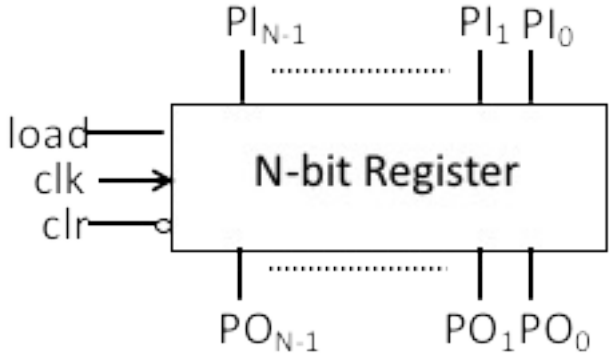


- No Memory state ↙ there is no Load control
- At each clock edge, input values are loaded into the FFs.
- Load input is missing

Registers With Parallel Load:



Registers With Parallel Load:



load

2:1 MUX

Parallel -in

PI_2

PI_1

PI_0

Feedback

Feedback

Feedback

D Q

clk $\bar{Q}$

clr

clk

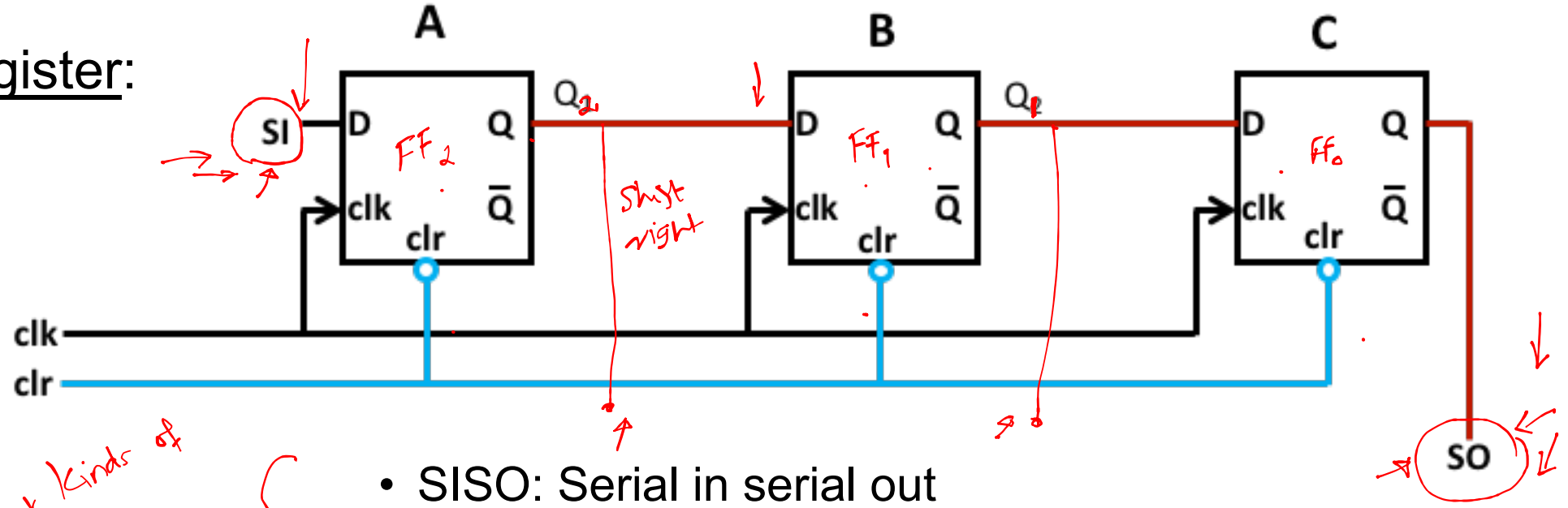
clr

PO_2

PO_1

PO_0

Shift Register:



Different kinds of Registers

- SISO: Serial in serial out
  - FIFO: First IN First OUT
  - LIFO: Last IN First OUT ← see later
- SIPO: Serial in parallel out
- PIPO: Parallel in parallel out ←
- PISO: Parallel in serial out ←
- Shift left
- Shift right
- Memory ←

first we saw this

Excitation and Truth Tables

How to change Q_p from 0 to 0 / 0 to 1 / 1 to 0 / 1 to 1

Q=0 R=1 Q=0 S=0 Value S and R