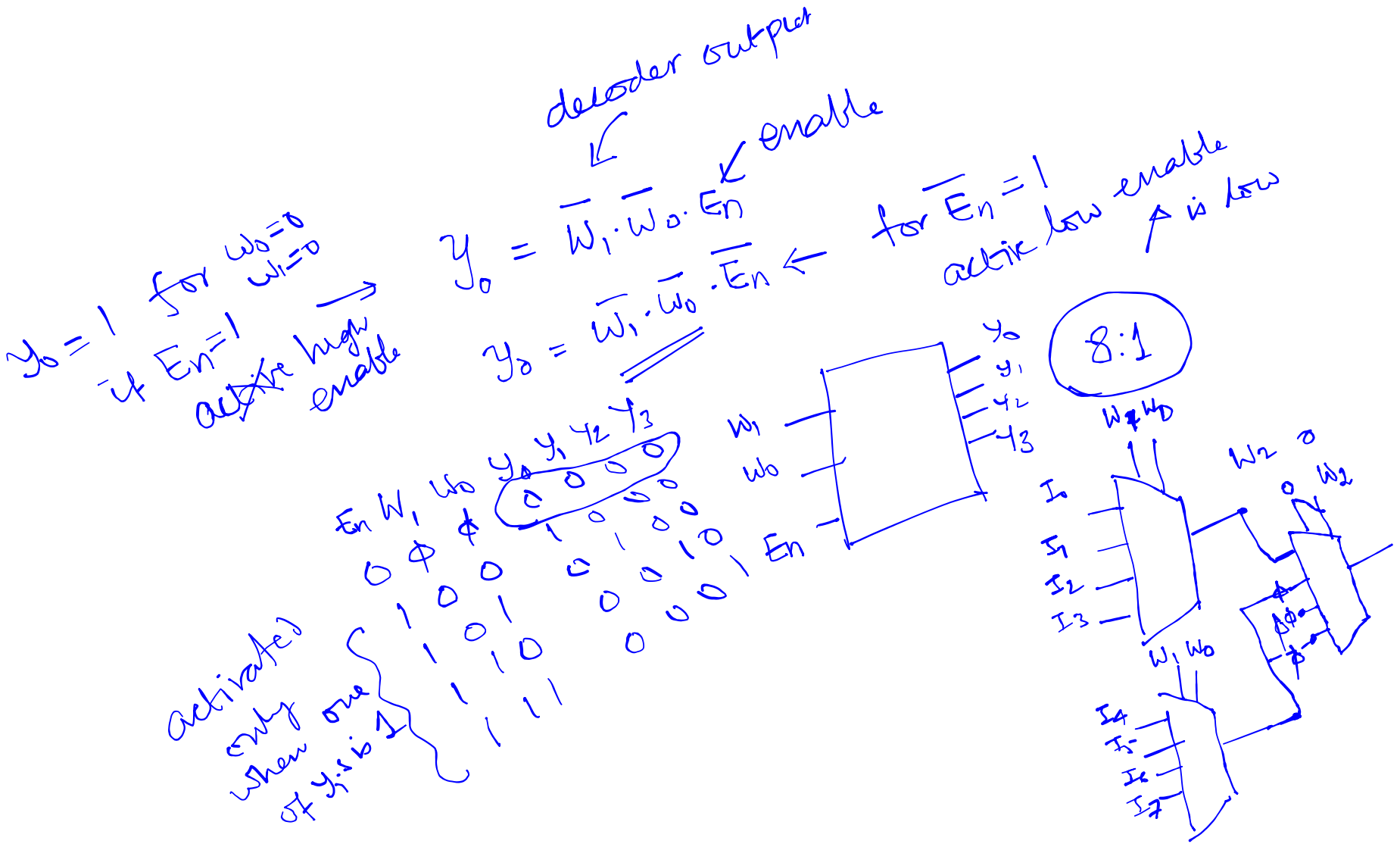
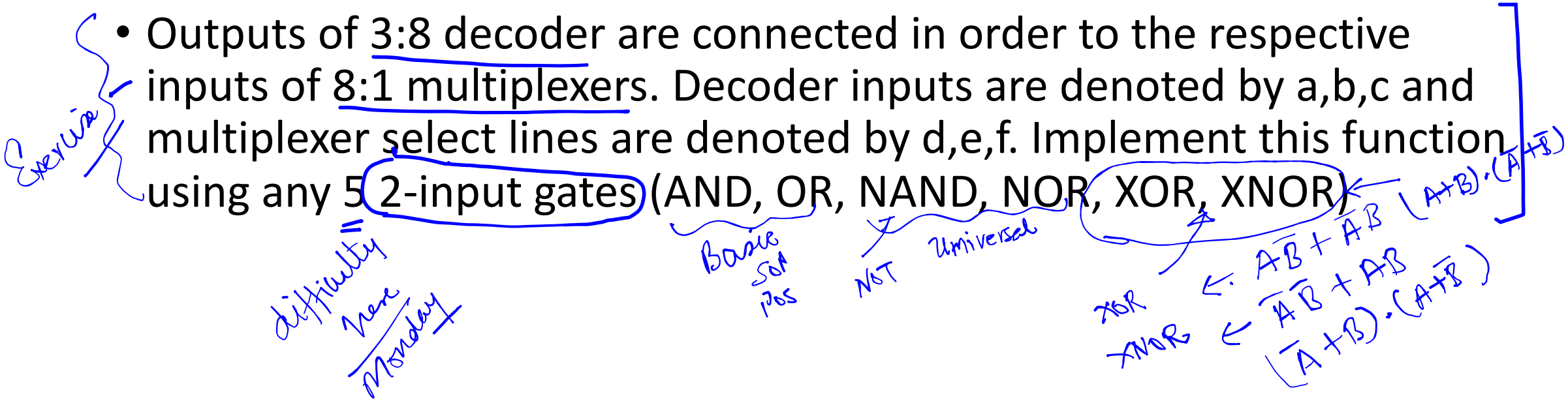

decoder output
enable
$y_0 = \overline{W_1} \cdot \overline{W_0} \cdot \overline{En}$
$y_0 = \overline{W_1} \cdot \overline{W_0} \cdot \overline{En}$
$y_0 = 1$ for $W_0 = 0$ $W_1 = 0$ if $En = 1$ active high enable
for $\overline{En} = 1$ active low enable
$\overline{En}$ is low
y_0 y_1 y_2 y_3
W_1 W_0 $\overline{En}$
0 0 0 1 0 0 0
0 0 1 0 1 0 0
0 1 0 0 0 1 0
0 1 1 0 0 0 1
activated only when one of y_i is 1
8:1
W_1 W_0
I_0 I_1 I_2 I_3
W_2 0 W_2
I_4 I_5 I_6 I_7

To help the class prepare better for end-semester examination and to help in evaluation, we have decided to hold a quiz every Saturday, starting March 5, 2022. Thus, we will have a quiz between 10:00AM and 10:20AM on March 5, 12, 19 and 26 and April 2, 2022. The last quiz on April 2, 2022 will be held in-person/off-line. If all of you are available on campus or in Delhi earlier, we will prefer to hold some of the other four quizzes also off-line.

HW Practice

- Outputs of 3:8 decoder are connected in order to the respective inputs of 8:1 multiplexers. Decoder inputs are denoted by a,b,c and multiplexer select lines are denoted by d,e,f. Implement this function using any 5 2-input gates (AND, OR, NAND, NOR, XOR, XNOR)



Encoder:

- A n-to-m-line *encoder* is a combinational circuit that converts information from *n* input lines to a minimum of m = $\lceil log_2 n \rceil$ output lines.

4:2 Encoders:

w_3	w_2	w_1	w_0	y_1	y_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

w_1w_0 / w_3w_2

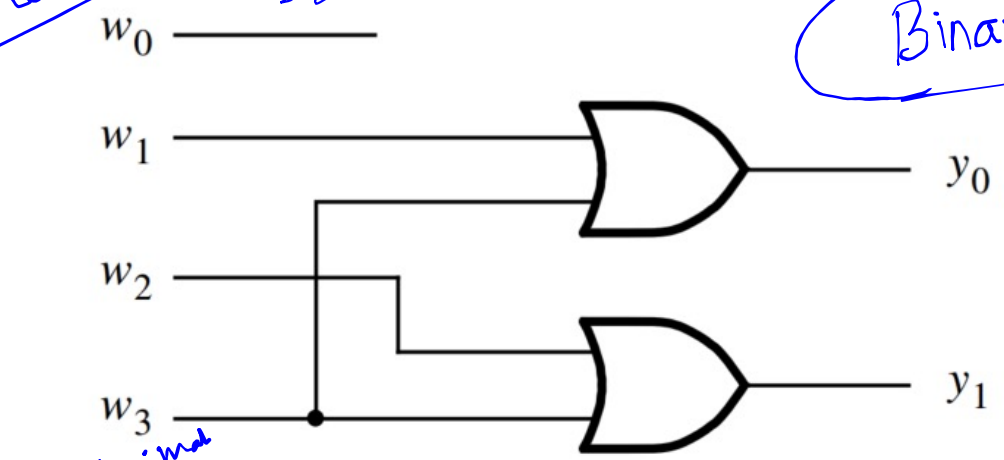
ϕ	0	ϕ	0
1	ϕ	ϕ	ϕ
ϕ	ϕ	ϕ	ϕ
1	ϕ	ϕ	ϕ

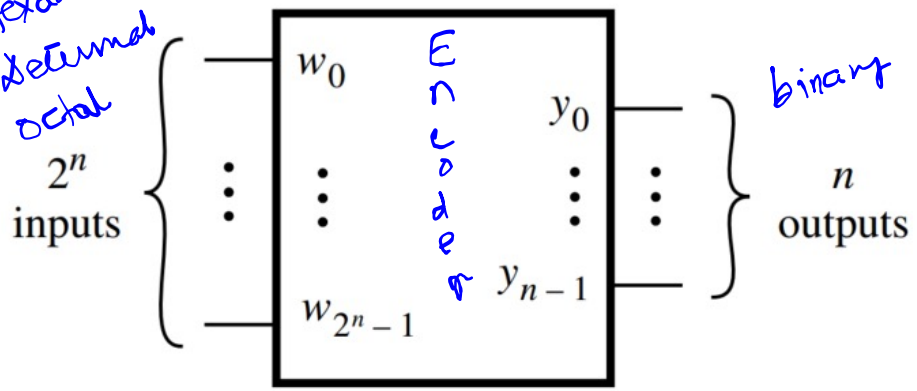
$$y_1 = w_3 + w_2$$

w_1w_0 / w_3w_2

ϕ	0	ϕ	1
0	ϕ	ϕ	ϕ
ϕ	ϕ	ϕ	ϕ
1	ϕ	ϕ	ϕ

$$y_0 = w_3 + w_1$$





8:3 Octal – Binary Encoder:

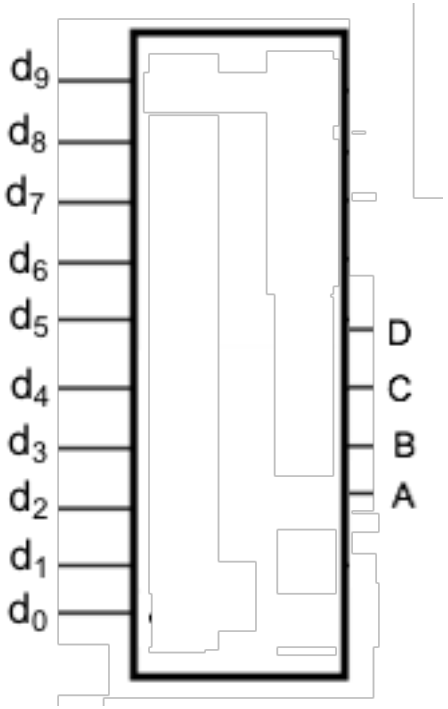
W_7	W_6	W_5	W_4	W_3	W_2	W_1	W_0	Y_2	Y_1	Y_0
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

10:4 Decimal-Binary Encoder:

$$m = \lceil log_2 10 \rceil = \lceil 3.322 \rceil = 4$$

BCD

d_9	d_8	d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0	D	C	B	A
0	0	0	0	0	0	0	0	0	1	0	0	0	0
0	0	0	0	0	0	0	0	1	0	0	0	0	1
0	0	0	0	0	0	0	1	0	0	0	0	1	0
0	0	0	0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	0	1	0	0	0	0	0	1	0	0
0	0	0	0	1	0	0	0	0	0	0	1	0	1
0	0	0	1	0	0	0	0	0	0	0	1	1	0
0	0	1	0	0	0	0	0	0	0	0	1	1	1
0	1	0	0	0	0	0	0	0	0	1	0	0	0
1	0	0	0	0	0	0	0	0	0	1	0	0	1



Encoders (Issues):

$$y_0 = w_1 + w_3$$

$$y_1 = w_2 + w_3$$

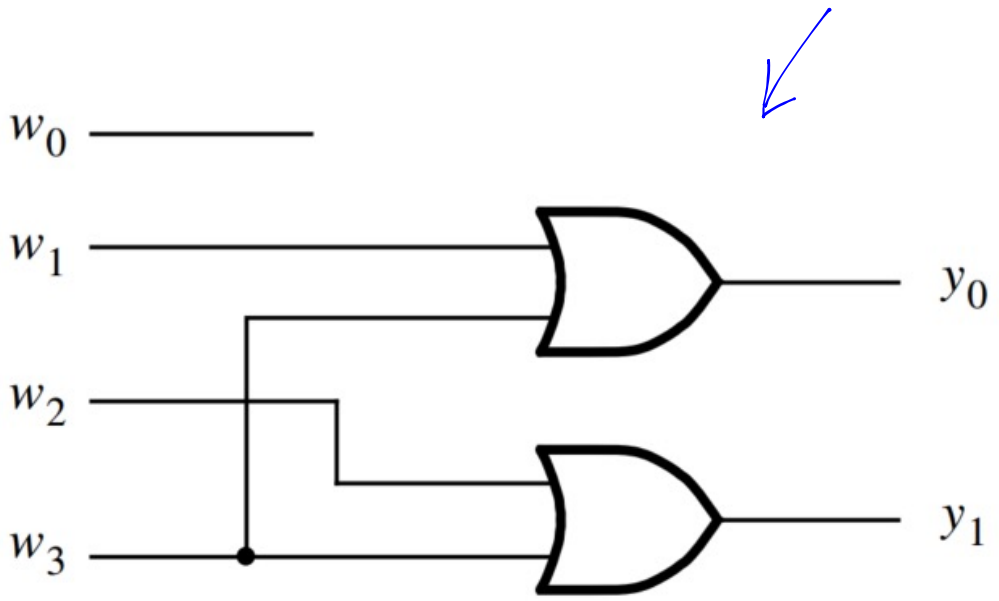
w_3	w_2	w_1	w_0	y_1	y_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1
0	0	0	0	0	0
0	0	1	1	0	1

Do not minimize

That exists

12 dc combs.

Avoid this



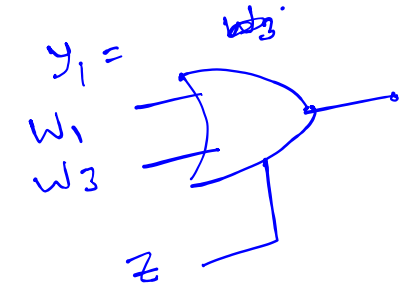
Priority Encoders:

w_3	w_2	w_1	w_0	y_1	y_0	z
0	0	0	0	d	d	0
0	0	0	1	0	0	1
0	0	1	ϕ	0	1	1
0	1	ϕ	ϕ	1	0	1
1	ϕ	ϕ	ϕ	1	1	1

$$z = w_3 + w_2 + w_1 + w_0$$

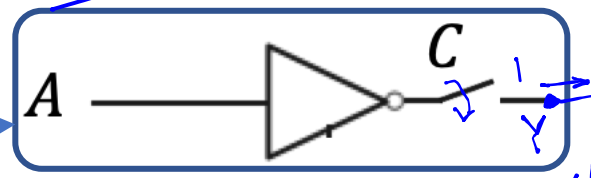
$$y_1 = w_3 + w_2$$

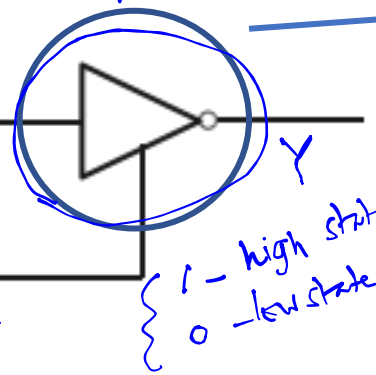
$$y_0 = w_3 + \overline{w_2} w_1$$



H.W: Design an Octal-Binary priority Encoder.

THREE STATE GATE or TRISTATED GATE:





If $C = 1 \rightarrow Y = \bar{A}$

If $C = 0 \rightarrow$ Output in High Impedance state.

- The third state is a *high-impedance* state in which (1) the logic behaves as an open circuit, which means that the output appears to be disconnected, (2) the circuit has no logic significance, and (3) the circuit connected to the output of the three-state gate is not affected by the inputs to the gate.

- The high-impedance state of a three-state gate provides a special feature not available in other gates. Because of this feature, many three-state gate outputs can be connected using wires to form a common line without endangering loading effects.

Three State Buffer: