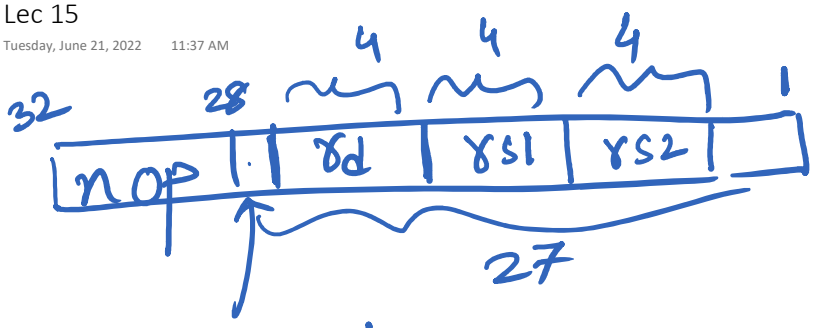
Lec 15

Tuesday, June 21, 2022 11:37 AM



add rd, rs1, (rs2/imm)

Imm. bit

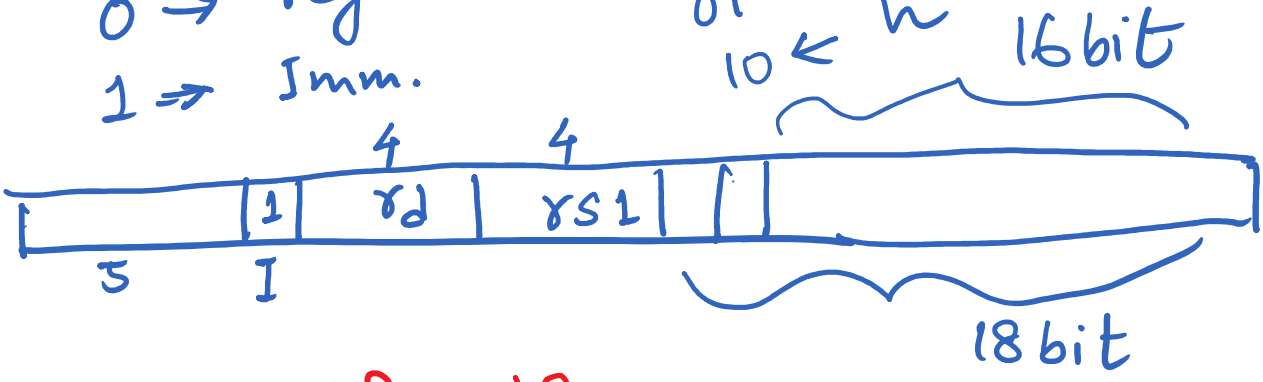
0 → reg.

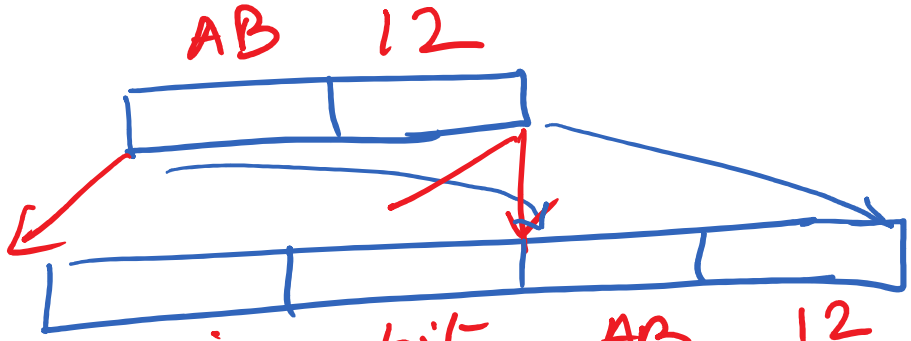
1 → Imm.

00 ← default

01 ← u

10 ← h





00 00 AB 12 ← u

AB 12 00 00 ← h

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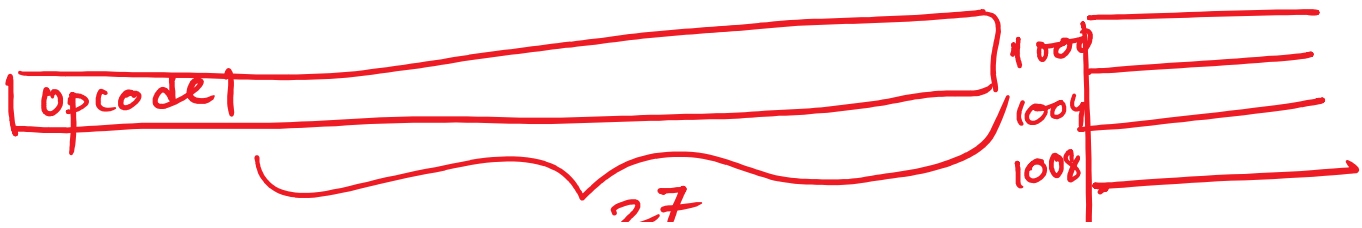
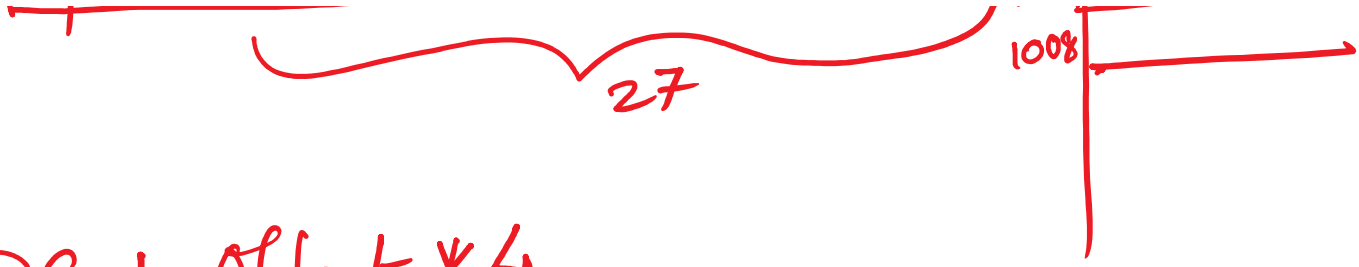
b, beq, bgt, call

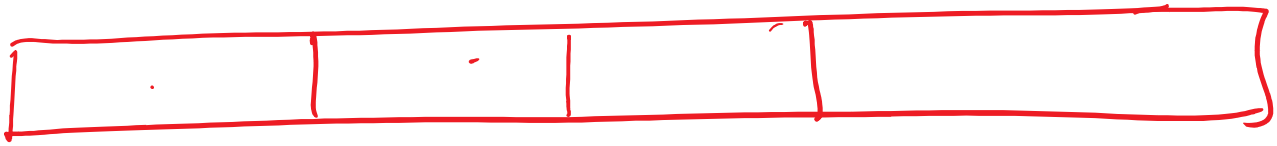




PC + Offset * 4

St [dest] [Source]

St Imm.[rs1], rs2



St. [rd], Imm [rs1]

r1 → ABCD 0000

ABCD1234

ABCD1234

movh r1, ABCD

add r1, r1, 1234