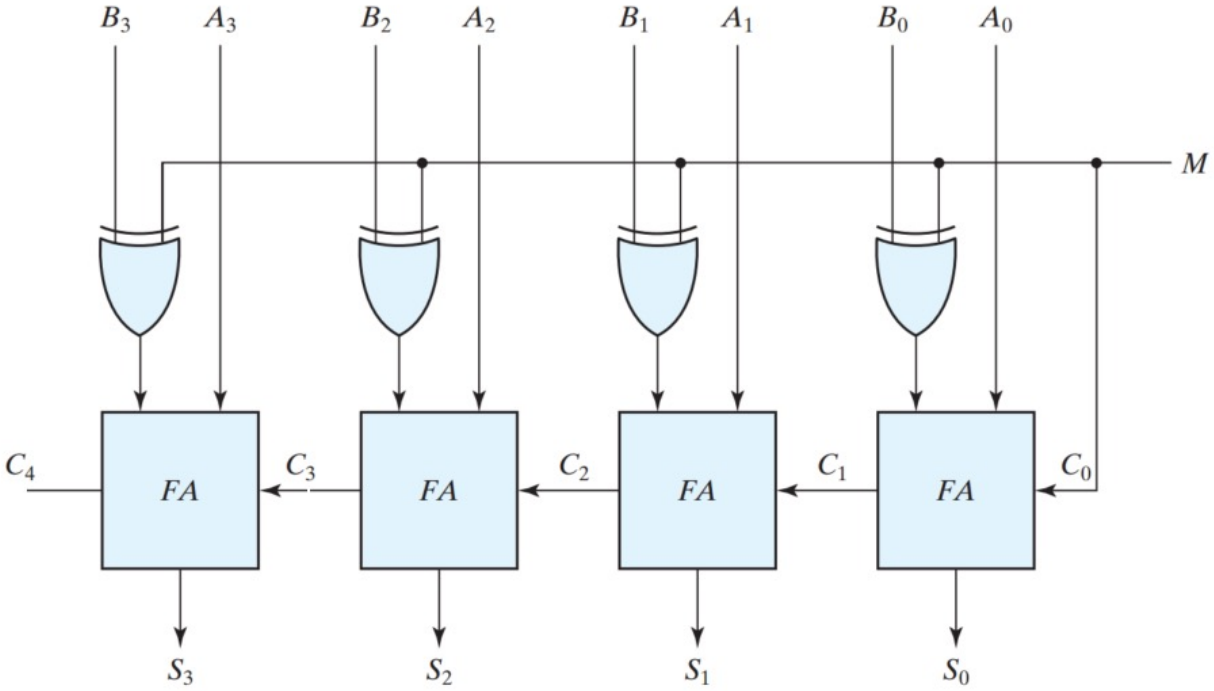
Adder/Subtractor

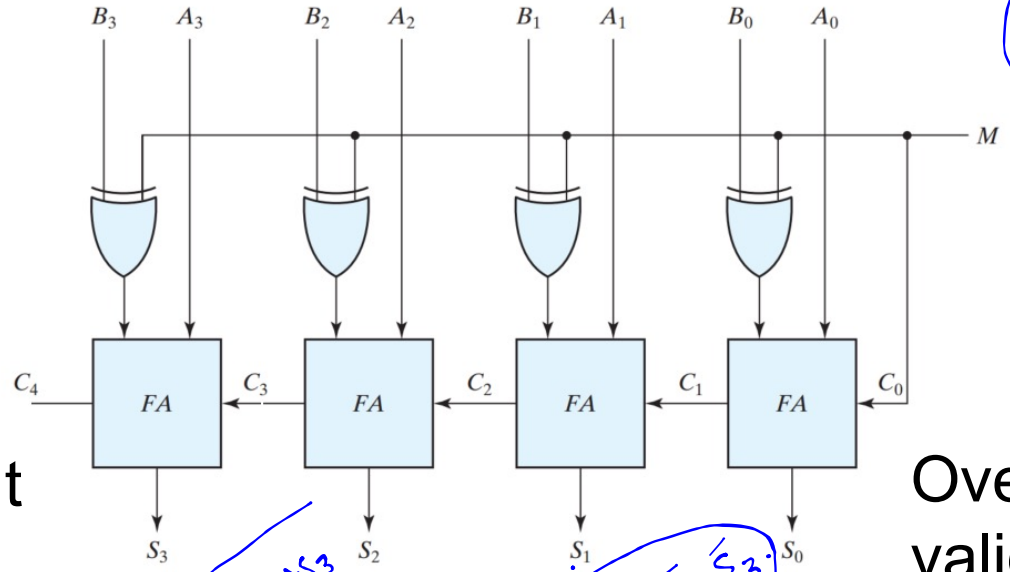
$C_3 = C_4 \rightarrow$ Valid
$C_3 \neq C_4$ invalid



- For adder/subtractor with signed number inputs, we would need to introduce three independent output flags 1) Output flag, V, goes high when the output is invalid, 2) Output flag, F_1, goes high when the sum is negative, and 3) Output flag, F_2, goes high when the sum is zero.

Overflow:

4-bit Signed 2's Complement addition



	1 1 0	
(+7)	0 1 1 1	
+ (−2)	+ 1 1 1 0	
(+5)	1 0 1 0 1	
	$C_3 = 1$	
	$C_4 = 1$	

Overflow exists, the result is valid and positive

	1 1 1	
(−7)	1 0 0 1	
+ (−1)	+ 1 1 1 1	
(−8)	1 1 0 0 0	
$F_1 = S_3$	$C_3 = 1$	
	$C_4 = 1$	

Overflow exists, the result is valid and negative

	0 0 0	
(−7)	1 0 0 1	
+ (+2)	+ 0 0 1 0	
(−5)	1 0 1 1	
$F_1 = S_3$	$C_3 = 0$	
	$C_4 = 0$	

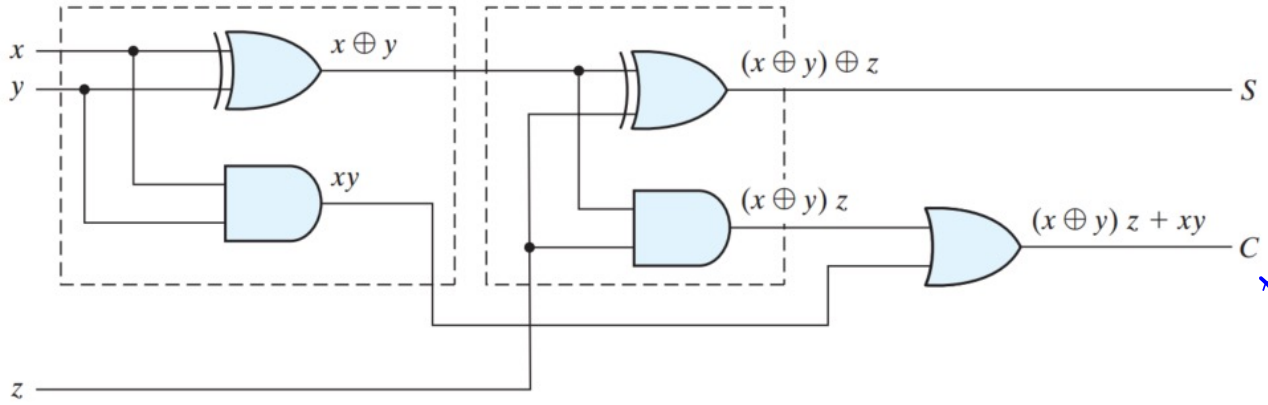
No Overflow exists, the result is valid and negative

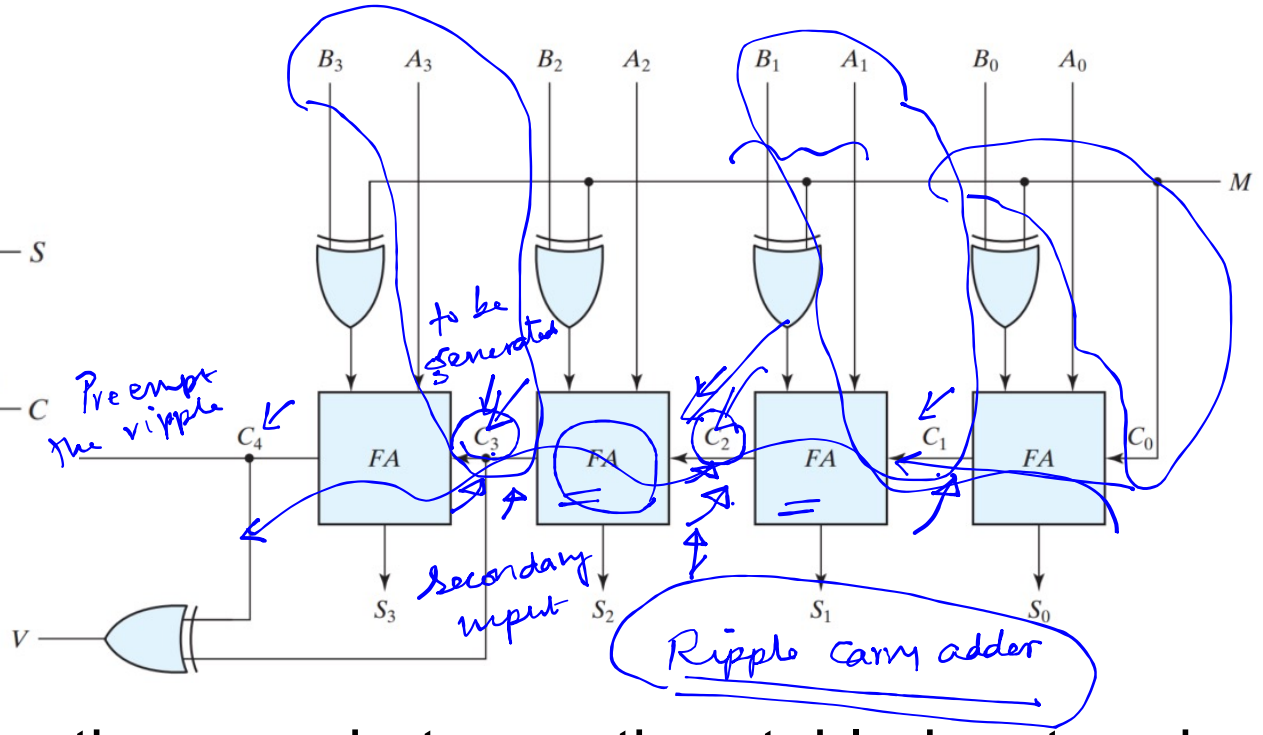
	0 0 0	
(−7)	1 0 0 1	
+ (−2)	+ 1 1 1 0	
(−9)	1 0 1 1 1	
	$C_3 = 0$	
	$C_4 = 1$	

	1 1 0	
(+7)	0 1 1 1	
+ (+2)	+ 0 0 1 0	
(+9)	1 0 0 1	
$V = C_4 \oplus C_3$	$C_3 = 1$	
	$C_4 = 0$	

The results are invalid (C_3 and C_4 are exclusive)

Propagation Delay:





- The longest propagation delay time (the time gap between the stable input and stable output) in an adder is the time it takes the carry to propagate through the full adders.
- Consider inputs A_3 and B_3 that are available as soon as input signals are applied to the adder. However, carry C_3 to this stage does not settle to its final value until C_2 is available from the previous stage. Similarly, C_2 has to wait for C_1 and so on down to C_0.

Carry Lookahead Logic:

P – Propagate and G – Generate.

$$P_i = A_i \oplus B_i \; ; \; G_i = A_i B_i$$

$$S_i = P_i \oplus C_i \; ; \; C_{i+1} = G_i + P_i C_i$$

C_0 = Input carry ; $C_1 = G_0 + P_0 C_0$

$$C_2 = G_1 + P_1 C_1 = G_1 + P_1 (G_0 + P_0 C_0)$$
$$= G_1 + P_1 G_0 + P_1 P_0 C_0$$

$$C_3 = G_2 + P_2 C_2 = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_0$$

Carry Lookahead Logic:

P – Propagate and G – Generate.

$$B_i = B_i^* \oplus M$$

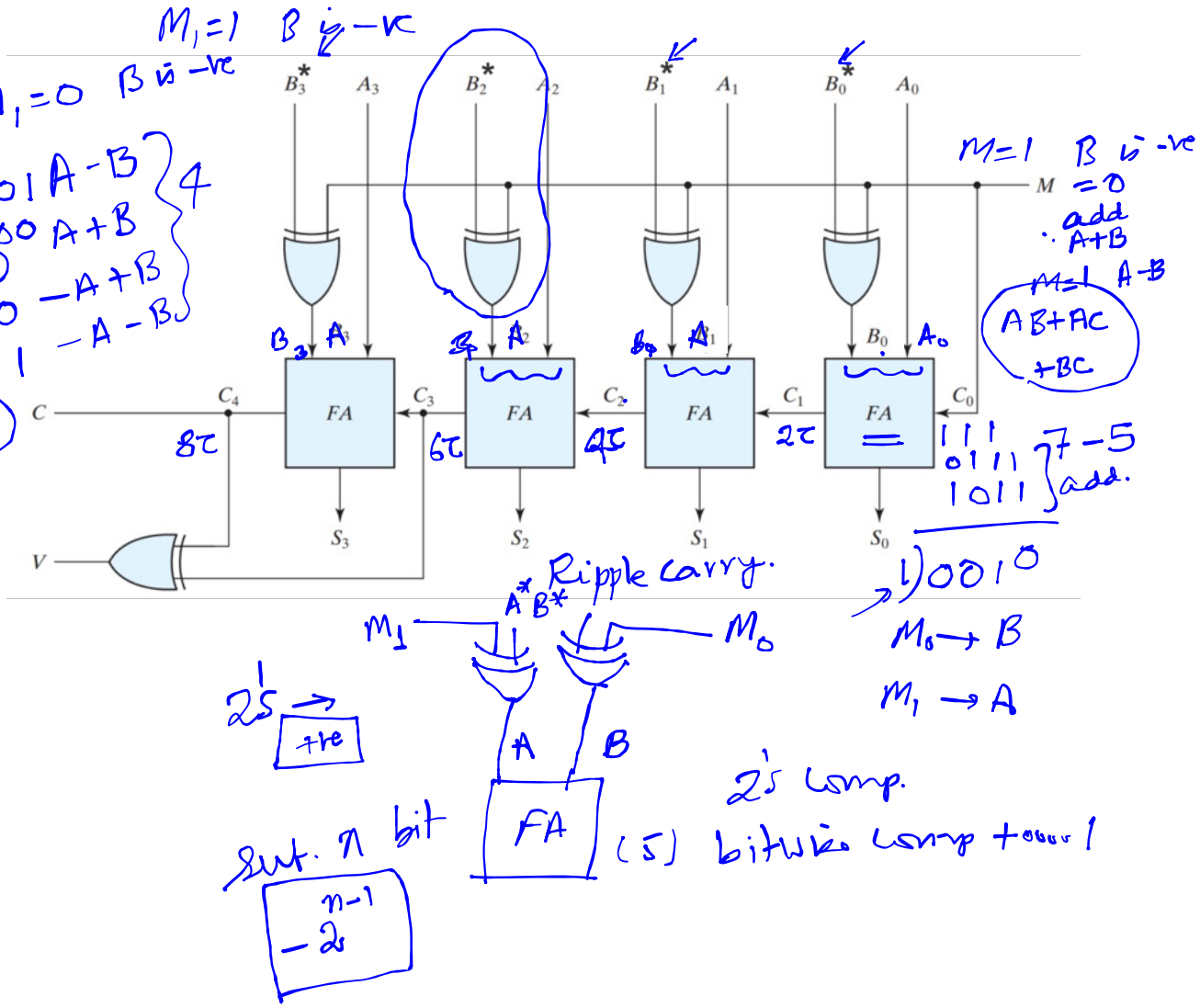
$$P_i = A_i \oplus B_i \; ; \; G_i = A_i B_i$$

$$S_i = P_i \oplus C_i \; ; \; C_{i+1} = G_i + P_i C_i$$

C_0 = Input carry ; $C_1 = G_0 + P_0 C_0$

$$C_2 = G_1 + P_1 C_1 = G_1 + P_1(G_0 + P_0 C_0)$$
$$= G_1 + P_1 G_0 + P_1 P_0 C_0$$

$$C_3 = G_2 + P_2 C_2 = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_0$$



Carry Lookahead Logic:

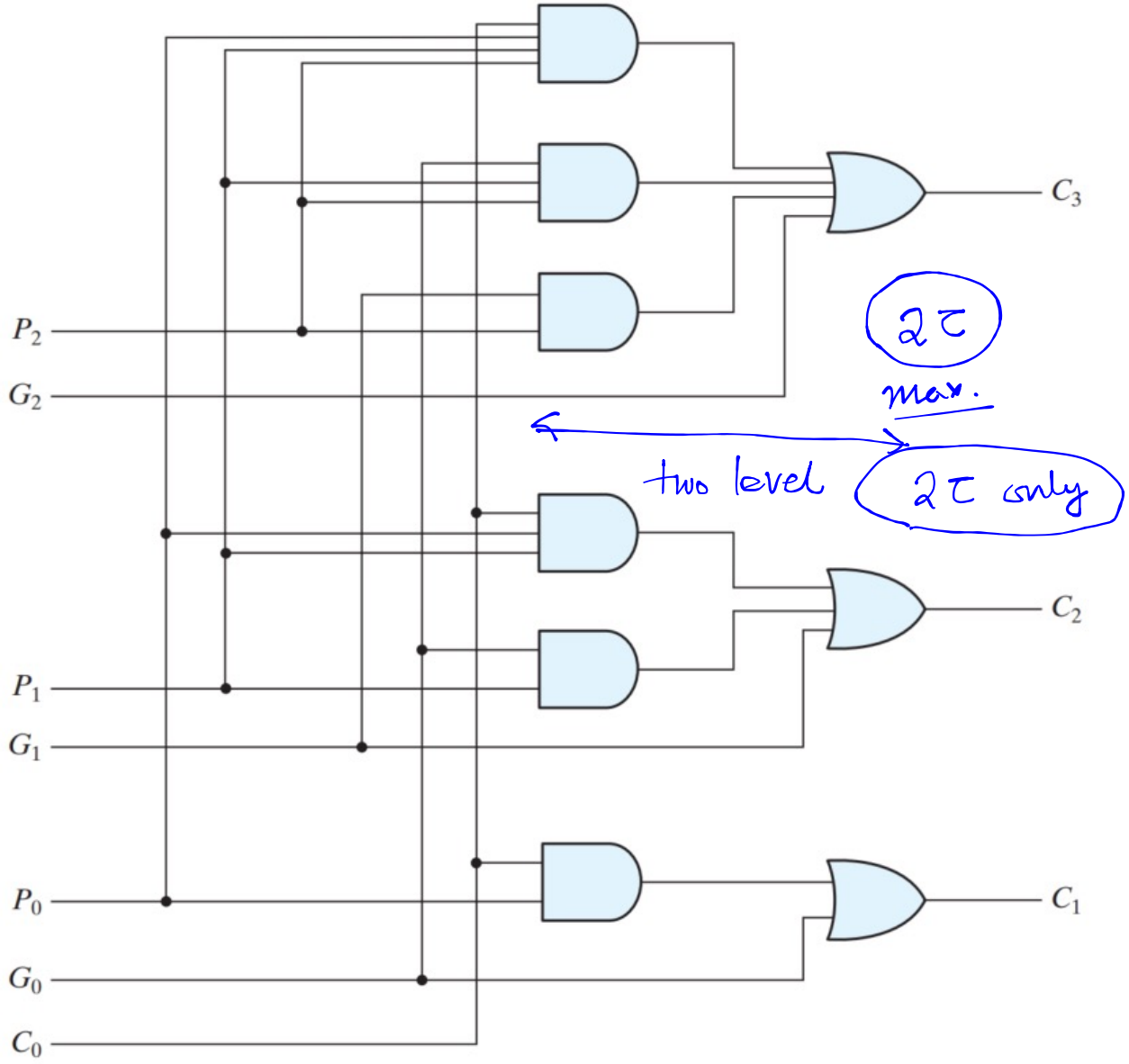
P – Propagate and G – Generate.

$$P_i = A_i \oplus B_i \; ; \; G_i = A_i B_i$$

$$S_i = P_i \oplus C_i \; ; \; \; C_{i+1} = G_i + P_i C_i$$

C_0 = Input carry ; $C_1 = G_0 + P_0 C_0$

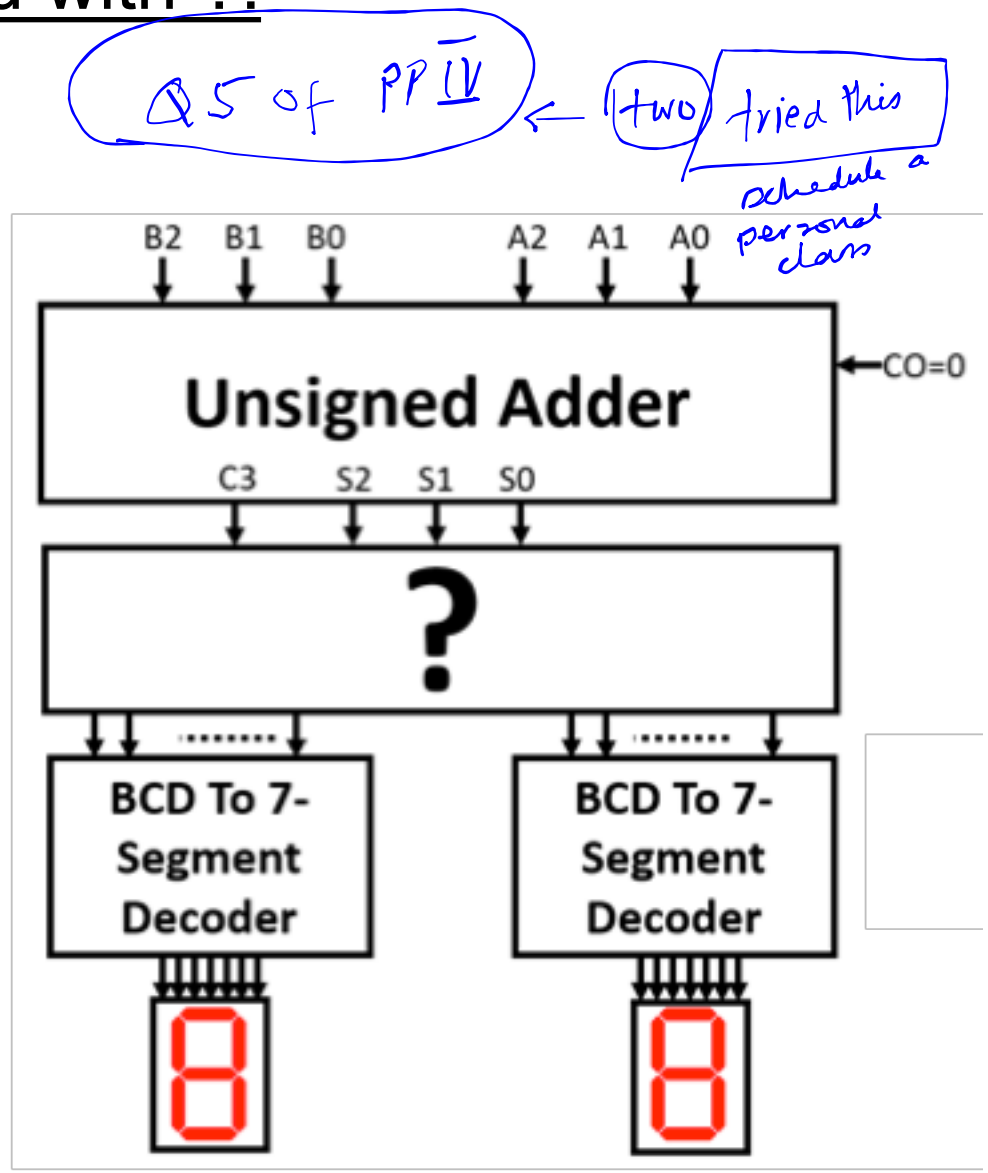
$$C_2 = G_1 + P_1 C_1 = G_1 + P_1 (G_0 + P_0 C_0)$$
$$= G_1 + P_1 G_0 + P_1 P_0 C_0$$



$$C_3 = G_2 + P_2 C_2 = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_0$$

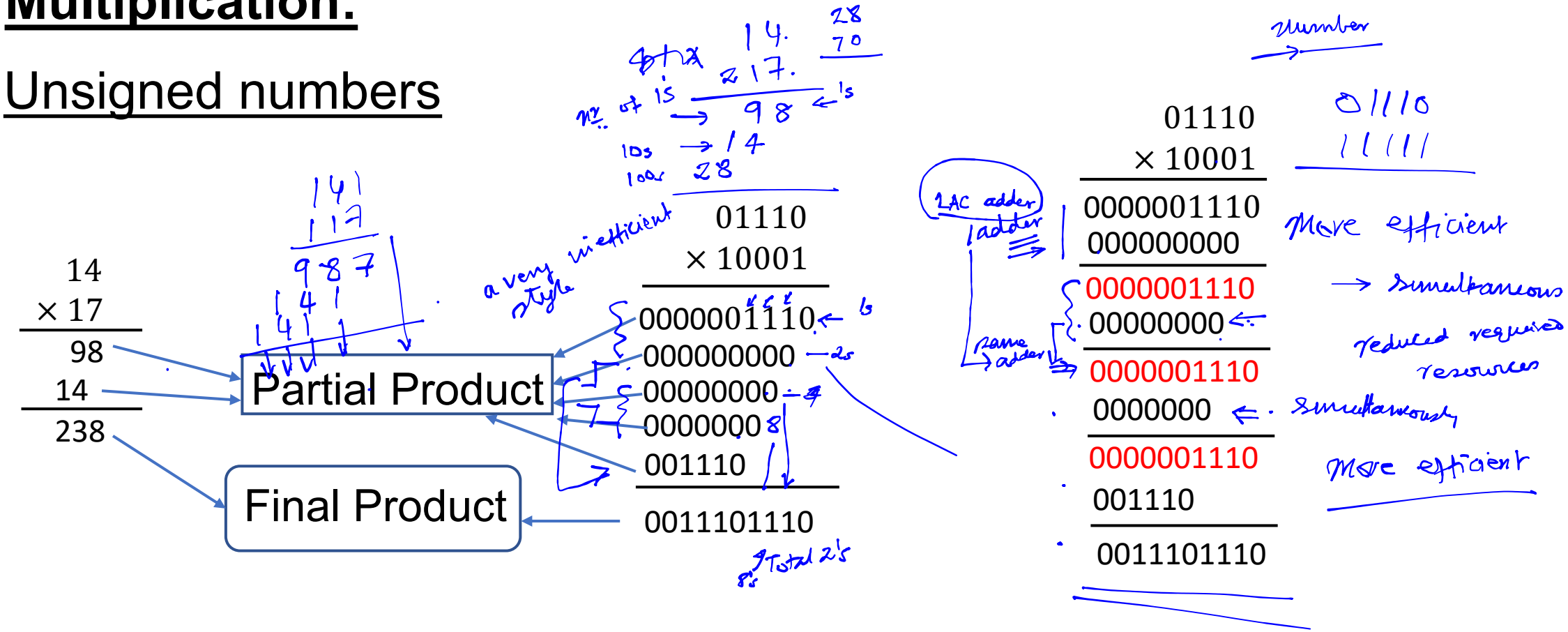
HW --- Identify the Functional Block marked with ?:

Consider the circuit shown where the output of a 3-bit adder needs to be displayed on the two digits of the 7-segment display. For example, if the adder output is 9, then circuit should display 09 where 0 should be displayed on left display and 9 on right display. Existing BCD-to-7 segment decoder works only when input number is between 0 and 9 and we have to use it since it has been hardwired to 7-segment display board. You need to design combinational circuit between Adder and 7-segment decoder (shown as question mark in the Figure) so that the adder output is correctly displayed on the 7-segment display.



Multiplication:

Unsigned numbers



Multiplication of signed 2's compliment numbers:

(one positive and one negative number)

$$\begin{array}{r} +14 \\ \times -15 \\ \hline 70 \\ 14 \\ \hline -210 \end{array}$$

$$\begin{array}{r} 01110 \\ \times 10001 \\ \hline 0000001110 \\ 000000000 \\ 00000000 \\ 0000000 \\ \hline 001110 \end{array}$$

$$\begin{array}{r} 01110 \\ \times 10001 \\ \hline 0000001110 \\ 000000000 \\ \hline 0000001110 \\ 00000000 \\ \hline 0000001110 \\ 0000000 \\ \hline 0000001110 \\ \hline 110010 \\ \hline 1100101110 \end{array}$$

Partial product to be subtracted since multiplier is negative.

2's compliment of the partial product to be subtracted.

Multiplication of signed 2's compliment numbers:

(both negative number)