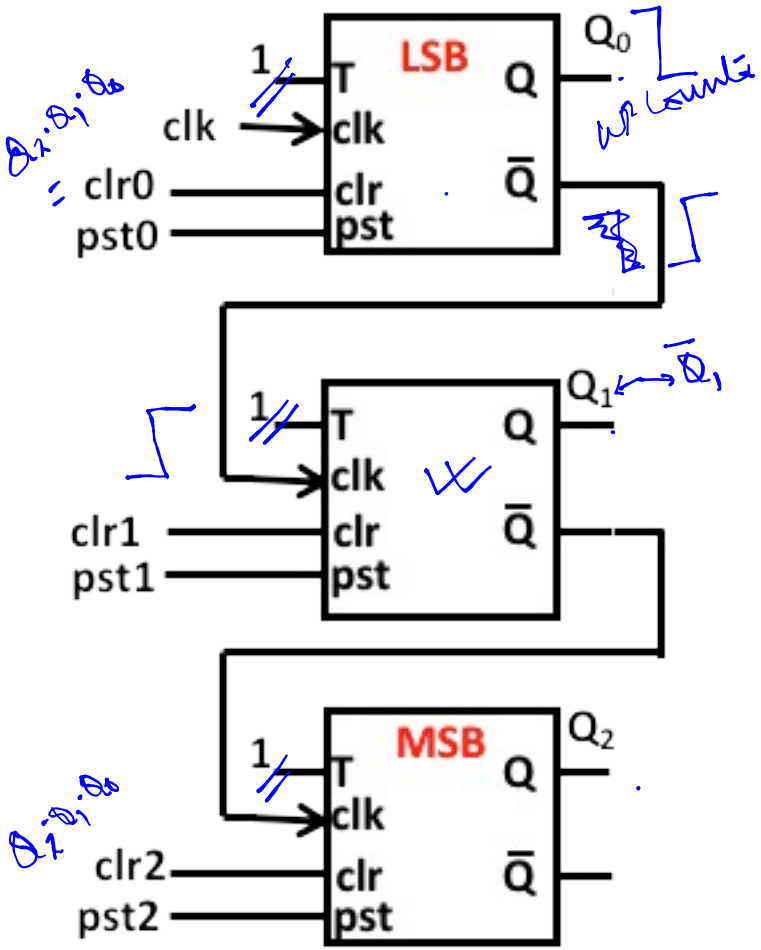
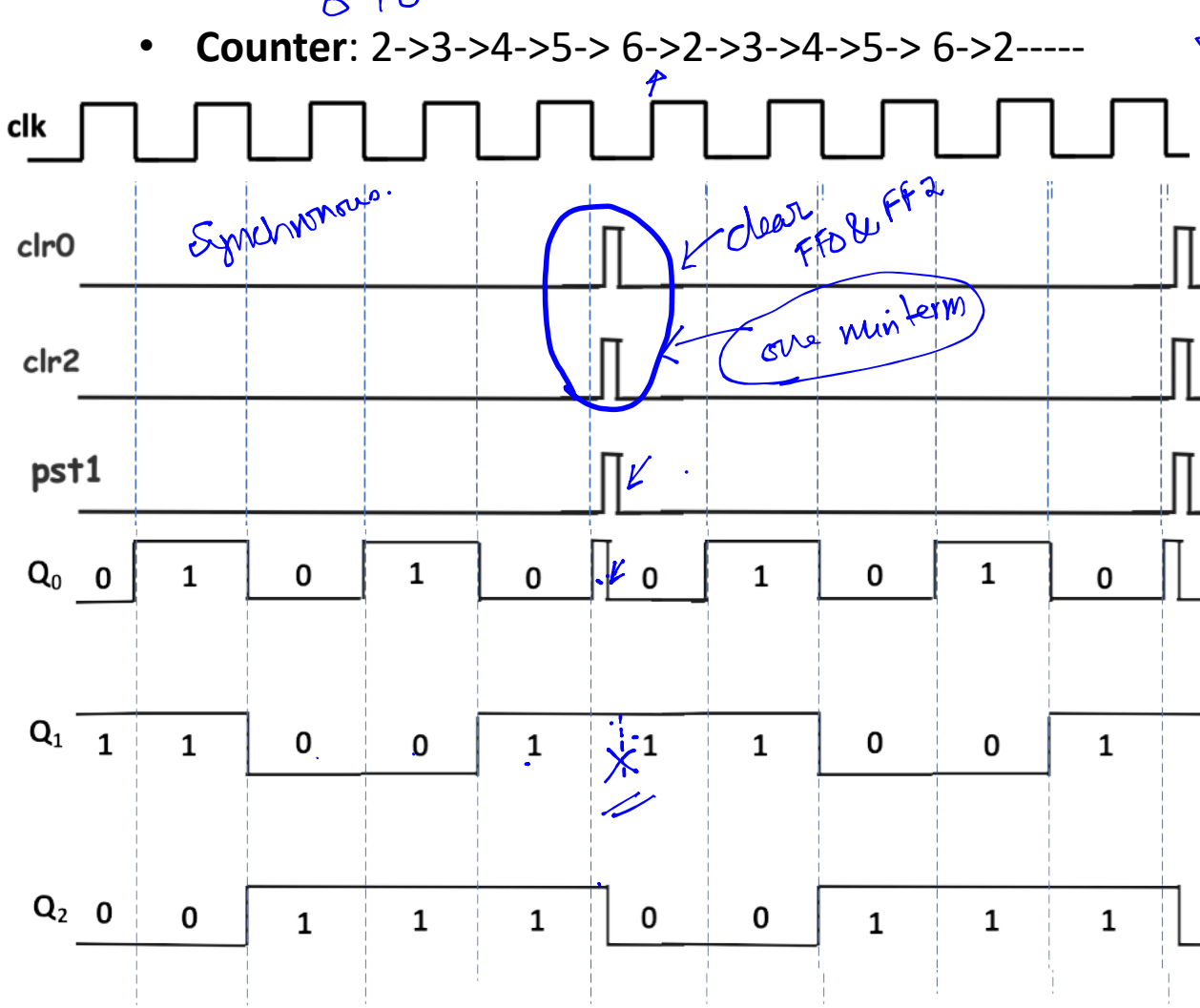
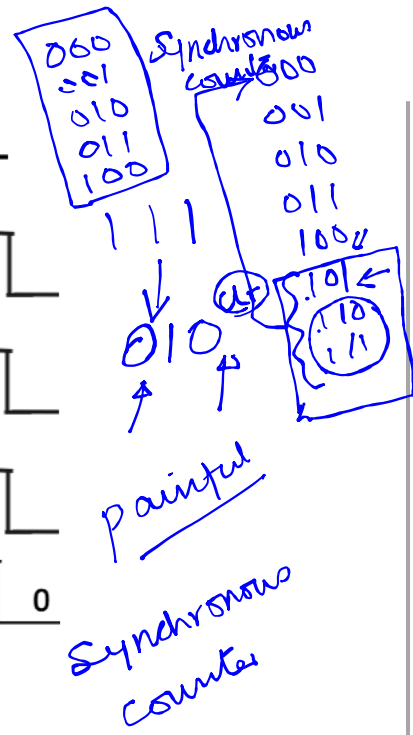
Binary Counter with Clear and Preset:

- **Counter**: 2->3->4->5-> 6->2->3->4->5-> 6->2-----

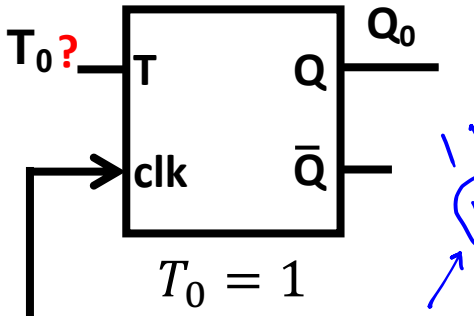




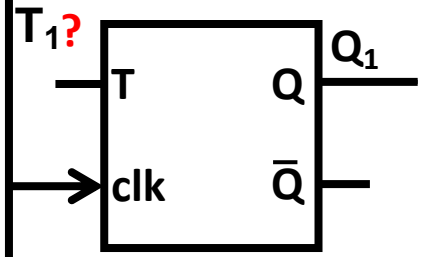


$$clr0 = clr2 = pst1 = Q_2 \cdot Q_1 \cdot Q_0 \;;\; clr1 = pst0 = pst2 = 0$$

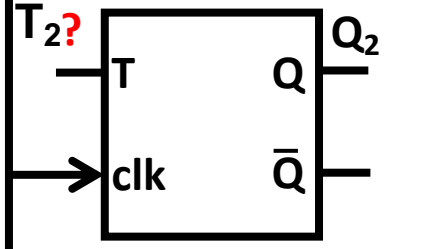
Synchronous Modulo-6 UP Counter using T-FF:



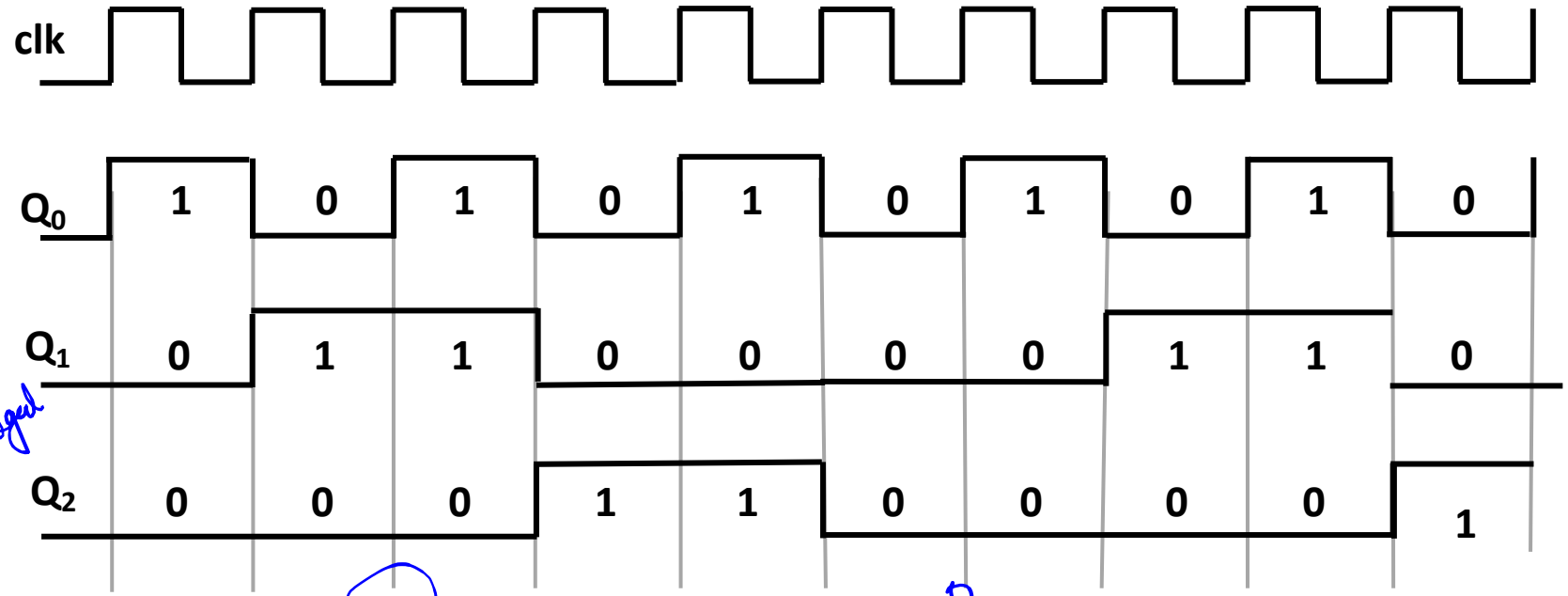
$T_0 = 1$



$T_1 = \overline{Q_2}Q_0$



$T_2 = Q_2Q_0 + Q_1Q_0$



Q_2Q_1 \ Q_0	0	1
00	0	0
01	0	1
11	ϕ	ϕ
10	0	1

T_2

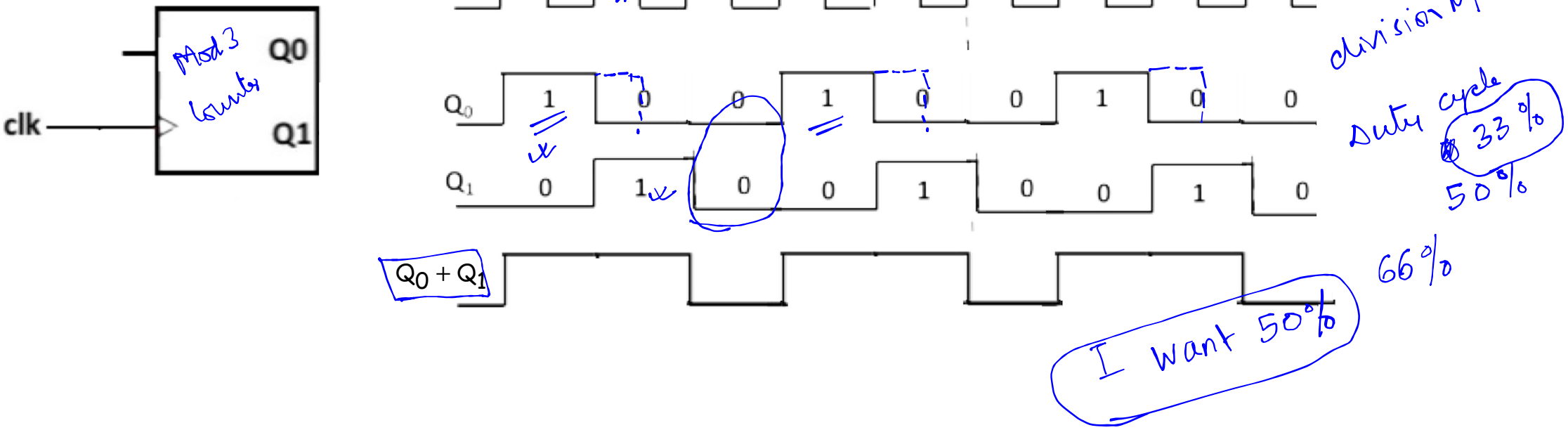
Q_2Q_1 \ Q_0	0	1
00	0	1
01	0	1
11	ϕ	ϕ
10	0	0

T_1

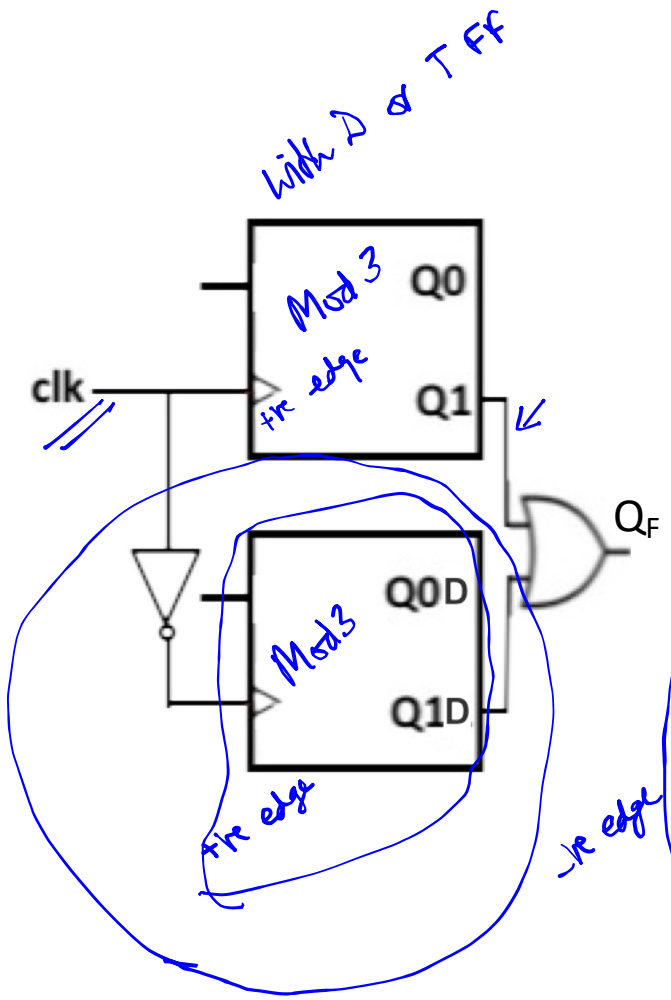
Q_2Q_1 \ Q_0	0	1
00	1	1
01	1	1
11	$\phi=0$	ϕ
10	1	1

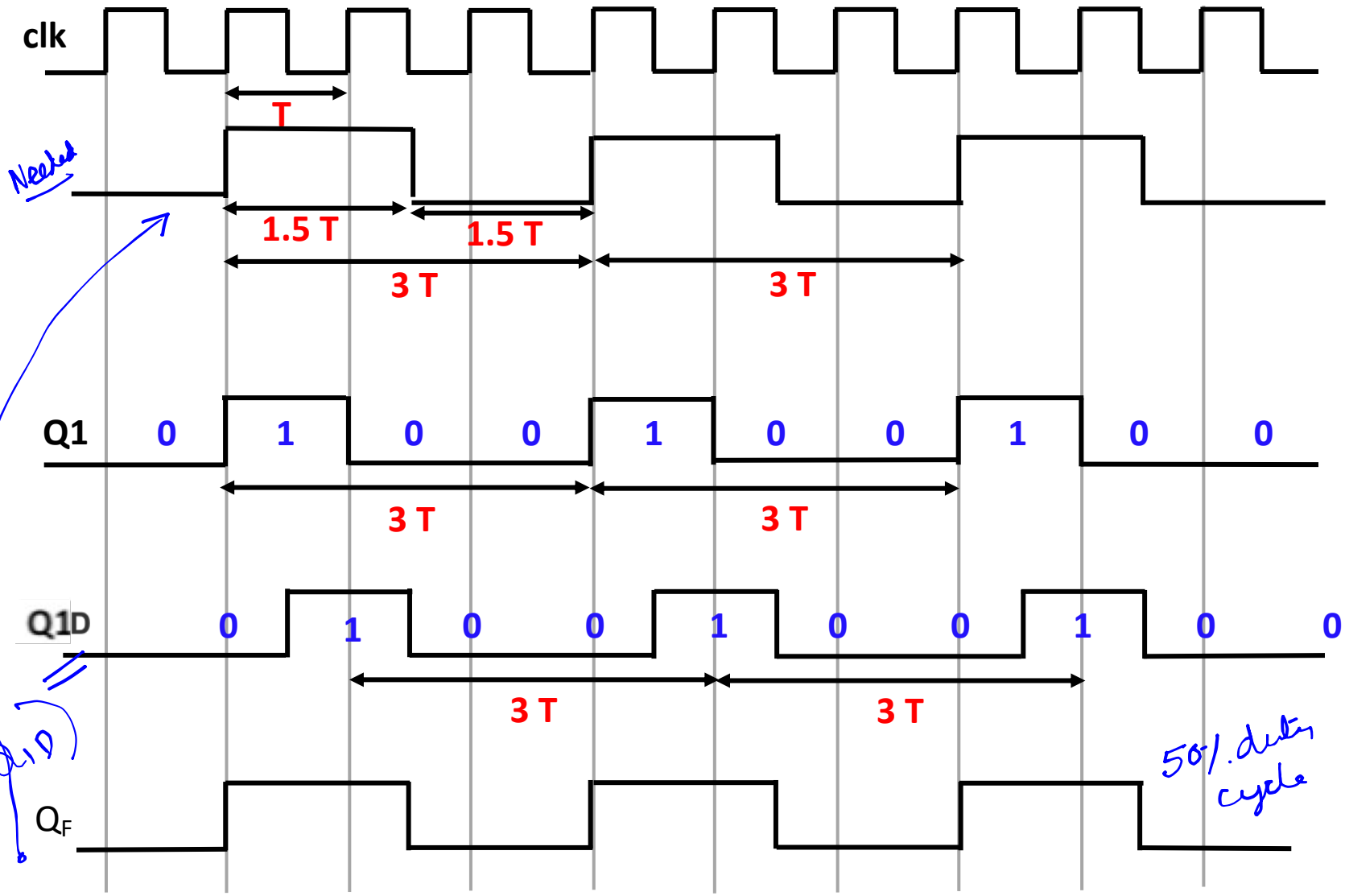
T_0

Frequency Division by 3:

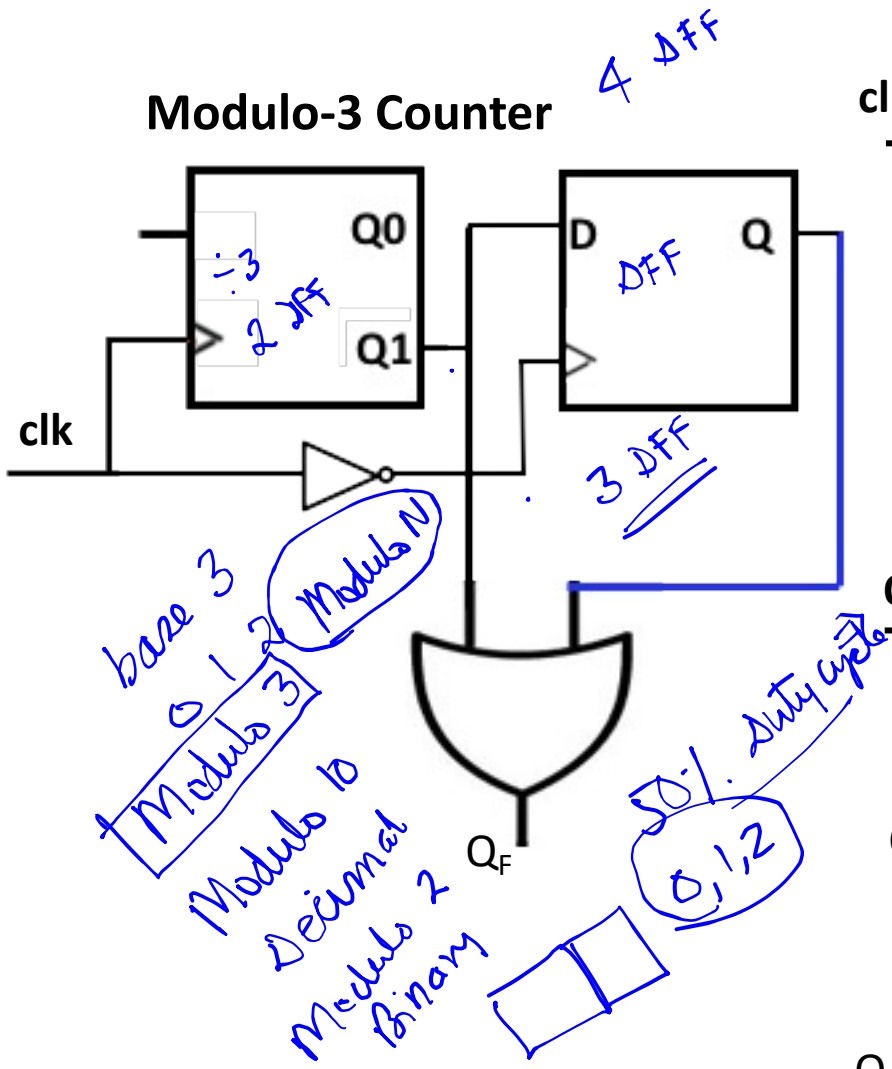


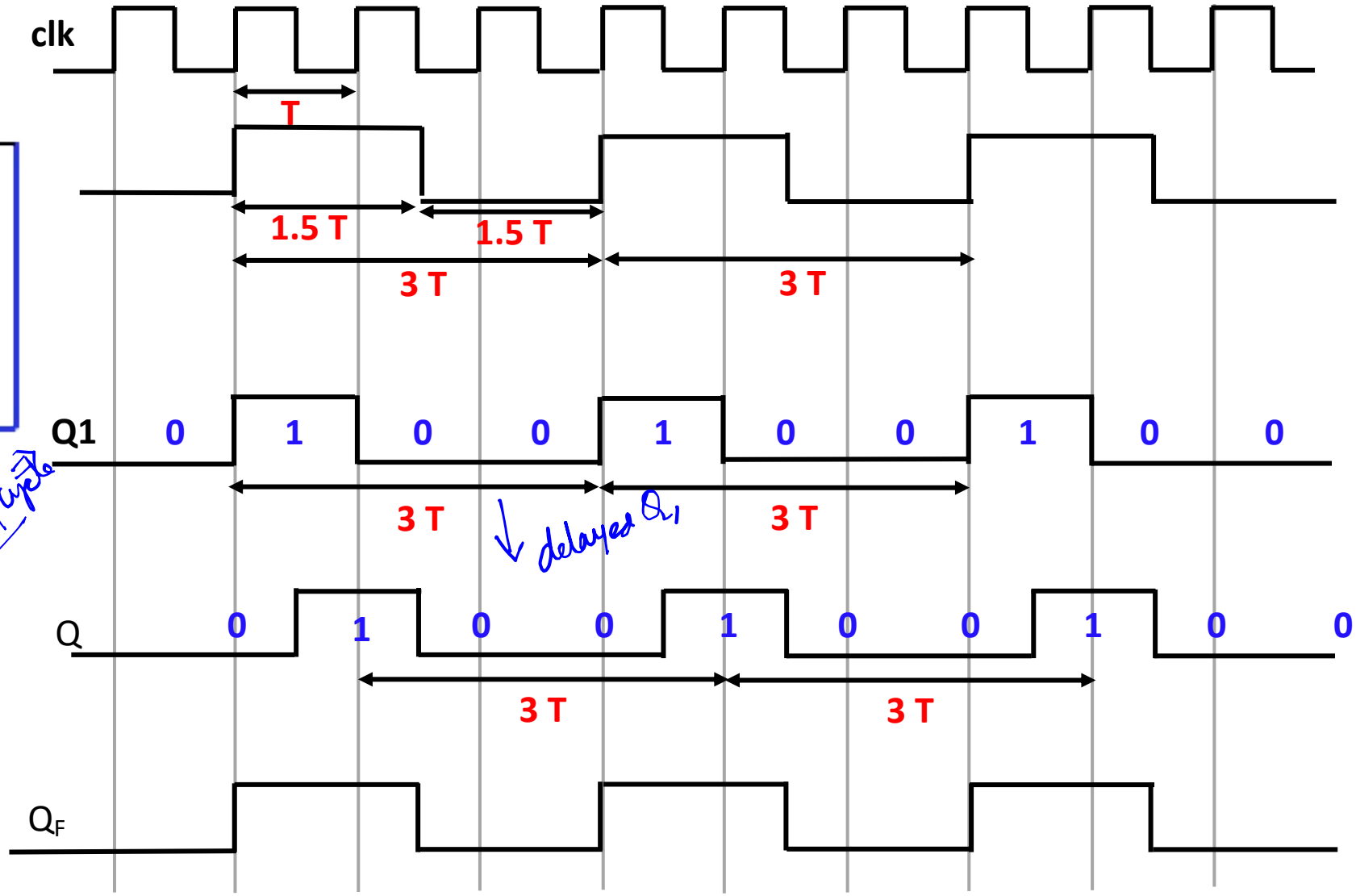
Frequency Division by 3 with Duty Cycle 50%: Alternative



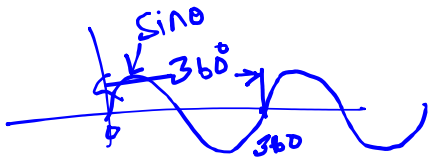


Frequency Division by 3 with Duty Cycle 50%:

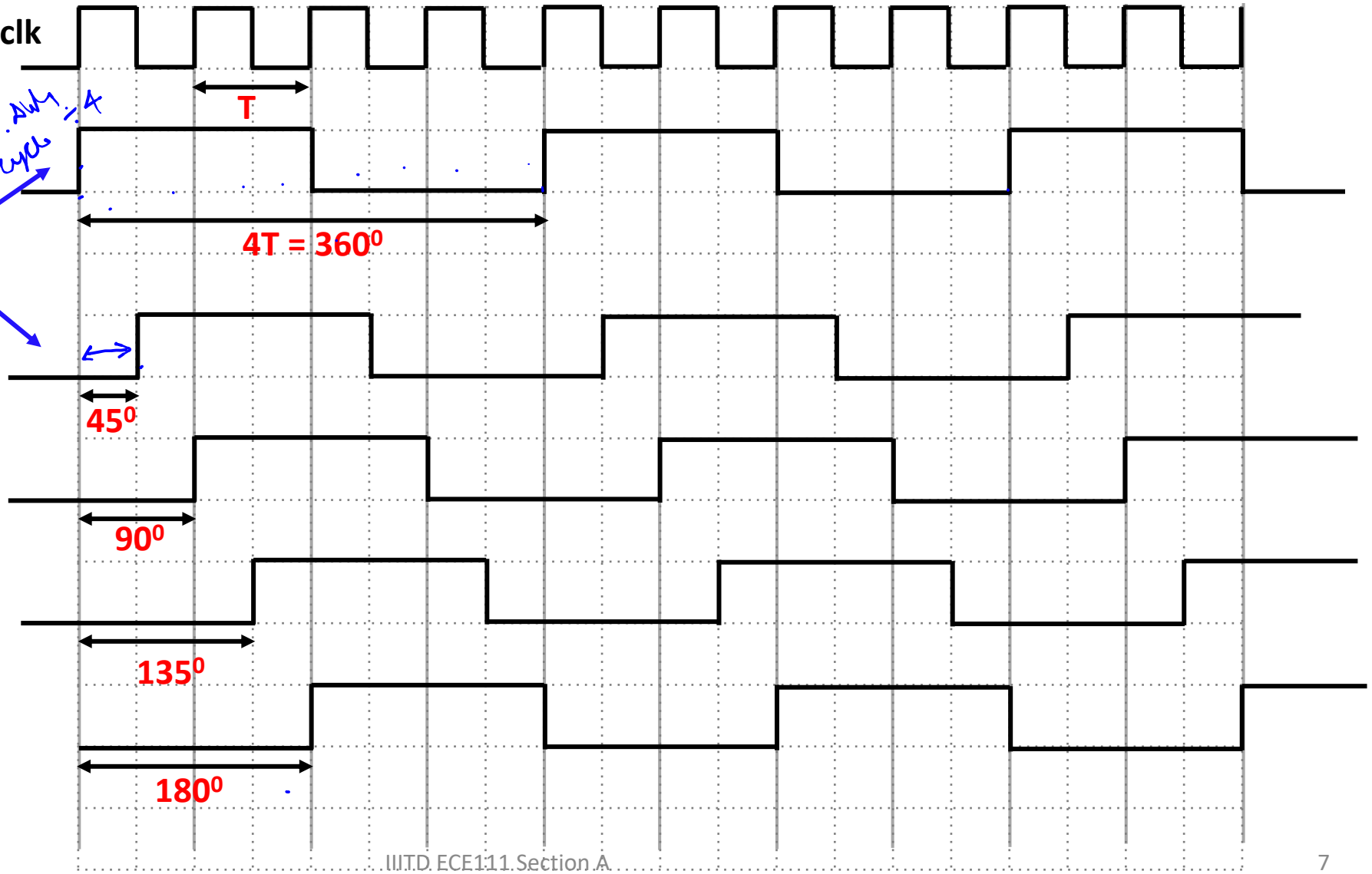




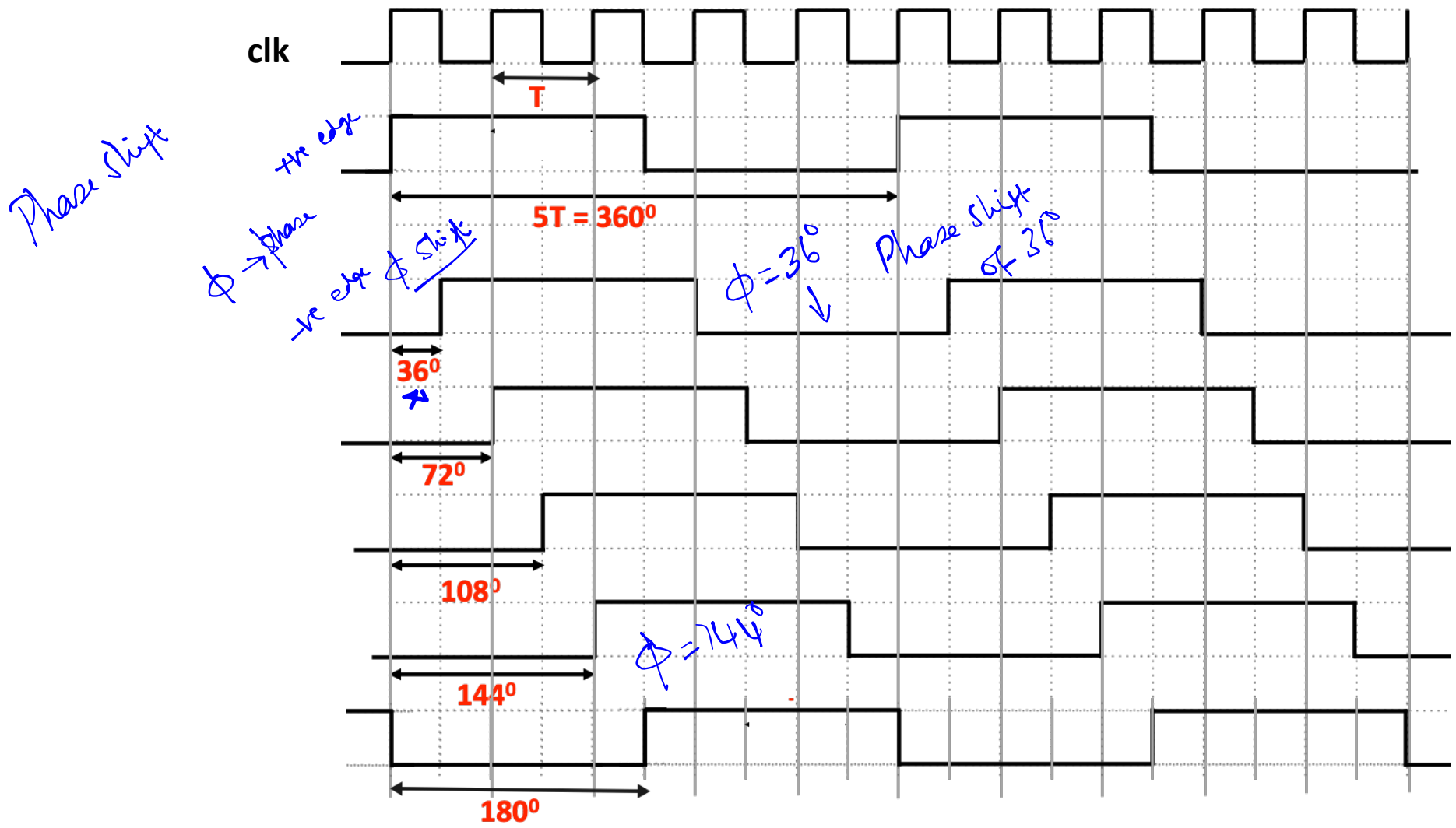
Frequency and Phase:



These two clocks have same frequency, but the phase difference is 45 degree.

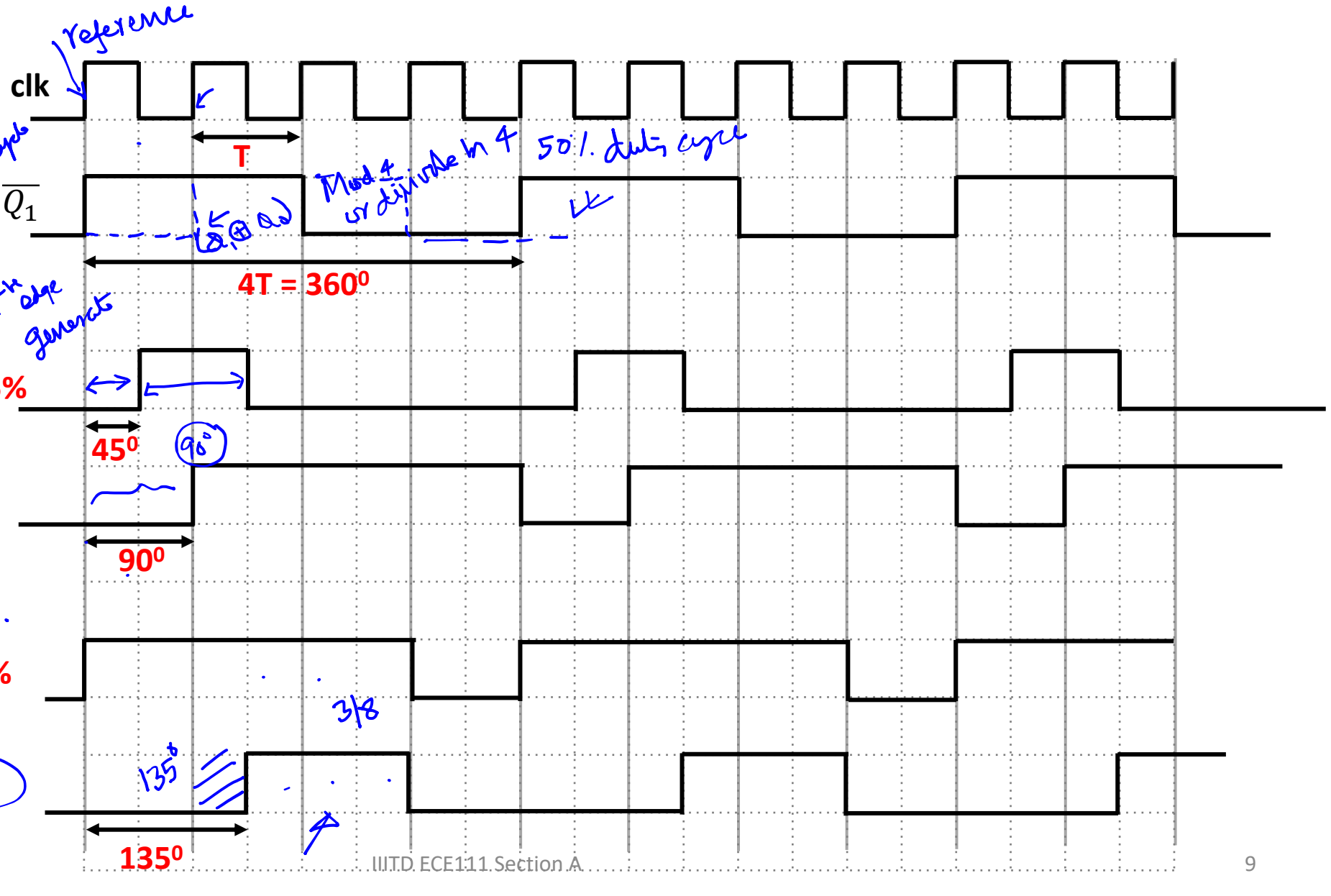


Frequency and Phase:



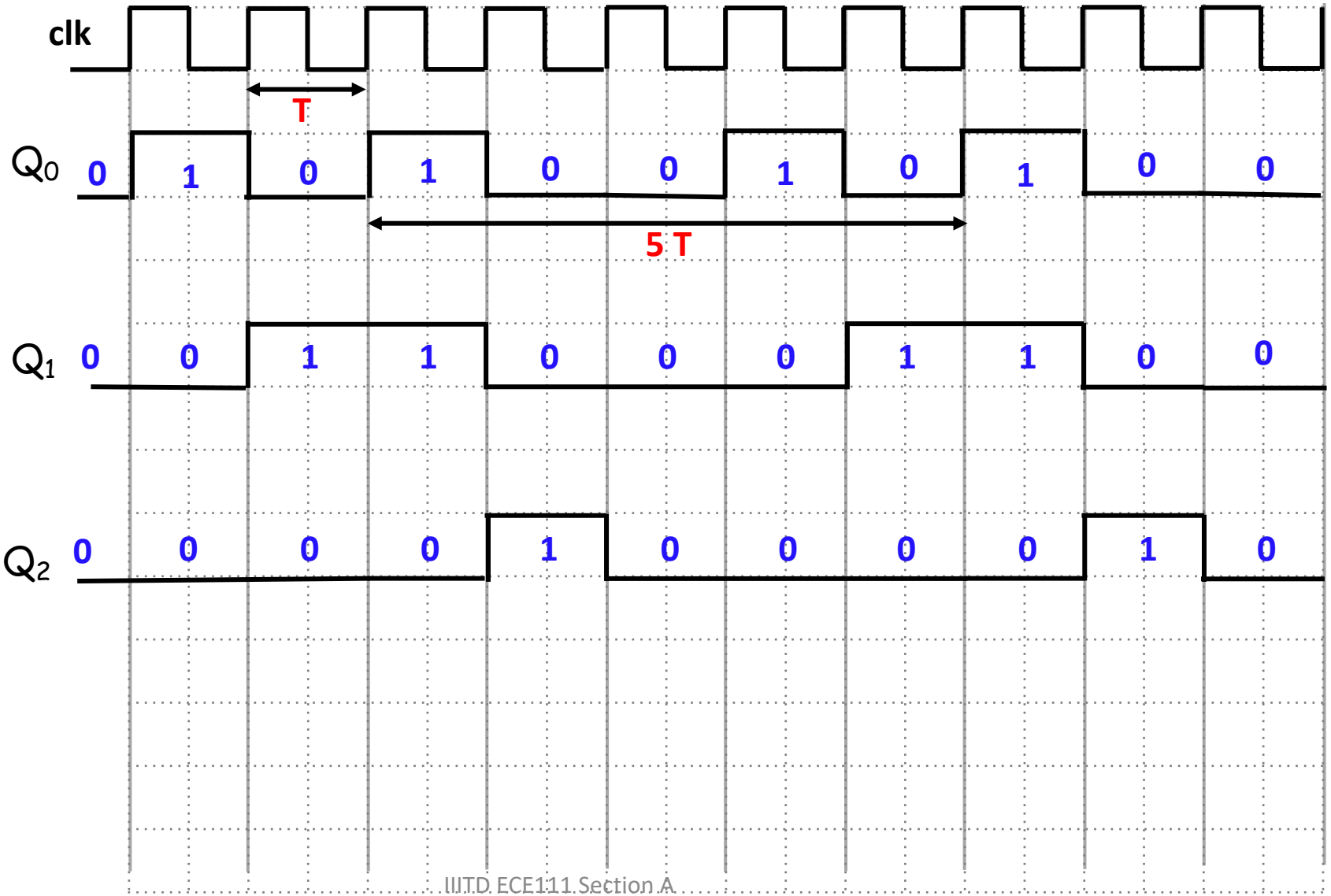
Frequency, Phase and Duty Cycle:

Q_1	Q_0
0	0
0	1
1	0
1	1



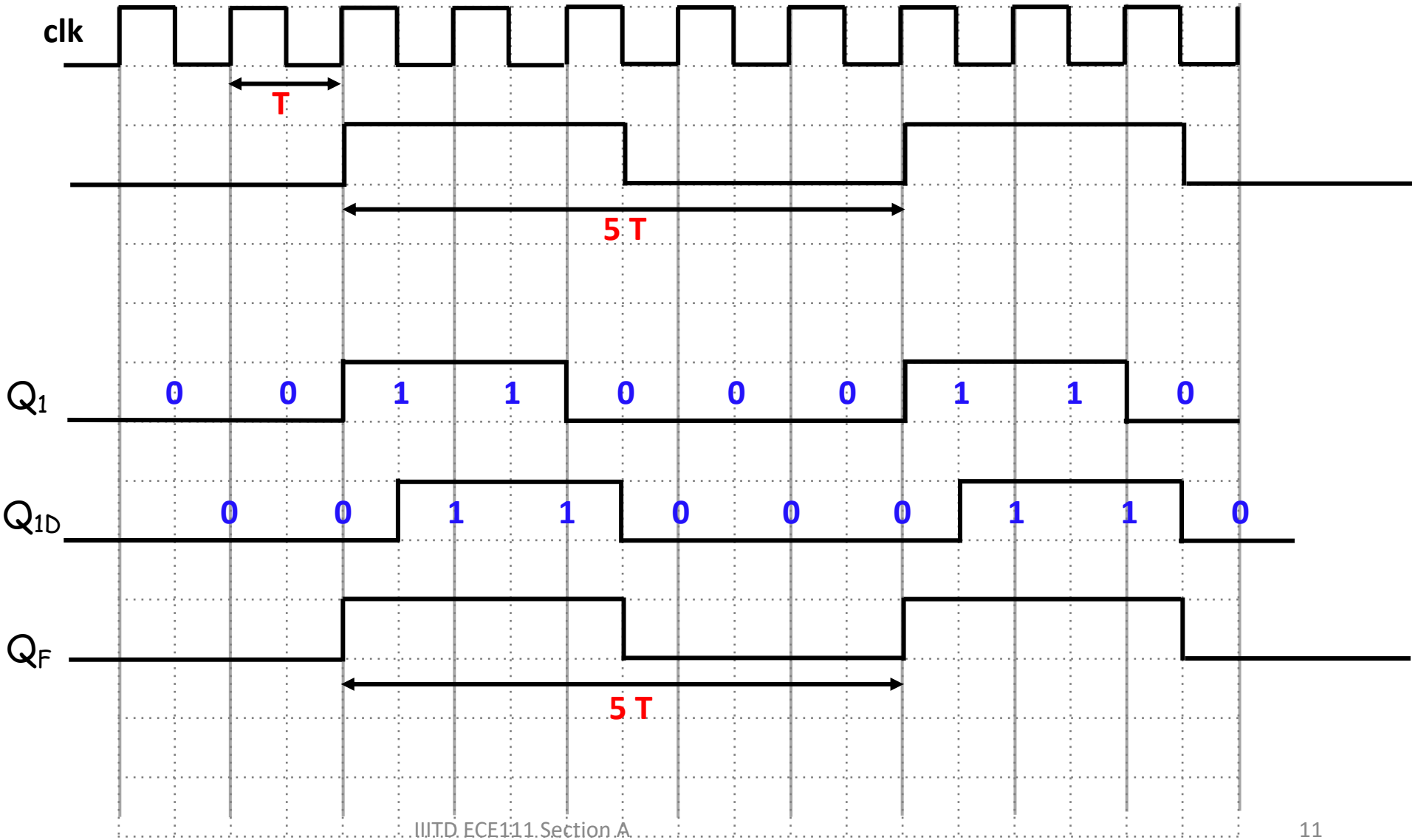
Frequency Division by 5:

Q_2	Q_1	Q_0
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0

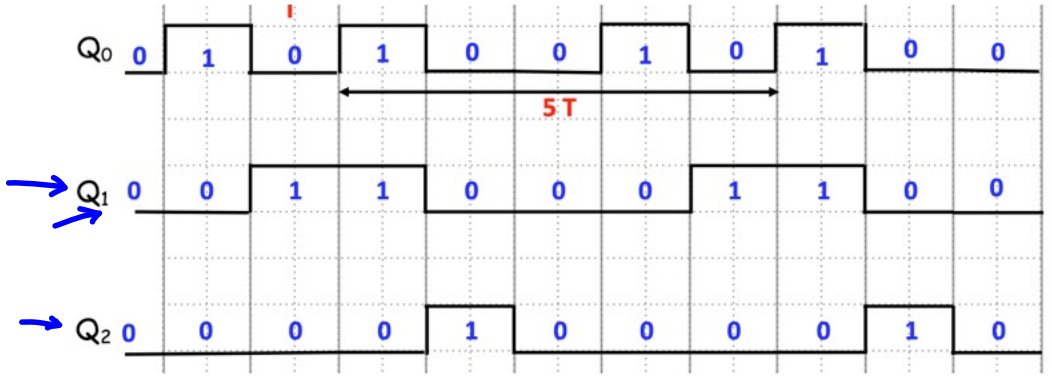


Frequency Division by 5 with 50% duty cycle:

Q_2	Q_1	Q_0
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0



Frequency Division by 5:

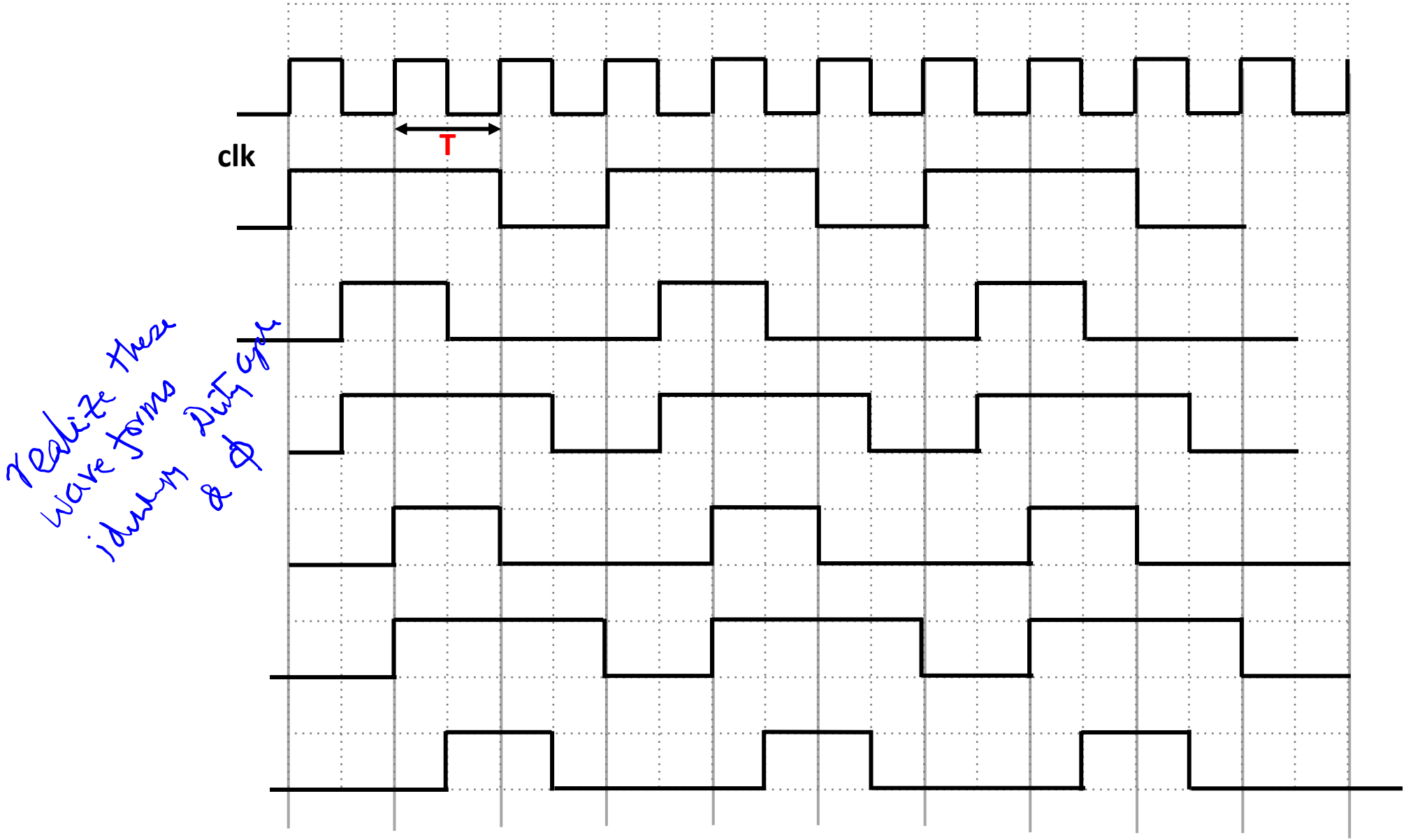


Q_2	Q_1	Q_0
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0

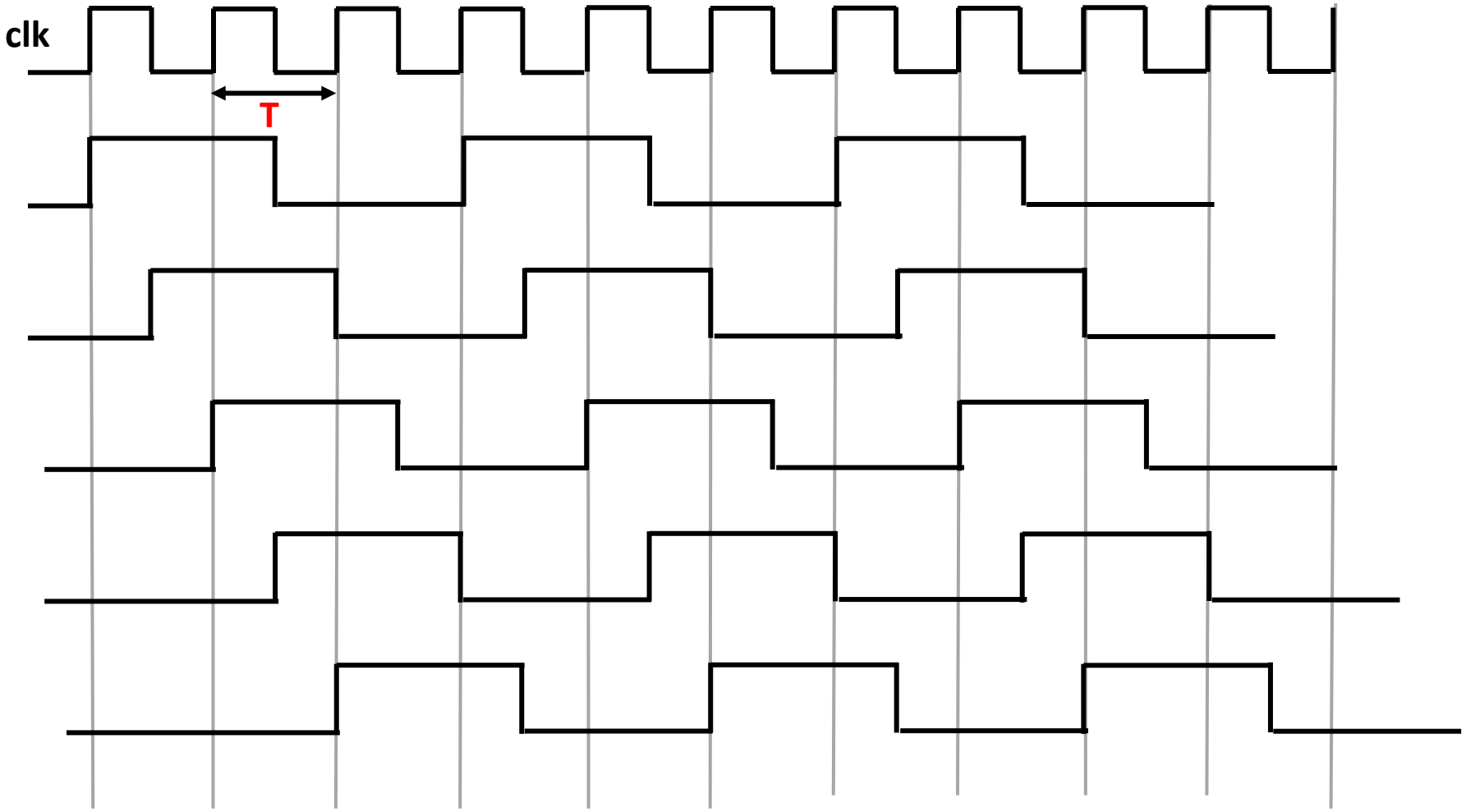
- Desired Duty cycle: 20% -> Use Q_2
- Desired Duty cycle: 40% -> Use Q_1
- Desired Duty cycle: 60% -> Use $Q_1 + Q_2$
- Desired Duty cycle: 50% -> Use Q_1 from +ve edge triggered DFF ORed with Q_1 from –ve edge triggered D-FF
- Desired Duty cycle: 30% -> Use Q_2 from +ve edge triggered DFF ORed with Q_2 from –ve edge triggered D-FF
- Desired Duty cycle: 80% -> Use $Q_2 + Q_1 + Q_0$

- **Minimum Duty cycle: 20% with resolution of 10%**
- **Phase resolution: 360/2T = 36 degree**

Frequency Division by 3 (HW):



Frequency Division by 3 (HW):



Homework

- Design the circuit which divides the input clock by 7 or 9 or 11, you can use the same approach.

Characteristics Equation of Various Flip Flops:

Device Type	Characteristic Equation
S-R Latch	$Q_n = S + \bar{R}Q_{n-1}$
D Latch	$Q_n = D$
Edge-Triggered D flip-flop	$Q_n = D$
D flip-flop with enable	$Q_n = En \cdot D + Q_{n-1}$
Master Slave S-R flip-flop	$Q_n = S + \bar{R}Q_{n-1}$
Master Slave J-K flip-flop	$Q_n = J \cdot \overline{Q_{n-1}} + \bar{K}Q_{n-1}$
Edge Triggered J-K flip-flop	$Q_n = J \cdot \overline{Q_{n-1}} + \bar{K}Q_{n-1}$
T flip-flop	$Q_n = \overline{Q_{n-1}}$
T flip-flop with enable	$Q_n = En \cdot \overline{Q_{n-1}} + \overline{En}Q_{n-1}$

Next week class on Monday & Wednesday 2:30 to 10:30 Free on Thursday

I will be available on the link for office hour on Thursday in class time