VHDL CODES

29 February 2024 01:31 AM

```
library ieee;
use ieee.std_logic_1164.all;

entity b2g_code is
port (b : in std_logic_vector(3 downto 0);
     g : out std_logic_vector(3 downto 0));
end b2g_code;

architecture b2g_arch of b2g_code is
 begin
g(3) <= b(3);
g(2) <= b(3) xor b(2);
g(1) <= b(2) xor b(1);
g(0) <= b(1) xor b(0);
 end b2g_arch;
```

```
library ieee;
use ieee.std_logic_1164.all;

entity g2b_code is
port (g : in std_logic_vector(3 downto 0);
     b : out std_logic_vector(3 downto 0));
end g2b_code;

architecture g2b_arch of g2b_code is
 begin
   b(3) <= g(3);
   b(2) <= g(3) xor g(2);
   b(1) <= g(3) xor g(2) xor g(1);
   b(0) <= g(3) xor g(2) xor g(1) xor g(0);
end g2b_arch;
```

VHDL code for full adder using the structural method

```
 library IEEE;
 use IEEE.STD_LOGIC_1164.ALL;
 use IEEE.STD_LOGIC_ARITH.ALL;
 use IEEE.STD_LOGIC_UNSIGNED.ALL;

 entity HA is
 Port ( A,B : in  STD_LOGIC;
        S,C : out  STD_LOGIC);
 end HA;

 architecture dataflow of HA is

 begin

 S <= A XOR B;
 C <= A AND B;

 end dataflow;
```

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity ORGATE is
     Port ( X,Y : in STD_LOGIC;
               Z : out STD_LOGIC);
end ORGATE;

architecture dataflow of ORGATE is

begin


Z <= X OR Y;
```

```
Z <= X OR Y;

end dataflow;
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity FAdder is
Port ( FA, FB, FC : in STD_LOGIC;
          FS, FCA : out STD_LOGIC);
end FAdder;

architecture structural of FAdder is

component HA is
Port ( A,B : in STD_LOGIC;
       S,C : out STD_LOGIC);
end component;
component ORGATE is
Port ( X,Y: in STD_LOGIC;
         Z: out STD_LOGIC);
end component;

SIGNAL S0,S1,S2:STD_LOGIC;

begin

U1:HA PORT MAP(A=>FA,B=>FB,S=>S0,C=>S1);
U2:HA PORT MAP(A=>S0,B=>FC,S=>FS,C=>S2);
U3:ORGATE PORT MAP(X=>S2,Y=>S1,Z=>FCA);

end structural;
```