

EXP I: Familiarize with lab instruments

In partnership with Aditya Pratap Singh (22020)

Objectives

1. Introduction to lab instruments
2. Running a LT Spice simulation

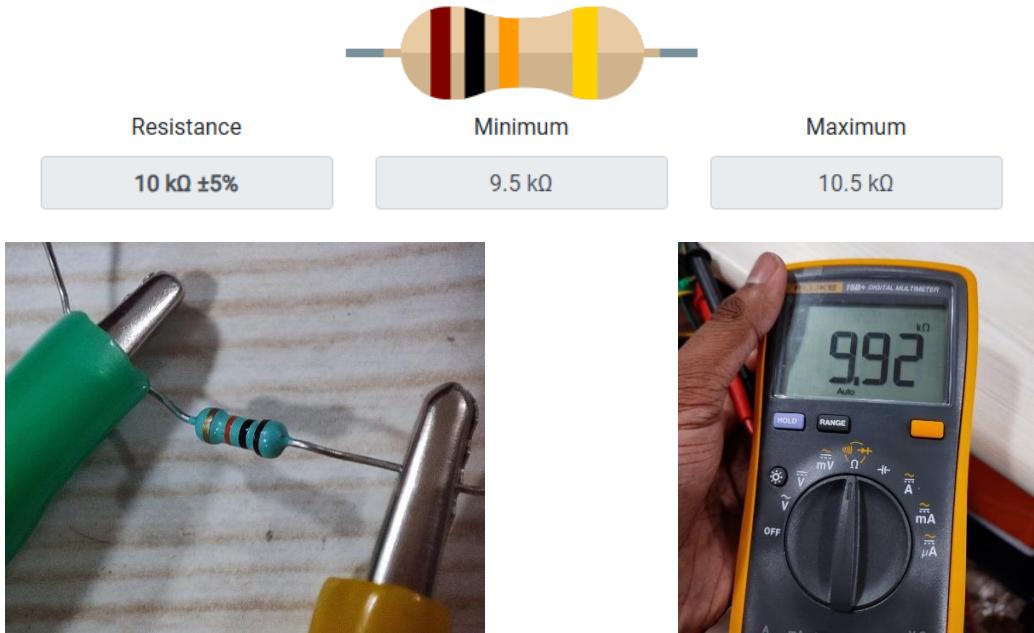
Introduction to lab instruments

Instruments studied

1. Multimeter
2. Oscilloscope
3. Function generator
4. Small resistors
5. DC power supply

Determining the resistance of given resistor

We determined the resistance of the given resistor using a multimeter. Based on the resistor's colour code, the expected resistance was approximately $10\text{k}\Omega$.



To measure the resistance, we set the multimeter dial to the resistance measurement mode and connected the test leads to the COM and Ω terminals. The multimeter's functionality was confirmed, as the measured resistance closely matched the calculated value, falling within the acceptable error range. This verified the accuracy of the multimeter in measuring resistance.

DC Power Supply and Voltage measurement

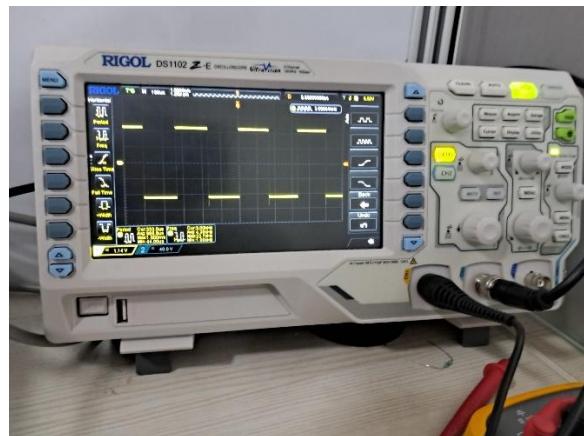
The DC power supply was set to 5V, and the output was then measured using a multimeter. To measure the voltage, the multimeter dial was set to voltage measurement mode, and the test leads were connected to the COM and V terminals.



The measured voltage closely matched the voltage set on the power supply, verifying the accuracy of both the power supply and the measurement procedure. This confirms that the setup and the method used to measure the voltage were correct.

Using the Oscilloscope and Function generator

We experimented with Oscilloscope and function generator. Making a function wave and trying to find its plot without the auto function, using knob. Adjusting scale and Location we finally get a good representation of the original function wave.



Left is function generator and right is oscilloscope. We generated a square wave function and observed the output on the oscilloscope.

1. First connect the wires with any one of the channels of oscilloscope and function generator.
2. Design a square wave in function generator by going to menu and selecting square wave.
3. Adjust the parameters on the oscilloscope to nicely visualize the wave output.

As it's shown, oscilloscope plots the square wave voltage input.

Precautions

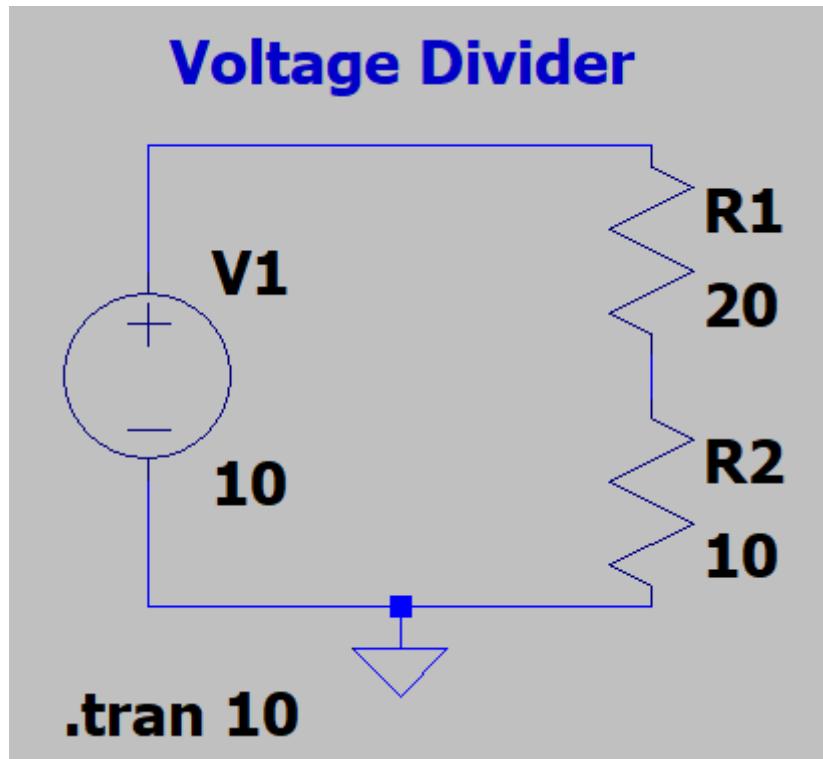
- One shouldn't operate at high voltages, as it can be dangerous. For our experiments, we should not go above 12 volts.
- Always turn off the power supply, multimeter, oscilloscope, and other equipment when not in use to conserve energy and prevent accidents.
- Before powering on any device, double-check all connections to ensure they are secure and correctly configured to prevent short circuits or equipment damage.
- Keep all instruments dry and away from liquids to prevent electrical hazards and equipment malfunction.
- Always ensure that all equipment is properly grounded to avoid electrical shocks and interference in measurements.

LT Spice Simulation

Prerequisites

Install LTSpice on your device. One can install it from [LTspice - EngineerZone \(analog.com\)](http://LTspice.EngineerZone.analog.com)

Schematic



We implemented a basic voltage divider on LTSpice with above schematic. We simulated it to compute and plot the voltages across both resistors.



Green is about both the resistors, while blue is about the 10Ω resistor. $\approx 3.4V$

We thus learnt very basic functionality of LTSpice software. It can be later used in our course to simulate advanced electronic circuitry.

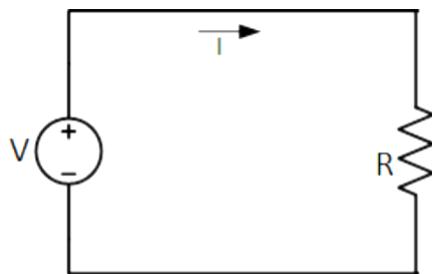
EXP II : Familiarization with DC and AC sources

In partnership with Aditya Pratap Singh (22020)

Objectives

1. Verification of ohm's law using IV characteristics (DC input).
2. Verification of ohm's law using IV characteristics (AC input).
3. Experiment to verify the Voltage Divider Rule.

Verification of ohm's law using IV characteristics (DC)



The circuit diagram for the experiment as shown above.

Required instruments

1. **Resistors:** 100Ω , 500Ω , $100k\Omega$, $500k\Omega$, $10M\Omega$ (1 each)
2. **Variable Voltage Source:** 0-12V with resolution of .5V or higher

Theory

Current through an ohmic resistor increases proportionally with the increase in applied voltage i.e.,

$$V = I \times R$$

where V is applied voltage, and I is the current through the ohmic resistor and R is the proportionality constant which is known as resistance.

Procedure

1. Make the circuit shown in a breadboard or kit provided.
2. Sweep the voltage from V_{\min} to V_{\max} in a small step (say 0.5V).
3. Measure the current using the digital multi-meter and record the values.
4. Plot the I-V characteristics in laboratory book.
5. Repeat the experiment from step 2 to step 4 for different values of R .

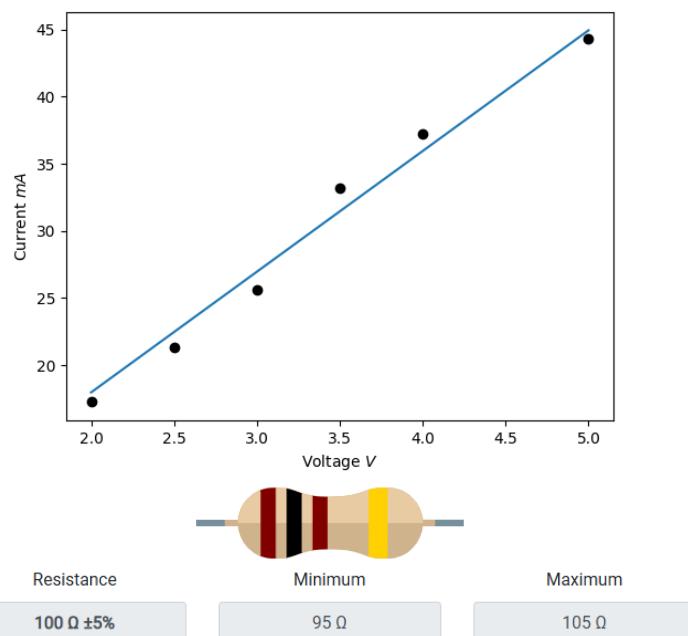
Take $V_{max} = 10V$ or $5V$ (Based on current change is less or more) and voltage step between $0.5V$ to $2V$.

Perform the test for 5 different resistances, $R = 100\Omega$, 500Ω , $100k\Omega$, $500k\Omega$, $10M\Omega$

The values of V_{min} , V_{max} , voltage step and R were given by the instructor in the lab.

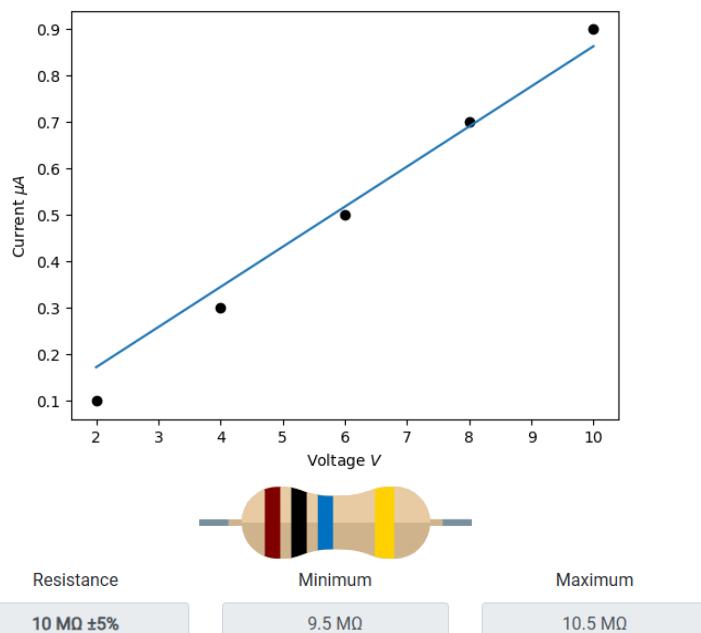
Observations

Voltage (V)	Current (mA)
2	17.26
2.5	21.36
3	25.64
3.5	33.23
4	37.25
5	44.30



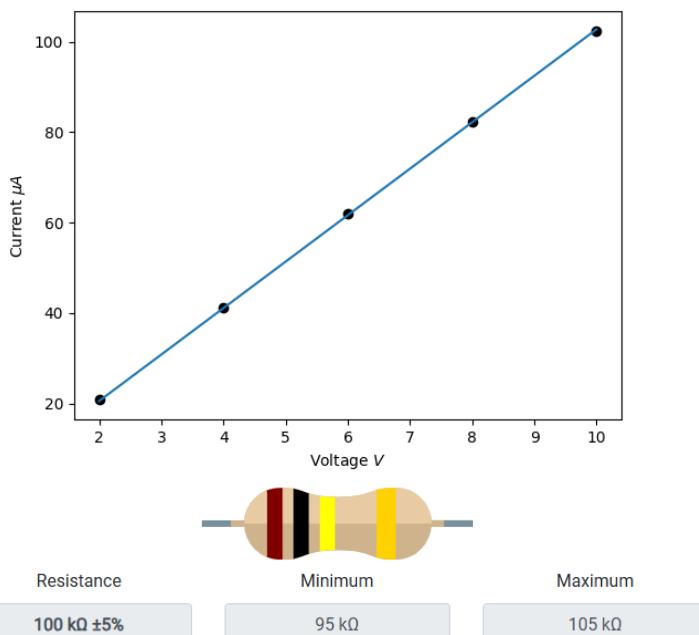
Resistance will be inverse of the slope of IV graph. Here the slope of best fit line is nearly $8.99k\Omega^{-1}$. Thus, the resistance calculated is nearly 111Ω .

Voltage (V)	Current (μ A)
2	0.1
4	0.3
6	0.5
8	0.7
10	0.9



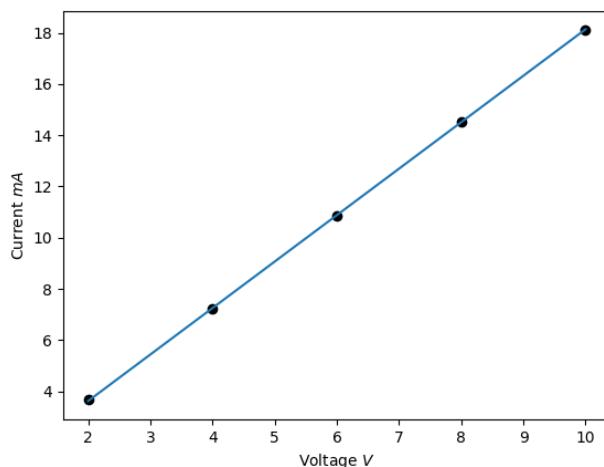
Resistance will be inverse of the slope of IV graph. Here the slope of best fit line is nearly $0.086\text{M}\Omega^{-1}$. Thus, the resistance calculated is nearly $11.5\text{M}\Omega$.

Voltage (V)	Current (μ A)
2	20.8
4	41.3
6	61.9
8	82.2
10	102.4



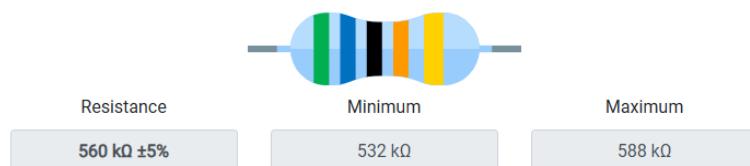
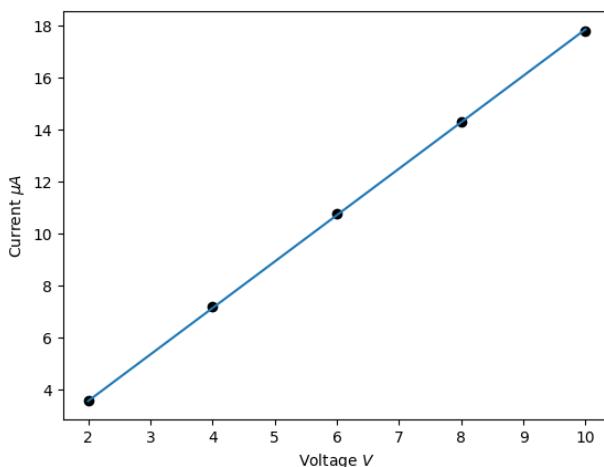
Resistance will be inverse of the slope of IV graph. Here the slope of best fit line is nearly $10.3\text{M}\Omega^{-1}$. Thus, the resistance calculated is nearly $97.4\text{k}\Omega$.

Voltage (V)	Current (mA)
2	3.69
4	7.21
6	10.87
8	14.54
10	18.12



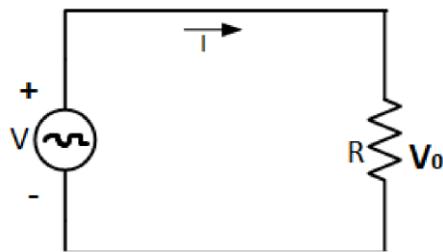
Resistance will be inverse of the slope of IV graph. Here the slope of best fit line is nearly $1.813\text{k}\Omega^{-1}$. Thus, the resistance calculated is nearly 551Ω .

Voltage (V)	Current (μ A)
2	3.6
4	7.2
6	10.8
8	14.3
10	17.8



Resistance will be inverse of the slope of IV graph. Here the slope of best fit line is nearly $1.79 \text{ M}\Omega^{-1}$. Thus, the resistance calculated is nearly $559 \text{ k}\Omega$.

Verification of ohm's law using IV characteristics (AC)



The above diagram shows the circuit involved in the experiment

Requirements

1. **Resistors:** 100Ω , 500Ω , $100k\Omega$, $500k\Omega$, $10M\Omega$ (1 each)
2. **Alternating Voltage Source:** With parametric V_{pp}

Theory

Resistors are bi-directional electronic passive component and hence the behaviour of the resistor does not change with the direction of current flowing through it. In AC circuits as shown in figure above, the direction of the current flowing through a component change with time and the change in the direction of has no effect on the behaviour of the resistor, thus the current will rise and fall as the applied voltage rises and falls. In this case, the current through and voltage across the resistor reach to a maximum value, then fall through zero and reach to a minimum value at the same time. i.e., they rise and fall simultaneously and are said to be "in-phase."

Procedure

1. Make the circuit shown in figure in a breadboard or kit provided.
2. Apply the AC voltage signal at the input side.
3. Measure the AC current using the digital multimeter/digital oscilloscope and record the values.
4. Plot the I-V characteristics in laboratory book.
5. Change the value of resistor R .
6. Repeat the experiment from step 2 to step 4.

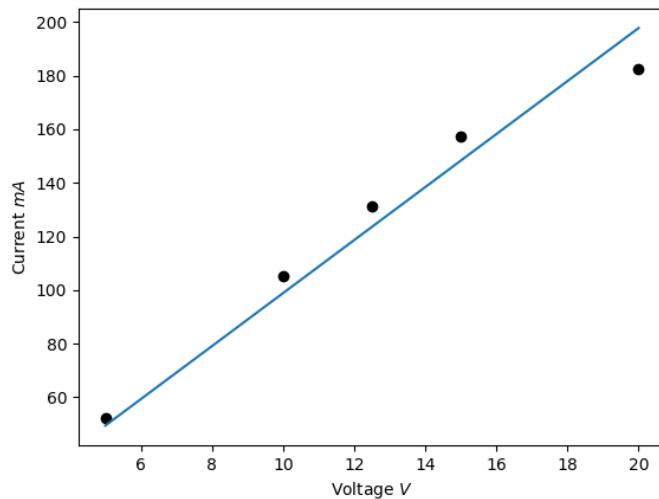
Take $V_{max} = 10V$ or $5V$ (Based on current change is less or more) and voltage step between $0.5V$ to $2V$.

Perform the test for 5 different resistances, $R = 100\Omega$, 500Ω , $100k\Omega$, $500k\Omega$, $10M\Omega$

Observation

For 100Ω resistance:

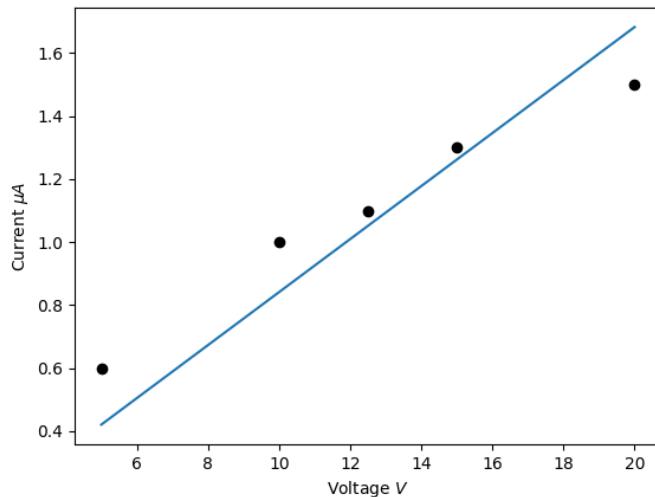
Voltage (V)	Current (mA)
5	52.4
10	105.1
12.5	131.1
15	157.5
20	182.3



Resistance will be inverse of the slope of IV graph. Here the slope of best fit line is nearly $9.89\text{k}\Omega^{-1}$. Thus, the resistance calculated is nearly 101.1Ω .

For $10\text{M}\Omega$ resistance:

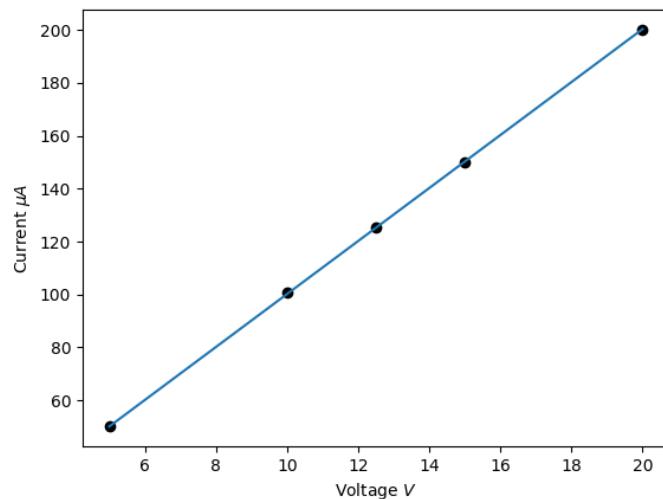
Voltage (V)	Current (μA)
5	.6
10	1.
12.5	1.1
15	1.3
20	1.5



Resistance will be inverse of the slope of IV graph. Here the slope of best fit line is nearly $0.084\text{M}\Omega^{-1}$. Thus, the resistance calculated is nearly $11.8\text{M}\Omega$.

For $100\text{k}\Omega$ resistance:

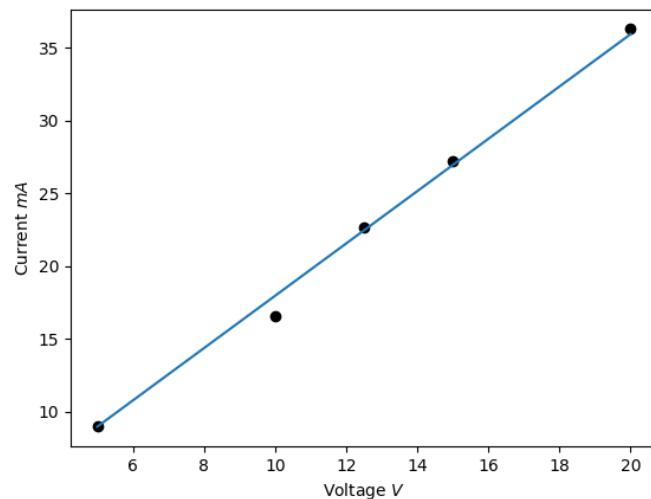
Voltage (V)	Current (μA)
5	50.04
10	100.64
12.5	125.38
15	150.12
20	200.16



Resistance will be inverse of the slope of IV graph. Here the slope of best fit line is nearly $10.02\text{M}\Omega^{-1}$. Thus, the resistance calculated is nearly $99\text{k}\Omega$.

For 560Ω resistance:

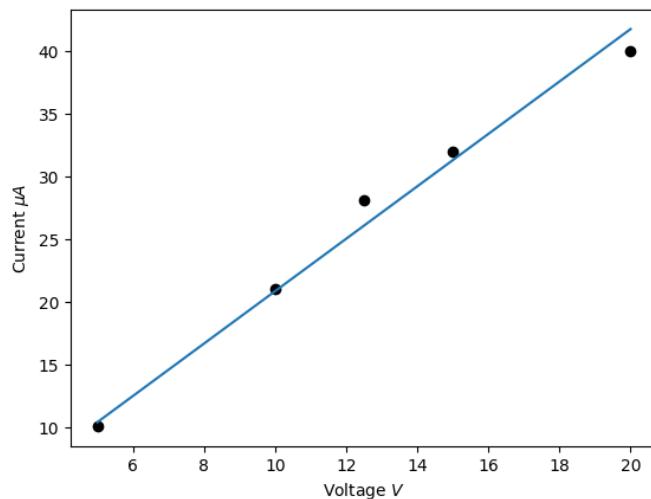
Voltage (V)	Current (mA)
5	9.05
10	16.58
12.5	22.67
15	27.24
20	36.3



Resistance will be inverse of the slope of IV graph. Here the slope of best fit line is nearly $1.8\text{k}\Omega^{-1}$. Thus, the resistance calculated is nearly 555.55Ω .

For $560\text{k}\Omega$ resistance:

Voltage (V)	Current (μA)
5	10.1
10	21.1
12.5	28.2
15	32.0
20	40.0



Resistance will be inverse of the slope of IV graph. Here the slope of best fit line is nearly $2.1\text{M}\Omega^{-1}$. Thus, the resistance calculated is nearly $478\text{k}\Omega$.

Experiment to verify the Voltage Divider Rule

The focus of this experiment is an examination of basic series DC circuits with resistors. A key element is Kirchhoff's Voltage Law which states that the sum of voltage rises around a loop must equal the sum of the voltage drops. The voltage divider rule will be investigated.

Theory Overview

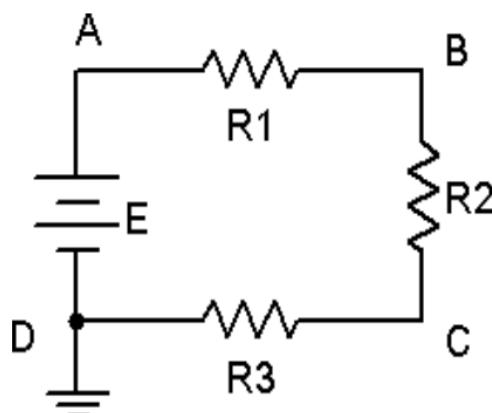
A series circuit is defined by a single loop in which all components are arranged in daisy-chain fashion. The current is the same at all points in the loop and may be found by dividing the total voltage source by the total resistance. The voltage drops across any resistor may then be found by multiplying that current by the resistor value. Consequently, the voltage drops in a series circuit are directly proportional to the resistance. An alternate technique to find the voltage is the voltage divider rule. This states that the voltage across any resistor (or combination of resistors) is equal to the total voltage source times the ratio of the resistance of interest to the total resistance.

Equation to find the voltage drop across any of the resistor, suppose, R₁,

$$V_1 = \frac{E \times R_1}{R_1 + R_2 + R_3}$$

Equipment

1. Adjustable DC Power Supply
2. Digital Multimeter
3. R₁ = 100
4. R₂ = 500
5. R₃ = 100k



Procedure

1. Using the circuit of Fig.1.3 with $R_1 = 1\text{ k}$, $R_2 = 2.2\text{ k}$, $R_3 = 3.3\text{ k}$, and $E = 5\text{ volts}$, determine the theoretical current and record it in table. Construct the circuit. Set the DMM to read DC current and insert it in the circuit at point A. Remember, ammeters go in-line and require the circuit to be opened for proper measurement. The red lead should be placed closer to the positive source terminal. Record this current. Repeat the current measurements at points B and C.
2. Using the theoretical current found in Step 1, apply Ohm's law to determine the expected voltage drops across R_1 , R_2 , and R_3 . Record these values.
3. Set the DMM to measure DC voltage. Remember, unlike current, voltage is measured across components. Place the DMM probes across R_1 and measure its voltage. Again, red lead should be placed closer to the positive source terminal. Record this value. Repeat this process for the voltages across R_2 and R_3 . Determine the percent deviation between theoretical and measured for each of the three resistor voltages and record.

Observation**E = 2V**

I Theory	I point A	I point B	I point C
19.88	20.9	20.9	20.9

Voltage across	Theory	Measured	Deviation
$R_1 = 100$.02	.02	0%
$R_2 = 500$.004	.003	25%
$R_3 = 100k$	2.01	2.01	0%

E = 10V

I Theory	I point A	I point B	I point C
99.4	101.6	101.6	101.5

Voltage across	Theory	Measured	Deviation
$R_1 = 100$.06	.056	12%
$R_2 = 500$.01	.01	0%
$R_3 = 100k$	9.96	9.96	0%

EXP III : RC and RL circuit

In partnership with Aditya Pratap Singh (22020)

Objectives:

1. Charging and discharging characteristics of capacitor using DC source.
2. Effect on the output of RC circuit for a square wave input signal.
3. Experiment with RL circuit with DC source. Record the voltage and current across the L with time.

Charging and discharging using DC source

Capacitor:

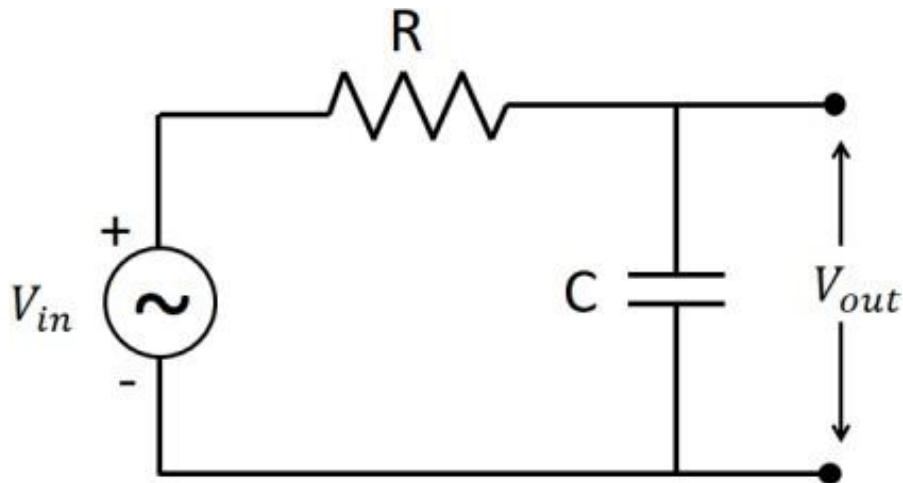
A discharged capacitor connected to a DC voltage source charges up with increase in the voltage of the source. Similarly, a charged capacitor discharges in opposite direction when the applied voltage of the DC source is reduced. Capacitors in this line can be compared with small batteries. The charge stored in a capacitor plates is proportional to the applied voltage and can be defined as, $Q = C \times V$, where Q is the stored charge, V is the applied voltage, and C is the proportionality constant which is known as capacitance.

The charging and discharging of capacitor generally takes some time and depends on the time constant (τ) i.e. the time taken for a certain percentage of charging and discharging of capacitor. As per the RC circuit given in Fig. 1.3, the capacitor will charge up through the resistor connected in series with time until the voltage across the capacitor (V_C) becomes equal to supply voltage (V_s). The time constant specifies the rate of charge or discharge and can be defined as, $\tau = R \times C$, where R is in ohm and C is in Farad where the τ is in seconds. In the given circuit, at any point of time (t) the voltage across the capacitor can be given by, $V_C = V_s(1 - e^{-\frac{t}{\tau}})$.

From the above equation, it is clear that at $t = 5\tau$, the capacitor becomes $\sim 100\%$ charged, i.e. $V_C \cong V_s$;

at $t = 4\tau$, the capacitor becomes $\sim 98\%$ charged, i.e. $V_C \cong 0.98V_s$; and at $t = \tau$, the capacitor becomes $\sim 63\%$ charged, i.e. $V_C \cong 0.63V_s$. In this situation, $t \leq 4\tau$ is known as transient period and $t > 4\tau$ is known as steady state where at $t=5\tau$,

the capacitor can be treated as fully charged. Similar is the case for discharging condition.



Results:

Input voltage = 5 V_{pp} square wave for all the experiments below

RC circuit with $R = 1\text{k}\Omega$ and $C = 90\text{nF}$ implies $\tau = 90\mu\text{s}$;

Time constant (μs)	Rise time (μs)	Fall time (μs)	V_{out} (Volts)
$\tau = 90$	45	45	1.41
$5 \tau = 450$	224	226	4.28
$8 \tau = 720$	359	361	4.99

RC circuit with $R=1\text{k}\Omega$ and $C=90\text{nF}$ and $\tau = 90\mu\text{s}$;

Time constant (μs)	Rise time (μs)	Fall time (μs)	V_{out} (Volts)
$\tau = 90$	45	45	0.85
$5 \tau = 450$	226	224	3.16
$8 \tau = 720$	360	360	4.01

RC circuit with $R=1\text{k}\Omega$ and $C=8.5\text{nF}$ and $\tau = 8.5\mu\text{s}$;

Time constant (μs)	Rise time (μs)	Fall time (μs)	V_{out} (Volts)
$\tau = 8.5$	4.23	4.27	1.13
$5 \tau = 42.5$	20.9	21.6	3.89
$8 \tau = 68$	33.2	34.8	4.71

RC circuit with $R=1\text{k}\Omega$ and $C=8.5\text{nF}$ and $\tau = 8.5\mu\text{s}$;

Time constant (μs)	Rise time (μs)	Fall time (μs)	V_{out} (Volts)
$\tau = 8.5$	4.24	4.26	0.66
$5 \tau = 42.5$	21.2	21.3	2.83
$8 \tau = 68$	33.8	34.2	3.22

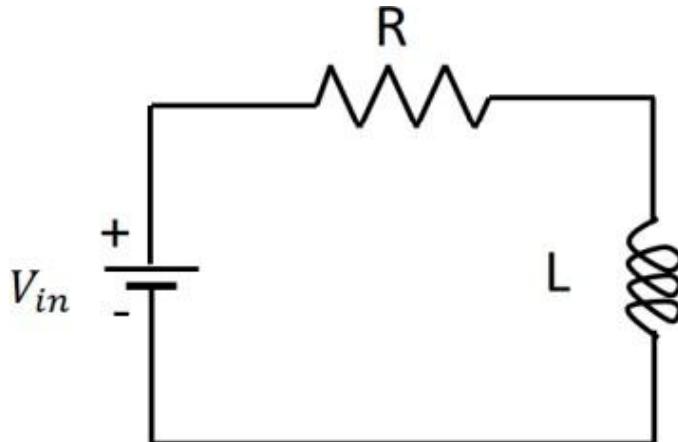
Inductor:

The series LR circuit is composed of an inductor (L) and resistor (R) connected in series along with a constant DC voltage source V. This is similar to that of RC circuit discussed in the previous experiment where capacitor (C) was used instead of inductor (L). Once the circuit is connected to a constant DC voltage source, the current starts flowing through the circuit but takes some time to reach to the maximum value as per ohms law i.e. V/R . The reason behind the delay of reaching maximum current is the self-induced emf within the coil i.e. inductor due to the magnetic flux as per Lenz's law. Thus, it takes some time for the applied voltage source to neutralize the self-induced emf and thereafter the current becomes constant. The rate of change of current and voltage depends on the time constant (τ), similar to that of RC circuit. In case of RL circuit, the time constant is determined and defined as, $\tau = L/R$, where τ is in seconds when inductance L is in Henry and resistance R is in ohms.

The voltage across the L (V_L) at any time t can be given by, $V_L = V e^{-\frac{t}{\tau}}$, where V is the applied voltage.

Similarly, the current through the L (I_L) at any time t can be given by,

$I_L = (V/R)(1 - e^{-\frac{t}{\tau}})$, where V is the applied voltage and R is the resistance.



Results:

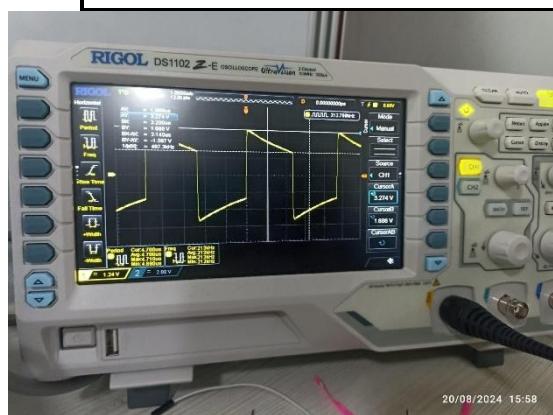
Input voltage = 5 V_{pp} square wave for all the experiments below

RL circuit with $R=1\text{k}\Omega$ and $L=4.7\text{mH}$ and $\tau = 4.7\mu\text{s}$,

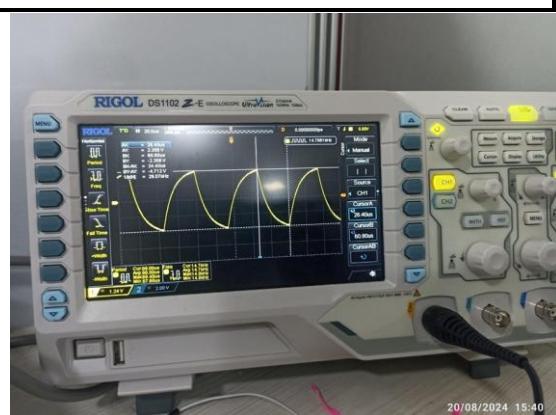
Time constant (μs)	V_{out} (Volts)
$\tau = 4.7$	1.62
$5 \tau = 23.5$	4.66

RL circuit with $R=1\text{k}\Omega$ and $L=4.7\text{mH}$ and $\tau = 4.7\mu\text{s}$,

Time constant (μs)	V_{out} (Volts)
$\tau = 4.7$	1.59
$5 \tau = 23.5$	4.64



Output waveform for Inductor



Output waveform for Capacitor

EXP IV :

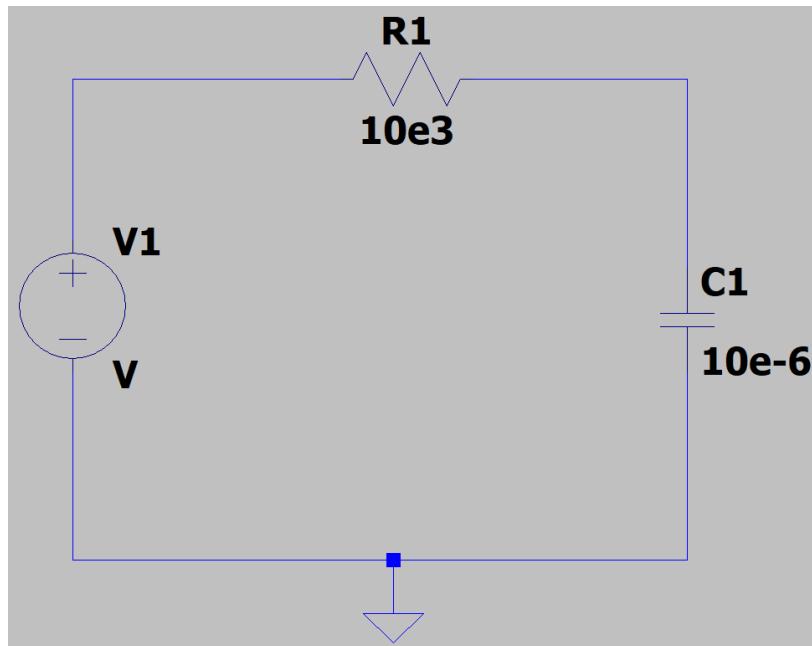
Low and High pass filters

In partnership with Aditya Pratap Singh (22020)

Objectives

1. Design a passive *low-pass filter* in LTspice and verify with experiment.
2. Design a passive *high-pass filter* in LTspice and verify with experiment.

Designing a low-pass filter



Representation of the circuit in LTSpice

Required Instruments

1. Breadboard
2. Signal Generator
3. Oscilloscope
4. Resistance ($1 \text{ k}\Omega$)
5. Capacitor ($1 \mu\text{F}$)
6. Connecting wires

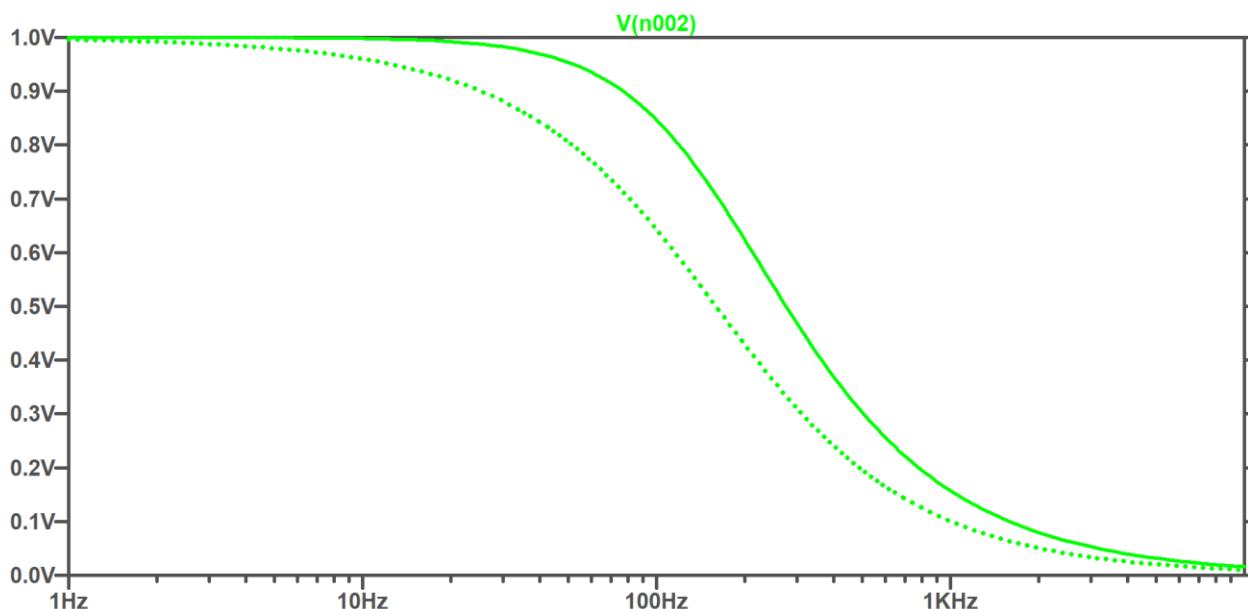
Theory

The RC low pass filter allows frequency signals below the cut-off frequency f_c :

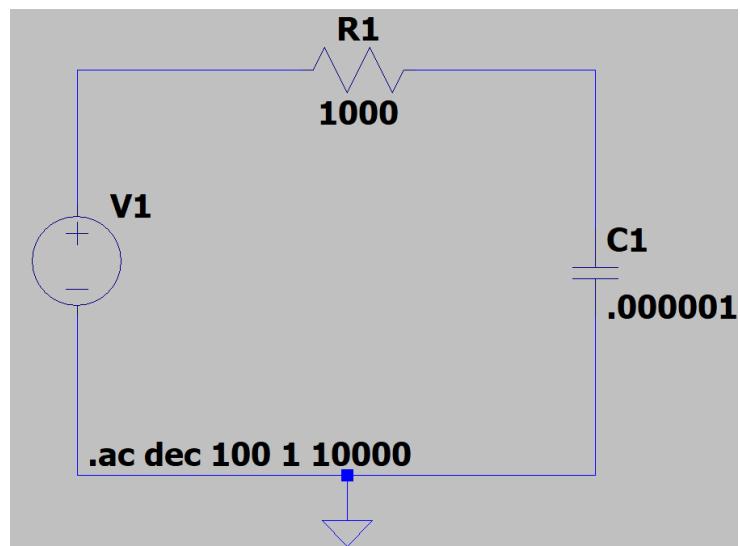
$$f_c = \frac{1}{2\pi RC}$$

The output voltage signal attenuates when the supply frequency is greater than the cut-off frequency as shown in figure below. At the cut-off frequency, capacitor C's capacitive reactance is equal to resistor R's resistance, causing the output voltage to be 0.707 times the input voltage (-3 dB).

$$Gain(dB) = 20 \log \frac{V_{out}}{V_{in}}$$



Here is the output of the simulation done on LTSpice, for the Voltage (Amplitude) about the capacitor for the input voltage being 2Vpp. The sim params were as follows:

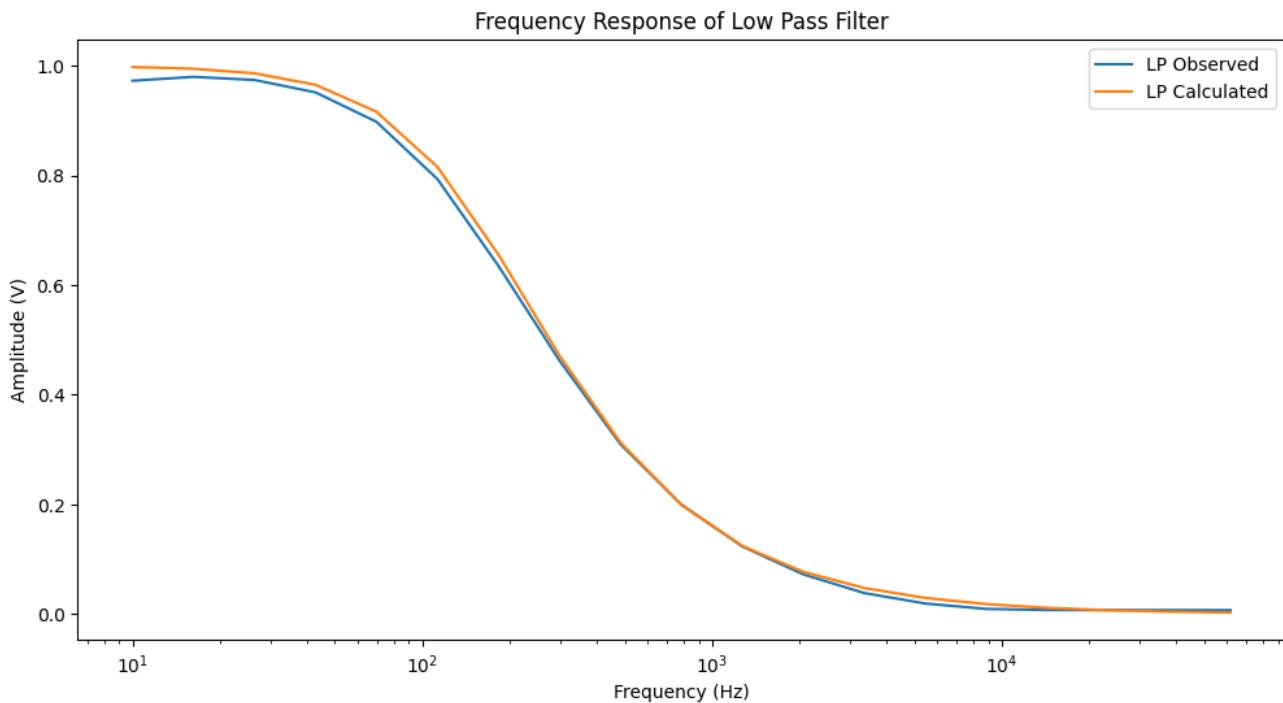


Procedure

1. Connect the circuit as shown in the circuit diagram..
2. Supply the AC sinusoidal signal from the signal generator.
3. Measure the AC output voltage from an oscilloscope (or) multimeter by varying the supply frequency.

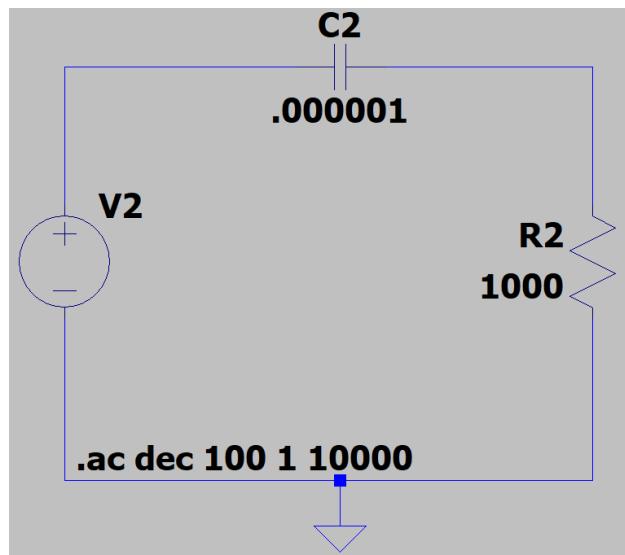
Results

We compare the experimental plots with the plots obtained from LTSpice above:



As you can see the results are close and within the margin of experimental error.

Designing a high-pass filter



Representation of the circuit in LTSpice

Required Instruments

1. Breadboard
2. Signal Generator
3. Oscilloscope
4. Resistance ($1\text{ k}\Omega$)
5. Capacitor ($1\text{ }\mu\text{F}$)
6. Connecting wires

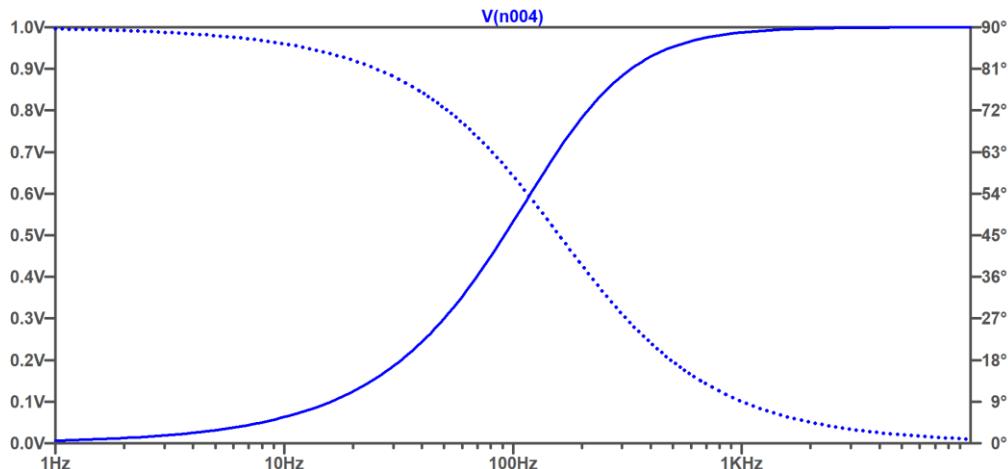
Theory

The RC high pass filter allows frequency signals above the cut-off frequency f_c :

$$f_c = \frac{1}{2\pi RC}$$

The output voltage signal attenuates when the supply frequency is greater than the cut-off frequency as shown in figure below. At the cut-off frequency, capacitor C's capacitive reactance is equal to resistor R's resistance, causing the output voltage to be 0.707 times the input voltage (-3 dB).

$$Gain(\text{dB}) = 20 \log \frac{V_{out}}{V_{in}}$$



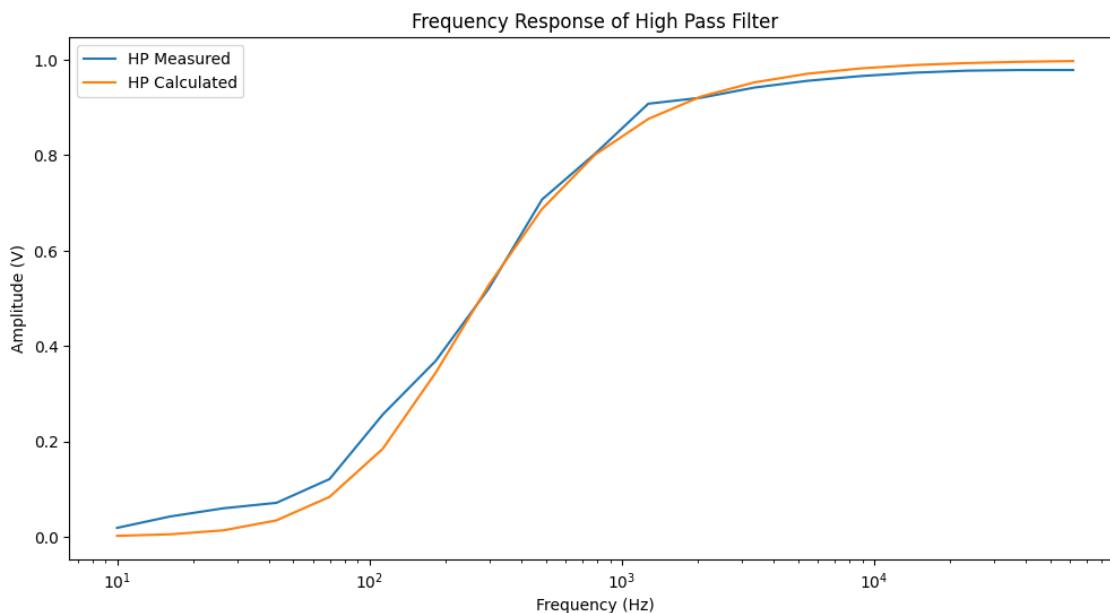
Here is the output of the simulation done on LTSpice, for the Voltage (Amplitude) about the capacitor for the input voltage being 2Vpp.

Procedure

1. Connect the circuit as shown in the circuit diagram.
2. Supply the AC sinusoidal signal from the signal generator.
3. Measure the AC output voltage from an oscilloscope (or) multimeter by varying the supply frequency.

Results

We compare the experimental plots with the plots obtained from LTSpice above:



As you can see the results are close and within the margin of experimental error.

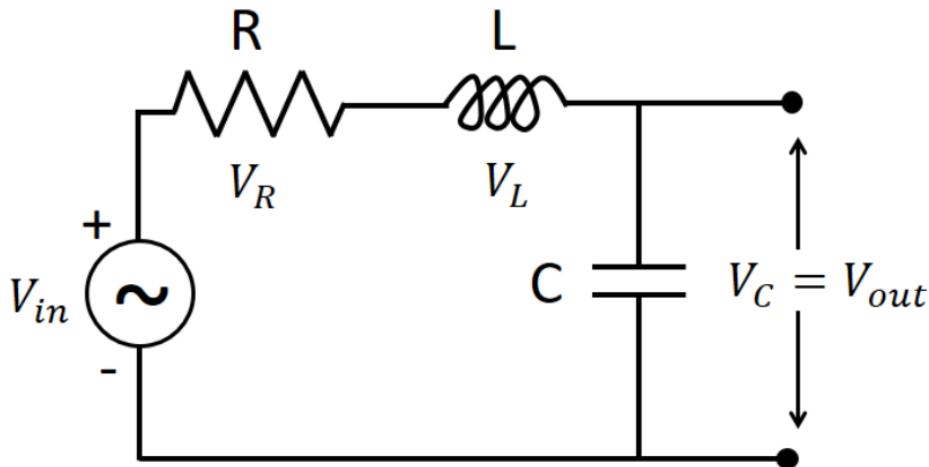
EXP V : RLC circuit

In partnership with Aditya Pratap Singh (22020)

Objectives

1. For the given RLC circuit, apply input signals of different frequencies and vary the resistance values for a fixed value of L and C and measure output voltage, $V_{out}(t)$.
2. Measuring V_{out} for these combinations for observing underdamp, overdamp and critically damped behaviour after adjusting the appropriate values of RLC.

RLC circuit with varying frequency and resistance



Brief theory

The series RLC circuit is composed of a resistor (R), a capacitor (C), and an inductor (L) connected in series as illustrated in figure. In case of a pure ohmic resistor the voltage and current waveforms are in-phase with each other. In case of pure inductance surface the voltage waveform leads the current by 90° and for pure capacitance the voltage lags the current by 90° .

The mentioned phase difference between the voltage and current depends on the reactance (X) of circuit. For a purely resistive circuit element, $X = 0$; for purely inductive circuit element, $X > 0$; and for purely capacitive circuit element, $X < 0$.

The reactance and impedance of the circuit elements are,

<i>Element</i>	<i>Resistance</i>	<i>Reactance (X)</i>	<i>Impedance (Z)</i>
<i>Resistor</i>	R	0	$Z = R$
<i>Inductor</i>	0	ωL	$z = j\omega L$
<i>Capacitor</i>	0	$\frac{1}{\omega C}$	$Z = \frac{1}{j\omega C}$

where ω is angular frequency

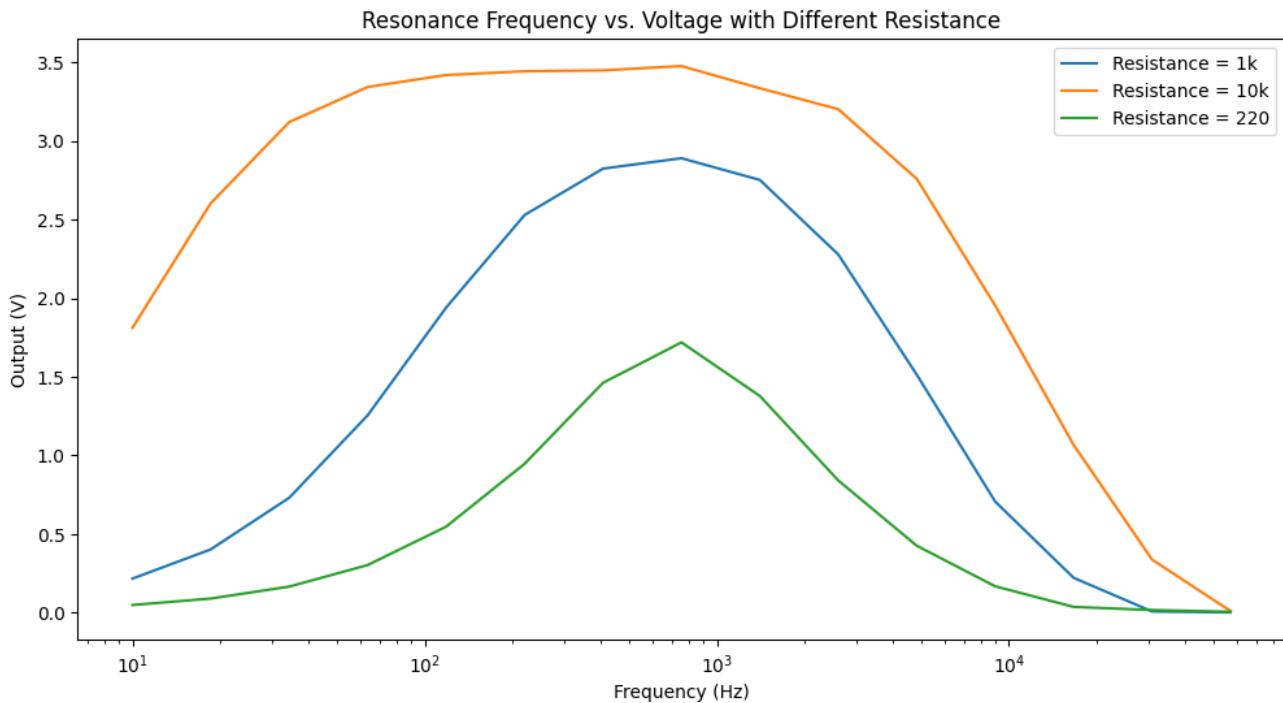
The RLC circuit in this case will help us to analyse each circuit element simultaneously. This circuit is like the series RL and RC circuits discussed previously, the difference in similar to case is that the reactance of both L and C will be counted together in overall reactance of the circuit. In the circuit under consideration consists of a single loop with the same current flowing through all three-circuit element. Since, the reactance's of L and C are a function of frequency ($\omega = 2\pi f$, f is frequency), hence the sinusoidal response of the circuit will vary with input frequency, f. In this case, the individual voltage drop of each circuit element, R, L, and C will be out of phase with each other.

Procedure

1. Connect the circuit as per figure above on breadboard using connecting wires.
2. Connect the function generator in the input of the circuit.
3. Connect one channel of the oscilloscope across the resistor (R) and the other channel with input.
4. Provide a sinusoidal signal of amplitude 5 V and a frequency of 50 Hz or as instructed by the lab instructor.
5. Record the output voltage signal across the resistor.
6. Thereafter, connect the oscilloscope across the inductor and record the output voltage signal.
7. Finally, connect the oscilloscope across the capacitor and record the output voltage signal.
8. Change the frequency and plot the frequency versus peak voltage to find the resonance
9. frequency, $\omega_0 = 1/\sqrt{LC}$.

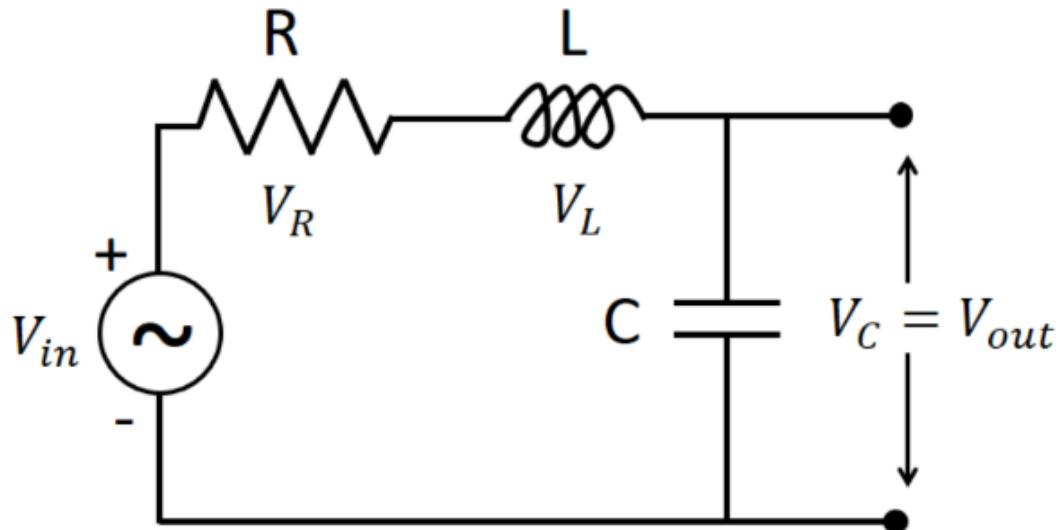
Results

We performed the experiment with three different resistances, $1\text{ k}\Omega$, $10\text{ k}\Omega$ and $220\text{ }\Omega$. The results are as follows:



Notice the peak is nearly at 730 Volts which is roughly equal to our resonance frequency for the circuit too.

Measuring Voltage for different damping conditions



We take the same circuit as we have taken in previous experiment.

Components Required:

1. Inductor
2. Capacitor
3. Resistor (less than, equal to, and more than 110)
4. Breadboard
5. Jumper wires
6. Oscilloscope

Brief Theory:

The basic discussion on the RLC circuit has been discussed in the previous experiment. If we consider KVL the, $V_R + V_L + V_C = V(t)$ where V_R , V_L , and V_C are the voltages across, R, L, and C, respectively and $V(t)$ is the input voltage signal. Substituting the values of the voltages across each electronic components we get,

$$RI(t) + L \frac{dI(t)}{dt} + V_0 + \frac{1}{C} \int_0^t I(\tau) d\tau = V(t)$$

for a unchanging voltage signal the same will reduce to,

$$\frac{d^2}{dt^2} I(t) + \frac{R}{L} \frac{d}{dt} I(t) + \frac{1}{LC} I(t) = 0$$

This can be written as the following form, $\frac{d^2}{dt^2} I(t) + 2\alpha \frac{d}{dt} I(t) + \omega_0^2 I(t) = 0$

Where $\alpha = R/2L$, is the attenuation or Neper frequency and $\omega_0 = 1/\sqrt{LC}$, is the angular frequency. The term α decides how fast the transient response will settle down. Depending on the electrical component values the circuit can be categorized as overdamped, critically damped, and underdamped. The following are the conditions for the same.

If $\alpha > \omega_0$ then it is overdamped

If $\alpha = \omega_0$ then it is critically damped

If $\alpha < \omega_0$ then it is underdamped

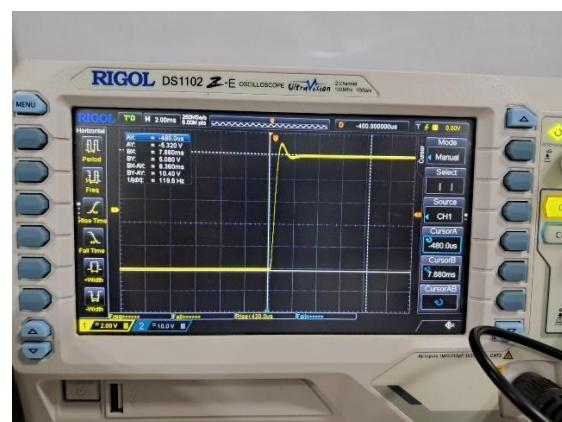
Procedure:

1. Connect the circuit as per figure above on breadboard.
 2. Connect the function generator in the input of the circuit.
 3. Connect one channel of the oscilloscope across the inductor (L) and the other channel with input.
 4. Provide a square wave of amplitude 1 V and a frequency of 50 Hz (adjust the signal if necessary) or as instructed by the lab instructor.
 5. Make the circuit for three different LC combinations as instructed by lab instructor for three different damping conditions.
 6. Expand the time scale of the oscilloscope to get the damping behavior of the circuit.
 7. Connect one channel of the oscilloscope across the capacitor (C) and the other channel with input.
 8. Perform the same experiment (4-6) and observe the damping behavior.

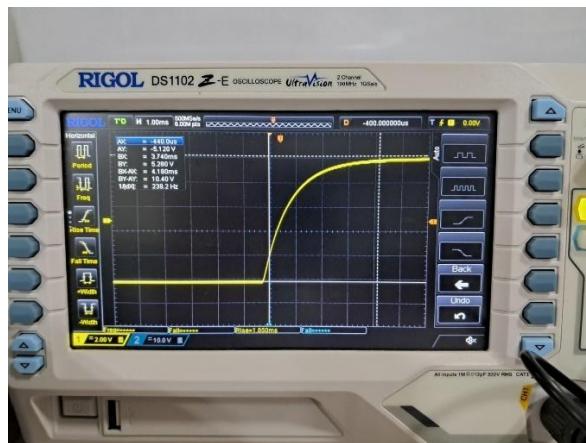
Results:



Overdamped



Underdamped



Critically damped

EXP VI : Diode Behaviour

In partnership with Aditya Pratap Singh (22020)

Objectives

1. I-V characteristics of a diode
2. Study of Full-wave and Half-wave rectifier circuit
3. Study of Clipper and Clamper circuit

I-V Characteristics of Diode

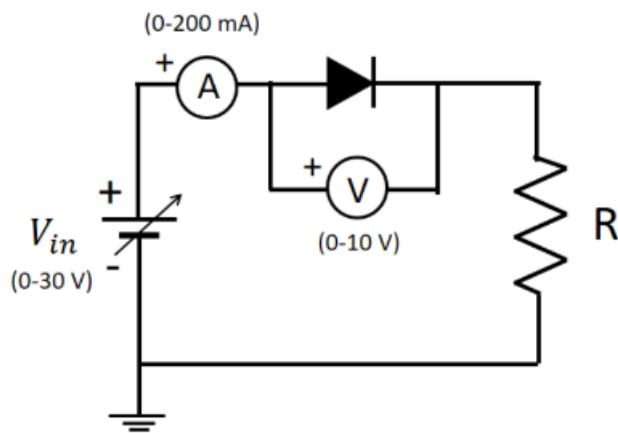


Fig. 4.1: circuit diagram of PN diode

Brief theory:

A diode is a unidirectional passive device, therefore the polarity of the power source connected to it counts. An ideal diode is a perfect conductor in one direction of current and an ideal insulator in the opposing direction. However, the diode does not behave as an ideal conductor or insulator in any scenario. A junction diode is essentially a semiconductor PN junction made up of p-type and n-type semiconductive regions. If the positive (negative) terminal of a voltage source is connected to the P-side (N-side) of the diode, the diode is said to be forward biased or ON; otherwise, it is reverse biased or OFF. A true semiconductor diode built of Silicon requires around 0.7 V forward bias before it can conduct current.

It conducts very little current in reverse bias, which should ideally be zero. The forward current moves from the region of p to n. The following formula represents the typical voltage-current (V-I) relationship in a true PN junction diode.,

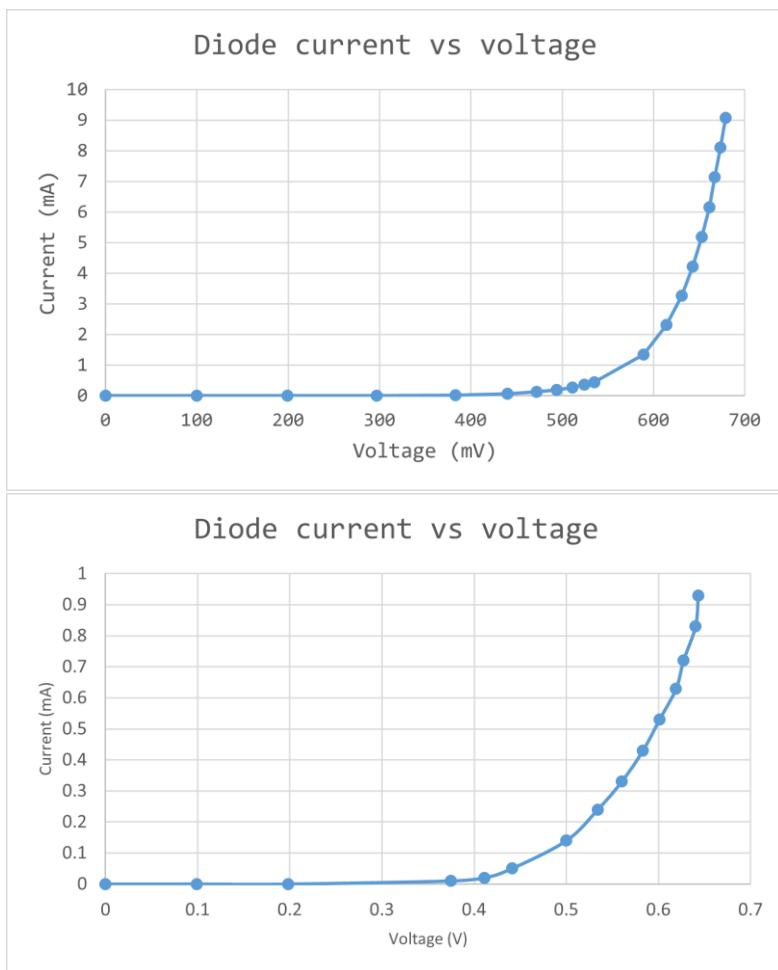
$$I = I_S(e^{\frac{V_D}{nV_T}} - 1)$$

Where, I is the diode current, I_S is the reverse bias saturation current or scale current, V_D is the applied voltage across the diode, V_T is the thermal voltage, and n is the ideality factor.

Procedure:

1. Connect the power supply, voltmeter, ammeter with the diode as shown in the figure above. Use two multimeters, one to measure current through diode and other to measure voltage across diode as shown in the Figure 4.1.
2. Increase voltage from the power supply from 0 V in step as shown in the observation table.
3. Measure voltage across diode and current through diode. Note down readings in the observation table.
4. Plot the graphs of Diode voltage vs. Diode current.

Results:



Forward bias:

	Supply V (V)	Diode V (mV)	Diode I (mA)
1	0	0	0
2	0.1	100	0
3	0.2	201	0
4	0.3	302	0
5	0.4	386	0
6	0.5	444	0.03
7	0.6	475	0.10
8	0.7	499	0.17
9	0.8	515	0.24
10	0.9	532	0.32
11	1	545	0.41
12	2	595	1.25
13	3	618	2.15
14	4	634	3.38
15	5	647	4.18
16	6	656	5.29
17	7	665	6.15
18	8	669	7.13
19	9	677	8.1
20	10	682	9.12

Reverse Bias:

	Supply V (V)	Diode V (V)	Diode I (mA)
1	0	0	0
2	0.1	0.099	0
3	0.2	0.198	0
4	0.5	0.375	0.01
5	0.7	0.411	0.02
6	1	0.441	0.05
7	2	0.5	0.14
8	3	0.534	0.24
9	4	0.56	0.33
10	5	0.583	0.43
11	6	0.601	0.53
12	7	0.619	0.63
13	8	0.627	0.72
14	9	0.64	0.83
15	10	0.643	0.93

Study of Full-wave and Half-wave rectifier circuit

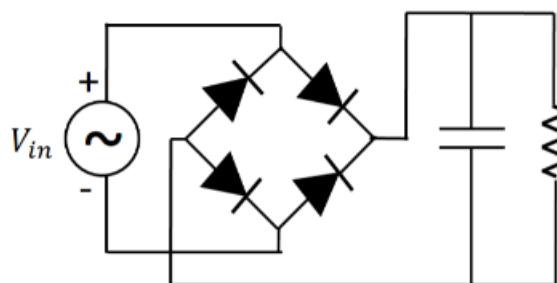
Brief theory:

Rectifiers are the electrical circuits that converts the alternating currents (i.e. the currents that changes its direction with time) to a direct current (i.e. the current that has only one direction) by either removing a section of the signal with one polarity or converting the polarity of the signal to a single one. Most used two types of rectifiers are the half-wave and full-wave rectifiers. The associated circuits are given in Figure 4.2.

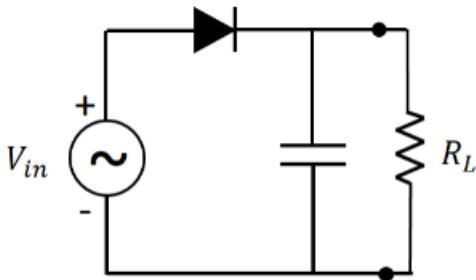
In case of half-wave rectifier, the diode conducts current only during the positive cycle of the sinusoidal input and blocks the negative cycle of the input. Hence, the output of the rectifier is only the positive cycle of the input signal. Thus, it is called half-wave rectifier as it only rectifies the half part of the full signal.

In case of full-wave rectifier, the 4 diodes are arranged in such a way that during positive cycle two of the 4 diodes conduct and during negative cycle the

other two of the 4 diodes will conduct. In both the cases, the current follows different paths and reflect as a positive signal at the output.

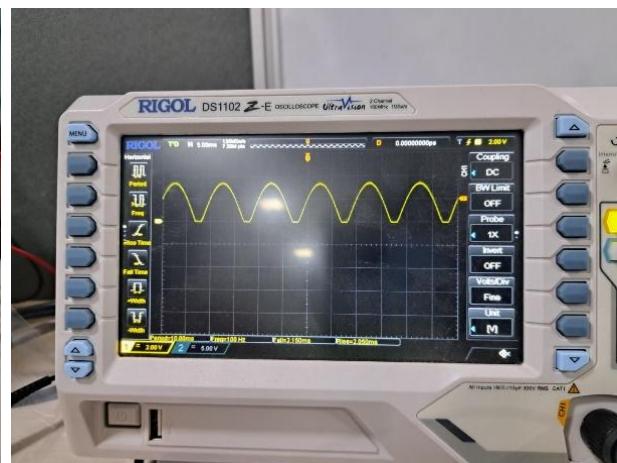
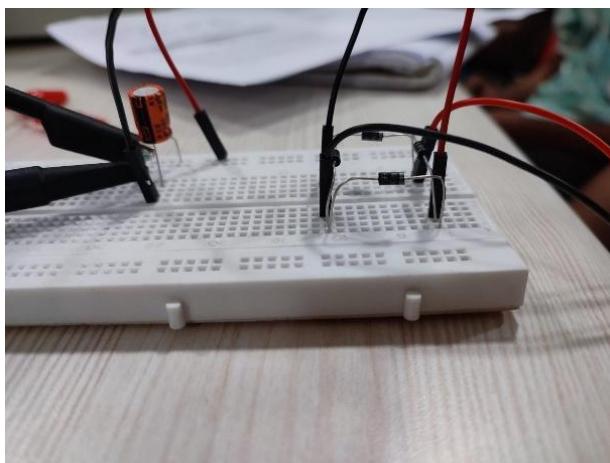


Full-Wave Rectifier

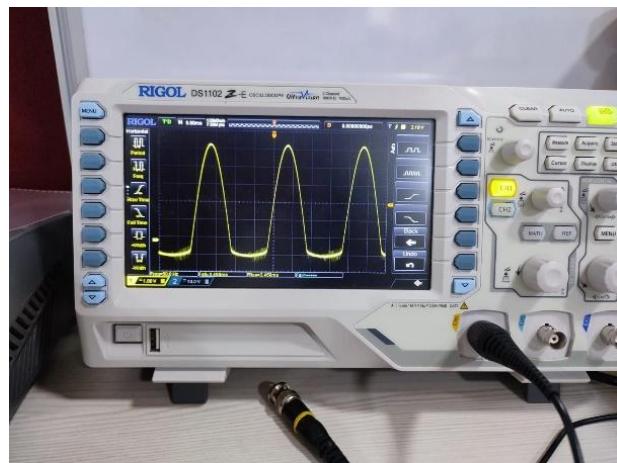


Half-Wave Rectifier

Full-wave rectifier:



Half Wave rectifier



Study of Clipper and clamper circuit

Brief theory:

Clipper Circuit: Clipping circuits are used to remove a part of a signal that is above or below a reference level. Clipping circuits are also known as limiters, amplitude selectors, or slicers. The half-wave rectifier is a good basic example of a clipper circuit where the reference level is zero, and the signal below zero voltage (i.e., negative) cannot pass through. A DC voltage source is put in series with the diode to alter the reference level to a desired value. Depending on the DC source's polarity and the diode's direction, the circuit will clip the input signal above or below the reference level set by the user.

Clamping Circuits: Conversely, a clamper circuit shifts a signal to a defined value. This circuit adds a DC component to the input signal. The circuit can work with a bias or no-bias condition. If the signal shifts above the central line of an input wave, it is called a positive clamper circuit; if it shifts downwards, it is called a negative clamper circuit.

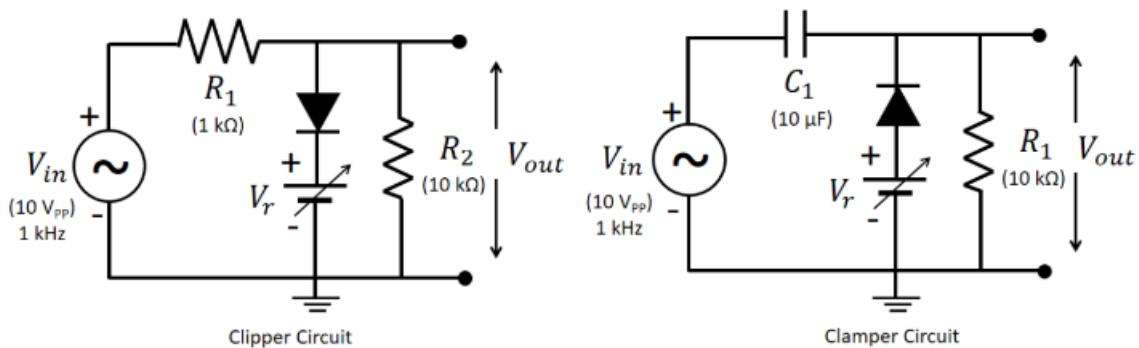
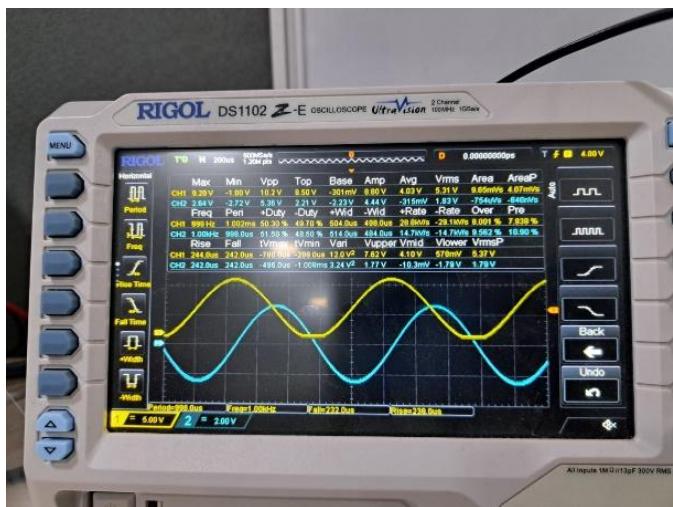
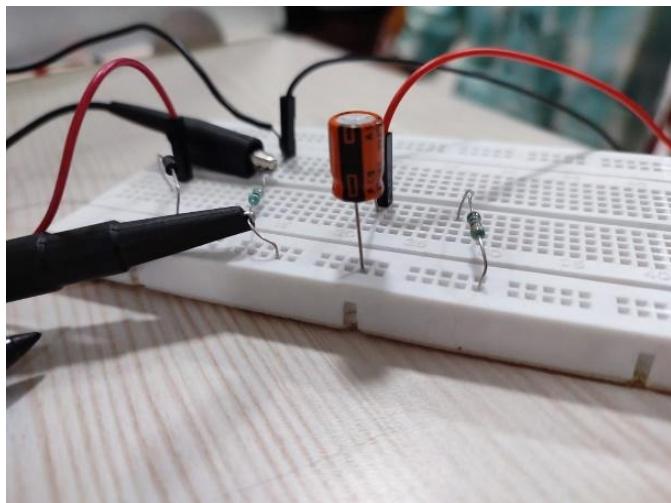


Fig 4.3: Clipper and Clamper circuit

Results:



Output of the clamper circuit



The clamper circuit



Output of the clipper circuit

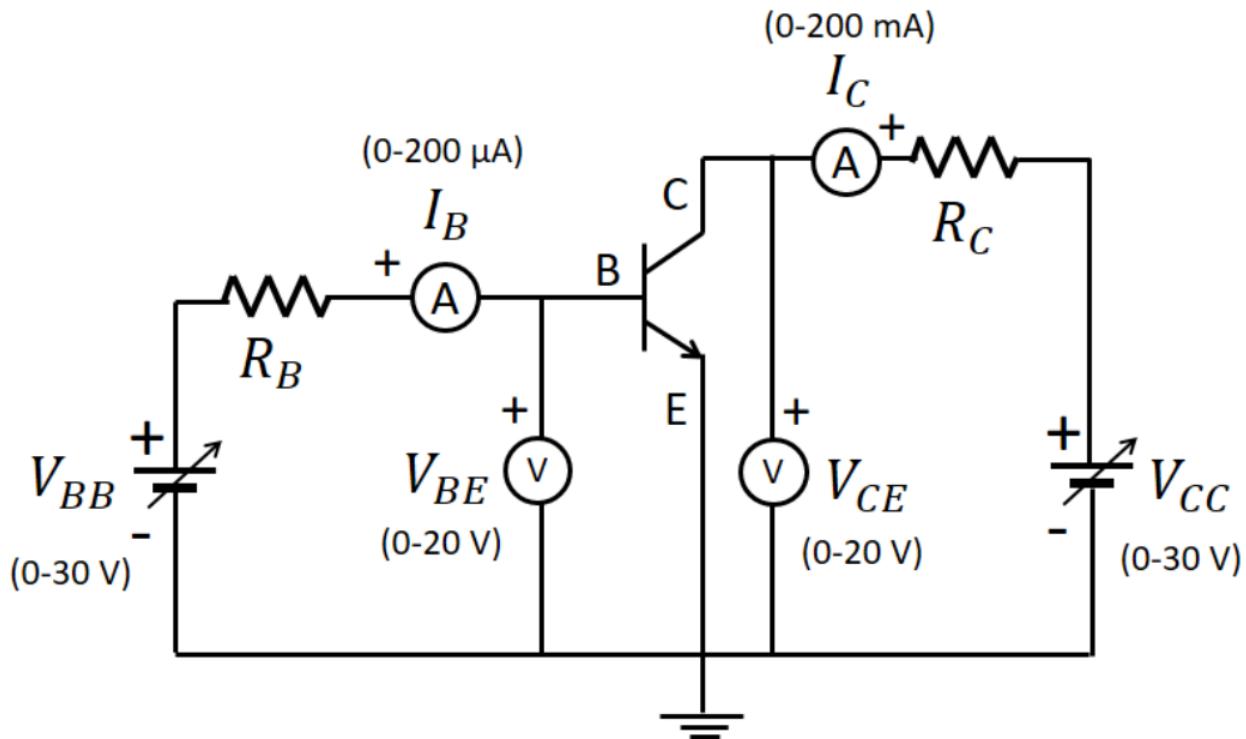
EXP VII : Bipolar Junction Transistor

In partnership with Aditya Pratap Singh (22020)

Objective

Study of Common emitter configuration (I_C vs V_{CE} for different V_{BE})

Common emitter configuration



Brief Theory:

Bipolar Junction Transistor (BJT) has three terminals namely, emitter (E), base (B), and collector (C). A BJT is composed of two PN junctions and the operation of BJT is mainly based on the PN junction characteristics. In case of a npn transistor in active region, under forward biased emitter-base (EB) junction, the majority carrier electrons in n-type emitter region are injected to thin p-type base region where the electrons as minority carrier diffuse towards the collector through the reverse biased collector-base (CB) junction. Some of the electrons recombine with holes in the thin p-type base region to produce a small base current (I_B) and the remaining reach collector as a collector current (I_C).

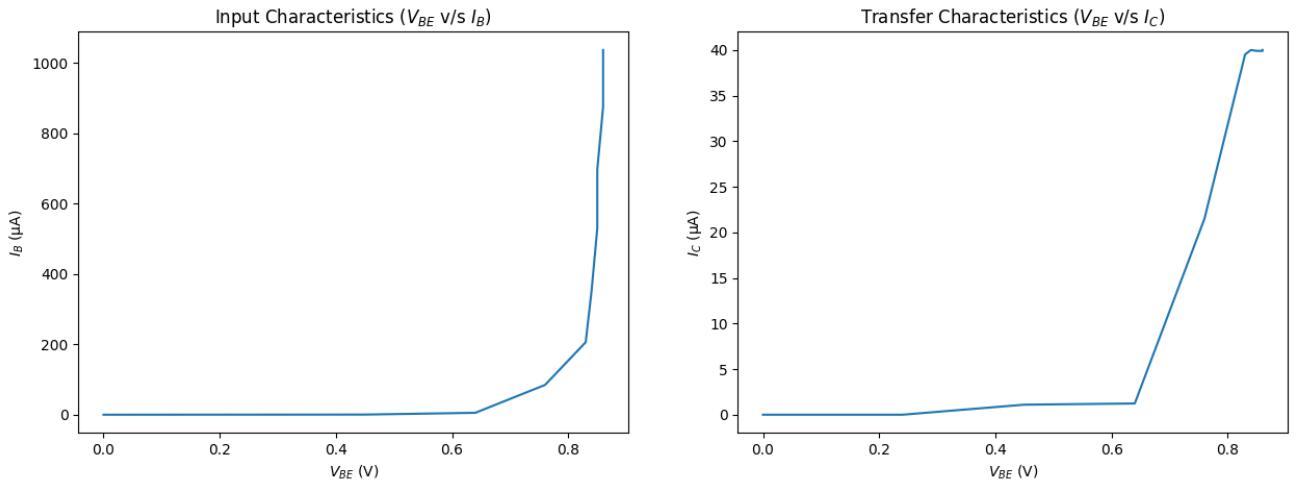
Hence, if there is no current from emitter (IE), then there will be almost no IC. Combining all the currents, the total emitter current, $I_E = I_B + I_C$.

In case of pnp transistor, the polarity of voltage sources must be reversed. Depending on the biasing of two junctions (i.e. EB and CB) transistor, the transistor can be said to be in different modes of operation.

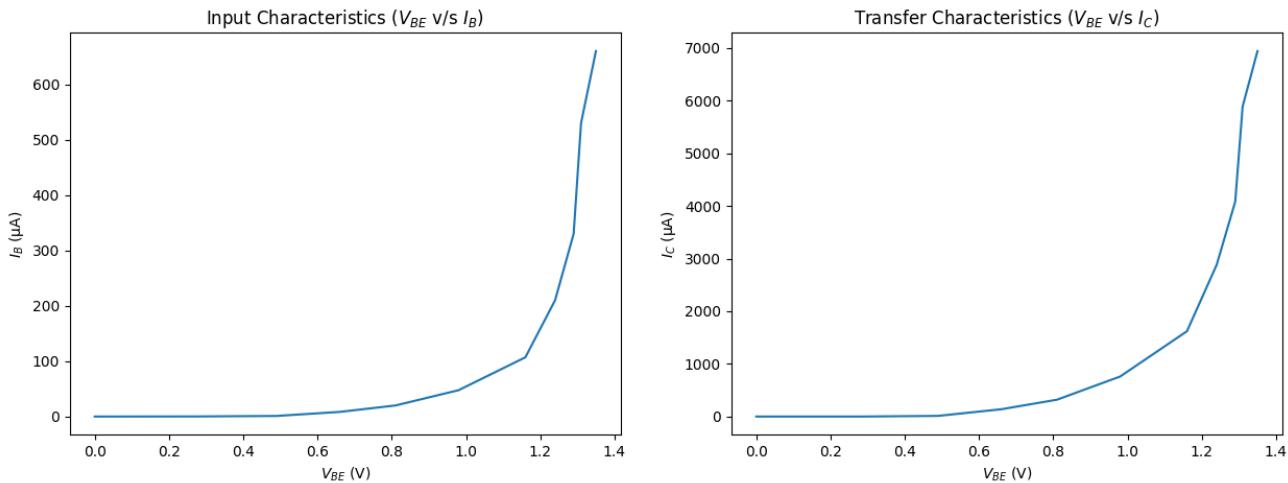
Operating Region	EB Junction	CB Junction	Remark
Cut-off	Reverse	Reverse	$I_E \approx I_B \approx I_C \approx 0$, Off-state, $V_{BE} < 0.7 V$
Active	Forward	Reverse	Amplifier gain (100-1000)
Saturation	Forward	Forward	Conducting
Reverse Saturation	Reverse	Forward	Reverse gain

Output characteristics are obtained between the output voltage and output current at constant input current. It is plotted between VCE and IC at constant IB in CE configuration.

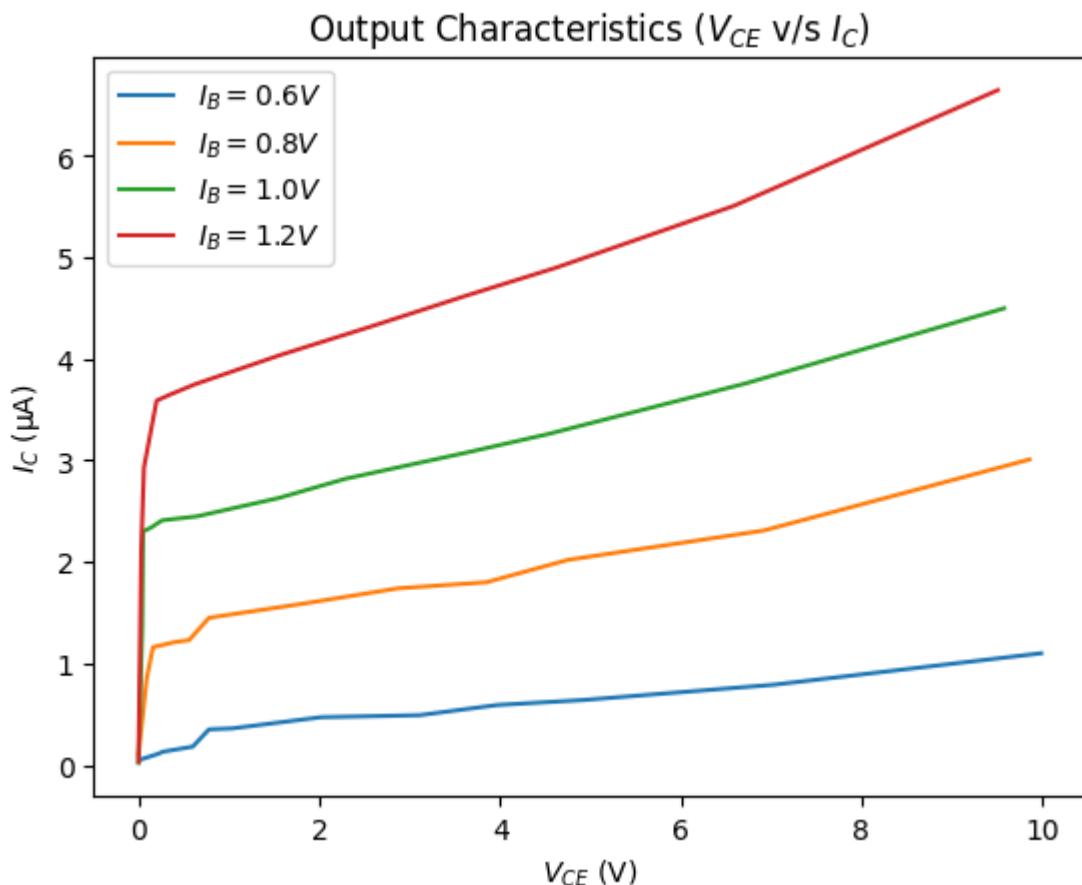
Results:



Above are the plots obtained for PNP



Above are the plots obtained for NPN



These are the output characteristic.

EXP VIII : Universal Gates

In partnership with Aditya Pratap Singh (22020)

Objective

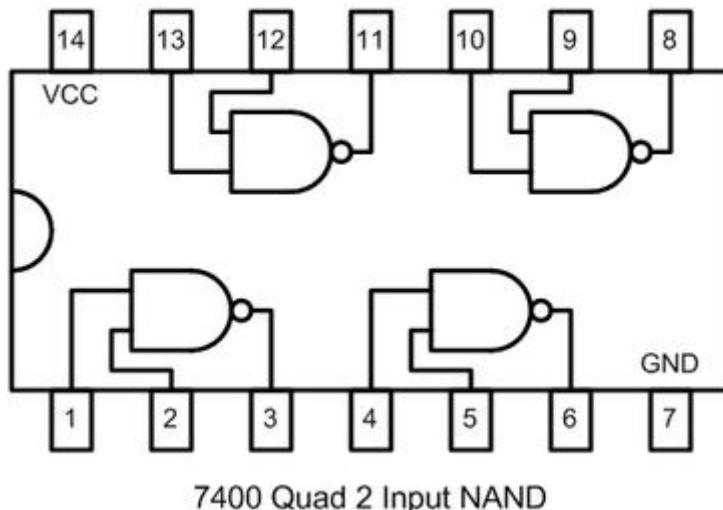
Realization of logic functions with the help of universal gates NAND and NOR Gate

Materials Required

- NAND IC – 7400
- NOR IC – 7404
- Bread Board
- Jumper wires
- LEDs
- DMM
- DC Power supply

Nand

NAND gate is a combination of two logic gates i.e. AND gate followed by NOT gate. So its output is complement of the output of an AND gate. This gate can have minimum two inputs. By using only NAND gates, we can realize all logic functions: AND, OR, NOT, Ex-OR, Ex-NOR, NOR. So this gate is also called as *universal gate*.



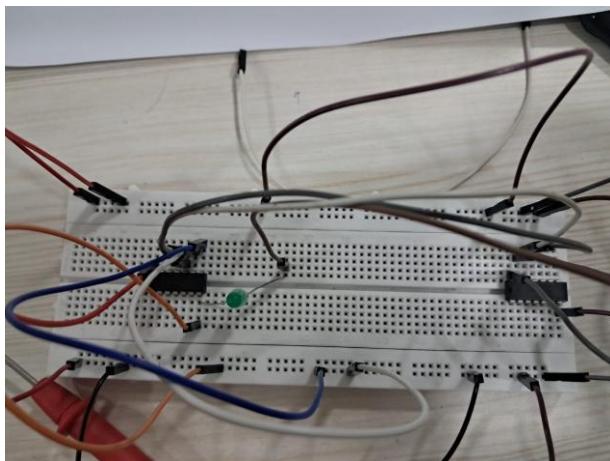
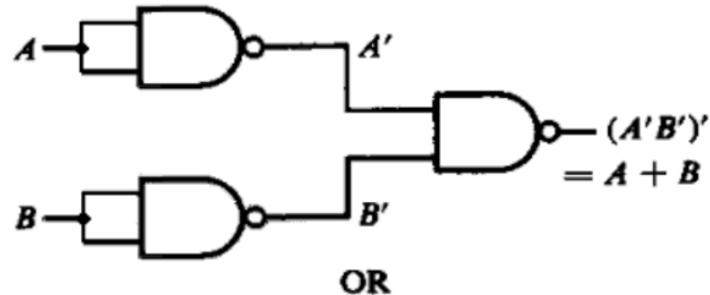
NAND gate as OR

From DeMorgan's theorems:

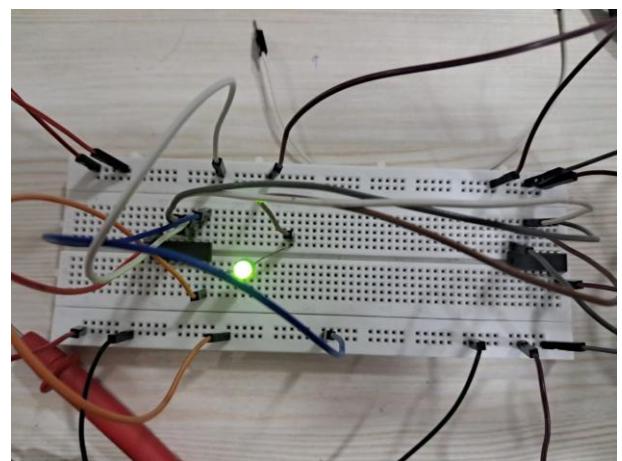
$$(A \cdot B)' = A' + B'$$

$$(A' \cdot B')' = A'' + B'' = A + B$$

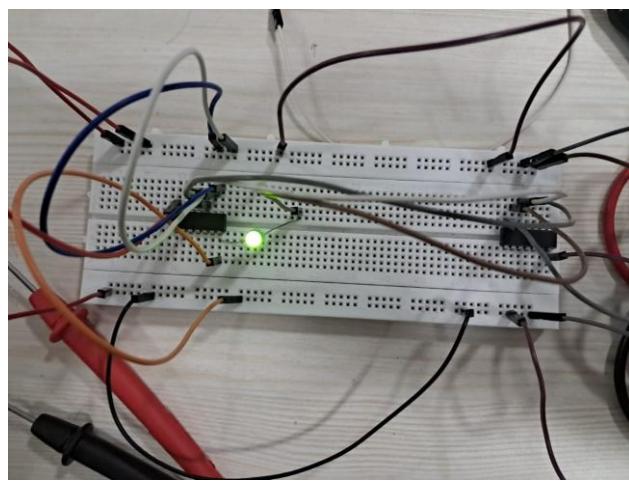
So, give the inverted inputs to a NAND gate, obtain OR operation at output.



0 or 0



1 or 0 / 0 or 1



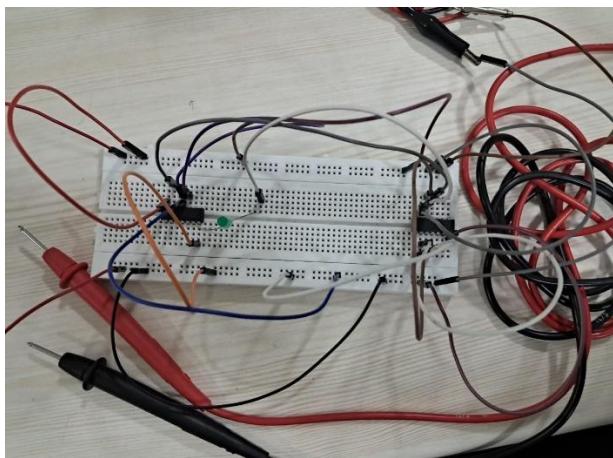
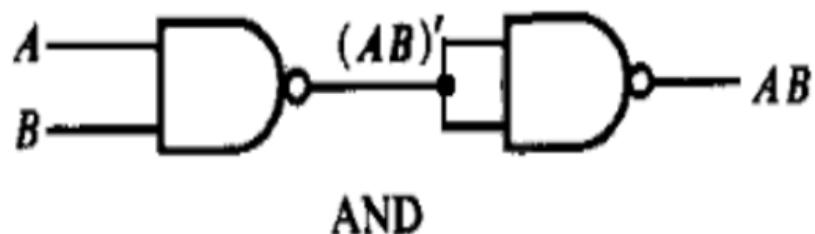
1 or 1

NAND gate as AND

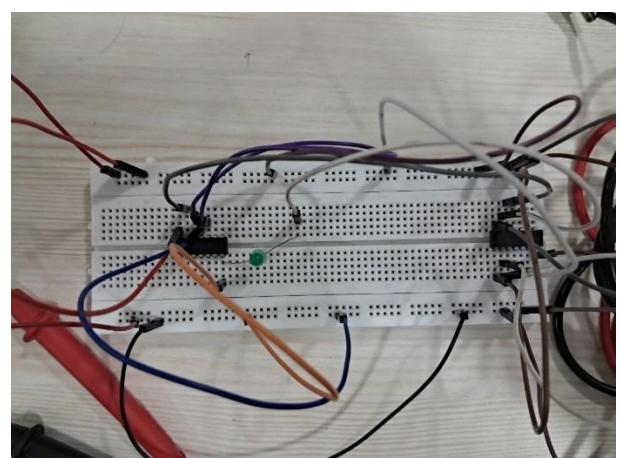
A NAND produces complement of AND gate. So, if the output of a NAND gate is inverted, overall output will be that of an AND gate.

$$Y = ((A \cdot B)')'$$

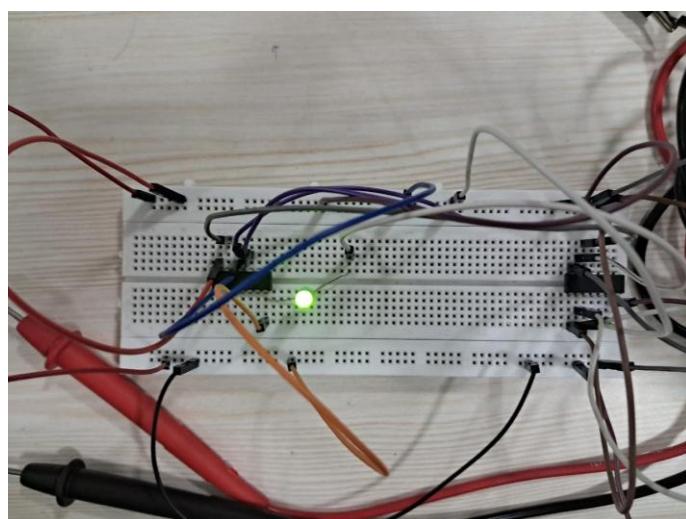
$$Y = (A \cdot B)$$



0 and 0



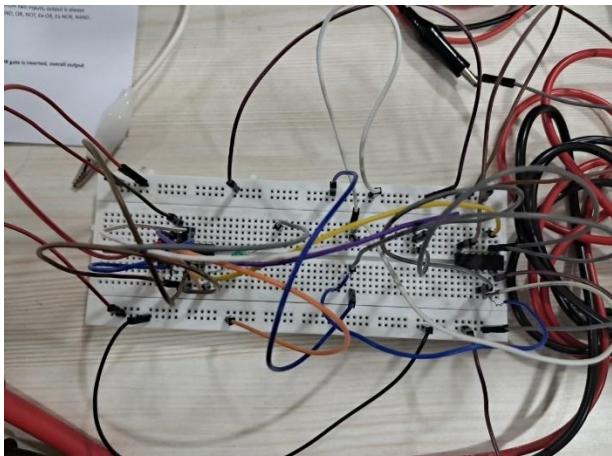
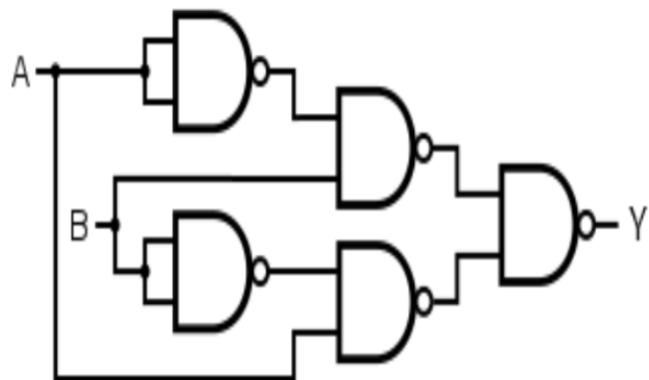
1 and 0 / 0 and 1



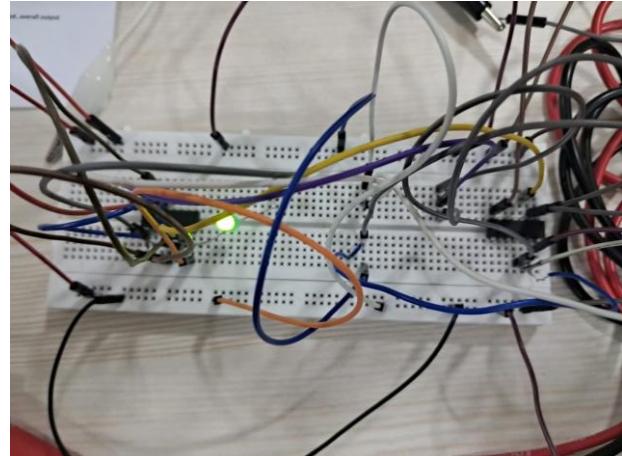
1 and 1

NAND gates as Ex-OR

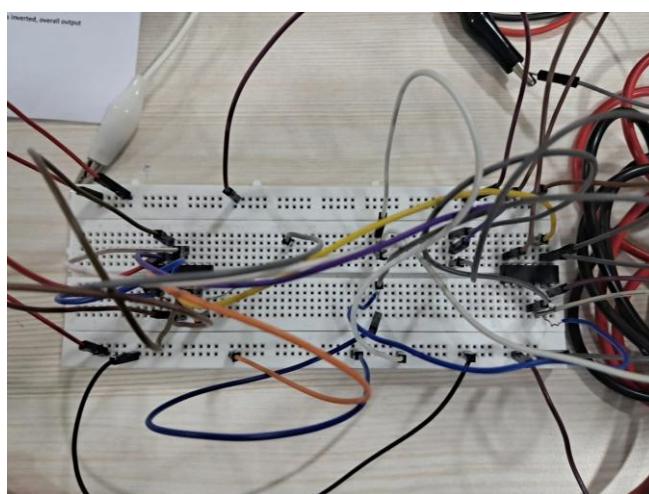
The output of a two input Ex-OR gate is shown by: $Y = A'B + AB'$. This can be achieved with the logic diagram shown in the left side.



0 xor 0



0 xor 1 / 1 xor 0

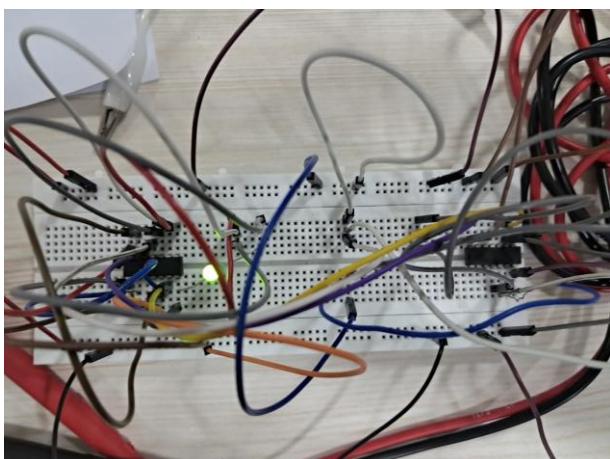
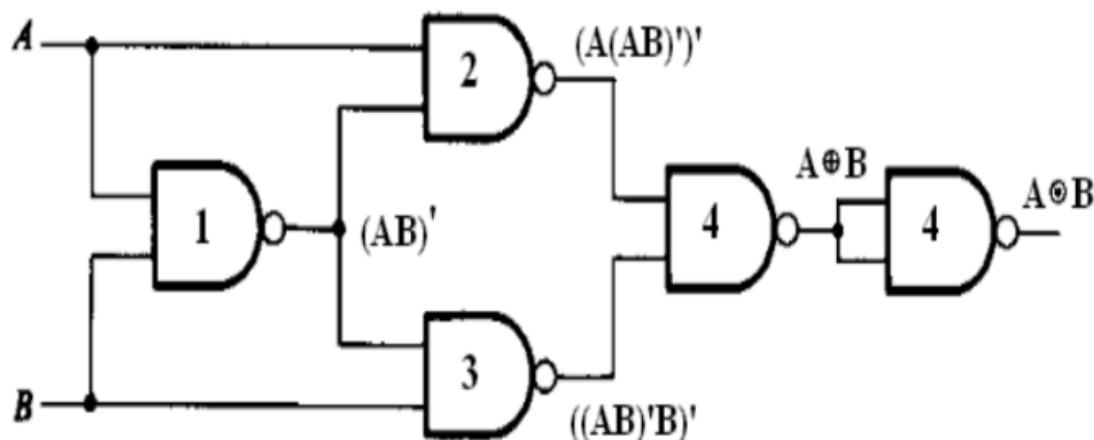


1 xor 1

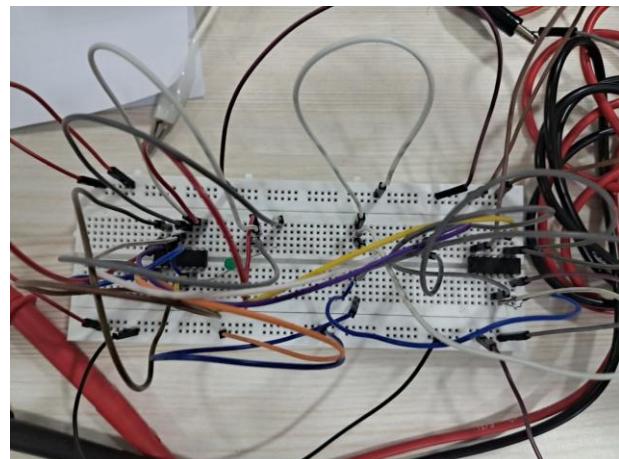
NAND gates as Ex-NOR

Ex-NOR gate is actually Ex-OR gate followed by NOT gate. So give the output of Ex-OR gate to a NOT gate, overall output is that of an Ex-NOR gate.

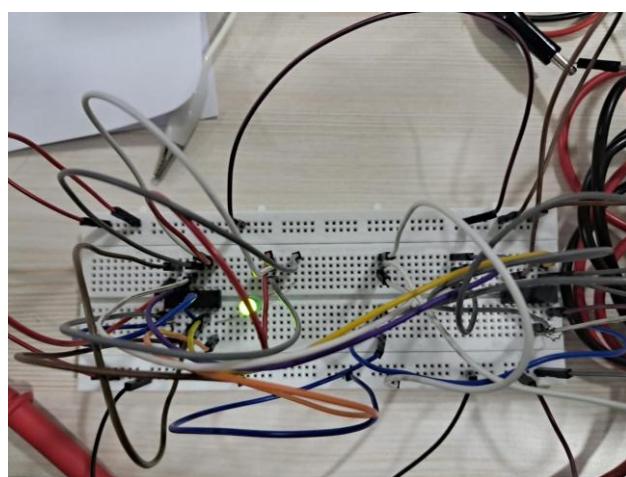
$$Y = AB + A'B'$$



0 n-xor 0



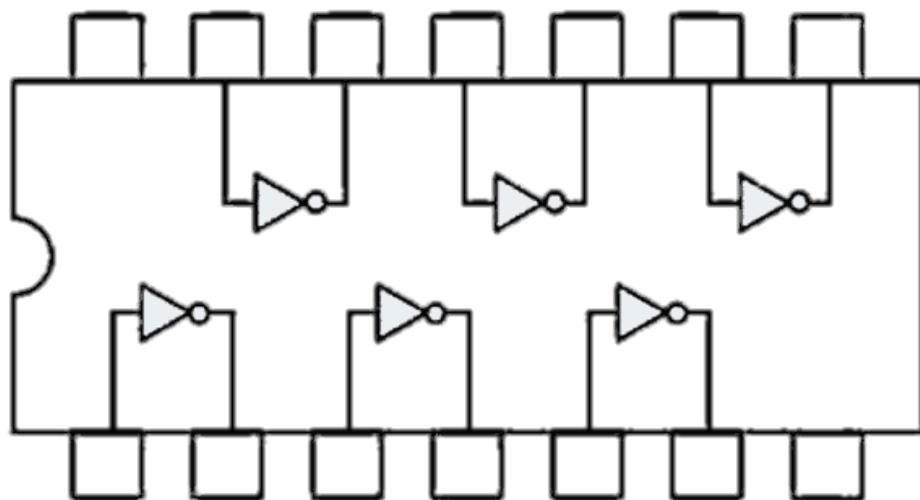
0 n-xor 1 / 1 n-xor 0



1 n-xor 1

NOR

NOR gate is actually a combination of two logic gates: OR gate followed by NOT gate. So its output is complement of the output of an OR gate. This gate can have minimum two inputs, output is always one. By using only NOR gates, we can realize all logic functions: AND, OR, NOT, Ex-OR, Ex-NOR, NAND. So this gate is also called universal gate.

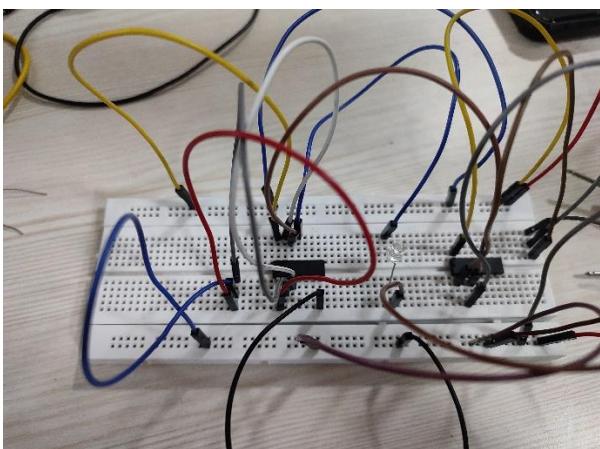
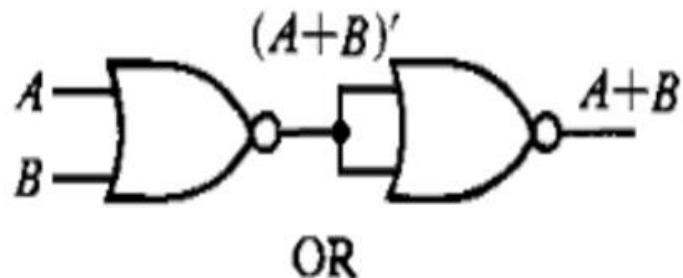


NOR gates as OR

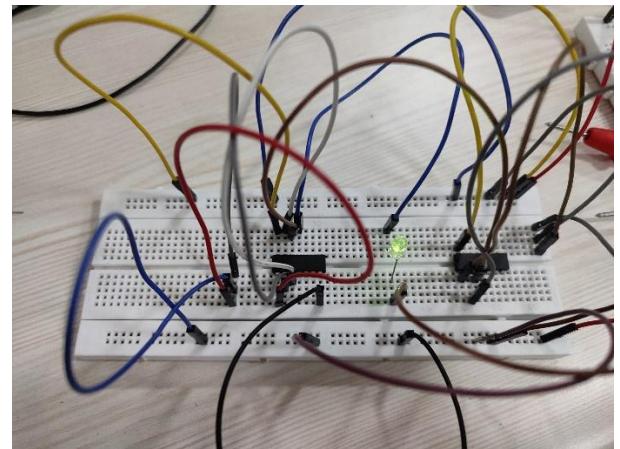
A NOR produces complement of OR gate. So, if the output of a NOR gate is inverted, overall output will be that of an OR gate.

$$Y = ((A + B)')'$$

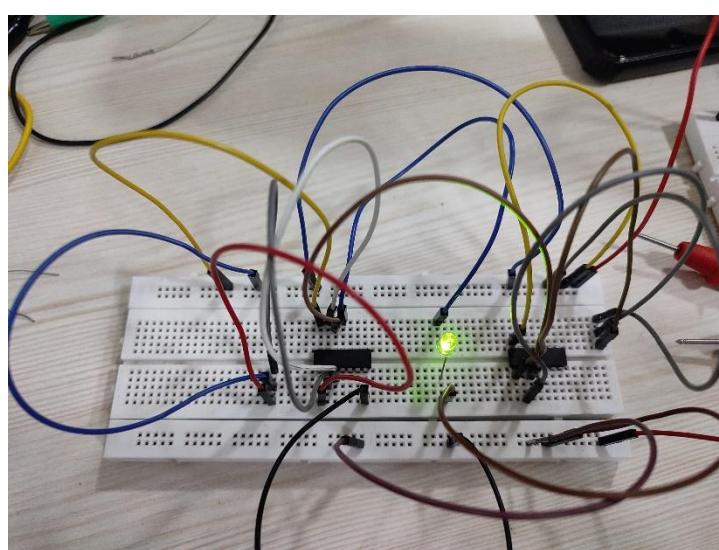
$$Y = (A + B)$$



0 or 0



0 or 1 / 1 or 0



1 or 1

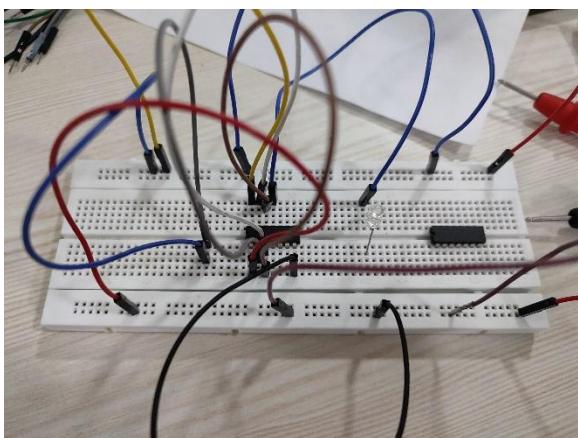
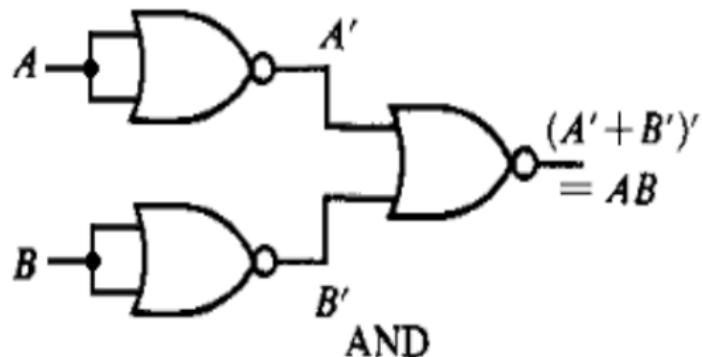
NOR gates as AND

From DeMorgan's theorems:

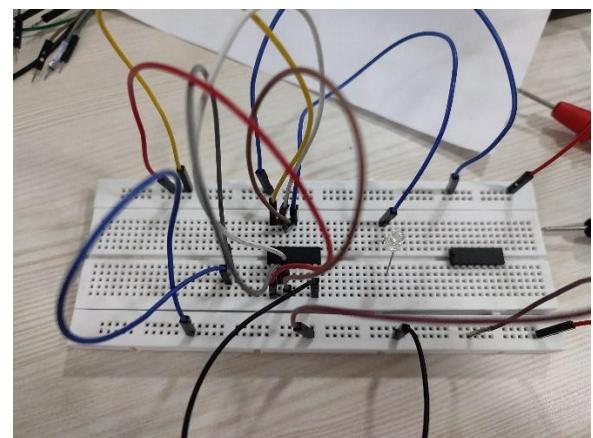
$$(A + B)' = A'B'$$

$$(A' + B')' = A''B'' = AB$$

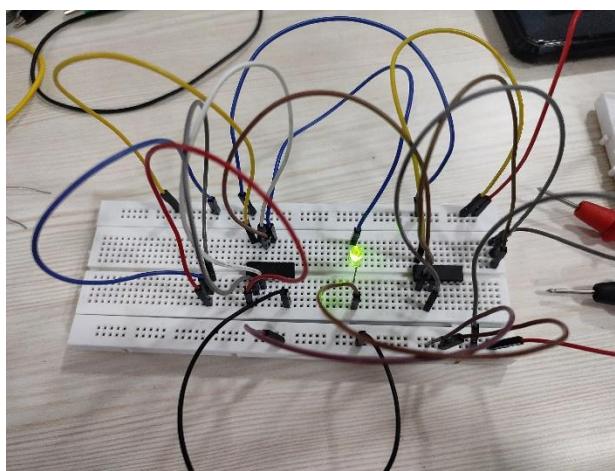
So, give the inverted inputs to a NOR gate, obtain AND operation at output.



0 and 0



0 and 1 / 1 and 0

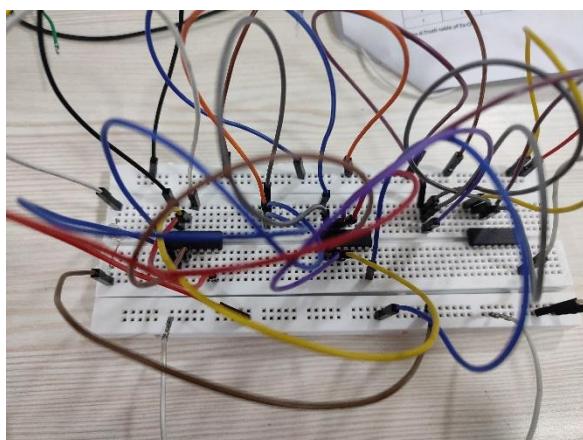
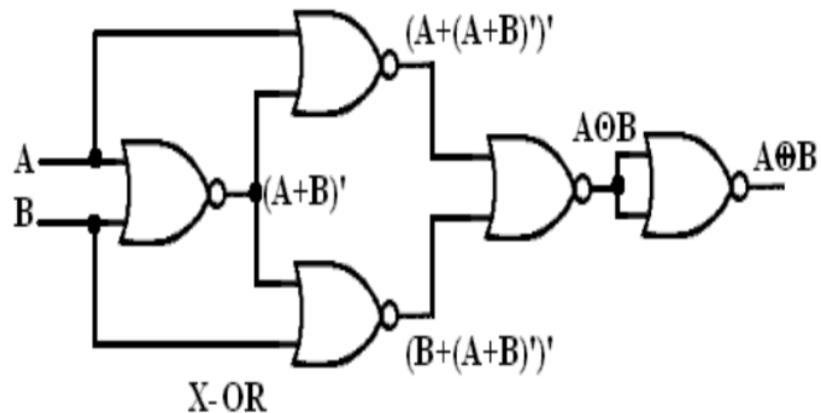


1 and 1

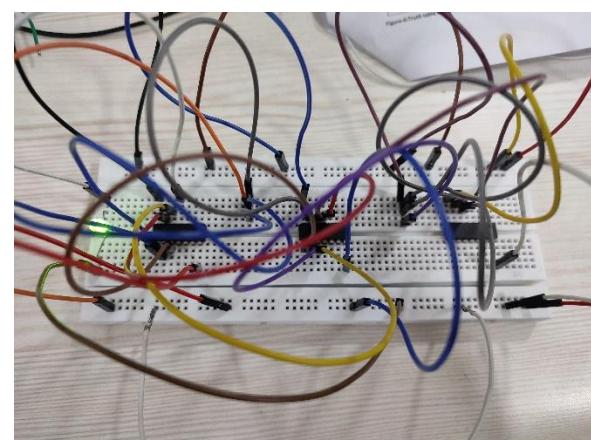
NOR gates as Ex-OR

Ex-OR gate is actually Ex-NOR gate followed by NOT gate. So give the output of Ex-NOR gate to a NOT gate, overall output is that of an Ex-OR gate.

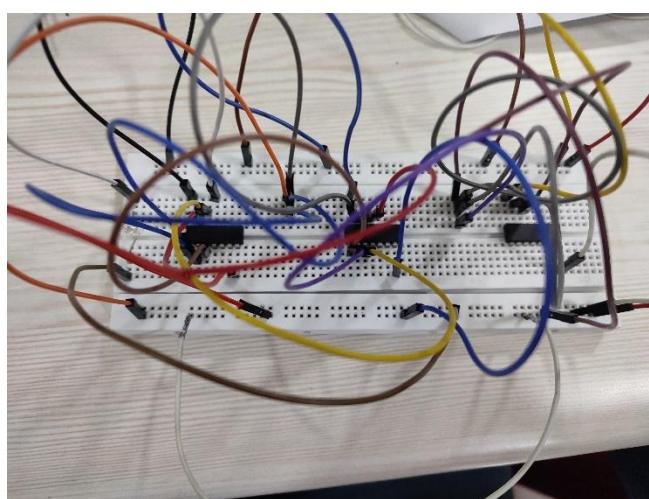
$$Y = A'B + AB'$$



0 xor 0



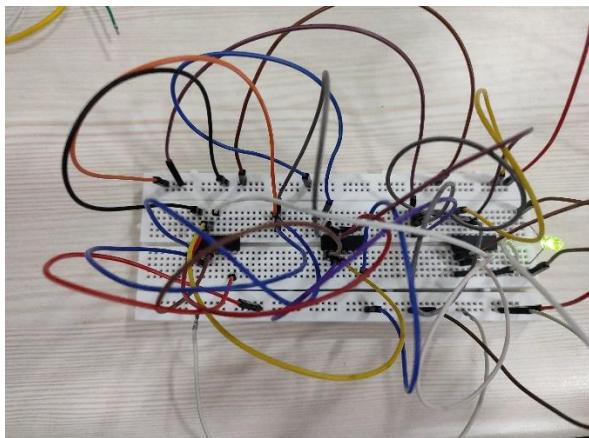
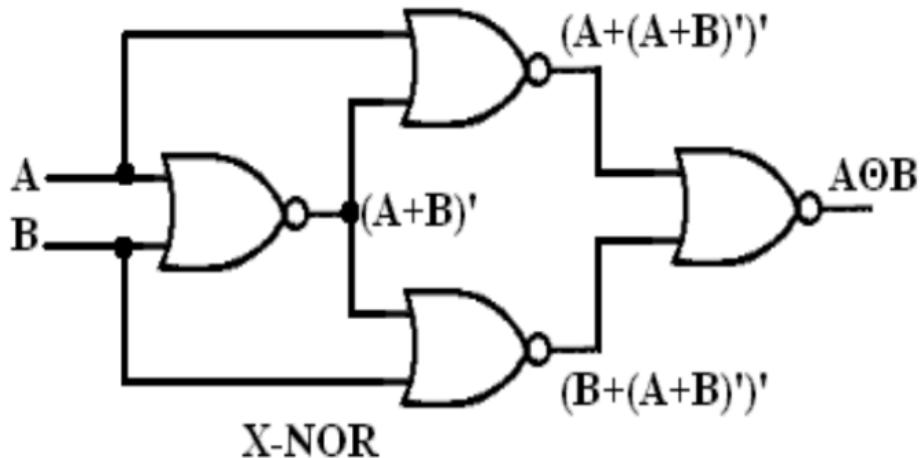
0 xor 1 / 1 xor 0



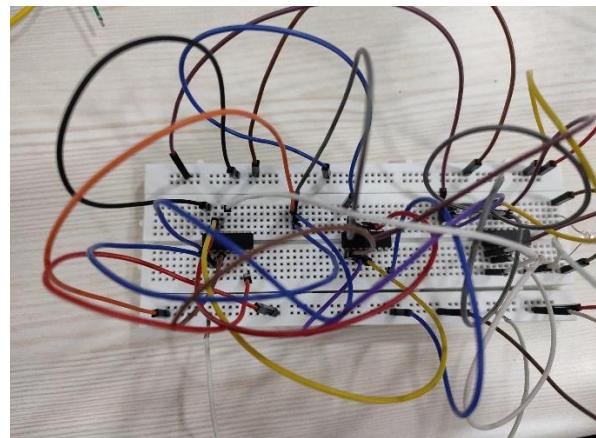
1 xor 1

NOR gates as Ex-NOR

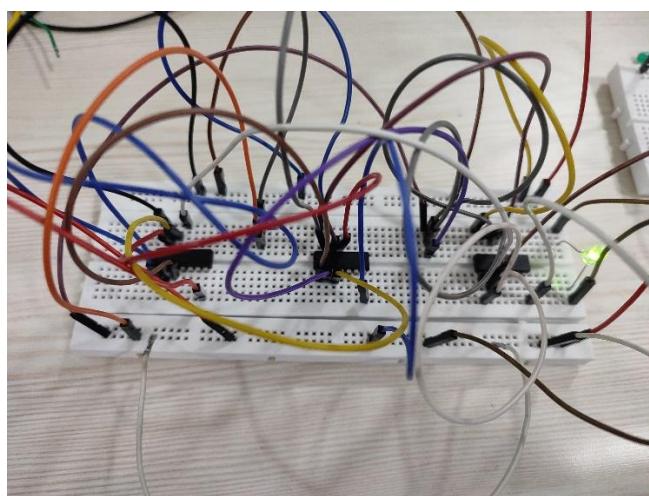
The output of a two input Ex-NOR gate is shown by: $Y = AB + A'B'$. This can be achieved with the logic diagram shown in the left side.



0 x-nor 0



0 x-nor 1 / 1 x-nor 0



1 x-nor 1

Results

The setup done through experiments are along the theory of truth tables. Thus we verify the setup and universality of NAND and NOR gates.

EXP IX : Schmitt Trigger

In partnership with Aditya Pratap Singh (22020)

Objective

To design a Schmitt trigger using Op-amp IC-741.

Theory

The Schmitt trigger converts a non-uniform waveform into a square wave or pulse. This configuration is identified as a squaring circuit. As the input voltage increases, it reaches a critical threshold value (the upper threshold point UTP) at which the output voltage shifts to negative saturation. As the input voltage decreases, it reaches a secondary threshold voltage (the lower threshold point LTP) where the output voltage achieves positive saturation. The output maintains its consistency when the voltage differential between UTP and LTP surpasses the noise threshold.

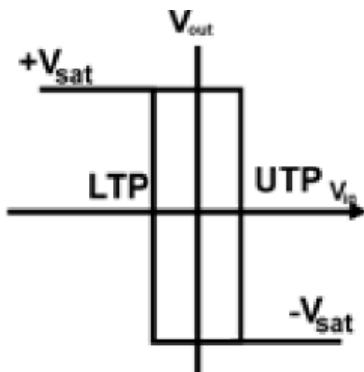
The input voltage V_{in} activates the output V_o whenever it surpasses specific voltage thresholds known as the Upper Threshold Voltage, V_{UTP} , and the Lower Threshold Voltage, V_{LTP} . The threshold voltages are computed as follows.

$$V_{UTP} = \left(\frac{R_1}{R_1 + R_2} \right) V_{sat} \quad \text{when } V_o = V_{sat}$$

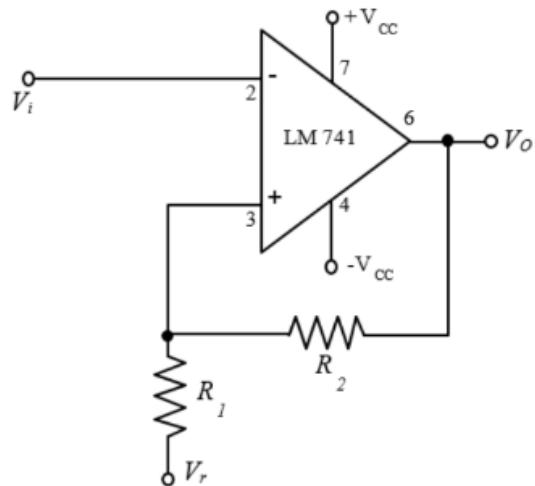
$$V_{LTP} = - \left(\frac{R_1}{R_1 + R_2} \right) V_{sat} \quad \text{when } V_o = -V_{sat}$$

The hysteresis width represents the variation between these two threshold voltages, specifically.

$$H = V_{UTP} - V_{LTP}$$

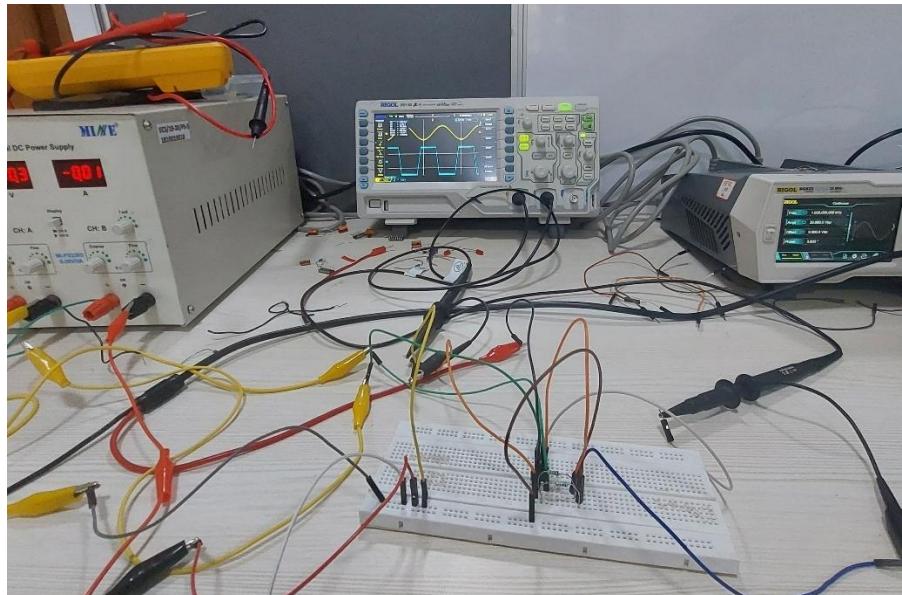
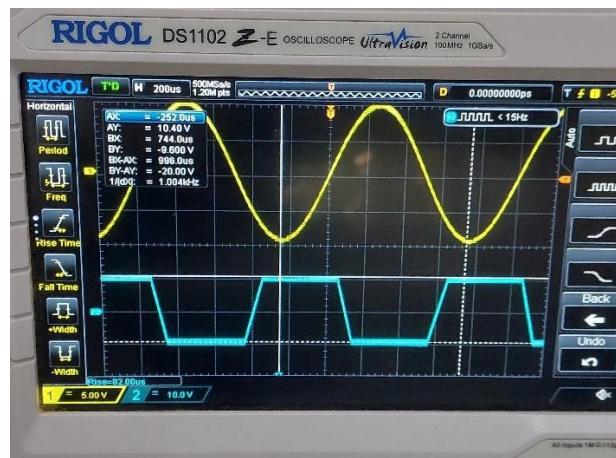
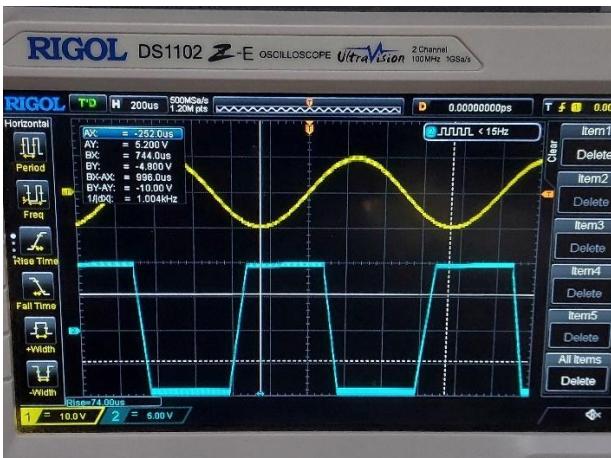


Schematic/circuit diagram:



Results:

(V_r, R_1, R_2)	$+V_{sat}$	$-V_{sat}$	V_{UTP}	V_{LTP}	Hysteresis $(H = V_{UTP} - V_{LTP})$
(0V, 10kΩ, 10kΩ)	9	-9	7	-7	14
(0.5V, 10kΩ, 10kΩ)	9	-9	7.5	-6.5	14
(0V, 10kΩ, 22kΩ)	9	-9	4.38	-4.38	8.76
(0.5V, 10kΩ, 22kΩ)	9	-9	4.88	-3.88	8.76



Discussion

We created the circuit for Schmitt trigger using the given Op-Amp and then noted V_{sat} and $-V_{sat}$ for different V_r , R_1 , R_2 .

Conclusion

It is dependent on the input whether the Schmitt trigger produces a pulse or a square wave, and it can produce either a high or low voltage as an output, depending on the input. Due to the fact that the Schmitt trigger possesses two distinct threshold voltages, it is resistant to noise.

EXP X: Digital Logic using Transistors

In partnership with Aditya Pratap Singh (22020)

Theory

Transistors

Transistors are made of materials like silicon or germanium that allow electrical current to flow through them in a controlled manner. The materials of transistors are doped, or “treated,” with impurities to create a structure called a p-n junction. The notations p and n refer to the type of dopant atoms (impurities) added to the semiconductor material. A transistor consists of three main parts: the emitter, the base, and the collector. The emitter serves as the source of electrons, the collector as the drain, and the base as the control terminal. The BC547 transistor is an NPN transistor. The working states of BC547 transistor include the following:

- Forward bias
- Reverse bias

In a forward bias mode, the two terminals like emitter and collector are connected to allow the flow of current through it. Whereas in a reverse bias mode, it doesn't allow the flow of current through it because it works as an open switch. Transistors are used in a wide variety of electronic devices and equipment like computer, cell phones, space and military applications, etc.

Logic gates

A gate is an electronic device which is used to compute a function on a two valued signal. Generally, all logic gates have one output and two inputs. Some logic gates like NOT or Inverter has only one input and one output. The inputs of the logic gates are designed to receive only binary data (only low 0 or high 1) by receiving the voltage input. Logic gates can be used in manufacturing binary counters, calculators, in decision making regarding automatic control, etc.

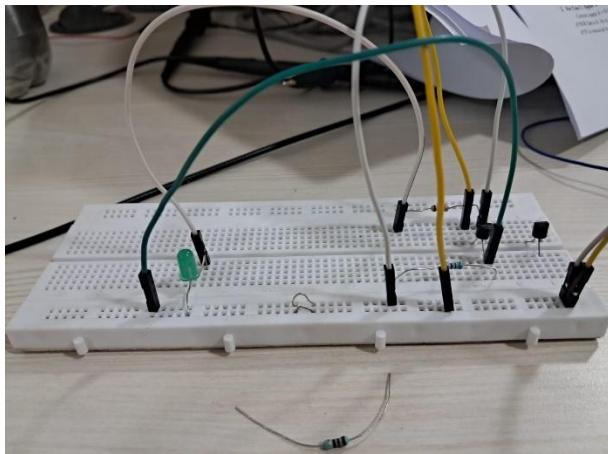
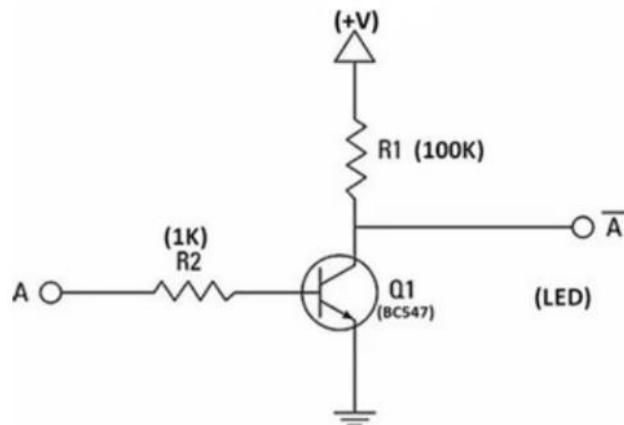
The main advantages of logic gates built using transistors can be summarized as given below:

- Transistors are cheaper than ICs.

- Transistorized logic gates can be operated with voltages as low as 1.5 V, while the IC counterparts need a minimum of 3 V.
- A transistorized logic gate can be customized to control heavier loads, which an IC based logic gate cannot do.

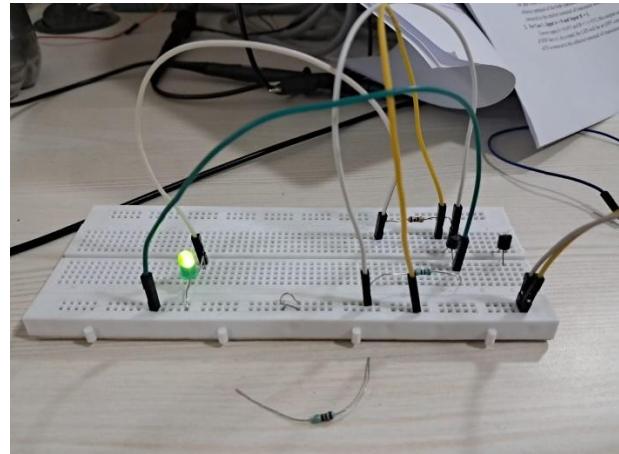
Gates

Not gate

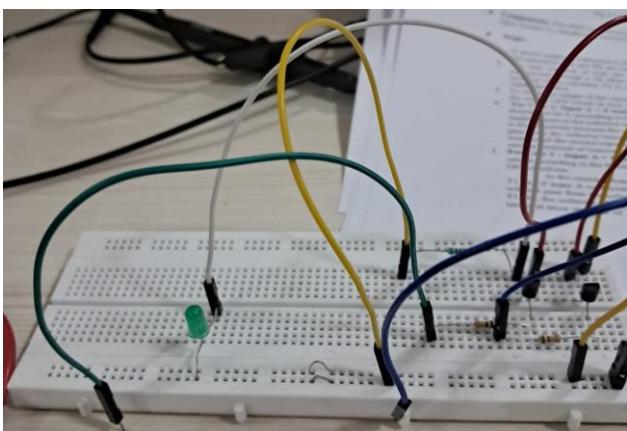
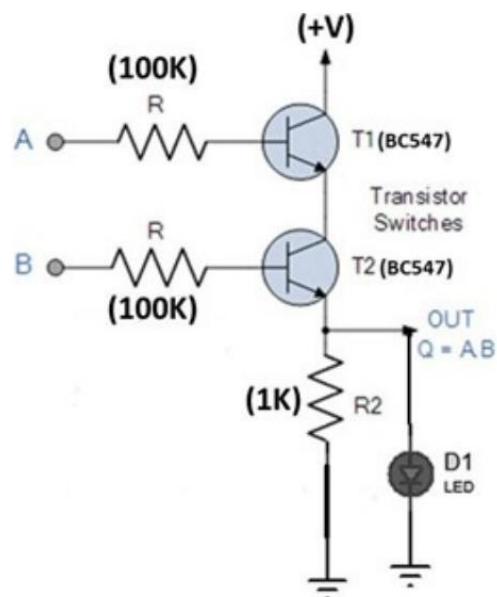


0

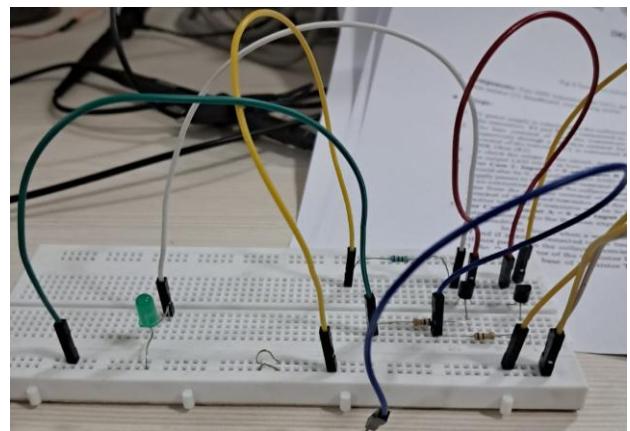
1



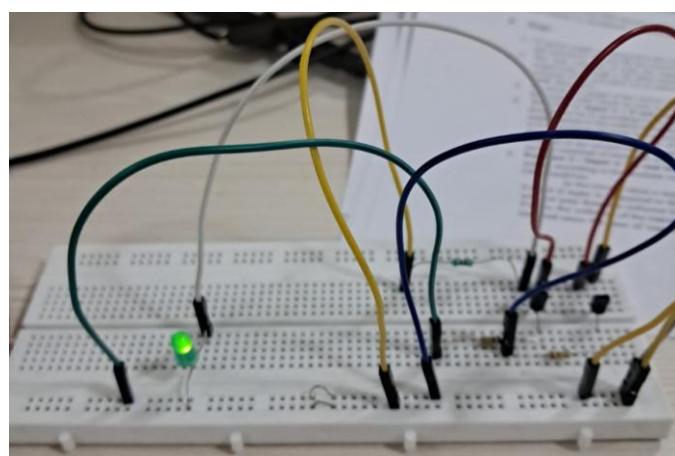
Input	Output
0	1
1	0

And gate

0 and 0



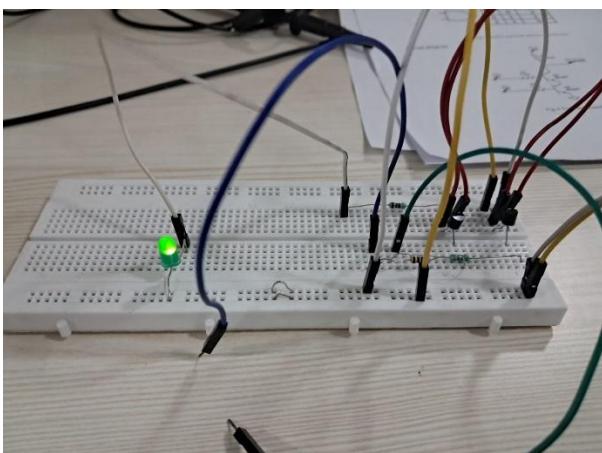
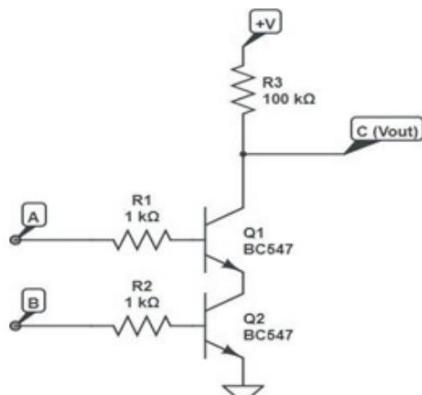
1 and 0 / 0 and 1



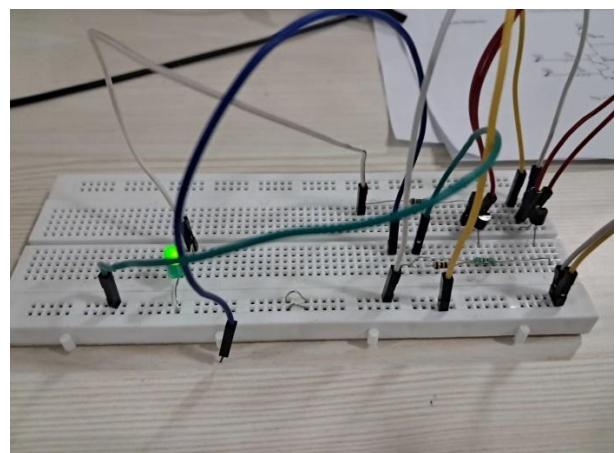
1 and 1

Input	Output
0, 0	0
0, 1 / 1, 0	0
1, 1	1

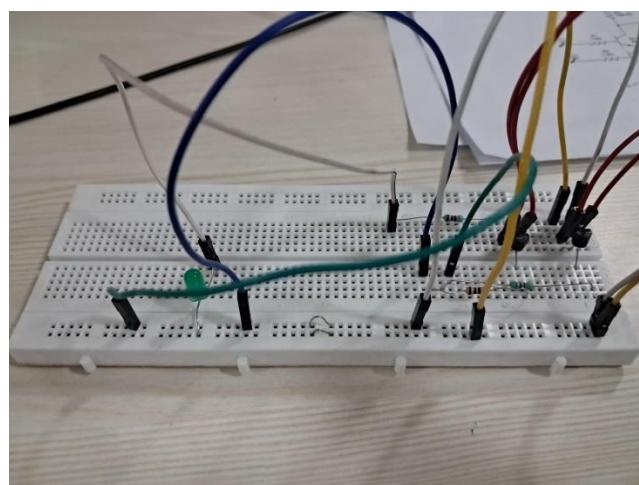
Nand gate



0 nand 0

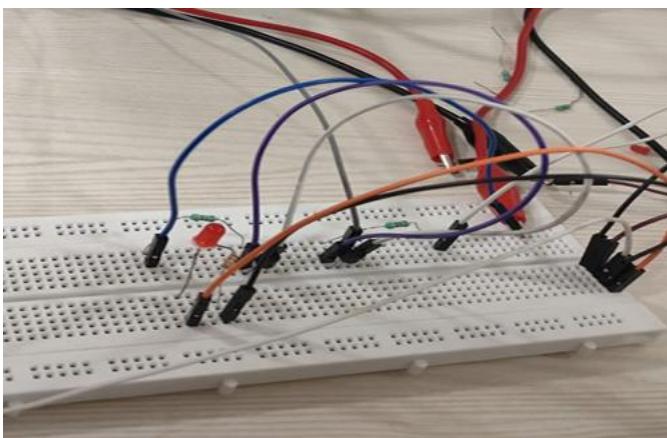
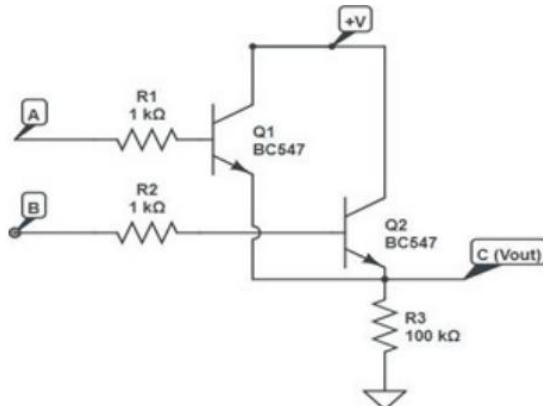


1 nand 0 / 0 nand 1

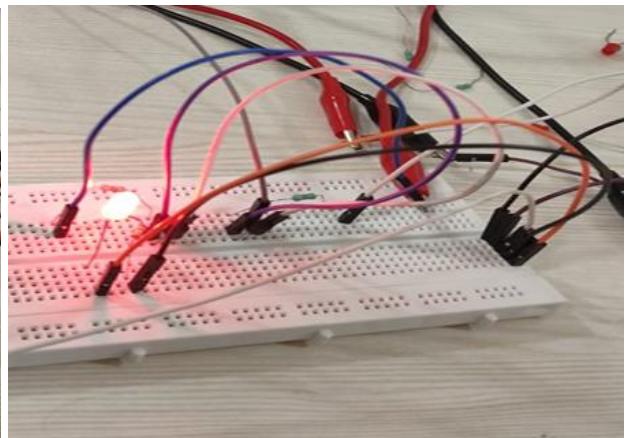


1 nand 1

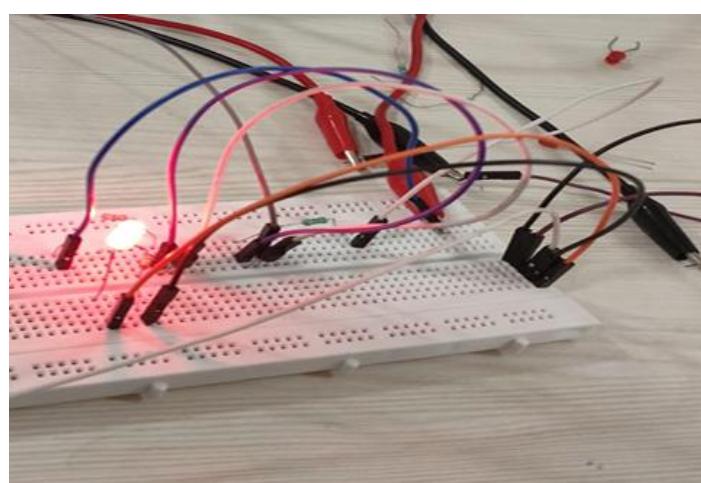
Input	Output
0, 0	1
0, 1 / 1, 0	1
1, 1	0

Or gate

0 or 0

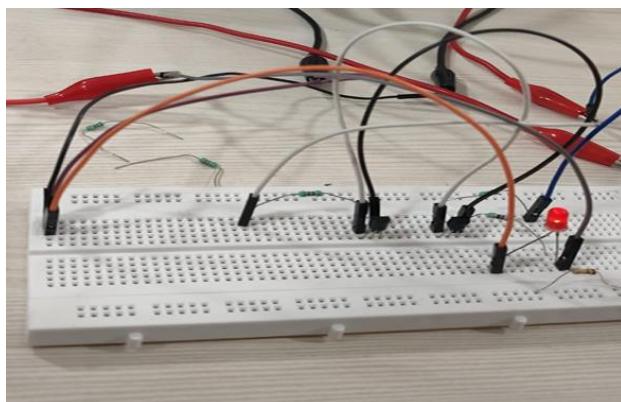
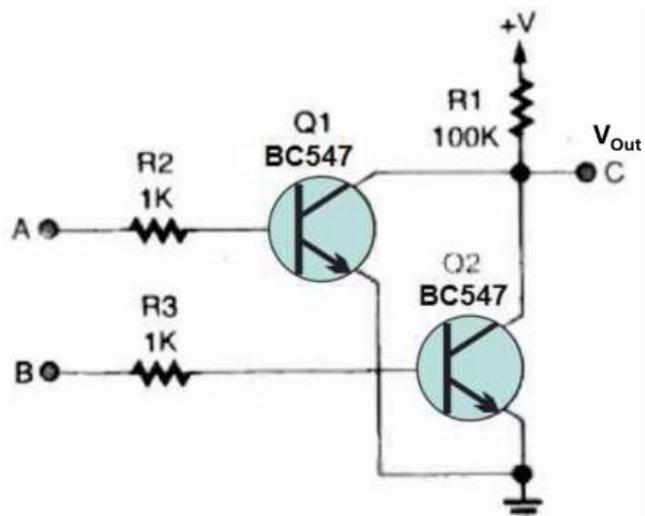


1 or 0 / 0 or 1

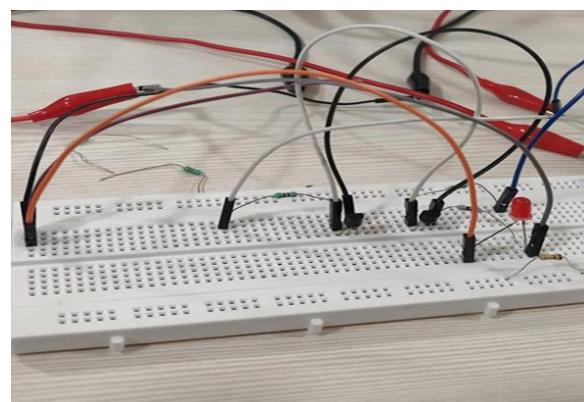


1 or 1

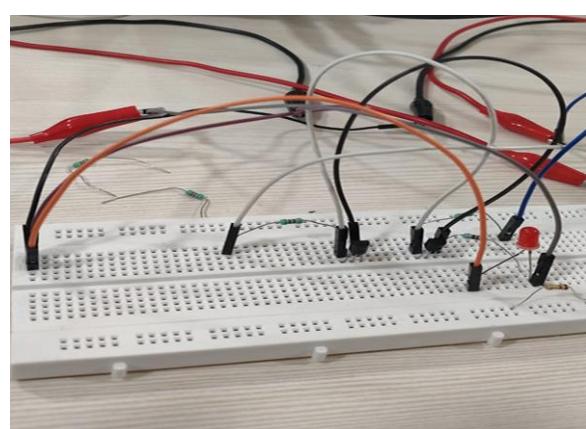
Input	Output
0, 0	0
0, 1 / 1, 0	1
1, 1	1

Nor gate

0 nor 0



1 nor 0 / 0 nor 1



1 nor 1

Input	Output
0, 0	1
0, 1 / 1, 0	0
1, 1	0

Result

We learned how to design NOT, AND, NAND, OR, and NOR gates using Bipolar Junction Transistors (BJTs). This involved understanding the fundamental working principles of BJTs in different modes, such as active, saturation, and cutoff. Each mode allows the transistor to perform distinct functions, which can be harnessed to implement various logic gates.

For instance, in cutoff mode, the BJT behaves like an open switch, while in saturation, it acts like a closed switch, which is crucial for creating reliable digital circuits. We also delved into the active mode, where the transistor can amplify signals, though it's less commonly used in logic gate applications. Beyond just creating basic gates, we explored optimized configurations that enhance the use of BJTs in logic circuits, highlighting their role as versatile components in digital electronics. This gave us a broader perspective on why BJTs are still relevant in designing logic gates and how their different operating regions can be leveraged for specific digital functionalities.

EXP XI: Familiarization with Op-Amp circuits

Objective

1. Design and realize Inverting amplifier using IC741Op-amp.
2. To study the working of op-amp as differentiator.
3. To study the working of op-amp as integrator.

Inverting amplifier using IC741Op-amp

Theory

An inverting amplifier utilizing an operational amplifier is a configuration in which the output waveform is phase-inverted relative to the input waveform. The input waveform will be amplified by the factor A_v (voltage gain of the amplifier) in magnitude, and its phase will be inverted. The signal intended for amplification is introduced to the inverting input of the operational amplifier via the input resistor R_1 . R_f denotes the feedback resistor. R_f and R_{in} collectively dictate the amplifier's gain. The gain of an inverting operational amplifier can be articulated using the equation

$$A_v = -\frac{R_f}{R_1}$$

Negative sign implies that the output signal is negated.

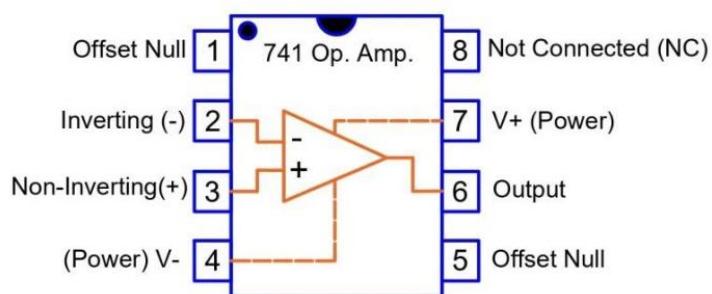


Fig.1.2: schematic of 741 OP-AMP

where

A_v is voltage gain

R_f is the feedback resistor value

R_1 is the input resistor value

There are two very important rules to remember about Inverting Amplifiers or any operational amplifier for that matter and these are.

- No Current Flows into the Input Terminals
- The Differential Input Voltage is Zero as $V_1 - V_2 = 0$ (Virtual Earth)

$$i = \frac{V_{in} - V_{out}}{R_{in} + R_f}$$

$$\text{therefore, } i = \frac{V_{in} - V_2}{R_{in}} = \frac{V_2 - V_{out}}{R_f}$$

$$i = \frac{V_{in}}{R_{in}} - \frac{V_2}{R_{in}} = \frac{V_2}{R_f} - \frac{V_{out}}{R_f}$$

$$\text{so, } \frac{V_{in}}{R_{in}} = V_2 \left[\frac{1}{R_{in}} + \frac{1}{R_f} \right] - \frac{V_{out}}{R_f}$$

$$\text{and as, } i = \frac{V_{in} - 0}{R_{in}} = \frac{0 - V_{out}}{R_f} \quad \frac{R_f}{R_{in}} = \frac{0 - V_{out}}{V_{in} - 0}$$

$$\text{the Closed Loop Gain (Av) is given as, } \frac{V_{out}}{V_{in}} = -\frac{R_f}{R_{in}}$$

Equipment required

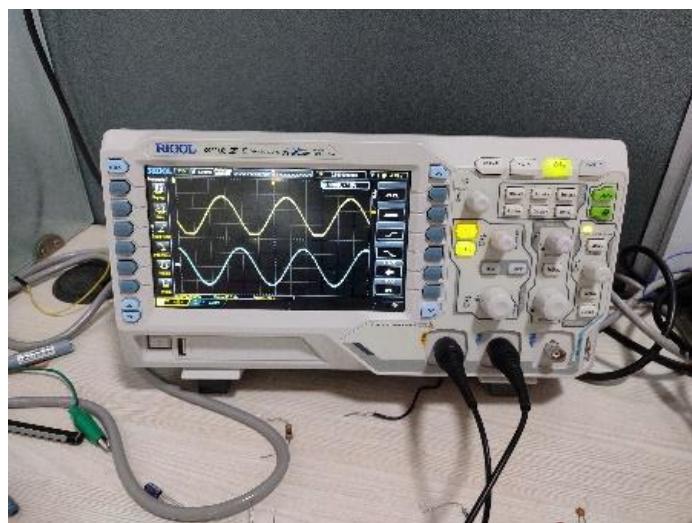
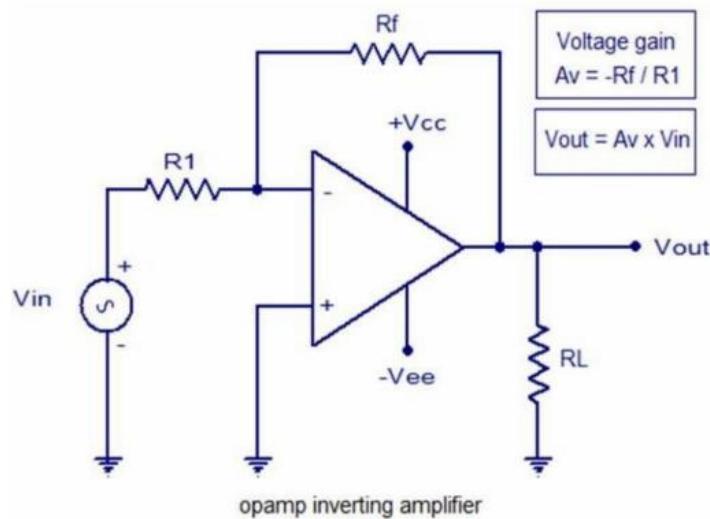
1. Function Generator
2. Op-amp (IC-741)
3. Resistors ($R_1=1\text{k}\Omega$, $R_f=10\text{k}\Omega$)
4. Dual power supply for supply of 10V

Procedure

- To obtain 3 different gain Av for different value of R_f
- Make the circuit shown in Figure in a breadboard or kit provided
- Apply the input signal V_{in} in the inverting terminal of

Observation Table

S. No.	V_{in} (V _{pp})	V_{out} (V _{pp})	R_{in} (kΩ)	R_{out} (kΩ)	A _v
1.	1	6.3	10	1	6.3



Working of OP-Amp differentiator

Theory

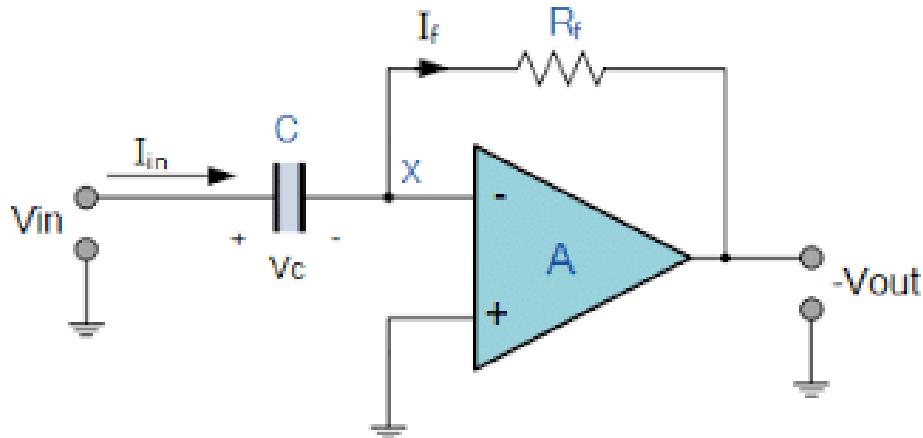
An operational amplifier differentiator is a circuit arrangement that generates an output voltage amplitude proportionate to the rate of change of the input voltage. It signifies that a variation in the input voltage signal will promptly result in a corresponding change in the output voltage.

$$V_{OUT} = -R_f C \frac{dV_{IN}}{dt}$$

The output voltage V_{out} is a constant equal to $-R_f * C$ multiplied by the temporal derivative of the input voltage V_{in} . The minus sign ($-$) signifies a 180° phase shift due to the connection of the input signal to the inverting input terminal of the operational amplifier.

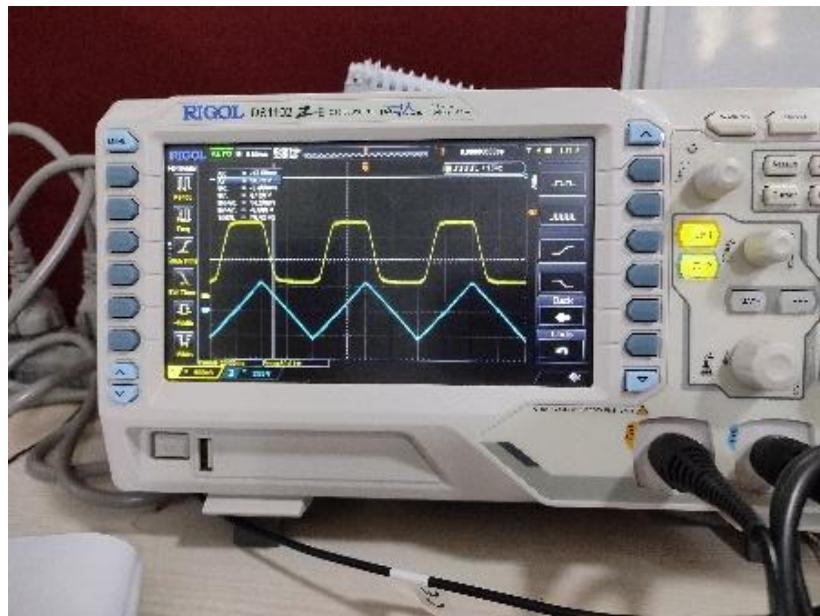
Procedure

- Make the circuit shown in figure in a breadboard
- C and R_f is fixed
- Apply the input signal V_{in} (Triangle wave)
- Check the corresponding output



Result

For a triangle wave input we get amplified square wave as output.



Working of OP-Amp as integrator

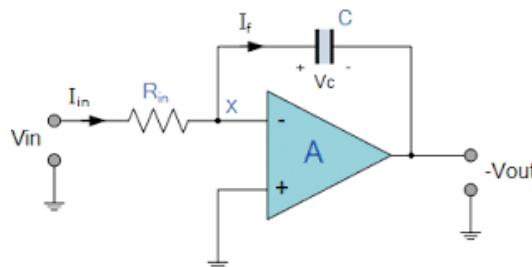
Theory

An op-amp integrator is an inverting amplifier whose output voltage is proportional to the negative integral of the input voltage, thereby replicating mathematical integration. The output voltage, V_{out} , is equivalent to the constant $-1/RC$ multiplied by the integral of the input voltage, V_{in} . Integrates (and inverts) the input signal $V_{in}(t)$ across the time period t , where $t_0 < t < t_1$, resulting in an output voltage at time $t = t_1$ of

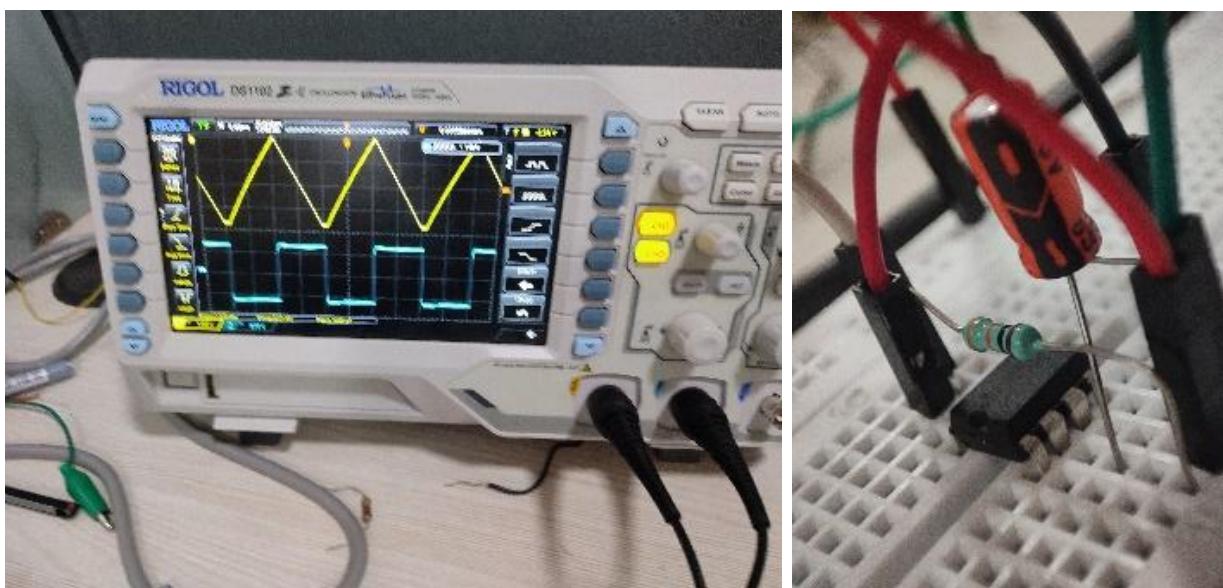
$$V_{OUT} = -\frac{1}{R_{IN}C} \int_0^t V_{IN} dt = -\int_0^t V_{IN} \frac{dt}{R_{IN}C}$$

Procedure

- Make the circuit shown in figure in a breadboard
- C and R_f is fixed
- Apply the input signal V_{in} (Square wave)
- Check the corresponding output



Results



Discussion

We initially construct the circuit for the inverting amplifier and validate the outcomes. Subsequently, we convert R₁ into a capacitor and construct a differentiating circuit. Subsequently, we interchange R_f and the capacitor to construct an integrating circuit.

An inverting amplifier, a differentiating circuit, an integrating circuit, and a great number of other circuits can all be created with the help of operational amplifiers, which are powerful devices that can be used to generate a wide variety of different circuits.