## EE2003: Computer Organisation

Indian Institute of Technology, Madras (Jul - Nov '23)

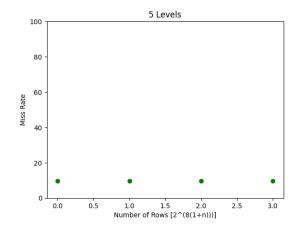
## Assignment 3: ChampSim Arnav Mahajan [EP21B004]

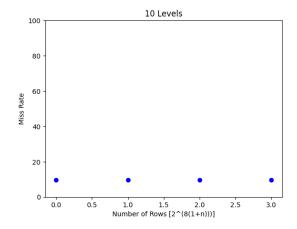
(P7) Plot the DTLB Miss Rate by varying the Physical Page size keeping the Virtual Memory size constant (at least 4 different sizes of rows). Also vary the number of levels of tables (at least 2 values including default). Analyze the result.

Tests

Sr. No.	Levels	Rows	DTLB Access	DTLB Miss	DTLB Miss Rate
1	5	$256 (2^8)$	21307082	2060264	9.6694%
2	5	$65536 (2^{16})$	21308911	2061138	9.6727%
3	5	$16777216 (2^{24})$	21308911	2061138	9.6727%
4	5	$4294967296 (2^{32})$	21308911	2061138	9.6727%
5	10	$256 (2^8)$	21307082	2060264	9.6694%
6	10	$65536 (2^{16})$	21308911	2061138	9.6727%
7	10	$16777216 \ (2^{24})$	21308911	2061138	9.6727%
8	10	$4294967296 (2^{32})$	21308911	2061138	9.6727%

## **DTLB Miss Rate**





## System Cache Configurations

Systems Cache Configurations obtained using the command 1scpu:

```
Architecture: x8 ds ds cCPU op. mode(s): x8 ds ds cPU op. x8 ds cPU op. x8
```