Preliminary Proposal Draft

I^2C Interface for APB

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1.0 Executive Summary

In current day and age it is often difficult and tedious to connect the current generation of chips to an external device. Most devices require an I^2C bus to connect, however the current chip iteration does not contain an I^2C bus. To rectify this issue, our team proposes that an I^2C bus is implemented on the next iteration of the chip. By implementing this common device standard, your chip will soon be able to communicate with even more devices (additional 1008 devices).

While the I^2C is a universally used standard, our iteration will set the new industry standard. Our current design includes flexibility for both master and slave control, an interface for connecting to an APB bus, and FIFO registers for storing data. Master mode allows the I^2C to control any devices connected to the I^2C bus, while slave allows these devices to send data to your chip. Including both a master and slave mode increases the flexibility and possible uses for your chip. In addition to a master and slave mode the I^2C bus will have flexible data transmission rates, opening the doorway for communication with even more devices.

Another important aspect of our proposal is the inclusion of an APB slave. This APB slave allows our interface to be quickly implemented into any pre-existing chip with an already created APB bus. In addition to an APB slave our proposal includes FIFO registers. FIFO registers provide a safe and efficient way of storing data for use on or off the chip. This registers work in conjunction with the APB slave to create an efficient and universal method of communication to the rest of your chip.

In addition, the device features two circular FIFO buffers, one for data to be transmitted, and one for data that has been received. This allows the module to send or receive several bytes of data consecutively without requiring intervention from the core. This simplifies software design and also frees up more clock cycles for the core.

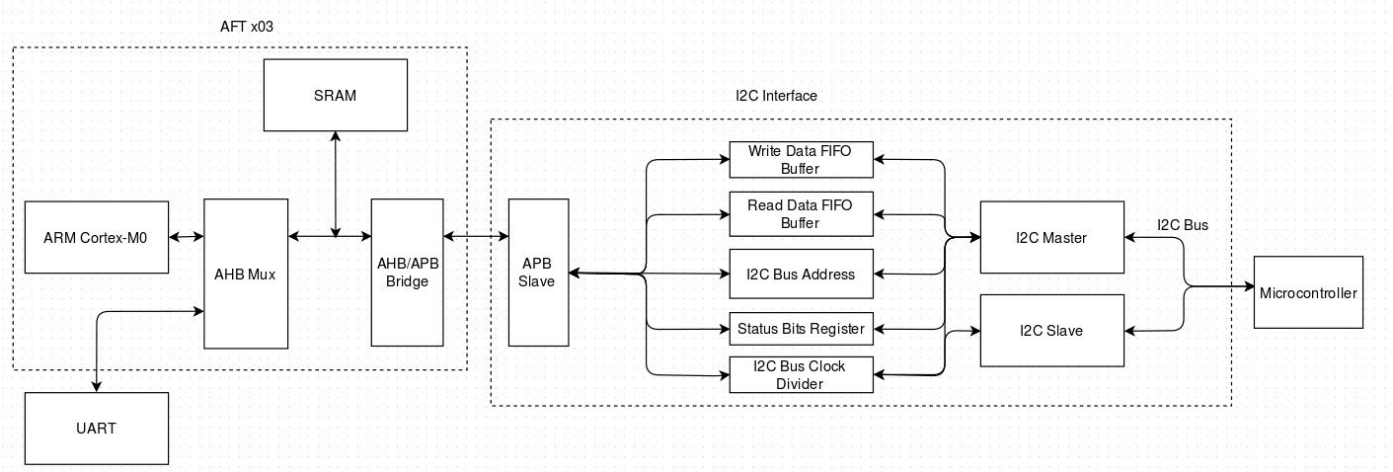
While all of these features sound great, it is also important to note the cost of implementing our interface. Our interface comes with the benefit of easy integration onto a pre-existing chip, so you will not have to worry about developing another device. In addition our interface will take up a relatively small amount of area on the chip, so the increase in chip complexity will not be an issue.

The rest of the proposal will provide the necessary technical details of the chip. Future proposals will delve even further into these details.

2.0 Design Specifications

2.1 System Usage

2.1.1 System Usage Diagram



2.1.2 Implemented Standards and Algorithms Overview

Inter Integrated Circuit Communication (I^2C):

- Mode (Master/Slave): Both
- Master Baud Rate: Adjustable (10kHz, 100kHz, 400kHz, 1MHz)
- Addressing mode (10bit/7bit): Adjustable
- Repeated Start: Implemented

ARM Advanced Peripheral Bus (APB)

- 32 bit wide data
- 32 bit wide address

First In First Out Receive/Transmit Buffers (FIFO):

- 16 byte long circular buffer
- Method of determining Empty/Full: An external buffer counters

2.2 Design Pinout

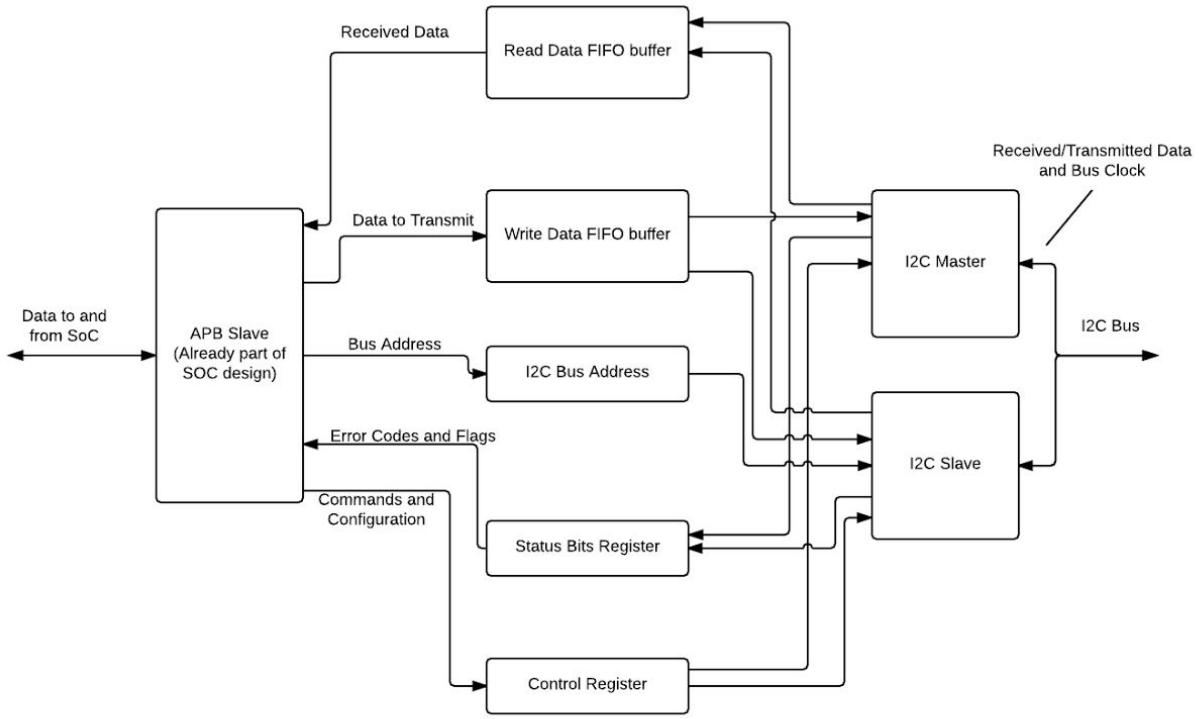
Table 2.2.1 : APB Interface Design Pinout

Signal Name	Type (Input/Output)	Number of Bits	Description
PCLK	Input	1	The System Clock. (Variable frequency)
PRESETn	Input	1	The Active Low reset signal.
PADDR	Input	32	The address bus line coming from the APB Slave Interface.
PSELx	Input	1	The select signal generated by the APB slave interface to select a slave ‘x’ for data transmission.
PENABLE	Input	1	The Active High enable signal that indicates subsequent cycles of APB data transfer.
PWRITE	Input	1	The write signal that indicates the direction of movement of data. This signal indicates APB write access when Active High and APB read access when Active Low.
PWDATA	Input	32	This is the signal that contains the data that needs to be written to the Slave.
PREADY	Output	1	The ready signal used by Slave to extend an APB transfer.
PRDATA	Output	32	This is the signal that contains the data that needs to be read from the Slave. This signal is driven by the selected slave during read cycles when PWRITE is LOW.
PSLVERR	Output	1	This is the Slave error signal that indicates the a failure in APB transfer.

Table 2.2.2 : I^2C Interface Design Pinout

SDA	Bi-directional	32	This is the signal that contains the data. Data is always placed on SDA when SCL goes LOW and sis sampled when the SCL goes HIGH.
SCL	Bi-directional	1	This is the clock signal that is generated by the current master. It might be forced to LOW by some slave devices when they need more time in generating data before the data being clocked out by the current master.

3.0 Design Architecture



Component	Description
APB Slave	This component allows the SoC to communicate with the I^2C by reading from and writing to its registers
Read Data FIFO Buffer	A circular buffer to store data that has been received
Write Data FIFO Buffer	A circular buffer to store data to be transmitted
I^2C Bus Address	A register to store the address that the I^2C slave will respond to
Status Bits Register	A register to hold flags such as buffer overflow, or transmission complete
Control Register	A register to store configuration information, for example 7 bit address mode vs 10 bit address mode.
I^2C Master	The I^2C Master that will read and write to slaves on the I^2C bus

I^2C Slave	The I^2C Slave that will respond to masters on the I^2C bus