I^2C Interface for APB

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We are planning to make an I^2C module containing a Master and Slave. The I^2C Master communicates with other slaves on the bus, which may be sensors or other microcontrollers. The Slave portion of the I^2C can be utilized to communicate on the bus with another microcontroller as well as the master. The I^2C controller will also be connected to a Advanced Peripheral Bus (APB), allowing it to be integrated into a System on Chip (SoC) design.

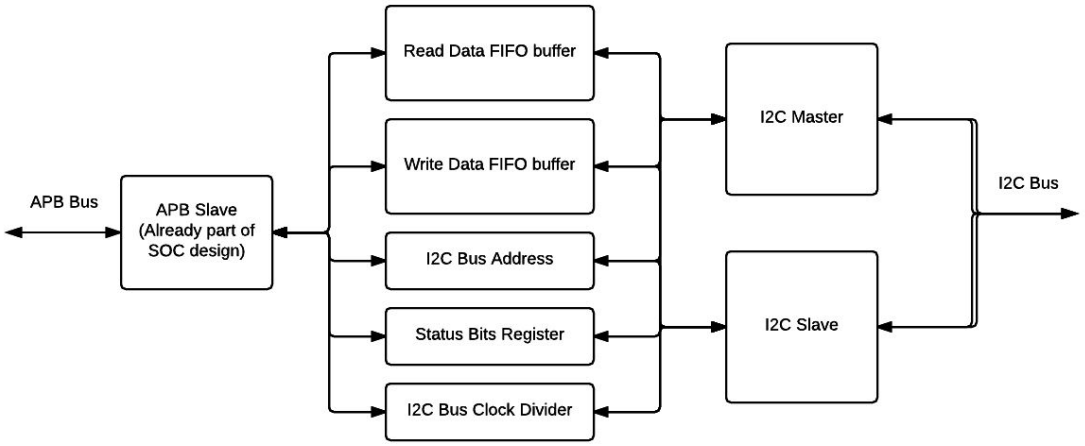
We chose this project because we are members of Professor Johnson's System on a Chip Extension Technologies (SoCET) team. The current design of the SoC has many communication modules such as SPI and UART, but does not yet have a I2C module. This is a very common protocol and would make a valuable addition to the design.

We are also making First Input First Output (FIFO) Buffers for writing and reading data from the APB. The commands from the Processor will be queued in the FIFO Buffers. The I^2C controller would have interrupts that generate flags instructing the shift registers to shift in and shift out the data bits being transmitted to and received from the slaves.

Utilizing a read buffer on the input data can help prevent data overrun errors from occurring when reading multiple bytes simultaneously. Similarly, using a write buffer on the output data can allow the core to schedule an array of data to be written and perform other tasks while the I^2C module transmits it on the bus.

The reason we are creating a new module, rather than implementing it on a microcontroller is because of the sheer complexity of the project. If we wanted to utilize a 9S12 for this project then a large issue would arise in the amount of computation time. The 9S12 would only be able to interface with a select few devices before being bogged down. Designing the I^2C to be its own module allows us to interface to multiple devices without lowering the processor speed.

Top Level Block Diagram



Brief Description of Functional Blocks

Block	Description
APB Slave	A block that already exists as part of the SOC design. It communicates with the APB bus to put data into and read from the registers and buffers in the I2C module
Read Data FIFO Buffer	A FIFO buffer to store data read from the I2C bus
Write Data FIFO Buffer	A FIFO buffer to store data to be written to the I2C bus
I2C Bus Address	The address of the I2C module to be addressed by other modules if it is a slave
Status Bit Register	A register to store flags such as overrun error, write complete, data ready, mode of operation (Master or Slave), ect.
I2C Bus Clock Divider	If the I2C is in Master mode, the value to divide the clock by to generate SCK on the I2C Bus