Arnav Surve

CNIT 176

Lab 06

10/5/2022

Combinatorial Circuits

A	B	C	(A'B' + C)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

Figure 1: Truth table for (A'B' + C)

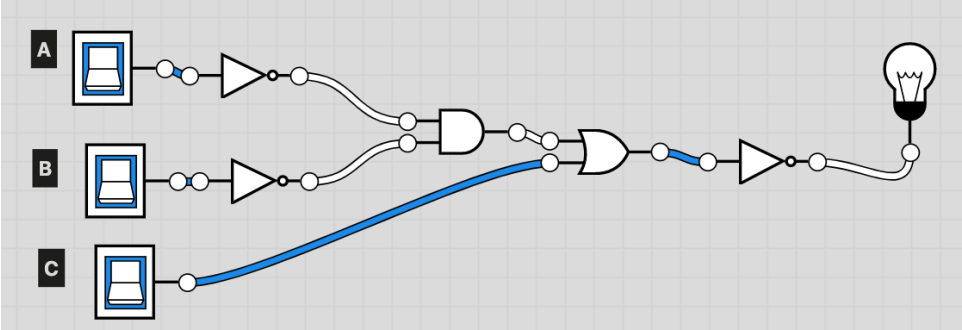

Figure 2: (A'B' + C) gate

Summary: In general, the gate is only true when C is true while either A or B are true, or both A & B are true.

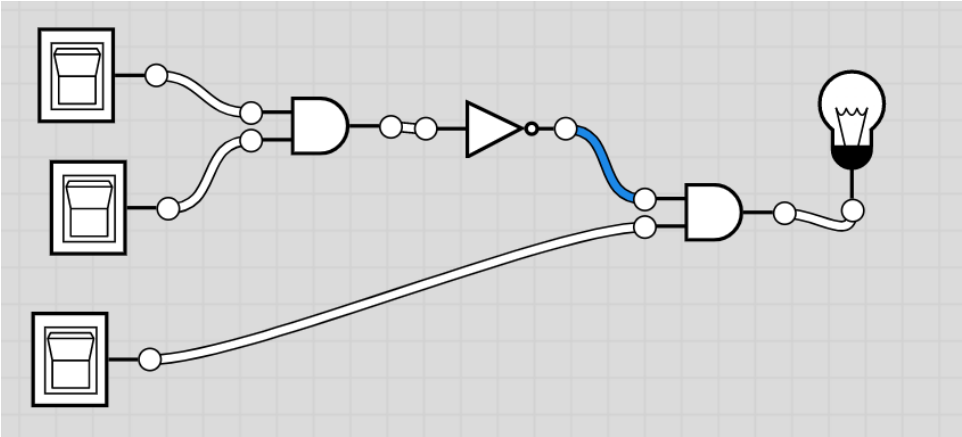

Figure 3: Combinatorial circuit 2

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

Figure 4: Truth table for combinatorial circuit 2

Compared to the first combinatorial circuit, this circuit is true only when C is true and either A or B are true. The circuit is **not true** when A and B are both true but **is true** when they are both false (while C is on).

Sequential Circuits

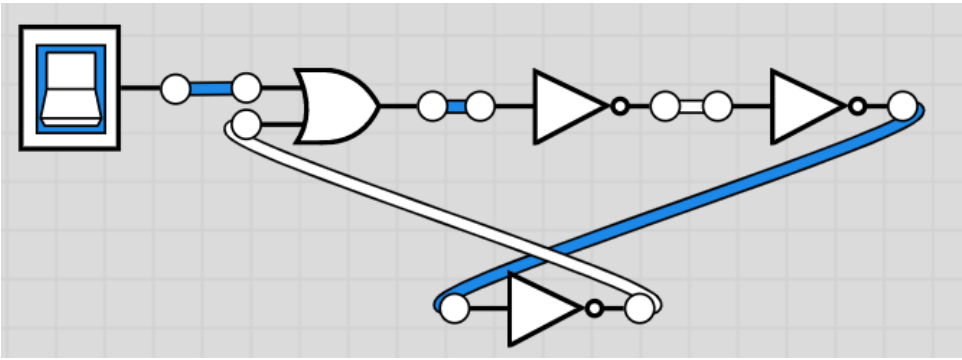

Figure 5: Ring oscillator

Previous Output	Current Output
0	1
1	0

Figure 6: Ring oscillator state table

The output of the last NOT gate is blinking at a rate of approx. 6 oscillations/second. I found this by slowing down a screen recording of the oscillator running and counting the number of times the output of the last NOT gate oscillates in the span of 1 second.

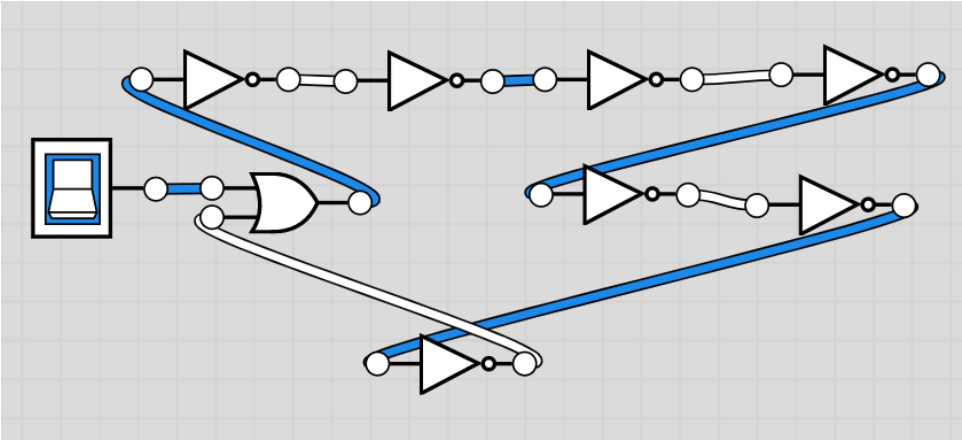

Figure 7: Longer ring oscillator

Using the same screen recording method that I used for figure 5, I observed the oscillation rate of the final NOT gate was 5 oscillations/second. I used 7 NOT gates in this example, 4 more than the initial ring oscillator. From these results, I can infer that an increased number of gates correlates with a lower clock speed, and vice versa.

SR Flip Flop

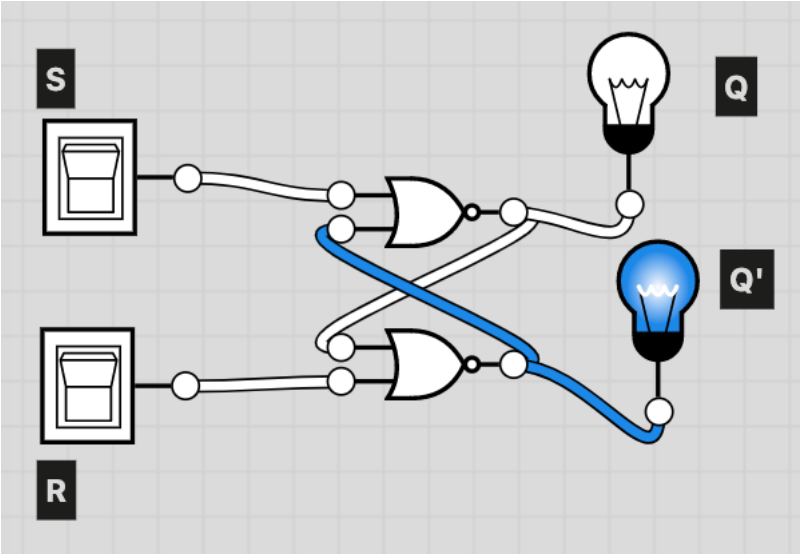

Figure 8: SR Flip Flop

S	R	Previous Q	Current Q	Current Q’
1	0	1	1	0
1	1	1	0	0
0	1	0	1	0
1	1	0	0	0
0	0	0	0	1

Figure 9: SR Flip Flop state table

SR Flip Flop with DeMorgan’s Law

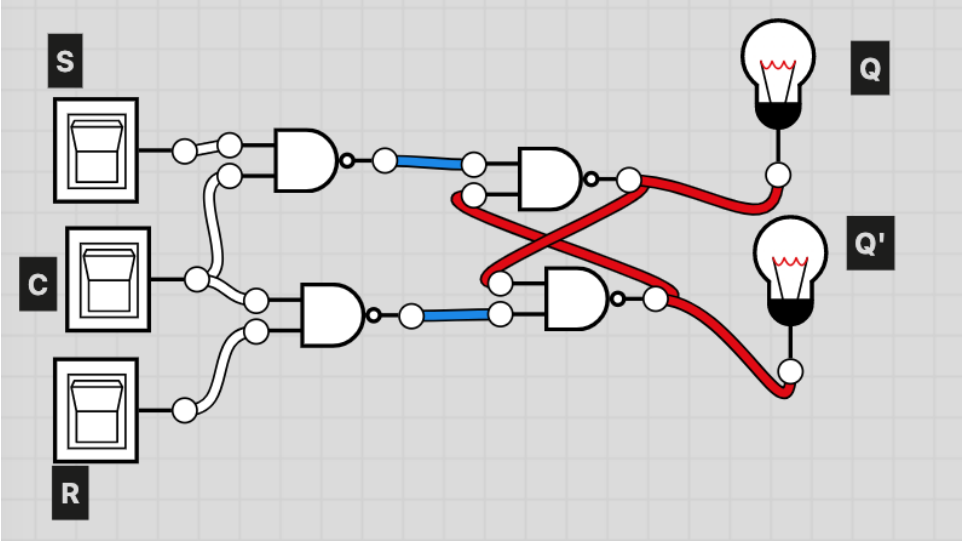

Figure 10: SR Flip Flop using DeMorgan’s law

The XNOR Gate

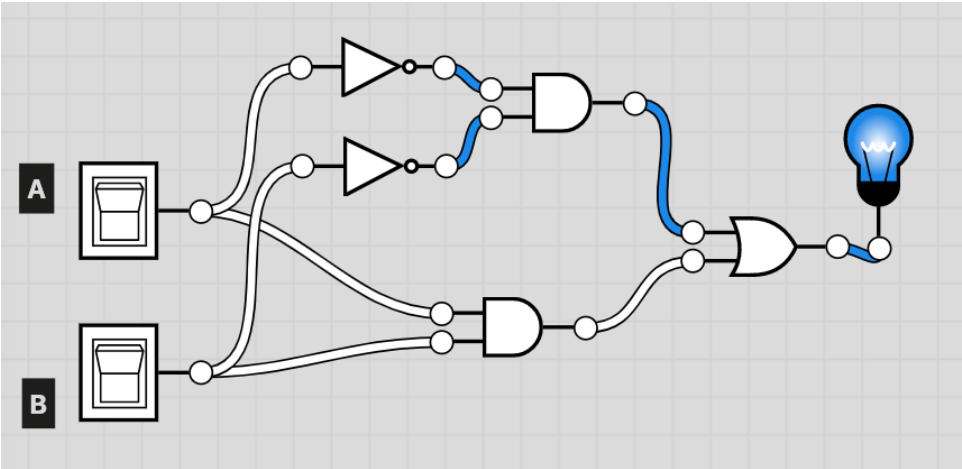

Figure 11: XNOR circuit with ANDs, ORs, NOTs only

Additional Circuit Practice

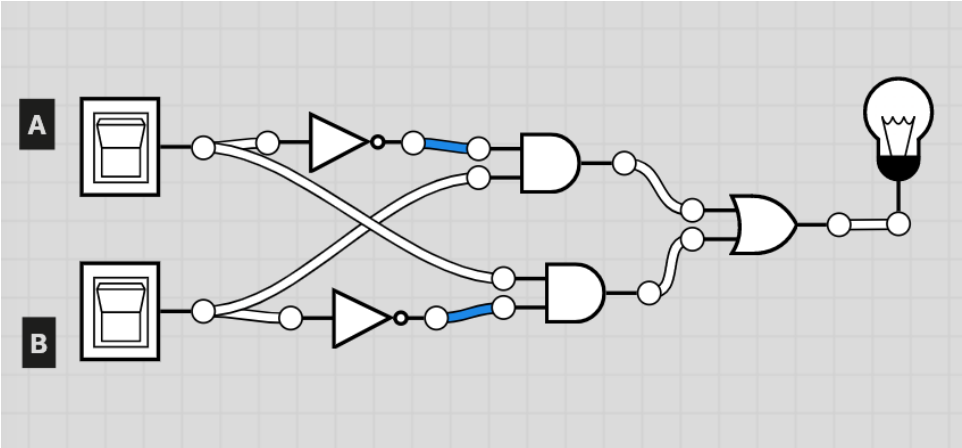

Figure 12: (A'*B)+(A*B')=A+B gate

A	B	(A'*B)+(A*B')=A+B
0	0	0
1	0	1
1	1	0
0	1	1

Figure 12: State table for (A'*B)+(A*B')=A+B

This gate has a similar truth table to the XOR gate where it is true when either A or B are true, but false when both or neither A or B are true. In terms of design, I would say this gate is an expanded version of the XOR gate using only AND, NOR, and NOT gates.