Arnav Surve
CNIT176
Lab 9
10/26/2022

Raspberry Pi 4B/3B+/3B/2B Comparison

	Pi 4 Model B	Pi 3 Model B+	Pi 3 Model B	Pi 2 Model B
RAM/RAM type	1GB, 2GB, 4GB, 8GB LPDDR4 SDRAM	1GB LPDDR2 SDRAM	1GB LPDDR2 SDRAM	1 GB SDRAM
CPU model/cores/clock speed/ ISA	Broadcom BCM2711 (Cortex-A72 ARM v8 64-bit) @ 1.5 GHz 4 cores	Broadcom BCM2837B0 (Cortex-A53 ARM 64-bit) @ 1.4GHz 4 cores	Broadcom BCM2837 (Cortex-A53 ARM 64-bit) @ 1.2 GHz 4 cores	Broadcom BCM2836 (Cortex-A7 ARM v7 32-bit) @ 900MHz 4 cores
GPU model/GFLOPS	VideoCore VI 32 GFLOPS	VideoCore IV 24 GFLOPS	VideoCore IV 24 GFLOPS	VideoCore IV 24 GFLOPS

Compared to NVIDIA GeForce RTX 3060Ti: 16.2 TFLOPS (teraflops)
The Pi 4B's GPU processing power is 32 GFlops compared to the RTX 3060ti's 16.2 TFlops. There are 1,000 GFlops in a TFlop so the 3060ti processes at 16,200 GFlops, which is 506.25 times faster than the Pi 4B.

LPDDR: low-power double data rate
SDRAM: synchronized dynamic random-access memory
GFLOPS: gigaflops

1. SoC architecture allows manufacturers to create smaller and simpler systems on a single chip, resulting in reduced energy consumption and smaller hardware footprint. Although SOCs can be used for any task, they are usually found in mobile computing applications such as smartphones & tablets as well as being used as replacements for microcontrollers.
2. Disadvantages of a SoC architecture are high initial cost of development & design, increased complexity due to integrating all systems on a single chip and being unsuitable for power-intensive applications.
   Today, the most common types of RAM being used are:
   - Static RAM (SRAM)
   - Dynamic RAM (DRAM)
   - Single Data Rate Synchronous Dynamic RAM (SDR SDRAM)
   - Double Data Rate Synchronous Dynamic RAM (DDR SDRAM, DDR2, DDR3, DDR4)

- Graphics Double Data Rate Synchronous Dynamic RAM (GDDR SDRAM, GDDR2, GDDR3, GDDR4, GDDR5)
- Flash Memory

3. Step 1: Fetch instruction – Instruction at the current program counter is fetched and stored in the instruction register (IR).
   Step 2: Decode instruction – Encoded instruction in IR is interpreted by decoder.
   Step 3: Perform ALU operation – Two operands will be operated on given operator (sum). ALU takes 2 values and returns one, result of the operation.
   Step 4: Access memory – LOAD copies value from RAM cache to register & STORE copies register value to RAM cache memory.
   Step 5: Update register file – Output of ALU is written to the register file.
   Step 6: Update program counter – update PC to address of next instruction.
4. PoP stacks single-component packages (RAM, CPU, etc.) or system-in-a-packages vertically. SoC combines all the necessary components of a computer into a single chip or circuit. On the raspberry pi, the RAM is mounted on top of the SoC meaning the RAM/SoC system is included using PoP.
5. SoC and PoP type chips are typically found on compact/mobile devices with limited space.
6. The raspberry pi operates using a RISC architecture, as it uses an ARM based processor, which RISC is specifically designed for. RISC-based machines execute one instruction (with fixed memory size) per clock cycle.

References

Chakrabarty, T. (2020, August 28). *What are the steps followed by CPU in computer to execute an instruction? " online class notes*. Online Class Notes. Retrieved October 26, 2022, from https://onlineclassnotes.com/what-are-steps-followed-by-cpu-to-execute-an-instruction/

Editorial. (2021, February 10). *System on a chip (SOC) - advantages and disadvantages explained*. RoboticsBiz. Retrieved October 26, 2022, from https://roboticsbiz.com/system-on-a-chip-soc-advantages-and-disadvantages-explained/

Sharma, S. (2013, May 5). System on a chip: What you need to know about socs. TechRadar. Retrieved October 26, 2022, from https://www.techradar.com/news/computing/pc/system-on-a-chip-what-you-need-to-know-about-socs-1147235/2