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Ans. to the ques. no-2

For a direct-mapped cache, a main memory address is viewed as consisting of three fields. These are-

(i) cache line number
(ii) main memory block number
(iii) number of lines in the cache

The chunks of memory handled by the cache are called cache lines. The size of these chunks is called the cache line size. A cache can only hold a limited number of lines, determined by the cache size.

The main memory block is RAM where input data is stored before and after processing in the CPU. The operating system and application program are also copied to RAM from disk for execution.

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If the cache has 2^n lines:

Line : Specify one of the 2^n cache lines.

Ans. to the ques no - 5

motivations for minimizing cache size are -

(i) Large memories (DRAM) are slow
(ii) Small memories (SRAM) are fast
(iii) Make the average access time small by
(iv) Servicing most accesses from a small, fast memory.
(v) Reduce the bandwidth required of the large memory.

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Ans. to the ques. no - 4

We know,

Average access time = L_1 access time + (L_1 access time + L_2 access time) + (L_1 access time + L_2 access time + L_3 access time)

Here,

L_1 access time = (0.35) (0.03)

$L_1 + L_2$ access time = (0.55) (0.03 + 0.3)

$L_1 + L_2 + L_3$ access time = (0.03 + 0.3 + 2)

∴ Average access time = (0.35) (0.03) + (0.55) (0.03 + 0.3) + (0.03 + 0.3 + 2)

= (0.0105) + (0.1815) + 2.33

= 2.522

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Ans. to the ques no-3

Block size = 4 bytes = 2^2 bytes = 2^2 words

∴ Number of bits in the word field = 2

cache size = 64 K bytes = $64 * 2^{10}$ bytes.

Total Number of address bits = 16 [As Hexadecimal Number]

∴ Number of bits in the tag field =

$16 - 6 - 5 = 5$.

For a given 16-bit address, the 5 most significant bits, represent the tag, the next 5 bits represent the Block, and the 6 least significant bits represent the Word.