1 cy62256v25_mx

- MDL Version: **01011**
- Title: **32K x 8 Asynchronous SRAM**
- Date: **18-May-2006**
- Memory Type: **sram**
- Vendor: **Cypress Semiconductor Corporation**

2 Timing Selection

This model can be configured to run in either timing-accurate or function-only (no timing) mode. In timing-accurate mode, the model implements both propagational delays and timing checks. In function-only mode, the model propagates output changes immediately and timing checks are disabled.

2.1 Function-only Mode Selection

To run in function-only mode, set the model's TimingVersion attribute to "none".

2.2 Timing-accurate Timing Version Selection

To run in timing-accurate mode, the model's TimingVersion attribute is set to select the device specific timing associated with a vendor's component. The following table provides a mapping between vendor component names and the corresponding TimingVersion attribute values.

Component to TimingVersion Mapping	
Component Name	TimingVersion
CY62256V25-100	100

Note: By default, this model uses TimingVersion "100".

3 Sources

The following sources were used as references for behavioral and timing characteristics in the development of this model.

1. Cypress Semiconductor Corporation “August 31, 2001”

4 Usage Notes

4.1 Configuring The Model

For information about configuring DesignWare Memory Models for use in simulation, refer to the installed version of the *Simulator Configuration Guide for Synopsys Models*. Or, for the most up-to-date version of this manual, see the *Simulator Configuration Guide for Synopsys Models* on the Synopsys external Web.

4.2 Using DesignWare Memory Models

For general information about using DesignWare Memory Models, refer to the installed version of the *DesignWare Memory Model User’s Manual*. Or, for the most up-to-date version of this manual, see the *DesignWare Memory Model User’s Manual* on the Synopsys external Web.

4.3 Using DesignWare SRAM Models

The DesignWare Memory Model documentation set also contains additional usage information that applies to all SRAM DesignWare Memory Models. For more information refer to the installed version of the *SRAM DesignWare Memory Model Reference*. Or, for the most up-to-date version of this manual, see the *SRAM DesignWare Memory Model Reference* on the Synopsys external Web.

4.4 Model Usage Notes

None

4.5 Model Port Description

The following table describes the pin interface for this model.

Model Port Description		
Port Name	Direction	Description
a[14:0]	in	Address Bus
ce_n	in	Chip Enable
io[7:0]	inout	IO Data Bus
oe_n	in	Output Enable
we_n	in	Write Enable

4.6 Default Attribute Setting

The following table describes the default attribute settings for this model.

Default Attribute Setting	
Model Attribute	Default Value
DefaultData	11111111
DelayRange	Max
MemoryFile	.
MessageLevel	15
ModelAlias	.
ModelConfig	32'h0
ModelId	-2
TimingVersion	100

4.7 Timing Data for TimingVersion 100

The following table provides a listing of the timing data values modeled when the model's TimingVersion is set to "100".

Timing Data for TimingVersion 100					
Parameter	Min	Typ	Max	Unit	Description
tAA	100.0	100.0	100.0	ns	Address to Output Data Valid
tACE	100.0	100.0	100.0	ns	Chip Enable Asserted to Output Data Valid When Chip Deselect Time (tDESEL) violated
tACE2	100.0	100.0	100.0	ns	Chip Enable Asserted to Output Data Valid When Chip Deselect Time (tDESEL) not violated
tAW	90.0	-	-	ns	Address Setup to Write End
tDOE	75.0	75.0	75.0	ns	Output Enable Asserted to Output Data Valid
tHA	0.0	-	-	ns	Address Hold from Write End (Chip

Timing Data for TimingVersion 100					
					Enable)
tHA_WE	0.0	-	-	ns	Address Hold from Write End (Write Enable)
tHD	0.0	-	-	ns	Data Hold from Write End (Chip Enable)
tHD_WE	0.0	-	-	ns	Data Hold from Write End (Write Enable)
tHZCE	50.0	50.0	50.0	ns	Chip Enable Deasserted to Output Data High Z
tHZOE	50.0	50.0	50.0	ns	Output Enable Deasserted to Output Data High Z
tHZWE	50.0	50.0	50.0	ns	Write Enable Asserted to Output Data High Z
tLZCE	10.0	-	-	ns	Chip Enable Asserted to Output Data Low Z
tLZOE	5.0	-	-	ns	Output Enable Asserted to Output Data Low Z
tLZWE	10.0	-	-	ns	Write Enable Deasserted to Output Data Low Z
tOHA	10.0	-	-	ns	Output Data Invalid from Address Change
tPWE	80.0	-	-	ns	Write Enable Pulse Width (Output Enable is Deasserted)
tPWE1	110.0	-	-	ns	Write Enable Pulse Width (Output Enable is Asserted)
tRC	100.0	-	-	ns	Read Cycle Time
tSA	0.0	-	-	ns	Address Setup to Write Start
tSCE	90.0	-	-	ns	Chip Enable Asserted to Write End
tSD	60.0	-	-	ns	Data Setup to Write End
tWC	100.0	-	-	ns	Write cycle time

4.8 Verilog Instantiation Example

Following is an example of instantiating this model within Verilog for the VCS simulator. In this example, a subset of the model's simulation attributes (Verilog parameters) are shown set to their default value. For a complete list of supported simulation attributes, see the table in section 4.6.

```
cy62256v25_mx_bus example_inst
  (
    .a    ( a    ),
    .ce_n ( ce_n ),
    .io   ( io   ),
    .oe_n ( oe_n ),
    .we_n ( we_n )
  );
defparam example_inst.DelayRange    = "Max";
defparam example_inst.MemoryFile    = ".";
defparam example_inst.MessageLevel  = "15";
defparam example_inst.ModelAlias    = ".";
defparam example_inst.ModelId       = "-2";
defparam example_inst.TimingVersion = "100";
```

4.9 VHDL Instantiation Example

Following is an example of instantiating this model within VHDL for the Scirocco simulator. In this example, a subset of the model's simulation attributes (VHDL generics) are shown set to their default value. For a complete list of supported simulation attributes, see the table in section 4.6.

```
example_inst : cy62256v25_mx
    generic map (
        DelayRange    => "Max",
        MemoryFile    => ".",
        MessageLevel  => "15",
        ModelAlias    => ".",
        ModelId       => "-2",
        TimingVersion => "100"
    )
    port map (
        a    => a,
        ce_n => ce_n,
        io   => io,
        oe_n => oe_n,
        we_n => we_n
    );
```

5 cy62256v25_mx Model History

Synopsys publishes model history and bug fixes on the *IP Directory for the cy62256v25_mx* . The behavior of DesignWare Memory Models may also be affected by revisions made to supporting utilities. For information concerning potential utility changes, please refer to *DesignWare Memory Model Release Notes* .