1 hy57v161610d_a_mx

- MDL Version: **01013**
- Title: **512K x 16Bit x 2 Banks Synchronous DRAM**
- Date: **09-May-2006**
- Memory Type: **sdram**
- Vendor: **Hyundai Electronics America**

2 Timing Selection

This model can be configured to run in either timing-accurate or function-only (no timing) mode. In timing-accurate mode, the model implements both propagational delays and timing checks. In function-only mode, the model propagates output changes immediately and timing checks are disabled.

2.1 Function-only Mode Selection

To run in function-only mode, set the model's TimingVersion attribute to "none".

2.2 Timing-accurate Timing Version Selection

To run in timing-accurate mode, the model's TimingVersion attribute is set to select the device specific timing associated with a vendor's component. The following table provides a mapping between vendor component names and the corresponding TimingVersion attribute values.

Component to TimingVersion Mapping	
Component Name	TimingVersion
HY57V161610D_A-5	5
HY57V161610D_A-55	55

Note: By default, this model uses TimingVersion "5".

3 Sources

The following sources were used as references for behavioral and timing characteristics in the development of this model.

1. Hyundai Electronics America “Rev. 3.7/Mar. 02”

4 Usage Notes

4.1 Configuring The Model

For information about configuring DesignWare Memory Models for use in simulation, refer to the installed version of the *Simulator Configuration Guide for Synopsys Models*. Or, for the most up-to-date version of this manual, see the *Simulator Configuration Guide for Synopsys Models* on the Synopsys external Web.

4.2 Using DesignWare Memory Models

For general information about using DesignWare Memory Models, refer to the installed version of the *DesignWare Memory Model User’s Manual*. Or, for the most up-to-date version of this manual, see the *DesignWare Memory Model User’s Manual* on the Synopsys external Web.

4.3 Using DesignWare SDRAM Models

The DesignWare Memory Model documentation set also contains additional usage information that applies to all SDRAM DesignWare Memory Models. For more information refer to the installed version of the *SDRAM DesignWare Memory Model Reference*. Or, for the most up-to-date version of this manual, see the *SDRAM DesignWare Memory Model Reference* on the Synopsys external Web.

4.4 Model Usage Notes

Device pins ldqm and udqm modeled as dqm bus. Timing values greater than 4 ms have been entered as 4 ms.

4.5 Model Port Description

The following table describes the pin interface for this model.

Model Port Description		
Port Name	Direction	Description
a[10:0]	in	Address Bus
ba	in	Bank Address
cas_n	in	Column Address Strobe
cke	in	Clock Enable
clk	in	System Clock
cs_n	in	Chip Enable
dqm[1:0]	in	Data Mask Enable
dq[15:0]	inout	InOut Data Bus
ras_n	in	Row Address Strobe
we_n	in	Write Enable

4.6 Default Attribute Setting

The following table describes the default attribute settings for this model.

Default Attribute Setting	
Model Attribute	Default Value
DefaultData	1111111111111111
DelayRange	Max
MemoryFile	.
MessageLevel	15
ModelAlias	.
ModelConfig	32’h0
ModelId	-2
TimingVersion	5

4.7 Timing Data for TimingVersion 5

The following table provides a listing of the timing data values modeled when the model’s TimingVersion is set to "5".

Timing Data for TimingVersion 5					
Parameter	Min	Typ	Max	Unit	Description
tAC3	4.5	4.5	4.5	ns	Access Time From Clock (CAS Latency = 3)
tAH	1.0	-	-	ns	Address Hold Time
tAS	1.5	-	-	ns	Address Setup Time
tBDL	0.0	-	-	ns	Last data-in to BST command period
tBDL_rel	1	-	-	clk	Last data-in to BST command period
tBSH3_rel	3	3	3	clk	BST command to bus Hi-impedance (CAS

Timing Data for TimingVersion 5					
					Latency = 3)
tCAC	0.0	0.0	0.0	ns	Column Access Time
tCBD	0.0	-	-	ns	Column to Column delay for different Bank
tCBD_rel	1	-	-	clk	Column to Column delay for different Bank
tCCD	0.0	-	-	ns	Column to Column delay for Same Bank
tCCD_rel	1	-	-	clk	Column to Column delay for Same Bank
tCDL	0.0	-	-	ns	Last data-in to WR/RD command period
tCDL_rel	1	-	-	clk	Last data-in to WR/RD command period
tCH	1.0	-	-	ns	Command Hold Time
tCHW	1.75	-	-	ns	Clock High Level Width
tCK3	5.0	-	-	ns	Clock Cycle Time (CAS Latency = 3)
tCKED_rel	1	1	1	clk	Clock Enable to clock disable or power-down entry mode
tCKH	1.0	-	-	ns	Clock Enable Hold Time
tCKS	1.5	-	-	ns	Clock Enable Setup Time
tCKSP	1.5	-	-	ns	Clock Enable Setup Time for Power Down
tCLW	1.75	-	-	ns	Clock Low Level Width
tCS	1.5	-	-	ns	Command Setup Time
tDAL3	0.0	-	-	ns	Data-in to ACT Command period (CAS Latency = 3)
tDAL3_rel	4	-	-	clk	Data-in to ACT Command period (CAS Latency = 3)
tDH	1.0	-	-	ns	Data-In Hold Time
tDPL3	0.0	-	-	ns	Data-in to PRE Command period (CAS Latency = 3)
tDPL3_rel	1	-	-	clk	Data-in to PRE Command period (CAS Latency = 3)
tDQD_rel	0	0	0	clk	Data Mask Enable to input data delay
tDQM_rel	0	0	0	clk	Data Mask Enable to data mask during write
tDQZ_rel	2	2	2	clk	Data Mask Enable to data Hi-impedance during READs (dqm Latency)
tDS	1.5	-	-	ns	Data-In Setup Time
tMRD	0.0	-	-	ns	Load Mode Register to ACT/REF command
tMRD_rel	2	-	-	clk	Load Mode Register to ACT/REF command
tOH3	1.5	-	-	ns	Data-out Hold Time (CAS Latency = 3)
tOHZ3	2.0	5.0	5.0	ns	Data-out high-impedance time (CAS Latency = 3)
tOLZ	2.0	-	-	ns	Data-out low-impedance time

Timing Data for TimingVersion 5					
tOWD_rel	2	2	2	clk	Last Data Out to Write Command Delay
tPED_rel	1	1	1	clk	Clock Enable to power-down exit setup mode
tPROZ_rel	3	3	3	clk	Data-out to Hi-impedance from PRE command (CAS Latency = 3)
tRAC	0.0	0.0	0.0	ns	Row Access Time
tRAS	40.0	-	100000.0	ns	ACT to PRE command period
tRAS_rel	0	-	-	clk	ACT to PRE command period
tRC	55.0	-	-	ns	ACT to ACT/REF command period.
tRCD	15.0	-	-	ns	ACT to RD/WR Command Period
tRCD_rel	0	-	-	clk	ACT to RD/WR Command Period
tRC_rel	0	-	-	clk	ACT to ACT/REF command period.
tRDL	0.0	-	-	ns	Last data-in to PRE command period
tRDL_rel	1	-	-	clk	Last data-in to PRE command period
tREF	4.0	-	-	ms	Refresh Period (REF-REF command interval)
tRP	0.0	-	-	ns	PRE To ACT Command Period
tRP_rel	3	-	-	clk	PRE To ACT Command Period
tRRC	55.0	-	-	ns	AutoRefresh Period.
tRRC_rel	0	-	-	clk	AutoRefresh Period.
tRRD	0.0	-	-	ns	ACT(0) to ACT(1) delay
tRRD_rel	2	-	-	clk	ACT(0) to ACT(1) delay
tSRE	0.0	-	-	ns	Self Refresh Exit Time
tSRE_rel	1	-	-	clk	Self Refresh Exit Time
tWR	0.0	-	-	ns	Write Recovery Time
tWR_rel	1	-	-	clk	Write Recovery Time
tWTL_rel	0	0	0	clk	Write command to input data delay
tXSR	55.0	-	-	ns	Self Refresh Exit to ACT command

4.8 Timing Data for TimingVersion 55

The following table provides a listing of the timing data values modeled when the model's TimingVersion is set to "55".

Timing Data for TimingVersion 55					
Parameter	Min	Typ	Max	Unit	Description
tAC3	5.0	5.0	5.0	ns	Access Time From Clock (CAS Latency = 3)
tAH	1.0	-	-	ns	Address Hold Time
tAS	1.5	-	-	ns	Address Setup Time
tBDL	0.0	-	-	ns	Last data-in to BST command period
tBDL_rel	1	-	-	clk	Last data-in to BST command period

Timing Data for TimingVersion 55					
tBSH3_rel	3	3	3	clk	BST command to bus Hi-impedance (CAS Latency = 3)
tCAC	0.0	0.0	0.0	ns	Column Access Time
tCBD	0.0	-	-	ns	Column to Column delay for different Bank
tCBD_rel	1	-	-	clk	Column to Column delay for different Bank
tCCD	0.0	-	-	ns	Column to Column delay for Same Bank
tCCD_rel	1	-	-	clk	Column to Column delay for Same Bank
tCDL	0.0	-	-	ns	Last data-in to WR/RD command period
tCDL_rel	1	-	-	clk	Last data-in to WR/RD command period
tCH	1.0	-	-	ns	Command Hold Time
tCHW	2.0	-	-	ns	Clock High Level Width
tCK3	5.5	-	-	ns	Clock Cycle Time (CAS Latency = 3)
tCKED_rel	1	1	1	clk	Clock Enable to clock disable or power-down entry mode
tCKH	1.0	-	-	ns	Clock Enable Hold Time
tCKS	1.5	-	-	ns	Clock Enable Setup Time
tCKSP	1.5	-	-	ns	Clock Enable Setup Time for Power Down
tCLW	2.0	-	-	ns	Clock Low Level Width
tCS	1.5	-	-	ns	Command Setup Time
tDAL3	0.0	-	-	ns	Data-in to ACT Command period (CAS Latency = 3)
tDAL3_rel	4	-	-	clk	Data-in to ACT Command period (CAS Latency = 3)
tDH	1.0	-	-	ns	Data-In Hold Time
tDPL3	0.0	-	-	ns	Data-in to PRE Command period (CAS Latency = 3)
tDPL3_rel	1	-	-	clk	Data-in to PRE Command period (CAS Latency = 3)
tDQD_rel	0	0	0	clk	Data Mask Enable to input data delay
tDQM_rel	0	0	0	clk	Data Mask Enable to data mask during write
tDQZ_rel	2	2	2	clk	Data Mask Enable to data Hi-impedance during READs (dqm Latency)
tDS	1.5	-	-	ns	Data-In Setup Time
tMRD	0.0	-	-	ns	Load Mode Register to ACT/REF command
tMRD_rel	2	-	-	clk	Load Mode Register to ACT/REF command
tOH3	2.0	-	-	ns	Data-out Hold Time (CAS Latency = 3)
tOHZ3	2.0	5.5	5.5	ns	Data-out high-impedance time (CAS Latency = 3)

Timing Data for TimingVersion 55					
tOLZ	2.0	-	-	ns	Data-out low-impedance time
tOWD_rel	2	2	2	clk	Last Data Out to Write Command Delay
tPED_rel	1	1	1	clk	Clock Enable to power-down exit setup mode
tPROZ_rel	3	3	3	clk	Data-out to Hi-impedance from PRE command (CAS Latency = 3)
tRAC	0.0	0.0	0.0	ns	Row Access Time
tRAS	38.5	-	100000.0	ns	ACT to PRE command period
tRAS_rel	0	-	-	clk	ACT to PRE command period
tRC	55.0	-	-	ns	ACT to ACT/REF command period.
tRCD	16.5	-	-	ns	ACT to RD/WR Command Period
tRCD_rel	0	-	-	clk	ACT to RD/WR Command Period
tRC_rel	0	-	-	clk	ACT to ACT/REF command period.
tRDL	0.0	-	-	ns	Last data-in to PRE command period
tRDL_rel	1	-	-	clk	Last data-in to PRE command period
tREF	4.0	-	-	ms	Refresh Period (REF-REF command interval)
tRP	0.0	-	-	ns	PRE To ACT Command Period
tRP_rel	3	-	-	clk	PRE To ACT Command Period
tRRC	55.0	-	-	ns	AutoRefresh Period.
tRRC_rel	0	-	-	clk	AutoRefresh Period.
tRRD	0.0	-	-	ns	ACT(0) to ACT(1) delay
tRRD_rel	2	-	-	clk	ACT(0) to ACT(1) delay
tSRE	0.0	-	-	ns	Self Refresh Exit Time
tSRE_rel	1	-	-	clk	Self Refresh Exit Time
tWR	0.0	-	-	ns	Write Recovery Time
tWR_rel	1	-	-	clk	Write Recovery Time
tWTL_rel	0	0	0	clk	Write command to input data delay
tXSR	55.0	-	-	ns	Self Refresh Exit to ACT command

4.9 Verilog Instantiation Example

Following is an example of instantiating this model within Verilog for the VCS simulator. In this example, a subset of the model's simulation attributes (Verilog parameters) are shown set to their default value. For a complete list of supported simulation attributes, see the table in section 4.6.

```
hy57v161610d_a_mx_bus example_inst
  (
    .a     ( a     ),
    .ba    ( ba    ),
    .cas_n ( cas_n ),
    .cke   ( cke   ),
    .clk   ( clk   ),
    .cs_n  ( cs_n  ),
    .dqm   ( dqm   ),
    .dq    ( dq    ),
    .ras_n ( ras_n ),
    .we_n  ( we_n  )
  );
defparam example_inst.DelayRange    = "Max";
defparam example_inst.MemoryFile    = ".";
defparam example_inst.MessageLevel  = "15";
defparam example_inst.ModelAlias    = ".";
defparam example_inst.ModelId       = "-2";
defparam example_inst.TimingVersion = "5";
```

4.10 VHDL Instantiation Example

Following is an example of instantiating this model within VHDL for the Scirocco simulator. In this example, a subset of the model's simulation attributes (VHDL generics) are shown set to their default value. For a complete list of supported simulation attributes, see the table in section 4.6.

```
example_inst : hy57v161610d_a_mx
    generic map (
        DelayRange    => "Max",
        MemoryFile    => ".",
        MessageLevel  => "15",
        ModelAlias    => ".",
        ModelId       => "-2",
        TimingVersion => "5"
    )
    port map (
        a     => a,
        ba    => ba,
        cas_n => cas_n,
        cke   => cke,
        clk   => clk,
        cs_n  => cs_n,
        dqm   => dqm,
        dq    => dq,
        ras_n => ras_n,
        we_n  => we_n
    );
```

5 hy57v161610d_a_mx Model History

Synopsys publishes model history and bug fixes on the *IP Directory for the hy57v161610d_a_mx* . The behavior of DesignWare Memory Models may also be affected by revisions made to supporting utilities. For information concerning potential utility changes, please refer to *DesignWare Memory Model Release Notes* .