1 km68257c_mx

- MDL Version: **01013**
- Title: **32K x 8 Asynchronous SRAM**
- Date: **29-May-2006**
- Memory Type: **sram**
- Vendor: **Samsung Electronics**

2 Timing Selection

This model can be configured to run in either timing-accurate or function-only (no timing) mode. In timing-accurate mode, the model implements both propagational delays and timing checks. In function-only mode, the model propagates output changes immediately and timing checks are disabled.

2.1 Function-only Mode Selection

To run in function-only mode, set the model's TimingVersion attribute to "none".

2.2 Timing-accurate Timing Version Selection

To run in timing-accurate mode, the model's TimingVersion attribute is set to select the device specific timing associated with a vendor's component. The following table provides a mapping between vendor component names and the corresponding TimingVersion attribute values.

Component to TimingVersion Mapping	
Component Name	TimingVersion
KM68257C-12	12
KM68257C-15	15
KM68257C-20	20

Note: By default, this model uses TimingVersion "12".

3 Sources

The following sources were used as references for behavioral and timing characteristics in the development of this model.

1. Samsung Electronics “Rev 4.0 February 1998”

4 Usage Notes

4.1 Configuring The Model

For information about configuring DesignWare Memory Models for use in simulation, refer to the installed version of the *Simulator Configuration Guide for Synopsys Models*. Or, for the most up-to-date version of this manual, see the *Simulator Configuration Guide for Synopsys Models* on the Synopsys external Web.

4.2 Using DesignWare Memory Models

For general information about using DesignWare Memory Models, refer to the installed version of the *DesignWare Memory Model User’s Manual*. Or, for the most up-to-date version of this manual, see the *DesignWare Memory Model User’s Manual* on the Synopsys external Web.

4.3 Using DesignWare SRAM Models

The DesignWare Memory Model documentation set also contains additional usage information that applies to all SRAM DesignWare Memory Models. For more information refer to the installed version of the *SRAM DesignWare Memory Model Reference*. Or, for the most up-to-date version of this manual, see the *SRAM DesignWare Memory Model Reference* on the Synopsys external Web.

4.4 Model Usage Notes

None

4.5 Model Port Description

The following table describes the pin interface for this model.

Model Port Description		
Port Name	Direction	Description
a[14:0]	in	Address Bus
cs_n	in	Chip Enable
io[8:1]	inout	IO Data Bus
oe_n	in	Output Enable
we_n	in	Write Enable

4.6 Default Attribute Setting

The following table describes the default attribute settings for this model.

Default Attribute Setting	
Model Attribute	Default Value
DefaultData	11111111
DelayRange	Max
MemoryFile	.
MessageLevel	15
ModelAlias	.
ModelConfig	32’h0
ModelId	-2
TimingVersion	12

4.7 Timing Data for TimingVersion 12

The following table provides a listing of the timing data values modeled when the model’s TimingVersion is set to "12".

Timing Data for TimingVersion 12					
Parameter	Min	Typ	Max	Unit	Description
tAA	12.0	12.0	12.0	ns	Address to Output Data Valid
tAS	0.0	-	-	ns	Address Setup to Write Start
tAW	9.0	-	-	ns	Address Setup to Write End
tCO	12.0	12.0	12.0	ns	Chip Enable Asserted to Output Data Valid When Chip Deselect Time (tDESEL) violated
tCO2	12.0	12.0	12.0	ns	Chip Enable Asserted to Output Data Valid When Chip Deselect Time (tDESEL) not violated
tCW	9.0	-	-	ns	Chip Enable Asserted to Write End
tDH	0.0	-	-	ns	Data Hold from Write End (Chip Enable)
tDH_WE	0.0	-	-	ns	Data Hold from Write End (Write Enable)

Timing Data for TimingVersion 12					
tDW	7.0	-	-	ns	Data Setup to Write End
tHZ	0.0	6.0	6.0	ns	Chip Enable Deasserted to Output Data High Z
tLZ	3.0	-	-	ns	Chip Enable Asserted to Output Data Low Z
tOE	6.0	6.0	6.0	ns	Output Enable Asserted to Output Data Valid
tOH	3.0	-	-	ns	Output Data Invalid from Address Change
tOHZ	0.0	6.0	6.0	ns	Output Enable Deasserted to Output Data High Z
tOLZ	0.0	-	-	ns	Output Enable Asserted to Output Data Low Z
tOW	0.0	-	-	ns	Write Enable Deasserted to Output Data Low Z
tRC	12.0	-	-	ns	Read Cycle Time
tWC	12.0	-	-	ns	Write cycle time
tWHZ	0.0	6.0	6.0	ns	Write Enable Asserted to Output Data High Z
tWP	9.0	-	-	ns	Write Enable Pulse Width (Output Enable is Deasserted)
tWP1	12.0	-	-	ns	Write Enable Pulse Width (Output Enable is Asserted)
tWR	0.0	-	-	ns	Address Hold from Write End (Chip Enable)
tWR_WE	0.0	-	-	ns	Address Hold from Write End (Write Enable)

4.8 Timing Data for TimingVersion 15

The following table provides a listing of the timing data values modeled when the model's TimingVersion is set to "15".

Timing Data for TimingVersion 15					
Parameter	Min	Typ	Max	Unit	Description
tAA	15.0	15.0	15.0	ns	Address to Output Data Valid
tAS	0.0	-	-	ns	Address Setup to Write Start
tAW	12.0	-	-	ns	Address Setup to Write End
tCO	15.0	15.0	15.0	ns	Chip Enable Asserted to Output Data Valid When Chip Deselect Time (tDESEL) violated
tCO2	15.0	15.0	15.0	ns	Chip Enable Asserted to Output Data Valid When Chip Deselect Time (tDESEL) not violated
tCW	11.0	-	-	ns	Chip Enable Asserted to Write End
tDH	0.0	-	-	ns	Data Hold from Write End (Chip Enable)
tDH_WE	0.0	-	-	ns	Data Hold from Write End (Write Enable)
tDW	8.0	-	-	ns	Data Setup to Write End
tHZ	0.0	7.0	7.0	ns	Chip Enable Deasserted to Output Data High

Timing Data for TimingVersion 15					
					Z
tLZ	3.0	-	-	ns	Chip Enable Asserted to Output Data Low Z
tOE	7.0	7.0	7.0	ns	Output Enable Asserted to Output Data Valid
tOH	3.0	-	-	ns	Output Data Invalid from Address Change
tOHZ	0.0	7.0	7.0	ns	Output Enable Deasserted to Output Data High Z
tOLZ	0.0	-	-	ns	Output Enable Asserted to Output Data Low Z
tOW	0.0	-	-	ns	Write Enable Deasserted to Output Data Low Z
tRC	15.0	-	-	ns	Read Cycle Time
tWC	15.0	-	-	ns	Write cycle time
tWHZ	0.0	8.0	8.0	ns	Write Enable Asserted to Output Data High Z
tWP	12.0	-	-	ns	Write Enable Pulse Width (Output Enable is Deasserted)
tWP1	15.0	-	-	ns	Write Enable Pulse Width (Output Enable is Asserted)
tWR	0.0	-	-	ns	Address Hold from Write End (Chip Enable)
tWR_WE	0.0	-	-	ns	Address Hold from Write End (Write Enable)

4.9 Timing Data for TimingVersion 20

The following table provides a listing of the timing data values modeled when the model's TimingVersion is set to "20".

Timing Data for TimingVersion 20					
Parameter	Min	Typ	Max	Unit	Description
tAA	20.0	20.0	20.0	ns	Address to Output Data Valid
tAS	0.0	-	-	ns	Address Setup to Write Start
tAW	13.0	-	-	ns	Address Setup to Write End
tCO	20.0	20.0	20.0	ns	Chip Enable Asserted to Output Data Valid When Chip Deselect Time (tDESEL) violated
tCO2	20.0	20.0	20.0	ns	Chip Enable Asserted to Output Data Valid When Chip Deselect Time (tDESEL) not violated
tCW	13.0	-	-	ns	Chip Enable Asserted to Write End
tDH	0.0	-	-	ns	Data Hold from Write End (Chip Enable)
tDH_WE	0.0	-	-	ns	Data Hold from Write End (Write Enable)
tDW	10.0	-	-	ns	Data Setup to Write End
tHZ	0.0	10.0	10.0	ns	Chip Enable Deasserted to Output Data High Z
tLZ	3.0	-	-	ns	Chip Enable Asserted to Output Data Low Z

Timing Data for TimingVersion 20					
tOE	9.0	9.0	9.0	ns	Output Enable Asserted to Output Data Valid
tOH	3.0	-	-	ns	Output Data Invalid from Address Change
tOHZ	0.0	10.0	10.0	ns	Output Enable Deasserted to Output Data High Z
tOLZ	0.0	-	-	ns	Output Enable Asserted to Output Data Low Z
tOW	0.0	-	-	ns	Write Enable Deasserted to Output Data Low Z
tRC	20.0	-	-	ns	Read Cycle Time
tWC	20.0	-	-	ns	Write cycle time
tWHZ	0.0	8.0	8.0	ns	Write Enable Asserted to Output Data High Z
tWP	13.0	-	-	ns	Write Enable Pulse Width (Output Enable is Deasserted)
tWP1	20.0	-	-	ns	Write Enable Pulse Width (Output Enable is Asserted)
tWR	0.0	-	-	ns	Address Hold from Write End (Chip Enable)
tWR_WE	0.0	-	-	ns	Address Hold from Write End (Write Enable)

4.10 Verilog Instantiation Example

Following is an example of instantiating this model within Verilog for the VCS simulator. In this example, a subset of the model's simulation attributes (Verilog parameters) are shown set to their default value. For a complete list of supported simulation attributes, see the table in section 4.6.

```
km68257c_mx_bus example_inst
  (
    .a    ( a    ),
    .cs_n ( cs_n ),
    .io   ( io   ),
    .oe_n ( oe_n ),
    .we_n ( we_n )
  );
defparam example_inst.DelayRange    = "Max";
defparam example_inst.MemoryFile    = ".";
defparam example_inst.MessageLevel  = "15";
defparam example_inst.ModelAlias    = ".";
defparam example_inst.ModelId       = "-2";
defparam example_inst.TimingVersion = "12";
```

4.11 VHDL Instantiation Example

Following is an example of instantiating this model within VHDL for the Scirocco simulator. In this example, a subset of the model's simulation attributes (VHDL generics) are shown set to their default value. For a complete list of supported simulation attributes, see the table in section 4.6.

```
example_inst : km68257c_mx
    generic map (
        DelayRange    => "Max",
        MemoryFile    => ".",
        MessageLevel  => "15",
        ModelAlias    => ".",
        ModelId       => "-2",
        TimingVersion => "12"
    )
    port map (
        a    => a,
        cs_n => cs_n,
        io   => io,
        oe_n => oe_n,
        we_n => we_n
    );
```

5 km68257c_mx Model History

Synopsys publishes model history and bug fixes on the *IP Directory for the km68257c_mx* . The behavior of DesignWare Memory Models may also be affected by revisions made to supporting utilities. For information concerning potential utility changes, please refer to *DesignWare Memory Model Release Notes* .