1 cy7c09169a_mx

- MDL Version: **01008**
- Title: **16K x 9 Synchronous Dual Port SRAM**
- Date: **18-Feb-2004**
- Memory Type: **mpssram**
- Vendor: **Cypress Semiconductor Corporation**

2 Timing Selection

This model can be configured to run in either timing-accurate or function-only (no timing) mode. In timing-accurate mode, the model implements both propagational delays and timing checks. In function-only mode, the model propagates output changes immediately and timing checks are disabled.

2.1 Function-only Mode Selection

To run in function-only mode, set the model's TimingVersion attribute to "none".

2.2 Timing-accurate Timing Version Selection

To run in timing-accurate mode, the model's TimingVersion attribute is set to select the device specific timing associated with a vendor's component. The following table provides a mapping between vendor component names and the corresponding TimingVersion attribute values.

Component to TimingVersion Mapping	
Component Name	TimingVersion
CY7C09169A-12	12
CY7C09169A-6	6
CY7C09169A-7	7
CY7C09169A-9	9

Note: By default, this model uses TimingVersion "6".

3 Sources

The following sources were used as references for behavioral and timing characteristics in the development of this model.

1. Cypress Semiconductor Corporation “September 19, 2001”

4 Usage Notes

4.1 Configuring The Model

For information about configuring DesignWare Memory Models for use in simulation, refer to the installed version of the *Simulator Configuration Guide for Synopsys Models*. Or, for the most up-to-date version of this manual, see the *Simulator Configuration Guide for Synopsys Models* on the Synopsys external Web.

4.2 Using DesignWare Memory Models

For general information about using DesignWare Memory Models, refer to the installed version of the *DesignWare Memory Model User’s Manual*. Or, for the most up-to-date version of this manual, see the *DesignWare Memory Model User’s Manual* on the Synopsys external Web.

4.3 Using DesignWare MPSSRAM Models

The DesignWare Memory Model documentation set also contains additional usage information that applies to all MPSSRAM DesignWare Memory Models. For more information refer to the installed version of the *MPSSRAM DesignWare Memory Model Reference*. Or, for the most up-to-date version of this manual, see the *MPSSRAM DesignWare Memory Model Reference* on the Synopsys external Web.

4.4 Model Usage Notes

None

4.5 Model Port Description

The following table describes the pin interface for this model.

Model Port Description		
Port Name	Direction	Description
adsl_n	in	Port1 Address Strobe Input
adsr_n	in	Port2 Address Strobe Input
al[13:0]	in	Port1 Address Inputs
ar[13:0]	in	Port2 Address Inputs
ce0l_n	in	Port1 Chip Enable Input
ce0r_n	in	Port2 Chip Enable Input
ce1l	in	Port1 Chip Enable Input
ce1r	in	Port2 Chip Enable Input
clkl	in	Port1 Clock Signal
clkr	in	Port2 Clock Signal
cntenl_n	in	Port1 Counter Enable Input
cntenr_n	in	Port2 Counter Enable Input
cntrstl_n	in	Port1 Counter Reset Input
cntrstr_n	in	Port2 Counter Reset Input
ft_n_pipel	in	Port 1 Flowthrough/Pipelined Select Input
ft_n_piper	in	Port 2 Flowthrough/Pipelined Select Input
iol[8:0]	inout	Port1 Data Bus Input/Output
ior[8:0]	inout	Port2 Data Bus Input/Output
oel_n	in	Port1 Output Enable Input
oer_n	in	Port2 Output Enable Input
r_w_nl	in	Port1 Read/Write Enable Input
r_w_nr	in	Port2 Read/Write Enable Input

4.6 Default Attribute Setting

The following table describes the default attribute settings for this model.

Default Attribute Setting	
Model Attribute	Default Value
DefaultData	111111111
DelayRange	Max
MemoryFile	.
MessageLevel	15
ModelAlias	.
ModelConfig	32’h0
ModelId	-2
TimingVersion	6

4.7 Timing Data for TimingVersion 12

The following table provides a listing of the timing data values modeled when the model's TimingVersion is set to "12".

Timing Data for TimingVersion 12					
Parameter	Min	Typ	Max	Unit	Description
tCCS	15.0	-	-	ns	Clock to Clock Setup Time
tCD1	25.0	25.0	25.0	ns	Clock to Data Valid Delay - Flowthrough
tCD2	12.0	12.0	12.0	ns	Clock to Data Valid Delay - Pipelined
tCH1	12.0	-	-	ns	Clock High Time - Flowthrough
tCH2	8.0	-	-	ns	Clock High Time - Pipelined
tCKHZ	2.0	9.0	9.0	ns	Clock to Output High Z Delay
tCKLZ	2.0	-	-	ns	Clock to Output Low Z Delay
tCL1	12.0	-	-	ns	Clock Low Time - Flowthrough
tCL2	8.0	-	-	ns	Clock Low Time - Pipelined
tCYC1	30.0	-	-	ns	Clock Cycle Time - Flowthrough
tCYC2	20.0	-	-	ns	Clock Cycle Time - Pipelined
tDC	2.0	-	-	ns	Data Output Hold after Clock Assertion
tHA	1.0	-	-	ns	Address Hold Time
tHAD	1.0	-	-	ns	Address Strobe Hold Time
tHC	1.0	-	-	ns	Chip Enable Hold Time
tHCN	1.0	-	-	ns	Counter Enable/Increment Hold Time
tHD	1.0	-	-	ns	Input Data Hold Time
tHRST	1.0	-	-	ns	Counter Reset Hold Time
tHW	1.0	-	-	ns	Read/Write Enable Hold Time
tOE	12.0	12.0	12.0	ns	Output Enable to Data Valid Delay
tOHZ	1.0	7.0	7.0	ns	Output Enable to Data High Z Delay
tOLZ	2.0	-	-	ns	Output Enable to Output Low Z Time
tSA	4.0	-	-	ns	Address Setup Time
tSAD	4.0	-	-	ns	Address Strobe Setup Time
tSC	4.0	-	-	ns	Chip Enable Setup Time
tSCN	4.0	-	-	ns	Counter Enable/Increment Setup Time
tSD	4.0	-	-	ns	Input Data Setup Time
tSRST	4.0	-	-	ns	Counter Reset Setup Time
tSW	4.0	-	-	ns	Read/Write Enable Setup Time

4.8 Timing Data for TimingVersion 6

The following table provides a listing of the timing data values modeled when the model's TimingVersion is set to "6".

Timing Data for TimingVersion 6					
Parameter	Min	Typ	Max	Unit	Description
tCCS	9.0	-	-	ns	Clock to Clock Setup Time
tCD1	15.0	15.0	15.0	ns	Clock to Data Valid Delay - Flowthrough
tCD2	6.5	6.5	6.5	ns	Clock to Data Valid Delay - Pipelined
tCH1	6.5	-	-	ns	Clock High Time - Flowthrough
tCH2	4.0	-	-	ns	Clock High Time - Pipelined
tCKHZ	2.0	9.0	9.0	ns	Clock to Output High Z Delay
tCKLZ	2.0	-	-	ns	Clock to Output Low Z Delay
tCL1	6.5	-	-	ns	Clock Low Time - Flowthrough
tCL2	4.0	-	-	ns	Clock Low Time - Pipelined
tCYC1	19.0	-	-	ns	Clock Cycle Time - Flowthrough
tCYC2	10.0	-	-	ns	Clock Cycle Time - Pipelined
tDC	2.0	-	-	ns	Data Output Hold after Clock Assertion
tHA	0.0	-	-	ns	Address Hold Time
tHAD	0.0	-	-	ns	Address Strobe Hold Time
tHC	0.0	-	-	ns	Chip Enable Hold Time
tHCN	0.0	-	-	ns	Counter Enable/Increment Hold Time
tHD	0.0	-	-	ns	Input Data Hold Time
tHRST	0.0	-	-	ns	Counter Reset Hold Time
tHW	0.0	-	-	ns	Read/Write Enable Hold Time
tOE	8.0	8.0	8.0	ns	Output Enable to Data Valid Delay
tOHZ	1.0	7.0	7.0	ns	Output Enable to Data High Z Delay
tOLZ	2.0	-	-	ns	Output Enable to Output Low Z Time
tSA	3.5	-	-	ns	Address Setup Time
tSAD	3.5	-	-	ns	Address Strobe Setup Time
tSC	3.5	-	-	ns	Chip Enable Setup Time
tSCN	3.5	-	-	ns	Counter Enable/Increment Setup Time
tSD	3.5	-	-	ns	Input Data Setup Time
tSRST	3.5	-	-	ns	Counter Reset Setup Time
tSW	3.5	-	-	ns	Read/Write Enable Setup Time

4.9 Timing Data for TimingVersion 7

The following table provides a listing of the timing data values modeled when the model's TimingVersion is set to "7".

Timing Data for TimingVersion 7					
Parameter	Min	Typ	Max	Unit	Description
tCCS	10.0	-	-	ns	Clock to Clock Setup Time
tCD1	18.0	18.0	18.0	ns	Clock to Data Valid Delay - Flowthrough
tCD2	7.5	7.5	7.5	ns	Clock to Data Valid Delay - Pipelined

Timing Data for TimingVersion 7					
tCH1	7.5	-	-	ns	Clock High Time - Flowthrough
tCH2	5.0	-	-	ns	Clock High Time - Pipelined
tCKHZ	2.0	9.0	9.0	ns	Clock to Output High Z Delay
tCKLZ	2.0	-	-	ns	Clock to Output Low Z Delay
tCL1	7.5	-	-	ns	Clock Low Time - Flowthrough
tCL2	5.0	-	-	ns	Clock Low Time - Pipelined
tCYC1	22.0	-	-	ns	Clock Cycle Time - Flowthrough
tCYC2	12.0	-	-	ns	Clock Cycle Time - Pipelined
tDC	2.0	-	-	ns	Data Output Hold after Clock Assertion
tHA	0.0	-	-	ns	Address Hold Time
tHAD	0.0	-	-	ns	Address Strobe Hold Time
tHC	0.0	-	-	ns	Chip Enable Hold Time
tHCN	0.0	-	-	ns	Counter Enable/Increment Hold Time
tHD	0.0	-	-	ns	Input Data Hold Time
tHRST	0.0	-	-	ns	Counter Reset Hold Time
tHW	0.0	-	-	ns	Read/Write Enable Hold Time
tOE	9.0	9.0	9.0	ns	Output Enable to Data Valid Delay
tOHZ	1.0	7.0	7.0	ns	Output Enable to Data High Z Delay
tOLZ	2.0	-	-	ns	Output Enable to Output Low Z Time
tSA	4.0	-	-	ns	Address Setup Time
tSAD	4.0	-	-	ns	Address Strobe Setup Time
tSC	4.0	-	-	ns	Chip Enable Setup Time
tSCN	4.0	-	-	ns	Counter Enable/Increment Setup Time
tSD	4.0	-	-	ns	Input Data Setup Time
tSRST	4.0	-	-	ns	Counter Reset Setup Time
tSW	4.0	-	-	ns	Read/Write Enable Setup Time

4.10 Timing Data for TimingVersion 9

The following table provides a listing of the timing data values modeled when the model’s TimingVersion is set to "9".

Timing Data for TimingVersion 9					
Parameter	Min	Typ	Max	Unit	Description
tCCS	15.0	-	-	ns	Clock to Clock Setup Time
tCD1	20.0	20.0	20.0	ns	Clock to Data Valid Delay - Flowthrough
tCD2	9.0	9.0	9.0	ns	Clock to Data Valid Delay - Pipelined
tCH1	12.0	-	-	ns	Clock High Time - Flowthrough
tCH2	6.0	-	-	ns	Clock High Time - Pipelined
tCKHZ	2.0	9.0	9.0	ns	Clock to Output High Z Delay
tCKLZ	2.0	-	-	ns	Clock to Output Low Z Delay

Timing Data for TimingVersion 9					
tCL1	12.0	-	-	ns	Clock Low Time - Flowthrough
tCL2	6.0	-	-	ns	Clock Low Time - Pipelined
tCYC1	25.0	-	-	ns	Clock Cycle Time - Flowthrough
tCYC2	15.0	-	-	ns	Clock Cycle Time - Pipelined
tDC	2.0	-	-	ns	Data Output Hold after Clock Assertion
tHA	1.0	-	-	ns	Address Hold Time
tHAD	1.0	-	-	ns	Address Strobe Hold Time
tHC	1.0	-	-	ns	Chip Enable Hold Time
tHCN	1.0	-	-	ns	Counter Enable/Increment Hold Time
tHD	1.0	-	-	ns	Input Data Hold Time
tHRST	1.0	-	-	ns	Counter Reset Hold Time
tHW	1.0	-	-	ns	Read/Write Enable Hold Time
tOE	10.0	10.0	10.0	ns	Output Enable to Data Valid Delay
tOHZ	1.0	7.0	7.0	ns	Output Enable to Data High Z Delay
tOLZ	2.0	-	-	ns	Output Enable to Output Low Z Time
tSA	4.0	-	-	ns	Address Setup Time
tSAD	4.0	-	-	ns	Address Strobe Setup Time
tSC	4.0	-	-	ns	Chip Enable Setup Time
tSCN	4.0	-	-	ns	Counter Enable/Increment Setup Time
tSD	4.0	-	-	ns	Input Data Setup Time
tSRST	4.0	-	-	ns	Counter Reset Setup Time
tSW	4.0	-	-	ns	Read/Write Enable Setup Time

4.11 Verilog Instantiation Example

Following is an example of instantiating this model within Verilog for the VCS simulator. In this example, a subset of the model's simulation attributes (Verilog parameters) are shown set to their default value. For a complete list of supported simulation attributes, see the table in section 4.6.

```
cy7c09169a_mx_bus example_inst
  (
    .adsl_n     ( adsl_n     ),
    .adsr_n     ( adsr_n     ),
    .al         ( al         ),
    .ar         ( ar         ),
    .ce0l_n     ( ce0l_n     ),
    .ce0r_n     ( ce0r_n     ),
    .ce1l       ( ce1l       ),
    .ce1r       ( ce1r       ),
    .clkl       ( clkl       ),
    .clkr       ( clkr       ),
    .cntenl_n   ( cntenl_n   ),
    .cntenr_n   ( cntenr_n   ),
    .cntrstl_n  ( cntrstl_n  ),
    .cntrstr_n  ( cntrstr_n  ),
    .ft_n_pipel ( ft_n_pipel ),
    .ft_n_piper ( ft_n_piper ),
    .iol        ( iol        ),
    .ior        ( ior        ),
    .oel_n      ( oel_n      ),
    .oer_n      ( oer_n      ),
    .r_w_nl     ( r_w_nl     ),
    .r_w_nr     ( r_w_nr     )
  );
defparam example_inst.DelayRange    = "Max";
defparam example_inst.MemoryFile    = ".";
defparam example_inst.MessageLevel  = "15";
defparam example_inst.ModelAlias    = ".";
defparam example_inst.ModelId       = "-2";
defparam example_inst.TimingVersion = "6";
```

4.12 VHDL Instantiation Example

Following is an example of instantiating this model within VHDL for the Scirocco simulator. In this example, a subset of the model's simulation attributes (VHDL generics) are shown set to their default value. For a complete list of supported simulation attributes, see the table in section 4.6.

```
example_inst : cy7c09169a_mx
    generic map (
        DelayRange    => "Max",
        MemoryFile    => ".",
        MessageLevel  => "15",
        ModelAlias    => ".",
        ModelId       => "-2",
        TimingVersion => "6"
    )
    port map (
        adsl_n     => adsl_n,
        adsr_n     => adsr_n,
        al         => al,
        ar         => ar,
        ce0l_n     => ce0l_n,
        ce0r_n     => ce0r_n,
        ce1l       => ce1l,
        ce1r       => ce1r,
        clkl       => clkl,
        clkr       => clkr,
        cntenl_n   => cntenl_n,
        cntenr_n   => cntenr_n,
        cntrstl_n  => cntrstl_n,
        cntrstr_n  => cntrstr_n,
        ft_n_pipel => ft_n_pipel,
        ft_n_piper => ft_n_piper,
        iol        => iol,
        ior        => ior,
        oel_n      => oel_n,
        oer_n      => oer_n,
        r_w_nl     => r_w_nl,
        r_w_nr     => r_w_nr
    );
```

5 cy7c09169a_mx Model History

Synopsys publishes model history and bug fixes on the *IP Directory for the cy7c09169a_mx* . The behavior of DesignWare Memory Models may also be affected by revisions made to supporting utilities. For information concerning potential utility changes, please refer to *DesignWare Memory Model Release Notes* .