1 cy7c0831v_mx

- MDL Version: **01008**
- Title: **128K x 18 Synchronous Pipelined Dual Port SRAM**
- Date: **18-Feb-2004**
- Memory Type: **mpssram**
- Vendor: **Cypress Semiconductor Corporation**

2 Timing Selection

This model can be configured to run in either timing-accurate or function-only (no timing) mode. In timing-accurate mode, the model implements both propagational delays and timing checks. In function-only mode, the model propagates output changes immediately and timing checks are disabled.

2.1 Function-only Mode Selection

To run in function-only mode, set the model's TimingVersion attribute to "none".

2.2 Timing-accurate Timing Version Selection

To run in timing-accurate mode, the model's TimingVersion attribute is set to select the device specific timing associated with a vendor's component. The following table provides a mapping between vendor component names and the corresponding TimingVersion attribute values.

Component to TimingVersion Mapping	
Component Name	TimingVersion
CY7C0831V-100	100
CY7C0831V-133	133
CY7C0831V-150	150

Note: By default, this model uses TimingVersion "150".

3 Sources

The following sources were used as references for behavioral and timing characteristics in the development of this model.

1. Cypress Semiconductor Corporation “April 22, 2002”

4 Usage Notes

4.1 Configuring The Model

For information about configuring DesignWare Memory Models for use in simulation, refer to the installed version of the *Simulator Configuration Guide for Synopsys Models*. Or, for the most up-to-date version of this manual, see the *Simulator Configuration Guide for Synopsys Models* on the Synopsys external Web.

4.2 Using DesignWare Memory Models

For general information about using DesignWare Memory Models, refer to the installed version of the *DesignWare Memory Model User’s Manual*. Or, for the most up-to-date version of this manual, see the *DesignWare Memory Model User’s Manual* on the Synopsys external Web.

4.3 Using DesignWare MPSSRAM Models

The DesignWare Memory Model documentation set also contains additional usage information that applies to all MPSSRAM DesignWare Memory Models. For more information refer to the installed version of the *MPSSRAM DesignWare Memory Model Reference*. Or, for the most up-to-date version of this manual, see the *MPSSRAM DesignWare Memory Model Reference* on the Synopsys external Web.

4.4 Model Usage Notes

None

4.5 Model Port Description

The following table describes the pin interface for this model.

Model Port Description		
Port Name	Direction	Description
adsl_n	in	Port1 Address Strobe Input
adsr_n	in	Port2 Address Strobe Input
al[16:0]	inout	Port1 Address Inputs
ar[16:0]	inout	Port2 Address Inputs
bl_n[1:0]	in	Port1 Byte Select Inputs
br_n[1:0]	in	Port2 Byte Select Inputs
ce0l_n	in	Port1 Chip Enable Input
ce0r_n	in	Port2 Chip Enable Input
ce1l	in	Port1 Chip Enable Input
ce1r	in	Port2 Chip Enable Input
clkl	in	Port1 Clock Signal
clkr	in	Port2 Clock Signal
cntenl_n	in	Port1 Counter Enable Input
cntenr_n	in	Port2 Counter Enable Input
cntintl_n	out	Port1 Counter Interrupt Output
cntintr_n	out	Port2 Counter Interrupt Output
cntrstl_n	in	Port1 Counter Reset Input
cntrstr_n	in	Port2 Counter Reset Input
cnt_msk_nl	in	Port1 Address Counter Mask Register Enable Input
cnt_msk_nr	in	Port2 Address Counter Mask Register Enable Input
intl_n	out	Port1 MailBox Interrupt Flag Output
intr_n	out	Port2 MailBox Interrupt Flag Output
dql[17:0]	inout	Port1 Data Bus Input/Output
dqr[17:0]	inout	Port2 Data Bus Input/Output
mrst_n	in	Global Master Reset Input
oel_n	in	Port1 Output Enable Input
oer_n	in	Port2 Output Enable Input
r_w_nl	in	Port1 Read/Write Enable Input
r_w_nr	in	Port2 Read/Write Enable Input

4.6 Default Attribute Setting

The following table describes the default attribute settings for this model.

Default Attribute Setting	
Model Attribute	Default Value
DefaultData	111111111111111111
DelayRange	Max
MemoryFile	.
MessageLevel	15

Default Attribute Setting	
Model Attribute	Default Value
ModelAlias	.
ModelConfig	32'h0
ModelId	-2
TimingVersion	150

4.7 Timing Data for TimingVersion 100

The following table provides a listing of the timing data values modeled when the model's TimingVersion is set to "100".

Timing Data for TimingVersion 100					
Parameter	Min	Typ	Max	Unit	Description
tCA2	5.0	5.0	5.0	ns	Clock to Counter Address Valid Delay - Pipelined
tCCS	8.0	-	-	ns	Clock to Clock Setup Time
tCD2	5.0	5.0	5.0	ns	Clock to Data Valid Delay - Pipelined
tCH2	4.0	-	-	ns	Clock High Time - Pipelined
tCKHZ	0.0	5.0	5.0	ns	Clock to Output High Z Delay
tCKLZ	1.0	-	-	ns	Clock to Output Low Z Delay
tCL2	4.0	-	-	ns	Clock Low Time - Pipelined
tCM2	5.0	5.0	5.0	ns	Clock to Mask Register Readback Valid Delay - Pipelined
tCYC2	10.0	-	-	ns	Clock Cycle Time - Pipelined
tDC	1.0	-	-	ns	Data Output Hold after Clock Assertion
tHA	0.5	-	-	ns	Address Hold Time
tHAD	0.5	-	-	ns	Address Strobe Hold Time
tHB	0.5	-	-	ns	Byte Select Hold Time
tHC	0.5	-	-	ns	Chip Enable Hold Time
tHCM	0.5	-	-	ns	Address Counter Mask Register Hold Time
tHCN	0.5	-	-	ns	Counter Enable/Increment Hold Time
tHD	0.5	-	-	ns	Input Data Hold Time
tHRST	0.5	-	-	ns	Counter Reset Hold Time
tHW	0.5	-	-	ns	Read/Write Enable Hold Time
tOE	5.0	5.0	5.0	ns	Output Enable to Data Valid Delay
tOHZ	0.0	5.0	5.0	ns	Output Enable to Data High Z Delay
tOLZ	0.0	-	-	ns	Output Enable to Output Low Z Time
tRCINT	0.5	7.5	7.5	ns	Counter Interrupt Reset Time
tRINT	0.5	10.0	10.0	ns	Mailbox Interrupt Flag Reset Time
tRS	10.0	-	-	ns	Master Reset Pulse Width
tRSF	8.0	8.0	8.0	ns	Master Reset to Output Inactive

Timing Data for TimingVersion 100					
tRSR	10.0	-	-	ns	Master Reset Recovery Time
tRSS	8.5	-	-	ns	Master Reset Setup Time
tRScntint	8.0	8.0	8.0	ns	Master Reset to Counter Interrupt Flag Reset Time
tSA	3.0	-	-	ns	Address Setup Time
tSAD	3.0	-	-	ns	Address Strobe Setup Time
tSB	3.0	-	-	ns	Byte Select Setup Time
tSC	3.0	-	-	ns	Chip Enable Setup Time
tSCINT	0.5	7.5	7.5	ns	Counter Interrupt Set Time
tSCM	3.0	-	-	ns	Address Counter Mask Register Setup Time
tSCN	3.0	-	-	ns	Counter Enable/Increment Setup Time
tSD	3.0	-	-	ns	Input Data Setup Time
tSINT	0.5	10.0	10.0	ns	Mailbox Interrupt Flag Set Time
tSRST	3.0	-	-	ns	Counter Reset Setup Time
tSW	3.0	-	-	ns	Read/Write Enable Setup Time

4.8 Timing Data for TimingVersion 133

The following table provides a listing of the timing data values modeled when the model's TimingVersion is set to "133".

Timing Data for TimingVersion 133					
Parameter	Min	Typ	Max	Unit	Description
tCA2	4.4	4.4	4.4	ns	Clock to Counter Address Valid Delay - Pipelined
tCCS	6.0	-	-	ns	Clock to Clock Setup Time
tCD2	4.4	4.4	4.4	ns	Clock to Data Valid Delay - Pipelined
tCH2	3.0	-	-	ns	Clock High Time - Pipelined
tCKHZ	0.0	4.4	4.4	ns	Clock to Output High Z Delay
tCKLZ	1.0	-	-	ns	Clock to Output Low Z Delay
tCL2	3.0	-	-	ns	Clock Low Time - Pipelined
tCM2	4.4	4.4	4.4	ns	Clock to Mask Register Readback Valid Delay - Pipelined
tCYC2	7.5	-	-	ns	Clock Cycle Time - Pipelined
tDC	1.0	-	-	ns	Data Output Hold after Clock Assertion
tHA	0.6	-	-	ns	Address Hold Time
tHAD	0.6	-	-	ns	Address Strobe Hold Time
tHB	0.6	-	-	ns	Byte Select Hold Time
tHC	0.6	-	-	ns	Chip Enable Hold Time
tHCM	0.6	-	-	ns	Address Counter Mask Register Hold Time
tHCN	0.6	-	-	ns	Counter Enable/Increment Hold Time

Timing Data for TimingVersion 133					
tHD	0.6	-	-	ns	Input Data Hold Time
tHRST	0.6	-	-	ns	Counter Reset Hold Time
tHW	0.6	-	-	ns	Read/Write Enable Hold Time
tOE	4.4	4.4	4.4	ns	Output Enable to Data Valid Delay
tOHZ	0.0	4.4	4.4	ns	Output Enable to Data High Z Delay
tOLZ	0.0	-	-	ns	Output Enable to Output Low Z Time
tRCINT	0.5	5.7	5.7	ns	Counter Interrupt Reset Time
tRINT	0.5	7.5	7.5	ns	Mailbox Interrupt Flag Reset Time
tRS	7.5	-	-	ns	Master Reset Pulse Width
tRSF	6.5	6.5	6.5	ns	Master Reset to Output Inactive
tRSR	7.5	-	-	ns	Master Reset Recovery Time
tRSS	6.0	-	-	ns	Master Reset Setup Time
tRScntint	7.0	7.0	7.0	ns	Master Reset to Counter Interrupt Flag Reset Time
tSA	2.5	-	-	ns	Address Setup Time
tSAD	2.5	-	-	ns	Address Strobe Setup Time
tSB	2.5	-	-	ns	Byte Select Setup Time
tSC	2.5	-	-	ns	Chip Enable Setup Time
tSCINT	0.5	5.7	5.7	ns	Counter Interrupt Set Time
tSCM	2.5	-	-	ns	Address Counter Mask Register Setup Time
tSCN	2.5	-	-	ns	Counter Enable/Increment Setup Time
tSD	2.5	-	-	ns	Input Data Setup Time
tSINT	0.5	7.5	7.5	ns	Mailbox Interrupt Flag Set Time
tSRST	2.5	-	-	ns	Counter Reset Setup Time
tSW	2.5	-	-	ns	Read/Write Enable Setup Time

4.9 Timing Data for TimingVersion 150

The following table provides a listing of the timing data values modeled when the model's TimingVersion is set to "150".

Timing Data for TimingVersion 150					
Parameter	Min	Typ	Max	Unit	Description
tCA2	4.0	4.0	4.0	ns	Clock to Counter Address Valid Delay - Pipelined
tCCS	5.2	-	-	ns	Clock to Clock Setup Time
tCD2	4.0	4.0	4.0	ns	Clock to Data Valid Delay - Pipelined
tCH2	2.7	-	-	ns	Clock High Time - Pipelined
tCKHZ	0.0	4.0	4.0	ns	Clock to Output High Z Delay
tCKLZ	1.0	-	-	ns	Clock to Output Low Z Delay
tCL2	2.7	-	-	ns	Clock Low Time - Pipelined

Timing Data for TimingVersion 150					
tCM2	4.0	4.0	4.0	ns	Clock to Mask Register Readback Valid Delay - Pipelined
tCYC2	6.7	-	-	ns	Clock Cycle Time - Pipelined
tDC	1.0	-	-	ns	Data Output Hold after Clock Assertion
tHA	0.6	-	-	ns	Address Hold Time
tHAD	0.6	-	-	ns	Address Strobe Hold Time
tHB	0.6	-	-	ns	Byte Select Hold Time
tHC	0.6	-	-	ns	Chip Enable Hold Time
tHCM	0.6	-	-	ns	Address Counter Mask Register Hold Time
tHCN	0.6	-	-	ns	Counter Enable/Increment Hold Time
tHD	0.6	-	-	ns	Input Data Hold Time
tHRST	0.6	-	-	ns	Counter Reset Hold Time
tHW	0.6	-	-	ns	Read/Write Enable Hold Time
tOE	4.0	4.0	4.0	ns	Output Enable to Data Valid Delay
tOHZ	0.0	4.0	4.0	ns	Output Enable to Data High Z Delay
tOLZ	0.0	-	-	ns	Output Enable to Output Low Z Time
tRCINT	0.5	5.0	5.0	ns	Counter Interrupt Reset Time
tRINT	0.5	6.7	6.7	ns	Mailbox Interrupt Flag Reset Time
tRS	7.0	-	-	ns	Master Reset Pulse Width
tRSF	6.0	6.0	6.0	ns	Master Reset to Output Inactive
tRSR	6.0	-	-	ns	Master Reset Recovery Time
tRSS	6.0	-	-	ns	Master Reset Setup Time
tRScntint	5.8	5.8	5.8	ns	Master Reset to Counter Interrupt Flag Reset Time
tSA	2.3	-	-	ns	Address Setup Time
tSAD	2.3	-	-	ns	Address Strobe Setup Time
tSB	2.3	-	-	ns	Byte Select Setup Time
tSC	2.3	-	-	ns	Chip Enable Setup Time
tSCINT	0.5	5.0	5.0	ns	Counter Interrupt Set Time
tSCM	2.3	-	-	ns	Address Counter Mask Register Setup Time
tSCN	2.3	-	-	ns	Counter Enable/Increment Setup Time
tSD	2.3	-	-	ns	Input Data Setup Time
tSINT	0.5	6.7	6.7	ns	Mailbox Interrupt Flag Set Time
tSRST	2.3	-	-	ns	Counter Reset Setup Time
tSW	2.3	-	-	ns	Read/Write Enable Setup Time

4.10 Verilog Instantiation Example

Following is an example of instantiating this model within Verilog for the VCS simulator. In this example, a subset of the model's simulation attributes (Verilog parameters) are shown set to their default value. For a complete list of supported simulation attributes, see the table in section 4.6.

```
cy7c0831v_mx_bus example_inst
  (
    .adsl_n     ( adsl_n     ),
    .adsr_n     ( adsr_n     ),
    .al         ( al         ),
    .ar         ( ar         ),
    .bl_n       ( bl_n       ),
    .br_n       ( br_n       ),
    .ce0l_n     ( ce0l_n     ),
    .ce0r_n     ( ce0r_n     ),
    .ce1l       ( ce1l       ),
    .ce1r       ( ce1r       ),
    .clkl       ( clkl       ),
    .clkr       ( clkr       ),
    .cntenl_n   ( cntenl_n   ),
    .cntenr_n   ( cntenr_n   ),
    .cntintl_n  ( cntintl_n  ),
    .cntintr_n  ( cntintr_n  ),
    .cntrstl_n  ( cntrstl_n  ),
    .cntrstr_n  ( cntrstr_n  ),
    .cnt_msk_nl ( cnt_msk_nl ),
    .cnt_msk_nr ( cnt_msk_nr ),
    .intl_n     ( intl_n     ),
    .intr_n     ( intr_n     ),
    .dql        ( dql        ),
    .dqr        ( dqr        ),
    .mrst_n     ( mrst_n     ),
    .oel_n      ( oel_n      ),
    .oer_n      ( oer_n      ),
    .r_w_nl     ( r_w_nl     ),
    .r_w_nr     ( r_w_nr     )
  );
defparam example_inst.DelayRange    = "Max";
defparam example_inst.MemoryFile    = ".";
defparam example_inst.MessageLevel  = "15";
defparam example_inst.ModelAlias    = ".";
defparam example_inst.ModelId       = "-2";
defparam example_inst.TimingVersion = "150";
```

4.11 VHDL Instantiation Example

Following is an example of instantiating this model within VHDL for the Scirocco simulator. In this example, a subset of the model's simulation attributes (VHDL generics) are shown set to their default value. For a complete list of supported simulation attributes, see the table in section 4.6.

```
example_inst : cy7c0831v_mx
    generic map (
        DelayRange    => "Max",
        MemoryFile    => ".",
        MessageLevel  => "15",
        ModelAlias    => ".",
        ModelId       => "-2",
        TimingVersion => "150"
    )
    port map (
        adsl_n     => adsl_n,
        adsr_n     => adsr_n,
        al         => al,
        ar         => ar,
        bl_n       => bl_n,
        br_n       => br_n,
        ce0l_n     => ce0l_n,
        ce0r_n     => ce0r_n,
        ce1l       => ce1l,
        ce1r       => ce1r,
        clkl       => clkl,
        clkr       => clkr,
        cntenl_n   => cntenl_n,
        cntenr_n   => cntenr_n,
        cntintl_n  => cntintl_n,
        cntintr_n  => cntintr_n,
        cntrstl_n  => cntrstl_n,
        cntrstr_n  => cntrstr_n,
        cnt_msk_nl => cnt_msk_nl,
        cnt_msk_nr => cnt_msk_nr,
        intl_n     => intl_n,
        intr_n     => intr_n,
        dql        => dql,
        dqr        => dqr,
        mrst_n     => mrst_n,
        oel_n      => oel_n,
        oer_n      => oer_n,
        r_w_nl     => r_w_nl,
```

```
        r_w_nr      => r_w_nr
    );
```

5 cy7c0831v_mx Model History

Synopsys publishes model history and bug fixes on the *IP Directory for the cy7c0831v_mx* . The behavior of DesignWare Memory Models may also be affected by revisions made to supporting utilities. For information concerning potential utility changes, please refer to *DesignWare Memory Model Release Notes* .