

1 cy7c1009b_mx

- MDL Version: **01012**
- Title: **128K x 8 Asynchronous SRAM**
- Date: **18-May-2006**
- Memory Type: **sram**
- Vendor: **Cypress Semiconductor Corporation**

2 Timing Selection

This model can be configured to run in either timing-accurate or function-only (no timing) mode. In timing-accurate mode, the model implements both propagational delays and timing checks. In function-only mode, the model propagates output changes immediately and timing checks are disabled.

2.1 Function-only Mode Selection

To run in function-only mode, set the model's TimingVersion attribute to "none".

2.2 Timing-accurate Timing Version Selection

To run in timing-accurate mode, the model's TimingVersion attribute is set to select the device specific timing associated with a vendor's component. The following table provides a mapping between vendor component names and the corresponding TimingVersion attribute values.

| Component to TimingVersion Mapping | |
|---|---------------|
| Component Name | TimingVersion |
| CY7C1009B-12 | 12 |
| CY7C1009B-15 | 15 |
| CY7C1009B-20 | 20 |
| CY7C1009B-25 | 25 |
| CY7C1009B-35 | 35 |

Note: By default, this model uses TimingVersion "12".

3 Sources

The following sources were used as references for behavioral and timing characteristics in the development of this model.

1. Cypress Semiconductor Corporation “Document #: 38-05038 Rev. ** Revised August 24, 2001”

4 Usage Notes

4.1 Configuring The Model

For information about configuring DesignWare Memory Models for use in simulation, refer to the installed version of the [Simulator Configuration Guide for Synopsys Models](#). Or, for the most up-to-date version of this manual, see the [Simulator Configuration Guide for Synopsys Models](#) on the Synopsys external Web.

4.2 Using DesignWare Memory Models

For general information about using DesignWare Memory Models, refer to the installed version of the [DesignWare Memory Model User's Manual](#). Or, for the most up-to-date version of this manual, see the [DesignWare Memory Model User's Manual](#) on the Synopsys external Web.

4.3 Using DesignWare SRAM Models

The DesignWare Memory Model documentation set also contains additional usage information that applies to all SRAM DesignWare Memory Models. For more information refer to the installed version of the [SRAM DesignWare Memory Model Reference](#). Or, for the most up-to-date version of this manual, see the [SRAM DesignWare Memory Model Reference](#) on the Synopsys external Web.

4.4 Model Usage Notes

None

4.5 Model Port Description

The following table describes the pin interface for this model.

| Model Port Description | | |
|------------------------|-----------|---------------|
| Port Name | Direction | Description |
| a[16:0] | in | Address Bus |
| ce1_n | in | Chip Enable 1 |
| ce2 | in | Chip Enable 2 |
| io[7:0] | inout | IO Data Bus |
| oe_n | in | Output Enable |
| we_n | in | Write Enable |

4.6 Default Attribute Setting

The following table describes the default attribute settings for this model.

| Default Attribute Setting | |
|---------------------------|---------------|
| Model Attribute | Default Value |
| DefaultData | 11111111 |
| DelayRange | Max |
| MemoryFile | . |
| MessageLevel | 15 |
| ModelAlias | . |
| ModelConfig | 32'h0 |
| ModelId | -2 |
| TimingVersion | 12 |

4.7 Timing Data for TimingVersion 12

The following table provides a listing of the timing data values modeled when the model's TimingVersion is set to "12".

| Timing Data for TimingVersion 12 | | | | | |
|----------------------------------|------|------|------|------|---|
| Parameter | Min | Typ | Max | Unit | Description |
| tAA | 12.0 | 12.0 | 12.0 | ns | Address to Output Data Valid |
| tACE | 12.0 | 12.0 | 12.0 | ns | Chip Enable 1 Asserted to Output Data Valid |
| tACE2 | 12.0 | 12.0 | 12.0 | ns | Chip Enable 2 Asserted to Output Data Valid |
| tAW | 10.0 | - | - | ns | Address Setup to Write End |
| tDOE | 6.0 | 6.0 | 6.0 | ns | Output Enable Asserted to Output Data Valid |
| tHA | 0.0 | - | - | ns | Address Hold from Write End (Chip Enable 1) |
| tHA2 | 0.0 | - | - | ns | Address Hold from Write End (Chip Enable 2) |
| tHA_WE | 0.0 | - | - | ns | Address Hold from Write End (Write Enable) |
| tHD | 0.0 | - | - | ns | Data Hold from Write End (Chip Enable 1) |
| tHD2 | 0.0 | - | - | ns | Data Hold from Write End (Chip Enable 2) |

| Timing Data for TimingVersion 12 | | | | | |
|----------------------------------|------|-----|-----|----|--|
| tHD_WE | 0.0 | - | - | ns | Data Hold from Write End (Write Enable) |
| tHZCE | 6.0 | 6.0 | 6.0 | ns | Chip Enable 1 Deasserted to Output Data High Z |
| tHZCE2 | 6.0 | 6.0 | 6.0 | ns | Chip Enable 2 Deasserted to Output Data High Z |
| tHZOE | 6.0 | 6.0 | 6.0 | ns | Output Enable Deasserted to Output Data High Z |
| tHZWE | 6.0 | 6.0 | 6.0 | ns | Write Enable Asserted to Output Data High Z |
| tLZCE | 3.0 | - | - | ns | Chip Enable 1 Asserted to Output Data Low Z |
| tLZCE2 | 3.0 | - | - | ns | Chip Enable 2 Asserted to Output Data Low Z |
| tLZOE | 0.0 | - | - | ns | Output Enable Asserted to Output Data Low Z |
| tLZWE | 3.0 | - | - | ns | Write Enable Deasserted to Output Data Low Z |
| tOHA | 3.0 | - | - | ns | Output Data Invalid from Address Change |
| tPWE | 10.0 | - | - | ns | Write Enable Pulse Width (Output Enable is Deasserted) |
| tPWE1 | 13.0 | - | - | ns | Write Enable Pulse Width (Output Enable is Asserted) |
| tRC | 12.0 | - | - | ns | Read Cycle Time |
| tSA | 0.0 | - | - | ns | Address Setup to Write Start |
| tSCE | 10.0 | - | - | ns | Chip Enable 1 Asserted to Write End |
| tSCE2 | 10.0 | - | - | ns | Chip Enable 2 Asserted to Write End |
| tSD | 7.0 | - | - | ns | Data Setup to Write End |
| tWC | 12.0 | - | - | ns | Write cycle time |

4.8 Timing Data for TimingVersion 15

The following table provides a listing of the timing data values modeled when the model's TimingVersion is set to "15".

| Timing Data for TimingVersion 15 | | | | | |
|----------------------------------|------|------|------|------|---|
| Parameter | Min | Typ | Max | Unit | Description |
| tAA | 15.0 | 15.0 | 15.0 | ns | Address to Output Data Valid |
| tACE | 15.0 | 15.0 | 15.0 | ns | Chip Enable 1 Asserted to Output Data Valid |
| tACE2 | 15.0 | 15.0 | 15.0 | ns | Chip Enable 2 Asserted to Output Data Valid |
| tAW | 12.0 | - | - | ns | Address Setup to Write End |
| tDOE | 7.0 | 7.0 | 7.0 | ns | Output Enable Asserted to Output Data Valid |
| tHA | 0.0 | - | - | ns | Address Hold from Write End (Chip Enable 1) |
| tHA2 | 0.0 | - | - | ns | Address Hold from Write End (Chip Enable 2) |
| tHA_WE | 0.0 | - | - | ns | Address Hold from Write End (Write Enable) |
| tHD | 0.0 | - | - | ns | Data Hold from Write End (Chip Enable 1) |

| Timing Data for TimingVersion 15 | | | | | |
|----------------------------------|------|-----|-----|----|--|
| tHD2 | 0.0 | - | - | ns | Data Hold from Write End (Chip Enable 2) |
| tHD_WE | 0.0 | - | - | ns | Data Hold from Write End (Write Enable) |
| tHZCE | 7.0 | 7.0 | 7.0 | ns | Chip Enable 1 Deasserted to Output Data High Z |
| tHZCE2 | 7.0 | 7.0 | 7.0 | ns | Chip Enable 2 Deasserted to Output Data High Z |
| tHZOE | 7.0 | 7.0 | 7.0 | ns | Output Enable Deasserted to Output Data High Z |
| tHZWE | 7.0 | 7.0 | 7.0 | ns | Write Enable Asserted to Output Data High Z |
| tLZCE | 3.0 | - | - | ns | Chip Enable 1 Asserted to Output Data Low Z |
| tLZCE2 | 3.0 | - | - | ns | Chip Enable 2 Asserted to Output Data Low Z |
| tLZOE | 0.0 | - | - | ns | Output Enable Asserted to Output Data Low Z |
| tLZWE | 3.0 | - | - | ns | Write Enable Deasserted to Output Data Low Z |
| tOHA | 3.0 | - | - | ns | Output Data Invalid from Address Change |
| tPWE | 12.0 | - | - | ns | Write Enable Pulse Width (Output Enable is Deasserted) |
| tPWE1 | 15.0 | - | - | ns | Write Enable Pulse Width (Output Enable is Asserted) |
| tRC | 15.0 | - | - | ns | Read Cycle Time |
| tSA | 0.0 | - | - | ns | Address Setup to Write Start |
| tSCE | 12.0 | - | - | ns | Chip Enable 1 Asserted to Write End |
| tSCE2 | 12.0 | - | - | ns | Chip Enable 2 Asserted to Write End |
| tSD | 8.0 | - | - | ns | Data Setup to Write End |
| tWC | 15.0 | - | - | ns | Write cycle time |

4.9 Timing Data for TimingVersion 20

The following table provides a listing of the timing data values modeled when the model's TimingVersion is set to "20".

| Timing Data for TimingVersion 20 | | | | | |
|----------------------------------|------|------|------|------|---|
| Parameter | Min | Typ | Max | Unit | Description |
| tAA | 20.0 | 20.0 | 20.0 | ns | Address to Output Data Valid |
| tACE | 20.0 | 20.0 | 20.0 | ns | Chip Enable 1 Asserted to Output Data Valid |
| tACE2 | 20.0 | 20.0 | 20.0 | ns | Chip Enable 2 Asserted to Output Data Valid |
| tAW | 15.0 | - | - | ns | Address Setup to Write End |
| tDOE | 8.0 | 8.0 | 8.0 | ns | Output Enable Asserted to Output Data Valid |
| tHA | 0.0 | - | - | ns | Address Hold from Write End (Chip Enable 1) |
| tHA2 | 0.0 | - | - | ns | Address Hold from Write End (Chip Enable 2) |
| tHA_WE | 0.0 | - | - | ns | Address Hold from Write End (Write Enable) |

| Timing Data for TimingVersion 20 | | | | | |
|----------------------------------|------|-----|-----|----|--|
| tHD | 0.0 | - | - | ns | Data Hold from Write End (Chip Enable 1) |
| tHD2 | 0.0 | - | - | ns | Data Hold from Write End (Chip Enable 2) |
| tHD_WE | 0.0 | - | - | ns | Data Hold from Write End (Write Enable) |
| tHZCE | 8.0 | 8.0 | 8.0 | ns | Chip Enable 1 Deasserted to Output Data High Z |
| tHZCE2 | 8.0 | 8.0 | 8.0 | ns | Chip Enable 2 Deasserted to Output Data High Z |
| tHZOE | 8.0 | 8.0 | 8.0 | ns | Output Enable Deasserted to Output Data High Z |
| tHZWE | 8.0 | 8.0 | 8.0 | ns | Write Enable Asserted to Output Data High Z |
| tLZCE | 3.0 | - | - | ns | Chip Enable 1 Asserted to Output Data Low Z |
| tLZCE2 | 3.0 | - | - | ns | Chip Enable 2 Asserted to Output Data Low Z |
| tLZOE | 0.0 | - | - | ns | Output Enable Asserted to Output Data Low Z |
| tLZWE | 3.0 | - | - | ns | Write Enable Deasserted to Output Data Low Z |
| tOHA | 3.0 | - | - | ns | Output Data Invalid from Address Change |
| tPWE | 12.0 | - | - | ns | Write Enable Pulse Width (Output Enable is Deasserted) |
| tPWE1 | 18.0 | - | - | ns | Write Enable Pulse Width (Output Enable is Asserted) |
| tRC | 20.0 | - | - | ns | Read Cycle Time |
| tSA | 0.0 | - | - | ns | Address Setup to Write Start |
| tSCE | 15.0 | - | - | ns | Chip Enable 1 Asserted to Write End |
| tSCE2 | 15.0 | - | - | ns | Chip Enable 2 Asserted to Write End |
| tSD | 10.0 | - | - | ns | Data Setup to Write End |
| tWC | 20.0 | - | - | ns | Write cycle time |

4.10 Timing Data for TimingVersion 25

The following table provides a listing of the timing data values modeled when the model's TimingVersion is set to "25".

| Timing Data for TimingVersion 25 | | | | | |
|----------------------------------|------|------|------|------|---|
| Parameter | Min | Typ | Max | Unit | Description |
| tAA | 25.0 | 25.0 | 25.0 | ns | Address to Output Data Valid |
| tACE | 25.0 | 25.0 | 25.0 | ns | Chip Enable 1 Asserted to Output Data Valid |
| tACE2 | 25.0 | 25.0 | 25.0 | ns | Chip Enable 2 Asserted to Output Data Valid |
| tAW | 20.0 | - | - | ns | Address Setup to Write End |
| tDOE | 10.0 | 10.0 | 10.0 | ns | Output Enable Asserted to Output Data Valid |
| tHA | 0.0 | - | - | ns | Address Hold from Write End (Chip Enable 1) |
| tHA2 | 0.0 | - | - | ns | Address Hold from Write End (Chip Enable 2) |

| Timing Data for TimingVersion 25 | | | | | |
|----------------------------------|------|------|------|----|--|
| tHA_WE | 0.0 | - | - | ns | Address Hold from Write End (Write Enable) |
| tHD | 0.0 | - | - | ns | Data Hold from Write End (Chip Enable 1) |
| tHD2 | 0.0 | - | - | ns | Data Hold from Write End (Chip Enable 2) |
| tHD_WE | 0.0 | - | - | ns | Data Hold from Write End (Write Enable) |
| tHZCE | 10.0 | 10.0 | 10.0 | ns | Chip Enable 1 Deasserted to Output Data High Z |
| tHZCE2 | 10.0 | 10.0 | 10.0 | ns | Chip Enable 2 Deasserted to Output Data High Z |
| tHZOE | 10.0 | 10.0 | 10.0 | ns | Output Enable Deasserted to Output Data High Z |
| tHZWE | 10.0 | 10.0 | 10.0 | ns | Write Enable Asserted to Output Data High Z |
| tLZCE | 5.0 | - | - | ns | Chip Enable 1 Asserted to Output Data Low Z |
| tLZCE2 | 5.0 | - | - | ns | Chip Enable 2 Asserted to Output Data Low Z |
| tLZOE | 0.0 | - | - | ns | Output Enable Asserted to Output Data Low Z |
| tLZWE | 5.0 | - | - | ns | Write Enable Deasserted to Output Data Low Z |
| tOHA | 5.0 | - | - | ns | Output Data Invalid from Address Change |
| tPWE | 15.0 | - | - | ns | Write Enable Pulse Width (Output Enable is Deasserted) |
| tPWE1 | 25.0 | - | - | ns | Write Enable Pulse Width (Output Enable is Asserted) |
| tRC | 25.0 | - | - | ns | Read Cycle Time |
| tSA | 0.0 | - | - | ns | Address Setup to Write Start |
| tSCE | 20.0 | - | - | ns | Chip Enable 1 Asserted to Write End |
| tSCE2 | 20.0 | - | - | ns | Chip Enable 2 Asserted to Write End |
| tSD | 15.0 | - | - | ns | Data Setup to Write End |
| tWC | 25.0 | - | - | ns | Write cycle time |

4.11 Timing Data for TimingVersion 35

The following table provides a listing of the timing data values modeled when the model's TimingVersion is set to "35".

| Timing Data for TimingVersion 35 | | | | | |
|----------------------------------|------|------|------|------|---|
| Parameter | Min | Typ | Max | Unit | Description |
| tAA | 35.0 | 35.0 | 35.0 | ns | Address to Output Data Valid |
| tACE | 35.0 | 35.0 | 35.0 | ns | Chip Enable 1 Asserted to Output Data Valid |
| tACE2 | 35.0 | 35.0 | 35.0 | ns | Chip Enable 2 Asserted to Output Data Valid |
| tAW | 25.0 | - | - | ns | Address Setup to Write End |
| tDOE | 15.0 | 15.0 | 15.0 | ns | Output Enable Asserted to Output Data Valid |
| tHA | 0.0 | - | - | ns | Address Hold from Write End (Chip Enable 1) |

| Timing Data for TimingVersion 35 | | | | | |
|----------------------------------|------|------|------|----|--|
| tHA2 | 0.0 | - | - | ns | Address Hold from Write End (Chip Enable 2) |
| tHA_WE | 0.0 | - | - | ns | Address Hold from Write End (Write Enable) |
| tHD | 0.0 | - | - | ns | Data Hold from Write End (Chip Enable 1) |
| tHD2 | 0.0 | - | - | ns | Data Hold from Write End (Chip Enable 2) |
| tHD_WE | 0.0 | - | - | ns | Data Hold from Write End (Write Enable) |
| tHZCE | 15.0 | 15.0 | 15.0 | ns | Chip Enable 1 Deasserted to Output Data High Z |
| tHZCE2 | 15.0 | 15.0 | 15.0 | ns | Chip Enable 2 Deasserted to Output Data High Z |
| tHZOE | 15.0 | 15.0 | 15.0 | ns | Output Enable Deasserted to Output Data High Z |
| tHZWE | 15.0 | 15.0 | 15.0 | ns | Write Enable Asserted to Output Data High Z |
| tLZCE | 5.0 | - | - | ns | Chip Enable 1 Asserted to Output Data Low Z |
| tLZCE2 | 5.0 | - | - | ns | Chip Enable 2 Asserted to Output Data Low Z |
| tLZOE | 0.0 | - | - | ns | Output Enable Asserted to Output Data Low Z |
| tLZWE | 5.0 | - | - | ns | Write Enable Deasserted to Output Data Low Z |
| tOHA | 5.0 | - | - | ns | Output Data Invalid from Address Change |
| tPWE | 20.0 | - | - | ns | Write Enable Pulse Width (Output Enable is Deasserted) |
| tPWE1 | 35.0 | - | - | ns | Write Enable Pulse Width (Output Enable is Asserted) |
| tRC | 35.0 | - | - | ns | Read Cycle Time |
| tSA | 0.0 | - | - | ns | Address Setup to Write Start |
| tSCE | 25.0 | - | - | ns | Chip Enable 1 Asserted to Write End |
| tSCE2 | 25.0 | - | - | ns | Chip Enable 2 Asserted to Write End |
| tSD | 20.0 | - | - | ns | Data Setup to Write End |
| tWC | 35.0 | - | - | ns | Write cycle time |

4.12 Verilog Instantiation Example

Following is an example of instantiating this model within Verilog for the VCS simulator. In this example, a subset of the model's simulation attributes (Verilog parameters) are shown set to their default value. For a complete list of supported simulation attributes, see the table in section 4.6.

```
cy7c1009b_mx_bus example_inst
(
    .a      ( a      ),
    .ce1_n  ( ce1_n  ),
    .ce2    ( ce2    ),
    .io     ( io     ),
    .oe_n   ( oe_n   ),
    .we_n   ( we_n   )
);
defparam example_inst.DelayRange      = "Max";
defparam example_inst.MemoryFile     = ".";
defparam example_inst.MessageLevel   = "15";
defparam example_inst.ModelAlias     = ".";
defparam example_inst.ModelId        = "-2";
defparam example_inst.TimingVersion  = "12";
```

4.13 VHDL Instantiation Example

Following is an example of instantiating this model within VHDL for the Scirocco simulator. In this example, a subset of the model's simulation attributes (VHDL generics) are shown set to their default value. For a complete list of supported simulation attributes, see the table in section 4.6.

```
example_inst : cy7c1009b_mx
  generic map (
    DelayRange      => "Max",
    MemoryFile      => ".",
    MessageLevel    => "15",
    ModelAlias      => ".",
    ModelId         => "-2",
    TimingVersion   => "12"
  )
  port map (
    a      => a,
    cel_n  => cel_n,
    ce2    => ce2,
    io     => io,
    oe_n   => oe_n,
    we_n   => we_n
  );
```

5 cy7c1009b_mx Model History

Synopsys publishes model history and bug fixes on the [IP Directory for the cy7c1009b_mx](#). The behavior of DesignWare Memory Models may also be affected by revisions made to supporting utilities. For information concerning potential utility changes, please refer to [DesignWare Memory Model Release Notes](#).