1 cy7c04314bv_mx

- MDL Version: **01008**
- Title: **16K x 18 Synchronous Quad Port SRAM**
- Date: **13-Feb-2004**
- Memory Type: **mpssram**
- Vendor: **Cypress Semiconductor Corporation**

2 Timing Selection

This model can be configured to run in either timing-accurate or function-only (no timing) mode. In timing-accurate mode, the model implements both propagational delays and timing checks. In function-only mode, the model propagates output changes immediately and timing checks are disabled.

2.1 Function-only Mode Selection

To run in function-only mode, set the model's TimingVersion attribute to "none".

2.2 Timing-accurate Timing Version Selection

To run in timing-accurate mode, the model's TimingVersion attribute is set to select the device specific timing associated with a vendor's component. The following table provides a mapping between vendor component names and the corresponding TimingVersion attribute values.

Component to TimingVersion Mapping	
Component Name	TimingVersion
CY7C04314BV-100	100
CY7C04314BV-133	133

Note: By default, this model uses TimingVersion "133".

3 Sources

The following sources were used as references for behavioral and timing characteristics in the development of this model.

1. Cypress Semiconductor Corporation “September 6, 2001”

4 Usage Notes

4.1 Configuring The Model

For information about configuring DesignWare Memory Models for use in simulation, refer to the installed version of the *Simulator Configuration Guide for Synopsys Models*. Or, for the most up-to-date version of this manual, see the *Simulator Configuration Guide for Synopsys Models* on the Synopsys external Web.

4.2 Using DesignWare Memory Models

For general information about using DesignWare Memory Models, refer to the installed version of the *DesignWare Memory Model User’s Manual*. Or, for the most up-to-date version of this manual, see the *DesignWare Memory Model User’s Manual* on the Synopsys external Web.

4.3 Using DesignWare MPSSRAM Models

The DesignWare Memory Model documentation set also contains additional usage information that applies to all MPSSRAM DesignWare Memory Models. For more information refer to the installed version of the *MPSSRAM DesignWare Memory Model Reference*. Or, for the most up-to-date version of this manual, see the *MPSSRAM DesignWare Memory Model Reference* on the Synopsys external Web.

4.4 Model Usage Notes

Device pins ubp1# and lbp1# modeled as bep1_n bus. Device pins ubp2# and lbp2# modeled as bep2_n bus. Device pins ubp3# and lbp3# modeled as bep3_n bus. Device pins ubp4# and lbp4# modeled as bep4_n bus.

4.5 Model Port Description

The following table describes the pin interface for this model.

Model Port Description		
Port Name	Direction	Description
ap1[13:0]	in	Port1 Address Inputs
ap2[13:0]	in	Port2 Address Inputs
ap3[13:0]	in	Port3 Address Inputs
ap4[13:0]	in	Port4 Address Inputs
bep1_n[1:0]	in	Port1 Byte Select Inputs
bep2_n[1:0]	in	Port2 Byte Select Inputs
bep3_n[1:0]	in	Port3 Byte Select Inputs
bep4_n[1:0]	in	Port4 Byte Select Inputs
ce0p1_n	in	Port1 Chip Enable Input
ce0p2_n	in	Port2 Chip Enable Input
ce0p3_n	in	Port3 Chip Enable Input
ce0p4_n	in	Port4 Chip Enable Input
ce1p1	in	Port1 Chip Enable Input
ce1p2	in	Port2 Chip Enable Input
ce1p3	in	Port3 Chip Enable Input
ce1p4	in	Port4 Chip Enable Input
clkp1	in	Port1 Clock Signal
clkp2	in	Port2 Clock Signal
clkp3	in	Port3 Clock Signal
clkp4	in	Port4 Clock Signal
intp1_n	out	Port1 MailBox Interrupt Flag Output
intp2_n	out	Port2 MailBox Interrupt Flag Output
intp3_n	out	Port3 MailBox Interrupt Flag Output
intp4_n	out	Port4 MailBox Interrupt Flag Output
iop1[17:0]	inout	Port1 Data Bus Input/Output
iop2[17:0]	inout	Port2 Data Bus Input/Output
iop3[17:0]	inout	Port3 Data Bus Input/Output
iop4[17:0]	inout	Port4 Data Bus Input/Output
mrst_n	in	Global Master Reset Input
oep1_n	in	Port1 Output Enable Input
oep2_n	in	Port2 Output Enable Input
oep3_n	in	Port3 Output Enable Input
oep4_n	in	Port4 Output Enable Input
r_w_np1	in	Port1 Read/Write Enable Input
r_w_np2	in	Port2 Read/Write Enable Input
r_w_np3	in	Port3 Read/Write Enable Input
r_w_np4	in	Port4 Read/Write Enable Input

4.6 Default Attribute Setting

The following table describes the default attribute settings for this model.

Default Attribute Setting	
Model Attribute	Default Value
DefaultData	111111111111111111
DelayRange	Max
MemoryFile	.
MessageLevel	15
ModelAlias	.
ModelConfig	32'h0
ModelId	-2
TimingVersion	133

4.7 Timing Data for TimingVersion 100

The following table provides a listing of the timing data values modeled when the model's TimingVersion is set to "100".

Timing Data for TimingVersion 100					
Parameter	Min	Typ	Max	Unit	Description
tCCS	9.0	-	-	ns	Clock to Clock Setup Time
tCD2	5.0	5.0	5.0	ns	Clock to Data Valid Delay - Pipelined
tCH2	4.0	-	-	ns	Clock High Time - Pipelined
tCKHZ	1.0	6.8	6.8	ns	Clock to Output High Z Delay
tCKLZ	1.0	-	-	ns	Clock to Output Low Z Delay
tCL2	4.0	-	-	ns	Clock Low Time - Pipelined
tCYC2	10.0	-	-	ns	Clock Cycle Time - Pipelined
tDC	1.0	-	-	ns	Data Output Hold after Clock Assertion
tHA	0.7	-	-	ns	Address Hold Time
tHB	0.7	-	-	ns	Byte Select Hold Time
tHC	0.7	-	-	ns	Chip Enable Hold Time
tHD	0.7	-	-	ns	Input Data Hold Time
tHW	0.7	-	-	ns	Read/Write Enable Hold Time
tOE	8.0	8.0	8.0	ns	Output Enable to Data Valid Delay
tOHZ	1.0	7.0	7.0	ns	Output Enable to Data High Z Delay
tOLZ	1.0	-	-	ns	Output Enable to Output Low Z Time
tRINT	1.0	10.0	10.0	ns	Mailbox Interrupt Flag Reset Time
tROF	8.0	8.0	8.0	ns	Master Reset to Output Inactive
tRS	10.0	-	-	ns	Master Reset Pulse Width
tRSR	10.0	-	-	ns	Master Reset Recovery Time

Timing Data for TimingVersion 100					
tSA	3.0	-	-	ns	Address Setup Time
tSB	3.0	-	-	ns	Byte Select Setup Time
tSC	3.0	-	-	ns	Chip Enable Setup Time
tSD	3.0	-	-	ns	Input Data Setup Time
tSINT	1.0	10.0	10.0	ns	Mailbox Interrupt Flag Set Time
tSW	3.0	-	-	ns	Read/Write Enable Setup Time

4.8 Timing Data for TimingVersion 133

The following table provides a listing of the timing data values modeled when the model's TimingVersion is set to "133".

Timing Data for TimingVersion 133					
Parameter	Min	Typ	Max	Unit	Description
tCCS	6.5	-	-	ns	Clock to Clock Setup Time
tCD2	4.7	4.7	4.7	ns	Clock to Data Valid Delay - Pipelined
tCH2	3.0	-	-	ns	Clock High Time - Pipelined
tCKHZ	1.0	4.8	4.8	ns	Clock to Output High Z Delay
tCKLZ	1.0	-	-	ns	Clock to Output Low Z Delay
tCL2	3.0	-	-	ns	Clock Low Time - Pipelined
tCYC2	7.5	-	-	ns	Clock Cycle Time - Pipelined
tDC	1.0	-	-	ns	Data Output Hold after Clock Assertion
tHA	0.7	-	-	ns	Address Hold Time
tHB	0.7	-	-	ns	Byte Select Hold Time
tHC	0.7	-	-	ns	Chip Enable Hold Time
tHD	0.7	-	-	ns	Input Data Hold Time
tHW	0.7	-	-	ns	Read/Write Enable Hold Time
tOE	6.5	6.5	6.5	ns	Output Enable to Data Valid Delay
tOHZ	1.0	6.0	6.0	ns	Output Enable to Data High Z Delay
tOLZ	1.0	-	-	ns	Output Enable to Output Low Z Time
tRINT	1.0	7.5	7.5	ns	Mailbox Interrupt Flag Reset Time
tROF	6.5	6.5	6.5	ns	Master Reset to Output Inactive
tRS	7.5	-	-	ns	Master Reset Pulse Width
tRSR	7.5	-	-	ns	Master Reset Recovery Time
tSA	2.3	-	-	ns	Address Setup Time
tSB	2.3	-	-	ns	Byte Select Setup Time
tSC	2.3	-	-	ns	Chip Enable Setup Time
tSD	2.3	-	-	ns	Input Data Setup Time
tSINT	1.0	7.5	7.5	ns	Mailbox Interrupt Flag Set Time
tSW	2.3	-	-	ns	Read/Write Enable Setup Time

4.9 Verilog Instantiation Example

Following is an example of instantiating this model within Verilog for the VCS simulator. In this example, a subset of the model's simulation attributes (Verilog parameters) are shown set to their default value. For a complete list of supported simulation attributes, see the table in section 4.6.

```
cy7c04314bv_mx_bus example_inst
  (
    .ap1     ( ap1     ),
    .ap2     ( ap2     ),
    .ap3     ( ap3     ),
    .ap4     ( ap4     ),
    .bep1_n  ( bep1_n  ),
    .bep2_n  ( bep2_n  ),
    .bep3_n  ( bep3_n  ),
    .bep4_n  ( bep4_n  ),
    .ce0p1_n ( ce0p1_n ),
    .ce0p2_n ( ce0p2_n ),
    .ce0p3_n ( ce0p3_n ),
    .ce0p4_n ( ce0p4_n ),
    .ce1p1   ( ce1p1   ),
    .ce1p2   ( ce1p2   ),
    .ce1p3   ( ce1p3   ),
    .ce1p4   ( ce1p4   ),
    .clkp1   ( clkp1   ),
    .clkp2   ( clkp2   ),
    .clkp3   ( clkp3   ),
    .clkp4   ( clkp4   ),
    .intp1_n ( intp1_n ),
    .intp2_n ( intp2_n ),
    .intp3_n ( intp3_n ),
    .intp4_n ( intp4_n ),
    .iop1    ( iop1    ),
    .iop2    ( iop2    ),
    .iop3    ( iop3    ),
    .iop4    ( iop4    ),
    .mrst_n  ( mrst_n  ),
    .oep1_n  ( oep1_n  ),
    .oep2_n  ( oep2_n  ),
    .oep3_n  ( oep3_n  ),
    .oep4_n  ( oep4_n  ),
    .r_w_np1 ( r_w_np1 ),
    .r_w_np2 ( r_w_np2 ),
    .r_w_np3 ( r_w_np3 ),
```

```
    .r_w_np4 ( r_w_np4 )
  );
defparam example_inst.DelayRange    = "Max";
defparam example_inst.MemoryFile    = ".";
defparam example_inst.MessageLevel  = "15";
defparam example_inst.ModelAlias    = ".";
defparam example_inst.ModelId       = "-2";
defparam example_inst.TimingVersion = "133";
```

4.10 VHDL Instantiation Example

Following is an example of instantiating this model within VHDL for the Scirocco simulator. In this example, a subset of the model's simulation attributes (VHDL generics) are shown set to their default value. For a complete list of supported simulation attributes, see the table in section 4.6.

```
example_inst : cy7c04314bv_mx
    generic map (
        DelayRange    => "Max",
        MemoryFile    => ".",
        MessageLevel  => "15",
        ModelAlias    => ".",
        ModelId       => "-2",
        TimingVersion => "133"
    )
    port map (
        ap1     => ap1,
        ap2     => ap2,
        ap3     => ap3,
        ap4     => ap4,
        bep1_n  => bep1_n,
        bep2_n  => bep2_n,
        bep3_n  => bep3_n,
        bep4_n  => bep4_n,
        ce0p1_n => ce0p1_n,
        ce0p2_n => ce0p2_n,
        ce0p3_n => ce0p3_n,
        ce0p4_n => ce0p4_n,
        ce1p1   => ce1p1,
        ce1p2   => ce1p2,
        ce1p3   => ce1p3,
        ce1p4   => ce1p4,
        clkp1   => clkp1,
        clkp2   => clkp2,
        clkp3   => clkp3,
        clkp4   => clkp4,
        intp1_n => intp1_n,
        intp2_n => intp2_n,
        intp3_n => intp3_n,
        intp4_n => intp4_n,
        iop1    => iop1,
        iop2    => iop2,
        iop3    => iop3,
        iop4    => iop4,
```

```
        mrst_n  => mrst_n,
        oep1_n  => oep1_n,
        oep2_n  => oep2_n,
        oep3_n  => oep3_n,
        oep4_n  => oep4_n,
        r_w_np1 => r_w_np1,
        r_w_np2 => r_w_np2,
        r_w_np3 => r_w_np3,
        r_w_np4 => r_w_np4
    );
```

5 cy7c04314bv_mx Model History

Synopsys publishes model history and bug fixes on the *IP Directory for the cy7c04314bv_mx* . The behavior of DesignWare Memory Models may also be affected by revisions made to supporting utilities. For information concerning potential utility changes, please refer to *DesignWare Memory Model Release Notes* .