1 cy7c007a_mx

- MDL Version: **01007**
- Title: **32K x 8 Dual-Port Static RAM**
- Date: **17-Feb-2004**
- Memory Type: **mpsram**
- Vendor: **Cypress Semiconductor Corporation**

2 Timing Selection

This model can be configured to run in either timing-accurate or function-only (no timing) mode. In timing-accurate mode, the model implements both propagational delays and timing checks. In function-only mode, the model propagates output changes immediately and timing checks are disabled.

2.1 Function-only Mode Selection

To run in function-only mode, set the model's TimingVersion attribute to "none".

2.2 Timing-accurate Timing Version Selection

To run in timing-accurate mode, the model's TimingVersion attribute is set to select the device specific timing associated with a vendor's component. The following table provides a mapping between vendor component names and the corresponding TimingVersion attribute values.

Component to TimingVersion Mapping	
Component Name	TimingVersion
CY7C007A-12	12
CY7C007A-15	15
CY7C007A-20	20

Note: By default, this model uses TimingVersion "12".

3 Sources

The following sources were used as references for behavioral and timing characteristics in the development of this model.

1. Cypress Semiconductor Corporation “January 10, 2001”

4 Usage Notes

4.1 Configuring The Model

For information about configuring DesignWare Memory Models for use in simulation, refer to the installed version of the *Simulator Configuration Guide for Synopsys Models*. Or, for the most up-to-date version of this manual, see the *Simulator Configuration Guide for Synopsys Models* on the Synopsys external Web.

4.2 Using DesignWare Memory Models

For general information about using DesignWare Memory Models, refer to the installed version of the *DesignWare Memory Model User’s Manual*. Or, for the most up-to-date version of this manual, see the *DesignWare Memory Model User’s Manual* on the Synopsys external Web.

4.3 Using DesignWare MPSRAM Models

The DesignWare Memory Model documentation set also contains additional usage information that applies to all MPSRAM DesignWare Memory Models. For more information refer to the installed version of the *MPSRAM DesignWare Memory Model Reference*. Or, for the most up-to-date version of this manual, see the *MPSRAM DesignWare Memory Model Reference* on the Synopsys external Web.

4.4 Model Usage Notes

None

4.5 Model Port Description

The following table describes the pin interface for this model.

Model Port Description		
Port Name	Direction	Description
al[14:0]	in	Address Bus (Port 1)
ar[14:0]	in	Address Bus (Port 2)
busyl_n	inout	Busy Pin (Port 1)
busyr_n	inout	Busy Pin (Port 2)
cel_n	in	Chip Enable 1 (Port 1)
cer_n	in	Chip Enable 1 (Port 2)
intl_n	out	Interrupt Pin (Port 1)
intr_n	out	Interrupt Pin (Port 2)
iol[7:0]	inout	IO Data Bus (Port 1)
ior[7:0]	inout	IO Data Bus (Port 2)
m_s_n	in	Master or Slave Select
oel_n	in	Output Enable (Port 1)
oer_n	in	Output Enable (Port 2)
r_w_nl	in	Read/Write Enable (Port 1)
r_w_nr	in	Read/Write Enable (Port 2)
seml_n	in	Semaphore Pin (Port 1)
semr_n	in	Semaphore Pin (Port 2)

4.6 Default Attribute Setting

The following table describes the default attribute settings for this model.

Default Attribute Setting	
Model Attribute	Default Value
DefaultData	11111111
DelayRange	Max
MemoryFile	.
MessageLevel	15
ModelAlias	.
ModelConfig	32’h0
ModelId	-2
TimingVersion	12

4.7 Timing Data for TimingVersion 12

The following table provides a listing of the timing data values modeled when the model’s TimingVersion is set to "12".

Timing Data for TimingVersion 12					
Parameter	Min	Typ	Max	Unit	Description
tAA	12.0	12.0	12.0	ns	Address to Output Data Valid
tACE	12.0	12.0	12.0	ns	Chip Enable Asserted to Output Data Valid
tAW	10.0	-	-	ns	Address Setup to Write End
tBDD	12.0	12.0	12.0	ns	Busy Disable to Valid Data
tBHA	12.0	12.0	12.0	ns	Busy Disable Time from Address Not Matched
tBHC	12.0	12.0	12.0	ns	Busy Disable Time from Chip Enable Deasserted
tBLA	12.0	12.0	12.0	ns	Busy Access Time from Address Match
tBLC	12.0	12.0	12.0	ns	Busy Access Time from Chip Enable Asserted
tDDD	20.0	20.0	20.0	ns	Write Data Valid to Read Data Delay
tDOE	8.0	8.0	8.0	ns	Output Enable Asserted to Output Data Valid
tHA	0.0	-	-	ns	Address Hold from Write End
tHD	0.0	-	-	ns	Data Hold from Write End
tHZCE	10.0	10.0	10.0	ns	Chip Enable Deasserted to Output Data High Z
tHZOE	10.0	10.0	10.0	ns	Output Enable Deasserted to Output Data High Z
tHZWE	10.0	10.0	10.0	ns	Read/Write Enable Asserted to Output Data High Z
tINR	12.0	12.0	12.0	ns	Interrupt Reset Time
tINS	12.0	12.0	12.0	ns	Interrupt Set Time
tLZCE	3.0	-	-	ns	Chip Enable Asserted to Output Data Low Z
tLZOE	3.0	-	-	ns	Output Enable Asserted to Output Data Low Z
tLZWE	3.0	-	-	ns	Read/Write Enable Deasserted to Output Data Low Z
tOHA	3.0	-	-	ns	Output Data Invalid from Address Change
tPS	5.0	-	-	ns	Arbitration Priority Setup Time
tPWE	10.0	-	-	ns	Write Pulse Width
tRC	12.0	-	-	ns	Read cycle time
tSA	0.0	-	-	ns	Address Setup to Write Start
tSAA	12.0	12.0	12.0	ns	Semaphore Address Access Time
tSCE	10.0	-	-	ns	Chip Enable Asserted to Write End
tSD	10.0	-	-	ns	Data Setup to Write End
tSOP	10.0	-	-	ns	Sem Flag Update Pulse(Output Enable or Semaphore)
tSPS	5.0	-	-	ns	Sem Flag Contention Window
tSWRD	5.0	-	-	ns	Sem Flag Write to Read Time
tWB	0.0	-	-	ns	Busy Input to Write
tWC	12.0	-	-	ns	Write cycle time
tWDD	25.0	25.0	25.0	ns	Write Pulse to Data Delay

Timing Data for TimingVersion 12					
tWH	11.0	-	-	ns	Write Hold After Busy

4.8 Timing Data for TimingVersion 15

The following table provides a listing of the timing data values modeled when the model's TimingVersion is set to "15".

Timing Data for TimingVersion 15					
Parameter	Min	Typ	Max	Unit	Description
tAA	15.0	15.0	15.0	ns	Address to Output Data Valid
tACE	15.0	15.0	15.0	ns	Chip Enable Asserted to Output Data Valid
tAW	12.0	-	-	ns	Address Setup to Write End
tBDD	15.0	15.0	15.0	ns	Busy Disable to Valid Data
tBHA	15.0	15.0	15.0	ns	Busy Disable Time from Address Not Matched
tBHC	15.0	15.0	15.0	ns	Busy Disable Time from Chip Enable Deasserted
tBLA	15.0	15.0	15.0	ns	Busy Access Time from Address Match
tBLC	15.0	15.0	15.0	ns	Busy Access Time from Chip Enable Asserted
tDDD	25.0	25.0	25.0	ns	Write Data Valid to Read Data Delay
tDOE	10.0	10.0	10.0	ns	Output Enable Asserted to Output Data Valid
tHA	0.0	-	-	ns	Address Hold from Write End
tHD	0.0	-	-	ns	Data Hold from Write End
tHZCE	10.0	10.0	10.0	ns	Chip Enable Deasserted to Output Data High Z
tHZOE	10.0	10.0	10.0	ns	Output Enable Deasserted to Output Data High Z
tHZWE	10.0	10.0	10.0	ns	Read/Write Enable Asserted to Output Data High Z
tINR	15.0	15.0	15.0	ns	Interrupt Reset Time
tINS	15.0	15.0	15.0	ns	Interrupt Set Time
tLZCE	3.0	-	-	ns	Chip Enable Asserted to Output Data Low Z
tLZOE	3.0	-	-	ns	Output Enable Asserted to Output Data Low Z
tLZWE	3.0	-	-	ns	Read/Write Enable Deasserted to Output Data Low Z
tOHA	3.0	-	-	ns	Output Data Invalid from Address Change
tPS	5.0	-	-	ns	Arbitration Priority Setup Time
tPWE	12.0	-	-	ns	Write Pulse Width
tRC	15.0	-	-	ns	Read cycle time
tSA	0.0	-	-	ns	Address Setup to Write Start
tSAA	15.0	15.0	15.0	ns	Semaphore Address Access Time
tSCE	12.0	-	-	ns	Chip Enable Asserted to Write End

Timing Data for TimingVersion 15					
tSD	10.0	-	-	ns	Data Setup to Write End
tSOP	10.0	-	-	ns	Sem Flag Update Pulse(Output Enable or Semaphore)
tSPS	5.0	-	-	ns	Sem Flag Contention Window
tSWRD	5.0	-	-	ns	Sem Flag Write to Read Time
tWB	0.0	-	-	ns	Busy Input to Write
tWC	15.0	-	-	ns	Write cycle time
tWDD	30.0	30.0	30.0	ns	Write Pulse to Data Delay
tWH	13.0	-	-	ns	Write Hold After Busy

4.9 Timing Data for TimingVersion 20

The following table provides a listing of the timing data values modeled when the model's TimingVersion is set to "20".

Timing Data for TimingVersion 20					
Parameter	Min	Typ	Max	Unit	Description
tAA	20.0	20.0	20.0	ns	Address to Output Data Valid
tACE	20.0	20.0	20.0	ns	Chip Enable Asserted to Output Data Valid
tAW	15.0	-	-	ns	Address Setup to Write End
tBDD	20.0	20.0	20.0	ns	Busy Disable to Valid Data
tBHA	20.0	20.0	20.0	ns	Busy Disable Time from Address Not Matched
tBHC	17.0	17.0	17.0	ns	Busy Disable Time from Chip Enable Deasserted
tBLA	20.0	20.0	20.0	ns	Busy Access Time from Address Match
tBLC	20.0	20.0	20.0	ns	Busy Access Time from Chip Enable Asserted
tDDD	30.0	30.0	30.0	ns	Write Data Valid to Read Data Delay
tDOE	12.0	12.0	12.0	ns	Output Enable Asserted to Output Data Valid
tHA	0.0	-	-	ns	Address Hold from Write End
tHD	0.0	-	-	ns	Data Hold from Write End
tHZCE	12.0	12.0	12.0	ns	Chip Enable Deasserted to Output Data High Z
tHZOE	12.0	12.0	12.0	ns	Output Enable Deasserted to Output Data High Z
tHZWE	12.0	12.0	12.0	ns	Read/Write Enable Asserted to Output Data High Z
tINR	20.0	20.0	20.0	ns	Interrupt Reset Time
tINS	20.0	20.0	20.0	ns	Interrupt Set Time
tLZCE	3.0	-	-	ns	Chip Enable Asserted to Output Data Low Z
tLZOE	3.0	-	-	ns	Output Enable Asserted to Output Data Low Z
tLZWE	3.0	-	-	ns	Read/Write Enable Deasserted to Output Data

Timing Data for TimingVersion 20					
					Low Z
tOHA	3.0	-	-	ns	Output Data Invalid from Address Change
tPS	5.0	-	-	ns	Arbitration Priority Setup Time
tPWE	15.0	-	-	ns	Write Pulse Width
tRC	20.0	-	-	ns	Read cycle time
tSA	0.0	-	-	ns	Address Setup to Write Start
tSAA	20.0	20.0	20.0	ns	Semaphore Address Access Time
tSCE	15.0	-	-	ns	Chip Enable Asserted to Write End
tSD	15.0	-	-	ns	Data Setup to Write End
tSOP	10.0	-	-	ns	Sem Flag Update Pulse(Output Enable or Semaphore)
tSPS	5.0	-	-	ns	Sem Flag Contention Window
tSWRD	5.0	-	-	ns	Sem Flag Write to Read Time
tWB	0.0	-	-	ns	Busy Input to Write
tWC	20.0	-	-	ns	Write cycle time
tWDD	45.0	45.0	45.0	ns	Write Pulse to Data Delay
tWH	15.0	-	-	ns	Write Hold After Busy

4.10 Verilog Instantiation Example

Following is an example of instantiating this model within Verilog for the VCS simulator. In this example, a subset of the model's simulation attributes (Verilog parameters) are shown set to their default value. For a complete list of supported simulation attributes, see the table in section 4.6.

```
cy7c007a_mx_bus example_inst
  (
    .al      ( al      ),
    .ar      ( ar      ),
    .busyl_n ( busyl_n ),
    .busyr_n ( busyr_n ),
    .cel_n   ( cel_n   ),
    .cer_n   ( cer_n   ),
    .intl_n  ( intl_n  ),
    .intr_n  ( intr_n  ),
    .iol     ( iol     ),
    .ior     ( ior     ),
    .m_s_n   ( m_s_n   ),
    .oel_n   ( oel_n   ),
    .oer_n   ( oer_n   ),
    .r_w_nl  ( r_w_nl  ),
    .r_w_nr  ( r_w_nr  ),
    .seml_n  ( seml_n  ),
    .semr_n  ( semr_n  )
  );
defparam example_inst.DelayRange    = "Max";
defparam example_inst.MemoryFile    = ".";
defparam example_inst.MessageLevel  = "15";
defparam example_inst.ModelAlias    = ".";
defparam example_inst.ModelId       = "-2";
defparam example_inst.TimingVersion = "12";
```

4.11 VHDL Instantiation Example

Following is an example of instantiating this model within VHDL for the Scirocco simulator. In this example, a subset of the model's simulation attributes (VHDL generics) are shown set to their default value. For a complete list of supported simulation attributes, see the table in section 4.6.

```
example_inst : cy7c007a_mx
    generic map (
        DelayRange    => "Max",
        MemoryFile    => ".",
        MessageLevel  => "15",
        ModelAlias    => ".",
        ModelId       => "-2",
        TimingVersion => "12"
    )
    port map (
        al      => al,
        ar      => ar,
        busyl_n => busyl_n,
        busyr_n => busyr_n,
        cel_n   => cel_n,
        cer_n   => cer_n,
        intl_n  => intl_n,
        intr_n  => intr_n,
        iol     => iol,
        ior     => ior,
        m_s_n   => m_s_n,
        oel_n   => oel_n,
        oer_n   => oer_n,
        r_w_nl  => r_w_nl,
        r_w_nr  => r_w_nr,
        seml_n  => seml_n,
        semr_n  => semr_n
    );
```

5 cy7c007a_mx Model History

Synopsys publishes model history and bug fixes on the *IP Directory for the cy7c007a_mx* . The behavior of DesignWare Memory Models may also be affected by revisions made to supporting utilities. For information concerning potential utility changes, please refer to *DesignWare Memory Model Release Notes* .