Design Analyzer™
Reference Manual

Version 2002.05, June 2002

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About this Manual

Synopsys Design Analyzer is a graphic interface for the Synopsys logic synthesis tools. This Design Analyzer Reference Manual describes how to use the Design Analyzer tool.

You must purchase some of the described features (such as netlist formats) as separate options.

This preface includes the following sections:

Audience

This manual is for beginning users of Design Analyzer. Both beginning and advanced users might choose to use the tool for a graphical representation of their design. The primary readers of this manual

- Have at least a basic knowledge of Synopsys Design Compiler
- Work as a logic designer or an electronics engineer
- Know the UNIX operating system
- Understand computer–aided engineering (CAE) tools

Related Publications

For additional information about Design Analyzer, see

- Synopsys Online Documentation (SOLD), which is included with the software for CD users or is available to download through the Synopsys Electronic Transfer (EST) system
- Documentation on the Web, which is available through SolvNet at http://solvnet.synopsys.com
- The Synopsys MediaDocs Shop, from which you can order printed copies of Synopsys documents, at http://mediadocs.synopsys.com

You might also want to refer to the documentation for the Synopsys Design Compiler tool.

Customer Support

Customer support is available through SolvNet online customer support and through contacting the Synopsys Technical Support Center.

Accessing SolvNet

SolvNet includes an electronic knowledge base of technical articles and answers to frequently asked questions about Synopsys tools. SolvNet also gives you access to a wide range of Synopsys online services including software downloads, documentation on the Web, and “Enter a Call With the Support Center.”

To access SolvNet,

1. Go to the SolvNet Web page at http://solvnet.synopsys.com.
2. If prompted, enter your user name and password. (If you do not have a Synopsys user name and password, click New Synopsys User Registration.)

If you need help using SolvNet, click SolvNet Help in the column on the left side of the SolvNet Web page.

Contacting the Synopsys Technical Support Center

If you have problems, questions, or suggestions, you can contact the Synopsys Technical Support Center in the following ways:

- Open a call to your local support center from the Web by going to http://solvnet.synopsys.com (Synopsys user name and password required), then clicking “Enter a Call With the Support Center.”
- Send an e-mail message to support_center@synopsys.com.
- Telephone your local support center.
  - Call (800) 245-8005 from within the continental United States.
  - Call (650) 584-4200 from Canada.
  - Find other local support center telephone numbers at http://www.synopsys.com/support/support_ctr.

Conventions

The following conventions are used in Synopsys documentation.

Convention	Description
`Courier`	Indicates command syntax. In command syntax and examples, shows system prompts, text from files, error messages, and reports printed by the system.
italic	Indicates a user specification, such as *`object_name`*
bold	In interactive dialogs, indicates user input (text you type).
[ ]	Denotes optional parameters, such as *`pin1`* [*`pin2 ... pinN`*]
|	Indicates a choice among alternatives, such as `low | medium | high` (This example indicates that you can enter one of three possible values for an option: low, medium, or high.)
_	Connects terms that are read as a single term by the system, such as `set_annotated_delay`
Control-c	Indicates a keyboard combination, such as holding down the Control key and pressing c.
\	Indicates a continuation of a command line.
/	Indicates levels of directory structure.
Edit > Copy	Indicates a path to a menu command, such as opening the Edit menu and choosing Copy.

About this Manual

xxx

1

Design Analyzer Overview

If you are familiar with the Design Analyzer interface, skip this chapter. Design Analyzer is the graphical interface for several Synopsys synthesis tools, including

- Behavioral Compiler
- BSD Compiler
- DC Expert
- DC Professional
- DC Ultra
- DesignPower
- DesignTime
- DesignWare Developer

- DFT Compiler
- FloorPlan Manager
- HDL Compiler
- Library Compiler
- Power Compiler
- VHDL Compiler

When using Design Analyzer, you work with a mouse and pointer to select objects. Although Design Analyzer does provide the Setup/ Command Window menu selection, which offers a command-line interface, there is also a command-line interface, called dc_shell, in which you enter UNIX commands, arguments, and options. This command-line interface is described in the *Design Compiler Command-Line Interface Guide*.

This chapter provides an overview of the Design Analyzer graphic interface concepts:

- Features
- Design Analyzer Windows
- Terms

Some features, such as showing the Verilog and VHDL design input formats or creating circuit test structures, are enabled only if you have purchased the corresponding tool or license.

Features

Design Analyzer allows you to select an object (such as a design), then to select an action. You can select objects and actions graphically or by name. Design Analyzer allows you to do the following actions:

- Set system variable values such as the technology library name.
- Read and write designs in multiple formats such as EDIF, netlist, PLA, Verilog, VHDL, and equation.
- Set constraints and attributes graphically on designs, cells, pins, nets, buses, and clocks.
- Work with hierarchical designs.
  - See and move through levels of hierarchy.
  - View designs and subdesigns as black boxes with named ports.
  - Graphically group and ungroup cells and subdesigns.
- Synthesize digital circuits.
  - Set the circuit's wire load model, indicate sequential-logic cells, and define the circuit's expected operating conditions.
  - Synthesize hierarchical circuits, maintaining design and subdesign boundaries while performing global optimizations.
  - Extract finite state machines (FSMs) from sequential logic, define state encodings and ordering, perform FSM-specific optimizations, and synthesize an equivalent sequential circuit.
  - Add test scan-path cells and logic to an existing design, create and format test vectors, and get reports on fault coverage.

- Generate, view, and plot schematics.
- Display timing information for ports, pins, cells, nets, and designs.
- Highlight paths in a schematic.
- Generate a variety of reports.

Design Analyzer Windows

The Design Analyzer graphical user interface (GUI) operates in the X Window System on UNIX.

Figure 1-1 shows the main GUI Design Analyzer window, and Figure 1-2 shows the Design Analyzer Command Window.

Figure 1-1 Synopsys Design Analyzer Window

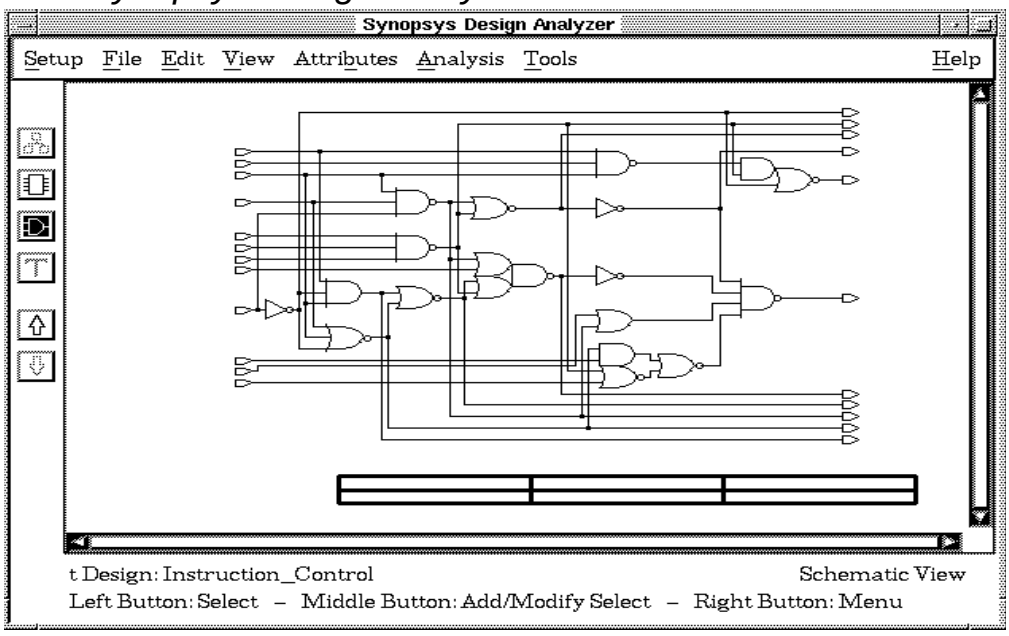
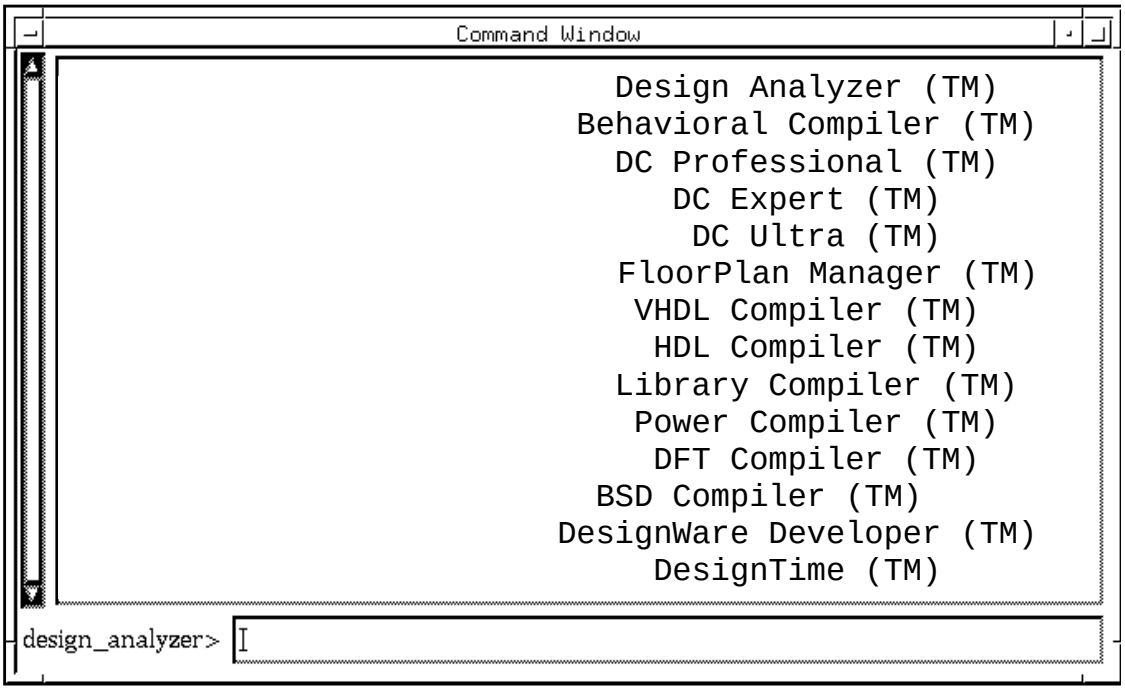


Figure 1-2 Design Analyzer Command Window



To use Design Analyzer

1. Start the X Window System and the window manager on your workstation.
2. Start Design Analyzer.

See Chapter 2, “Using Design Analyzer,” for information on starting the tool. The X Window System is a graphical, window-based environment. Programs running in this environment create and use one or more windows. The window manager controls the appearance of all windows on your screen.

The X Window System uses a client-server model.

client

A terminal that receives shared service from a server. Client programs that run under the X Window System can run on a variety of computers, including HP, Sun, and others. A client can communicate with multiple servers.

server

The terminal that provides shared services to workstations over a network. A server can communicate with multiple clients.

Terms

The following section describes graphic elements in Design Analyzer, which allow you to set selections and display information about the design and the tool.

Dialog Box

A dialog box displays information or solicits data. Use a dialog box to see and change values through a variety of the following controls.

Text box

A text box can contain a number, a name, or an arbitrary string of characters. Most text can be edited, although some text is read-only.

Push buttons

A push button is a named box where you click to designate, confirm, or cancel an option. Some push buttons bring up nested dialog boxes; these push buttons have names followed by an ellipsis (...), just like nested menu selections.

Toggle button

A toggle button is enabled or disabled. You can enable more than one toggle button at a time.

Radio button

A radio button appears in a series with other radio buttons that allow only one selection.

Scroll bar

A scroll bar appears when some information (such as a list of file names or a schematic) is larger than the available viewing area. Click the bar to scroll the screen in the corresponding direction.

List box

A list box contains a selection from an existing list of items (often a list of file and directory names). Clicking a selection writes that selection in the associated text box where you can edit it if needed.

Option menu

An option menu contains a set of predetermined choices such as design input formats or object types. You can choose only one of the displayed choices.

Scale

A scale graphically represents a range of values such as color values.

Figure 1-3 shows a dialog box (Edit > Insert Pads) with two groups of radio buttons, two push buttons, and two text boxes.

Figure 1-3 Dialog Box with Buttons, Option Menus, Text Boxes

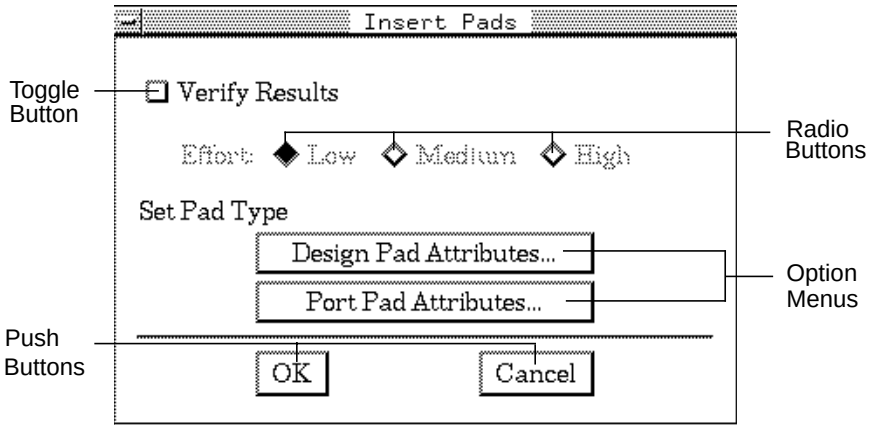
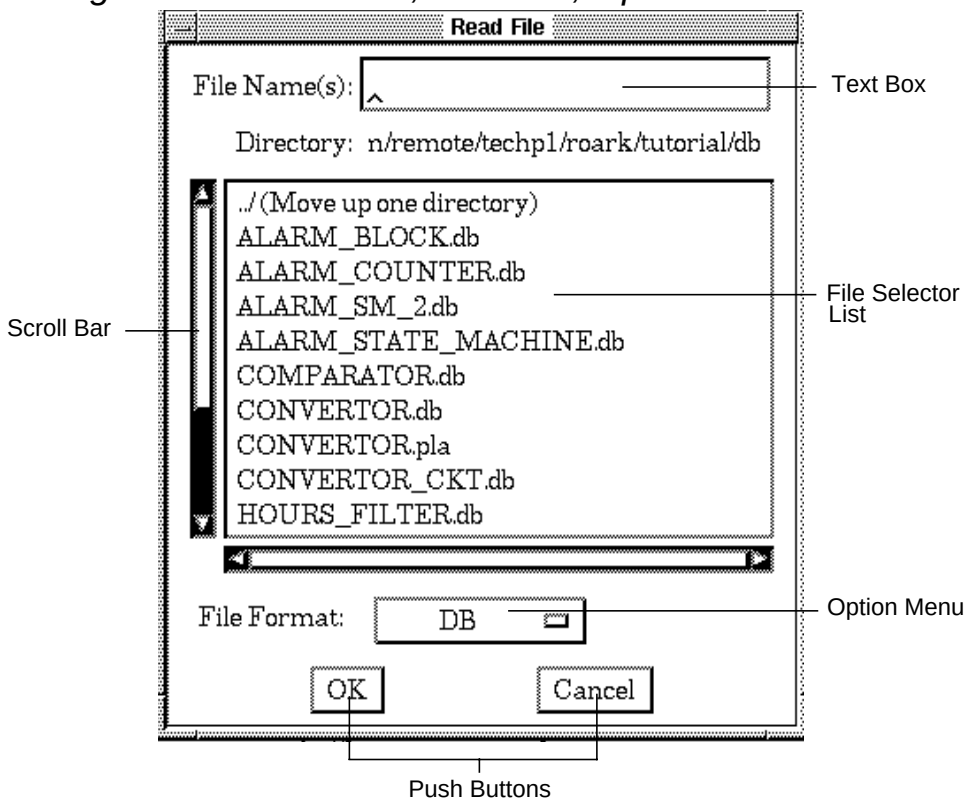


Figure 1-4 shows a dialog box (File > Read) with a file selector list and its associated text box, a scroll bar, two push buttons, and an option menu.

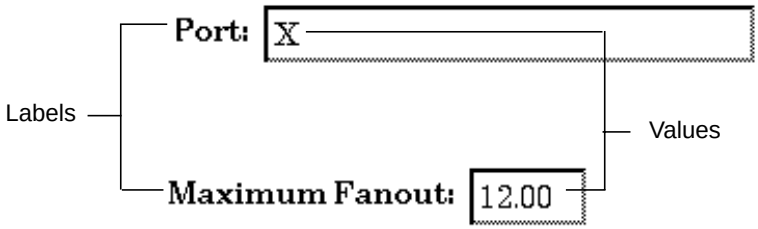
Figure 1-4 Dialog Box: File Selector, Text Box, Option Menu



Text Box

A text box has a label and a value. A text box and an option menu are different. When you click in a text box, a text-editing cursor appears; when you click an option menu, a list of choices appears. Figure 1-5 shows typical text boxes.

Figure 1-5 Text Boxes



The value can be a name, a number, or a string.

Name

The name of an object such as a file name.

Number

A numeric value such as the arrival time of a signal.

String

Any combination of characters such as a logical expression.

Most text boxes can be edited; however, some are display-only. If you click display-only text, the text blinks.

To enter a value, click the left mouse button in the field to get a text cursor, then type the value you want.

To edit in text boxes, use the following characters:

Backspace or Delete

Erases the previous character.

Control-u

Clears the text box.

Control-a

Moves the cursor to the beginning of the text box.

Control-e

Moves the cursor to the end of the text box.

Control-b

Moves the cursor back one character.

Control-f

Moves the cursor forward one character.

Control-k

Deletes all characters from the cursor location to the end of the line.

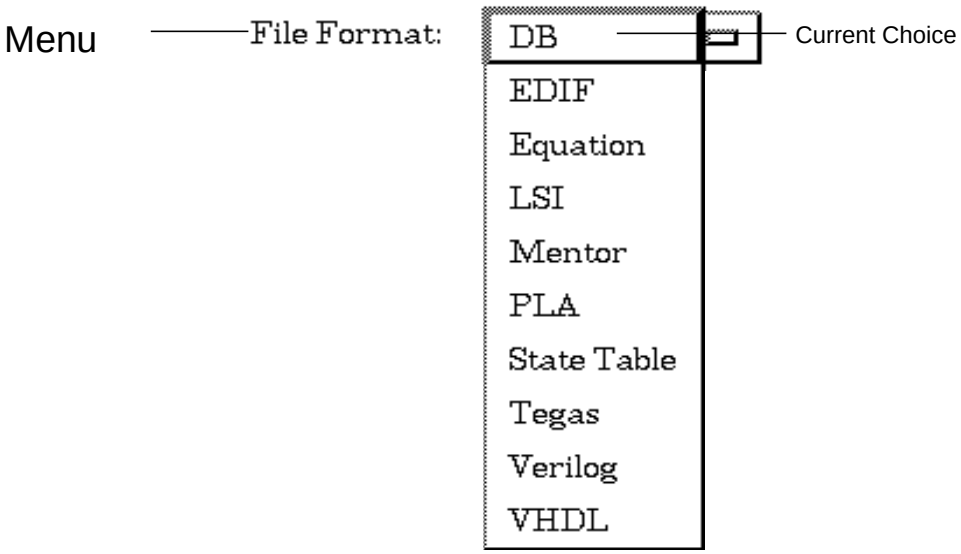
Option Menu

An option menu is a complete set of valid choices. You can select only one choice from the list.

To display an option menu, click the left mouse button in the box. The option menu appears with the current choice boxed.

Figure 1-6 shows an option menu box with the current choice, DB, boxed.

Figure 1-6 Option Menu



To select from the menu,

1. Drag the cursor to the choice you want.
2. Release the mouse button.

To close an option menu without making a choice,

1. Drag the cursor out of the menu area.
2. Release the mouse button.

Button

A button is a graphical control element of a dialog box that activates a choice. To activate an on-screen button, click it with the left mouse button.

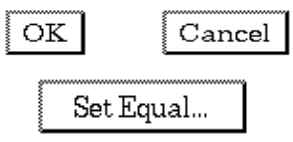
Design Analyzer uses three types of buttons:

- Push buttons
- Toggle buttons
- Radio buttons

Push Button

When you click a push button, an action occurs. Figure 1-7 shows some typical push buttons.

Figure 1-7 Push Buttons



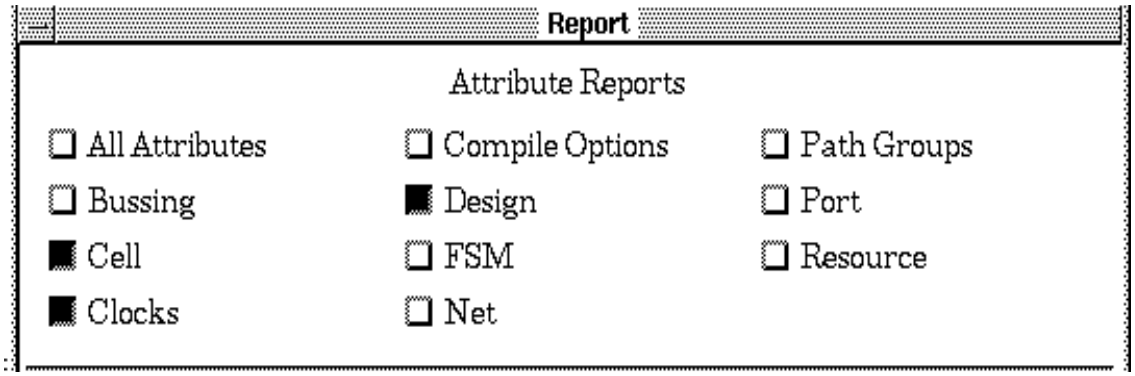
When a push button label contains an ellipsis (...), clicking the button displays another dialog box.

Toggle Button

A toggle button is a small, square box. A toggle button is either enabled (filled in) or disabled (outlined).

Some toggle buttons are arranged in groups corresponding to the selection's command options. You can enable any number of toggle buttons in a group. Figure 1-8 shows the Report dialog box (Analysis > Report). The Net toggle button corresponds to the report_net command. Enabling one of these toggle buttons sets the corresponding command option to true; disabling it sets the command option to false.

Figure 1-8 Toggle Buttons in a Group Box

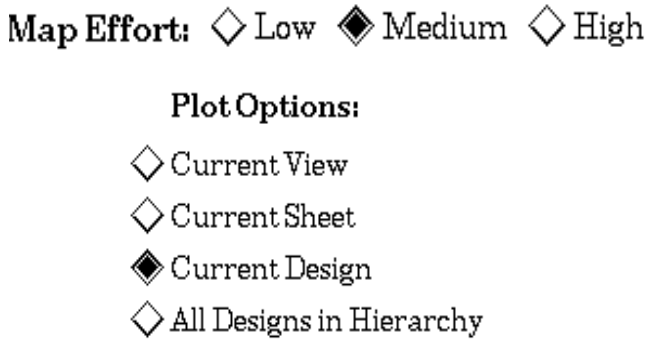


Radio Button

Radio buttons represent mutually exclusive alternatives; you can enable only one radio button in a set. A radio button has a small diamond shape.

Figure 1-9 shows two sets of radio buttons: one horizontal and one vertical.

Figure 1-9 Radio Buttons

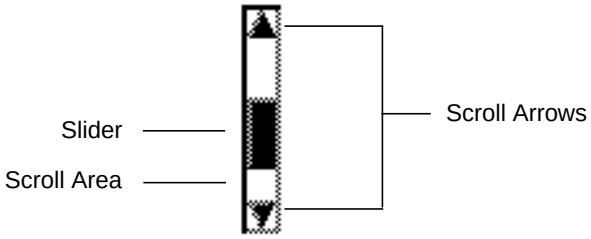


Scroll Bar

Scroll bars are graphical controls you move to see information that is not currently visible. Scroll bars can be horizontal or vertical; some windows have both.

Figure 1-10 shows a scroll bar, which consists of a slider with scroll arrows.

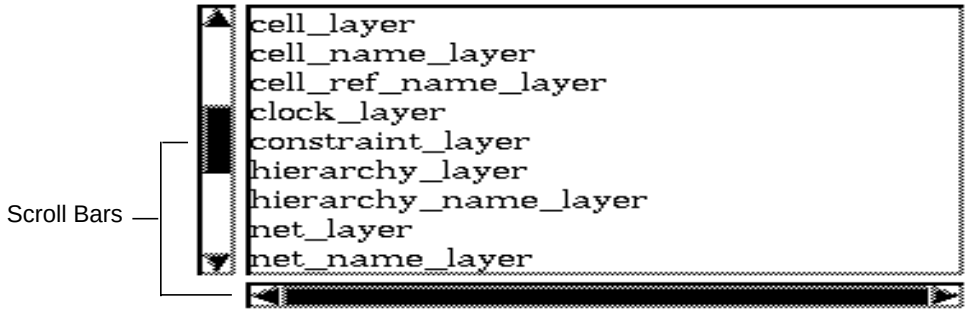
Figure 1-10 Scroll Bar



Scroll bars enable you to move through lists, text, and schematics.

Lists of names or paragraphs of text often have a vertical scroll bar and might have a horizontal scroll bar. Schematics have both vertical and horizontal scroll bars Figure 1-11 shows a list with vertical and horizontal scroll bars.

Figure 1-11 List with Vertical and Horizontal Scroll Bars



The vertical scroll bar is in the middle of its scroll area, indicating there are more items above and below the current view. The horizontal scroll bar is full, indicating the entire horizontal view is visible.

Clicking on a vertical scroll arrow moves the view up or down one line.

You can resize the Design Analyzer windows; changing the size of the viewing area also changes the size of the scroll bar relative to the scroll area.

Scroll bars are especially useful when you are in a close-up view.

You can move a scroll bar in three ways:

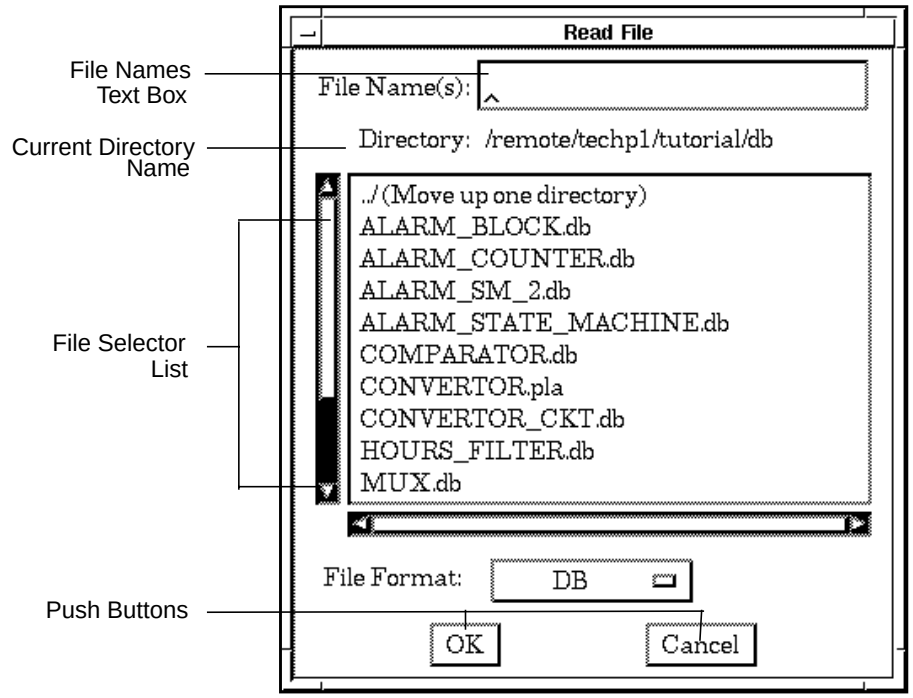
- Drag the slider to move the view to the position you want.
- Click a scroll arrow to move the view up or down one line for text, or about half of the scroll bar's width or height for graphics.
- Click anywhere in the scroll area to scroll the text or schematic about one window's length or width in the indicated direction.

File Selector

To select one or more file names, use a file selector. Type file names in the text box or select them from the directory list.

A file selector has a text box, a current directory name, a file selector list, and the standard push buttons: OK and Cancel. Initially, the File Name(s) text box is blank, and the file selector list shows the contents of the current directory. Figure 1-12 shows a file selector.

Figure 1-12 File Selector



To leave the dialog box without making a selection, click Cancel.

To enter one or more file names directly, use relative or absolute path names,

1. Type the names in the File Name(s) text box, separated by spaces.

2. Press Return or click OK.

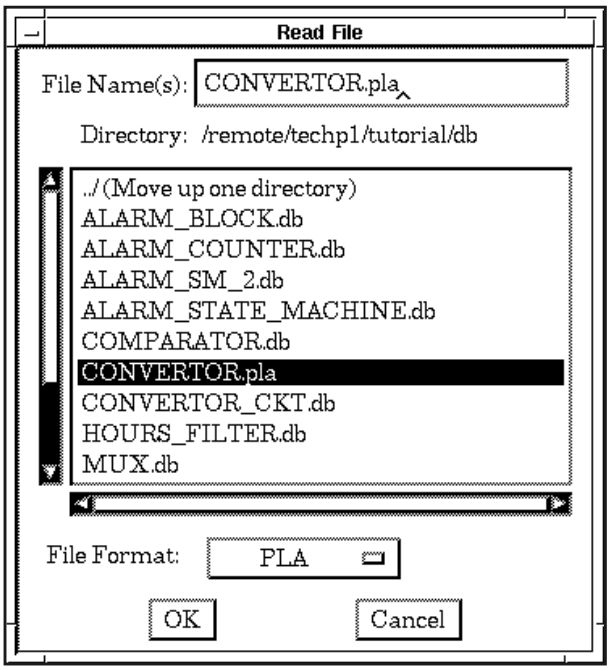
When you enter a directory name in the File Name(s) box, the Directory field automatically updates. You cannot directly edit the Directory field; it is a display-only field.

To graphically select a file,

1. Click the name you want with the left mouse button.
2. Click OK to accept the file name displayed in the File Name(s) text box.

The name becomes highlighted and it appears in the File Name(s) text box. Figure 1-13 shows that Convertor.pla is selected.

Figure 1-13 Select One File Name



The size of the scroll bar is directly proportional to the displayed portion of the file list. If the scroll bar does not fill the entire scroll area (as in Figure 1-13), additional file names exist that do not appear in the display area. Drag the scroll bar with the left mouse button to bring the other file names into view.

SHORTCUT

Double-click a file name to select and accept it.

To add another file name to the File Name(s) text box, click the name with the middle mouse button. When reading in more than one file name, make sure they have the same file format.

Click OK to accept the displayed file names.

Move to a different directory either by typing the directory name you want in the File Name(s) text box or by graphically moving through the directory hierarchy.

To move to any directory directly,

1. Enter its path name in the File Name(s) text box.
2. Press Return or click OK.

To move to a displayed directory,

1. Click its name.
2. Click OK.

All displayed directory names end in a slash (/). The parent directory name (../) always appears at the top of the list. Access it by double-clicking ../ (Move up one directory).

When you select a directory name, the name automatically appears in the File Name(s) text box. To go to the selected directory, press Return or click OK.

SHORTCUT

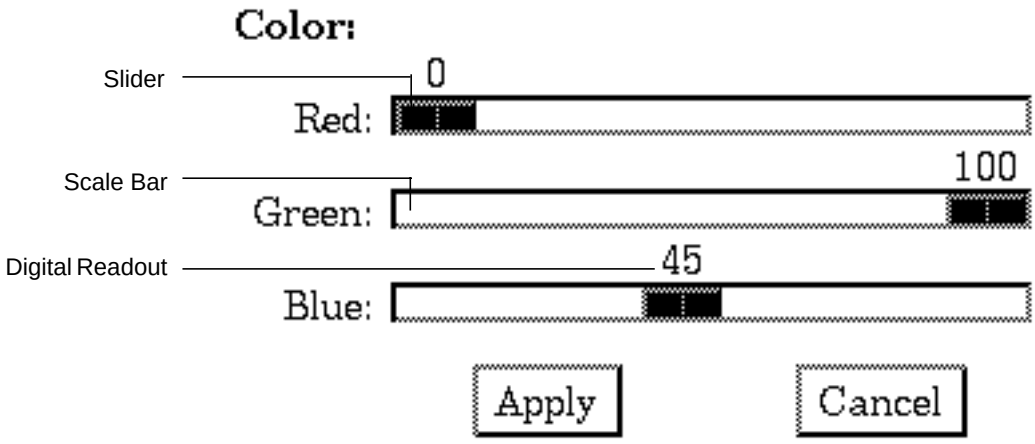
Double-click a directory name to select and go to it.

When you enter a directory name in the File Name(s) text box, the Directory field is automatically updated and the new directory's contents appear in the file selector list.

Scales

A scale, such as in Figure 1-14, represents a value with a defined numeric range. A scale contains a slider, scale bar, and a digital readout.

Figure 1-14 Scales



As you drag the slider right and left, the value of the digital readout changes according to the position of the slider. The first two scale bars in Figure 1-14 show the associated numeric range (0 to 100). The bottom slider is less than half-way, with a digital value of 45.

Click Apply to use the displayed slider values; click Cancel to remove the window.

Use scales to define the color of schematic layers (View > Style).

2

Using Design Analyzer

This chapter describes the basics of the Design Analyzer tool.

- Introducing the Design Example
- Starting Design Analyzer
- Quitting Design Analyzer
- Using the Design Viewer
- Traversing a Design Hierarchy
- Executing Tasks
- Monitoring Task Progress
- Analyzing the Results
- Using the Command-Line Interface
- Customizing the Design Analyzer Environment

- Describing the Menu Bar

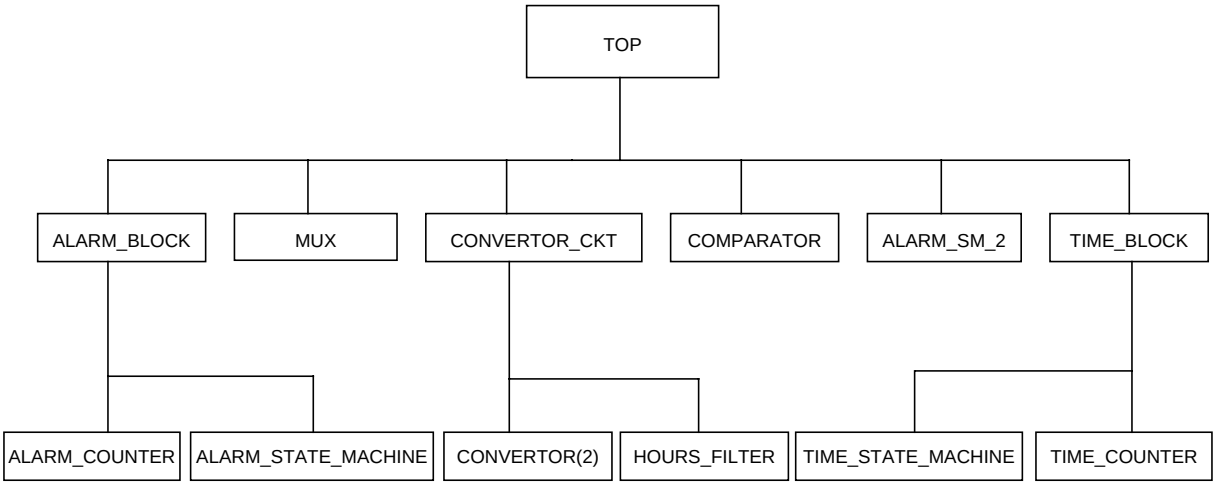
Introducing the Design Example

The example throughout this manual optimizes a simple hierarchical design for a digital display alarm clock. The TOP design contains the six blocks, or subdesigns, of the alarm clock design. These subdesigns are

- ALARM_BLOCK
- MUX
- CONVERTOR_CKT
- COMPARATOR
- ALARM_SM_2
- TIME_BLOCK

Figure 2-1 shows the hierarchy for the alarm clock design.

Figure 2-1 Alarm Clock Design Hierarchy



TOP

TOP is the top-level block of the alarm clock design. TOP contains references to all the subdesigns. Each subdesign performs a separate function of the alarm clock design.

ALARM_BLOCK

ALARM_BLOCK is a two-level hierarchical block. ALARM_BLOCK controls the alarm-setting function of the design.

ALARM_BLOCK has four input signals:

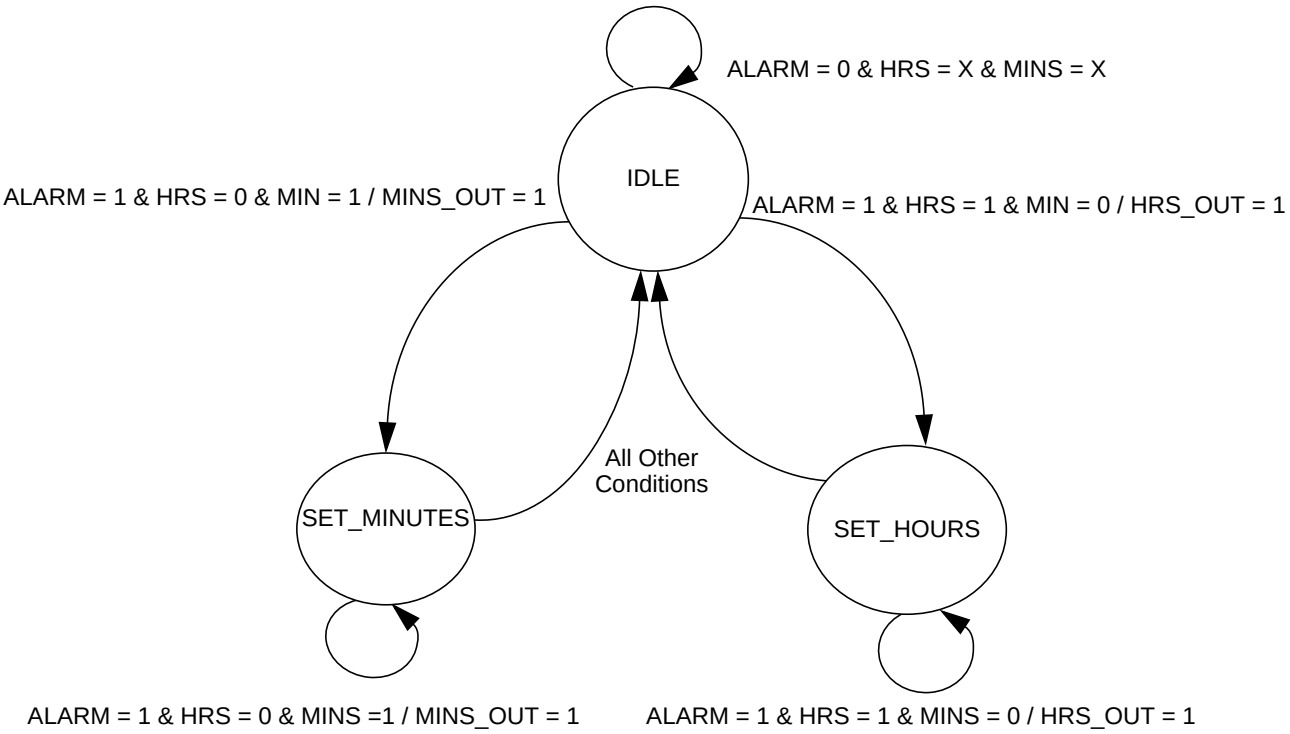
- ALARM is used with HRS or MINS to set alarm time.
- CLK is the system clock.
- HRS is used with ALARM to set alarm hours.
- MINS is used with ALARM to set alarm minutes.

ALARM_BLOCK has two output signals that are hours and minutes of the alarm time. The output signals are input signals to the MUX and COMPARATOR blocks.

ALARM_BLOCK instantiates two subdesigns:

- ALARM_COUNTER increments alarm hours and minutes and reflects AM and PM settings.
- ALARM_STATE_MACHINE sets the alarm time, as shown in Figure 2-2. The ALARM_STATE_MACHINE has three states: SET_MINUTES, IDLE, and SET_HOURS.

Figure 2-2 Alarm State Machine State Diagram



If the block state is IDLE, it waits for a set of input signals that can change the state to SET_MINUTES or SET_HOURS.

When ALARM=1, HRS=0, and MINS=1, the state changes to SET_MINUTES. From this state, a MINS_OUT pulse is fed into the ALARM_COUNTER block, which increments the minutes count. While the block is in the SET_MINUTES state, the minutes continue to increment in ALARM_COUNTER.

The SET_HOURS state functions the same as SET_MINUTES, except SET_HOURS is activated when ALARM=1, HRS=1, and MINS=0. SET_HOURS sends an HRS_OUT pulse to ALARM_COUNTER to increment the hours.

MUX

MUX determines the time setting to display. MUX enables either the time of day or the alarm time to display.

MUX has five main input signals:

- ALARM is used with HRS or MINS to set alarm time.
- ALARM_HRS is alarm hours from ALARM_BLOCK.
- ALARM_MIN is alarm minutes from ALARM_BLOCK.
- TIME_HRS is time-of-day hours from TIME_BLOCK.
- TIME_MIN is time-of-day minutes from TIME_BLOCK.

MUX processes these input signals and feeds the information to CONVERTOR_CKT allowing CONVERTOR_CKT to display the appropriate time. The default display is the time of day. When ALARM=1, the alarm time appears.

MUX also processes and enables the AM and PM settings.

CONVERTOR_CKT

The CONVERTOR_CKT hierarchical block implements a binary-coded-decimal (BCD)-to-seven-segment decoder function. CONVERTOR_CKT converts the alarm time or time-of-day binary representations to signals that determine the alarm clock number display.

CONVERTOR_CKT instantiates two subdesigns:

- CONVERTOR has two instances in the CONVERTOR_CKT design. One CONVERTOR instance converts the binary representation of hours; the other CONVERTOR instance converts minutes. CONVERTOR_CKT prepares the converted information for a seven-segment LED display.
- HOURS_FILTER disables a zero-digit display in the ten-digit column of the hours for time settings under 10:00 and over 12:59. For example, hours are filtered so that the time–of–day display for nine o’clock is 9:00 instead of 09:00.

COMPARATOR

COMPARATOR compares the time of day to the alarm time.

COMPARATOR has four main input signals:

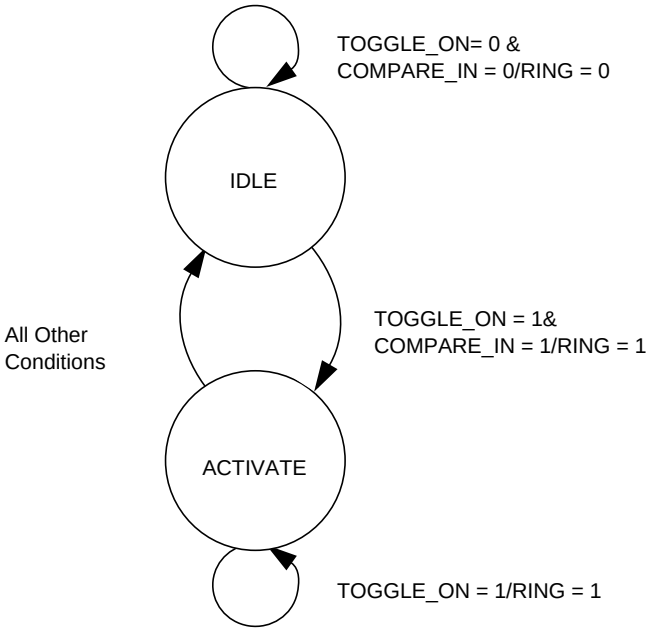
- ALARM_HRS is alarm hours from ALARM_BLOCK.
- ALARM_MIN is alarm minutes from ALARM_BLOCK.
- TIME_HRS is time-of-day hours from TIME_BLOCK.
- TIME_MIN is time-of-day minutes from TIME_BLOCK.

When the alarm, time of day, AM, and PM settings are equal, COMPARATOR sends a signal to the ALARM_SM_2 block.

ALARM_SM_2

ALARM_SM_2 is a state machine that has two states, IDLE and ACTIVATE, as shown in Figure 2-3.

Figure 2-3 Activate Alarm State Diagram



ALARM_SM_2 has three input signals:

- COMPARE_IN is from the COMPARATOR block; it equals 1 when time of day equals alarm time.
- TOGGLE_ON turns the alarm on or off.
- CLOCK is the system clock.

When the alarm time equals the time of day and TOGGLE_ON=1 (or ON), ALARM_SM_2 goes to the ACTIVATE state. From this state, the block sends a signal to RING to enable the alarm to sound. ALARM_SM_2 remains in the ACTIVATE state as long as the TOGGLE_ON is on or until alarm time is reset.

TIME_BLOCK

TIME_BLOCK is similar to ALARM_BLOCK; however, it controls the time-of-day feature of the design. TIME_BLOCK is a two-level hierarchical block. TIME_BLOCK has four input signals:

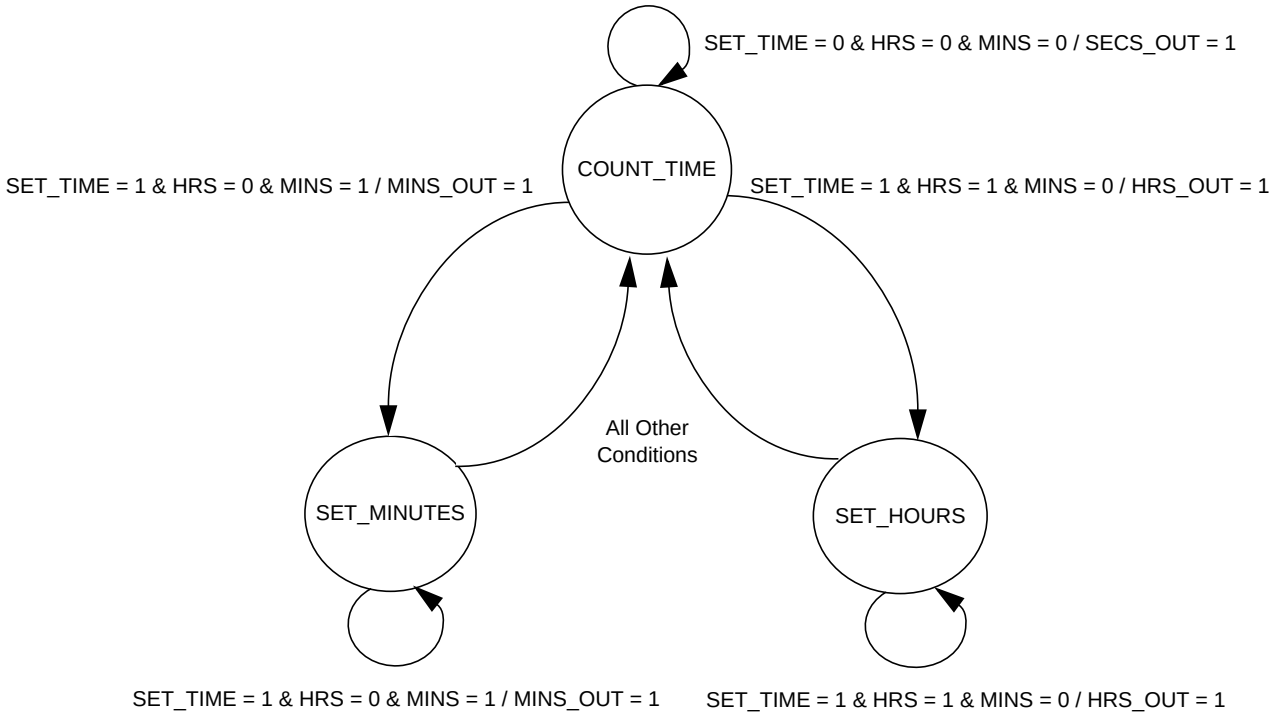
- SET_TIME is used with HRS or MINS to set the time of day.
- CLK is the system clock.
- HRS is used with SET_TIME to set time-of-day hours.
- MINS is used with SET_TIME to set time-of-day minutes.

  Time-of-day hours and minutes are the two TIME_BLOCK output signals. These output signals are input signals to the MUX and COMPARATOR blocks.

TIME_BLOCK instantiates two subdesigns:

- TIME_COUNTER increments hours and minutes for the time of day and reflects AM and PM settings.
- TIME_STATE_MACHINE is used to set and keep the time of day. The state machine has three states, as shown in Figure 2-4.

Figure 2-4 Time State Machine State Diagram



When TIME_STATE_MACHINE is in the COUNT_TIME state, it outputs a pulse every second that updates the time of day. This pulse is fed into the TIME_COUNTER block. The block stays in the COUNT_TIME state until it receives a set of inputs that change the state to SET_MINUTES or SET_HOURS.

When SET_TIME=1, HRS=0, and MINS=1, the state changes to SET_MINUTES. From this state, a MINS_OUT pulse is fed into the TIME_COUNTER block to increment the minutes. As long as the block is in the SET_MINUTES state, the minutes continue to increment in TIME_COUNTER.

The SET_HOURS state functions the same as SET_MINUTES, except the SET_HOURS state is activated when SET_TIME=1, HRS=1, and MINS=0. SET_HOURS sends an HRS_OUT pulse to TIME_COUNTER to increment the hours.

Starting Design Analyzer

You invoke Design Analyzer from a UNIX shell, either directly on your machine or in a shell created on the remote host.

To start Design Analyzer,

1. Start the X Window System and the window manager on your UNIX terminal.
2. Start the Design Analyzer interface.

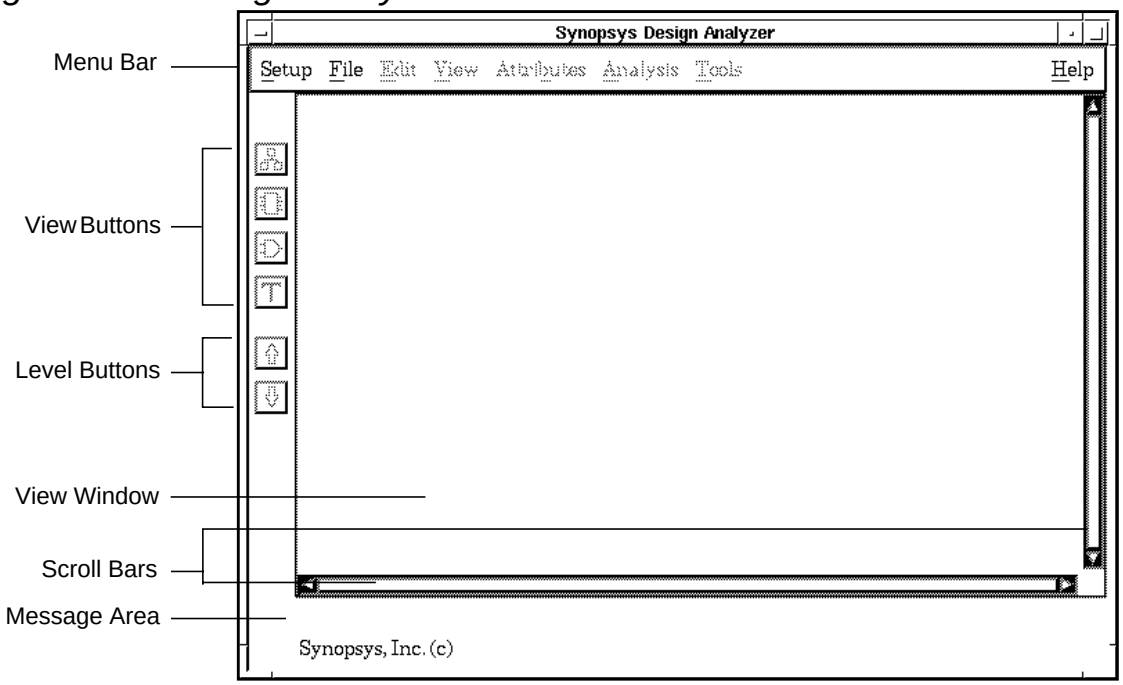
   ```
   % design_analyzer
   ```

*For details on how to install and set up Design Analyzer and its directories, see the *Installation Guide*.

The Design Analyzer window shown in Figure 2-5, appears on your screen. Several parts comprise the top level of Design Analyzer:

- A menu bar with the names of the eight primary menus
- Six buttons on the left side: three view buttons, a Text View button, and two level buttons
- The central view window, including vertical and horizontal scroll bars
- Two message lines at the bottom of the window: the top line tells you what you are viewing and the bottom line is for status messages

Figure 2-5 Design Analyzer Window



The Design Analyzer window has a frame (border) around it provided by the Motif wireless manager (MWM) window manager for the UNIX system. These borders control the size, shape, and location of an MWM window.

Quitting Design Analyzer

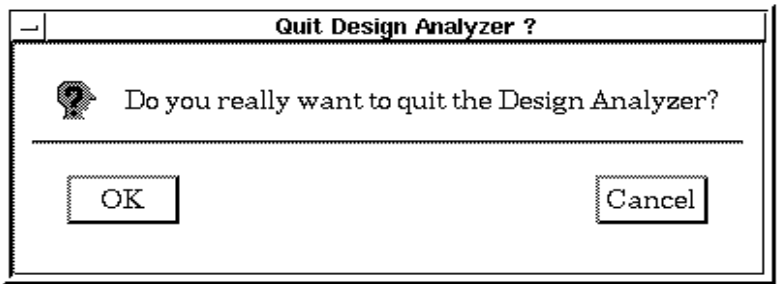
You can quit Design Analyzer at any time.

To quit Design Analyzer,

1. Click the File menu (move the cursor onto the word File in the menu bar, then click the left mouse button).
2. Click Quit.

Figure 2-6 shows the dialog box to confirm you want to quit.

Figure 2-6 Design Analyzer: Quit Dialog Box



SHORTCUT

With the cursor in the Design Analyzer window, type Meta-F Q. The F stands for File menu, and the Q stands for Quit. Move the cursor into the Quit dialog box, and press Return. Return is equivalent to clicking the outlined OK button.

Using the Design Viewer

Design Analyzer uses four different views of designs. The first view shows all designs in memory. The other three views represent different aspects of a design.

Designs View

Shows all designs and subdesigns in memory. A certain type of icon represents each design: HDL, netlist, finite state machine, or PLA. Designs View is the initial view.

From the Designs View, you select a design for exploration or for setting design attributes and constraints.

Hierarchy View

Shows a design as a set of one or more named subdesigns.

The Hierarchy View displays all the subdesigns (cell instances) in one level of a design hierarchy. You can move up and down the levels of hierarchy.

From the Hierarchy View, you can see the relationship between levels of a design and work with the individual subdesigns.

Symbol View

Shows a design as a black box with input and output ports.

From the Symbol View, you can set attributes and constraints for a design and its ports. Attributes specify design-specific information such as the arrival times and strengths of input signals. Constraints are design-specific requirements or goals for the optimizer such as the maximum circuit area or the maximum signal propagation time through the circuit to one or more outputs.

Schematic View

Shows a design as a schematic composed of instances, nets, and ports. An instance in a schematic can be a subdesign.

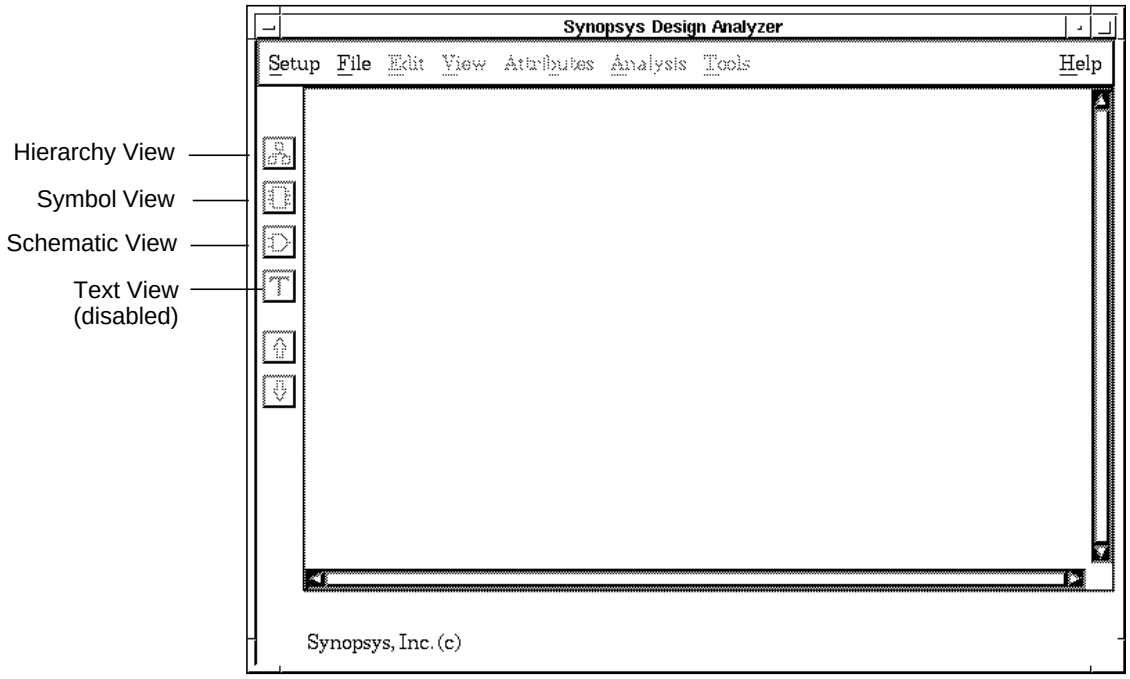
The followings sections describe each of the four views, using the TOP hierarchical design as an example.

Note:

The disabled T button (Text View) is not used in version 3.4 and later.

Symbol, Hierarchy, and Schematic Views show individual designs. You can move among these three views with the view buttons designated in Figure 2-7.

Figure 2-7 Three Views of a Design



The following sections describe each of the four views, using the TOP hierarchical design as an example.

To move among views of a design, you can

- Use the View menu's Change View submenu.
- Click a view button.

SHORTCUT

From the Symbol View, double-click the design. The first click selects the design, and the next click displays the Schematic View.

In a hierarchical design, each subdesign displays in any view. You can move up and down levels of hierarchy in each view.

Design Analyzer provides two level buttons to move up or down a design's hierarchy. When inside a design, you can move down into any of its subdesigns, then move back up. This gives you complete access to a design's hierarchy. The Hierarchy View of any level shows that level's subdesigns.

Designs View

When you read in a design using the Read selection from the File menu, you see the initial Designs View, showing all designs and subdesigns. See Figure 2-8.

To select an individual design,

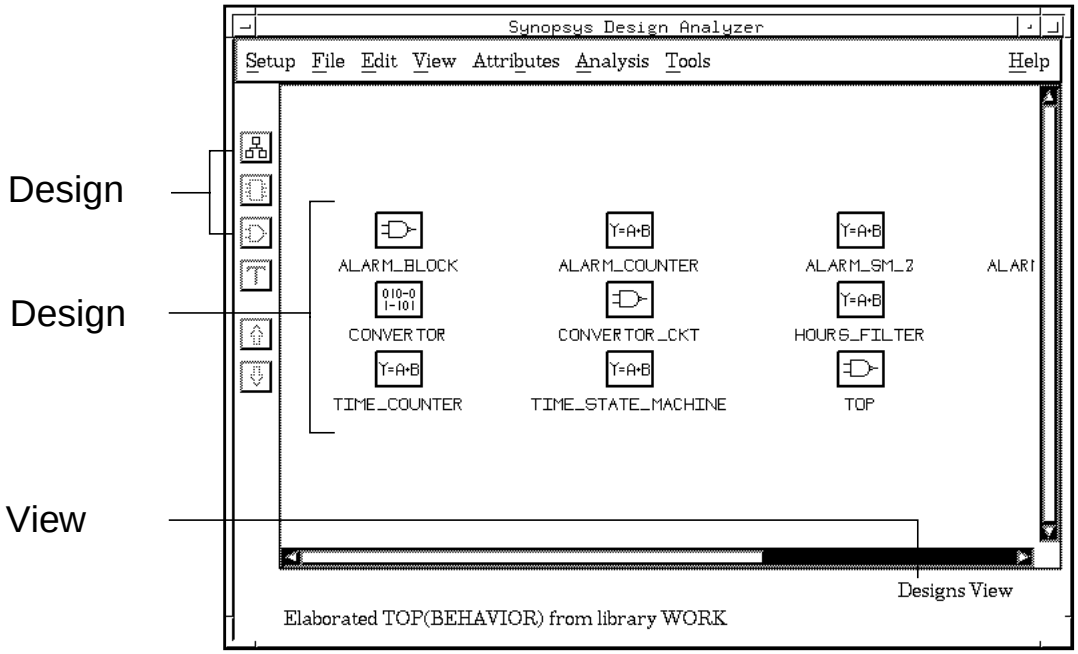
1. Select it.
2. Push into it.

For example, select the TOP design by clicking it with the left mouse button, then push into it by clicking the down-arrow button (on the left side of the window).

SHORTCUT

To push directly into a design, move the cursor onto the design, then double-click the left mouse button.

Figure 2-8 Designs View



To get to the Designs View from any other view, continue clicking the up-arrow button until you reach the Designs View.

When you read in another design, the Designs View automatically updates. All designs in memory appear as icons in alphabetical order by name.

Icons represent designs in the Designs View and Hierarchy View. A design icon appears as one of the types shown in Figure 2-9, which depend on a design's current representation.

Figure 2-9 Design Icons

The design representations are

EQUATION

Equation, or non-netlist VHDL or Verilog format.

PLA

Programmable logic array format.

FSM

Finite state machine design represented as a state table.

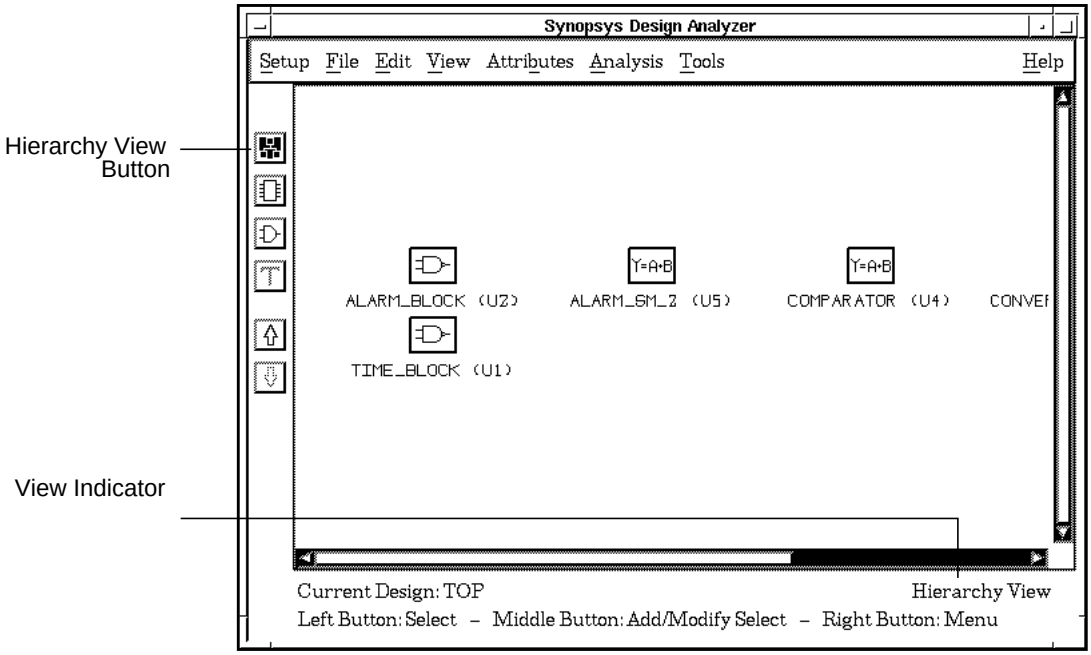
NETLIST

Design read in as a netlist (including structural VHDL and Verilog) or optimized.

Hierarchy View

Select View > Change View > Hierarchy from the menu to see the Hierarchy View of the TOP design, as shown in Figure 2-10.

Figure 2-10 Hierarchy View



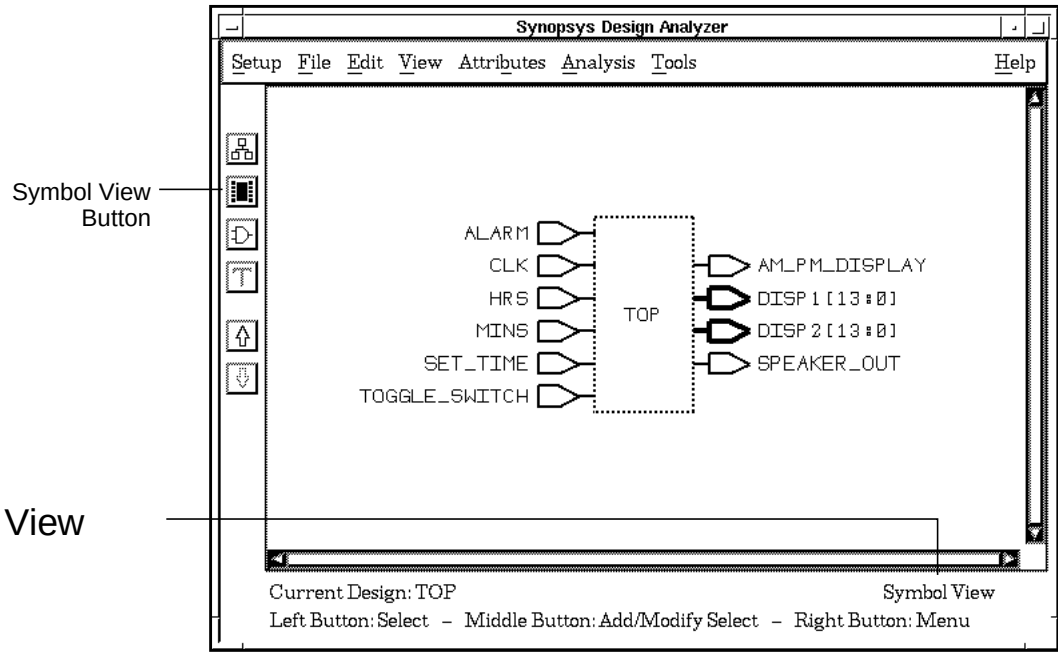
The TOP design is composed of six subdesigns on this level: ALARM_BLOCK, MUX, CONVERTOR_CKT, COMPARATOR, ALARM_SM_2, AND TIME_BLOCK.

Note that the Hierarchy View button (upper left) is highlighted and that the current design name (TOP) and current view (Hierarchy View) appear in the bottom margin.

Symbol View

When you push into the TOP design, you see its Symbol View first, as shown in Figure 2-11.

Figure 2-11 Symbol View



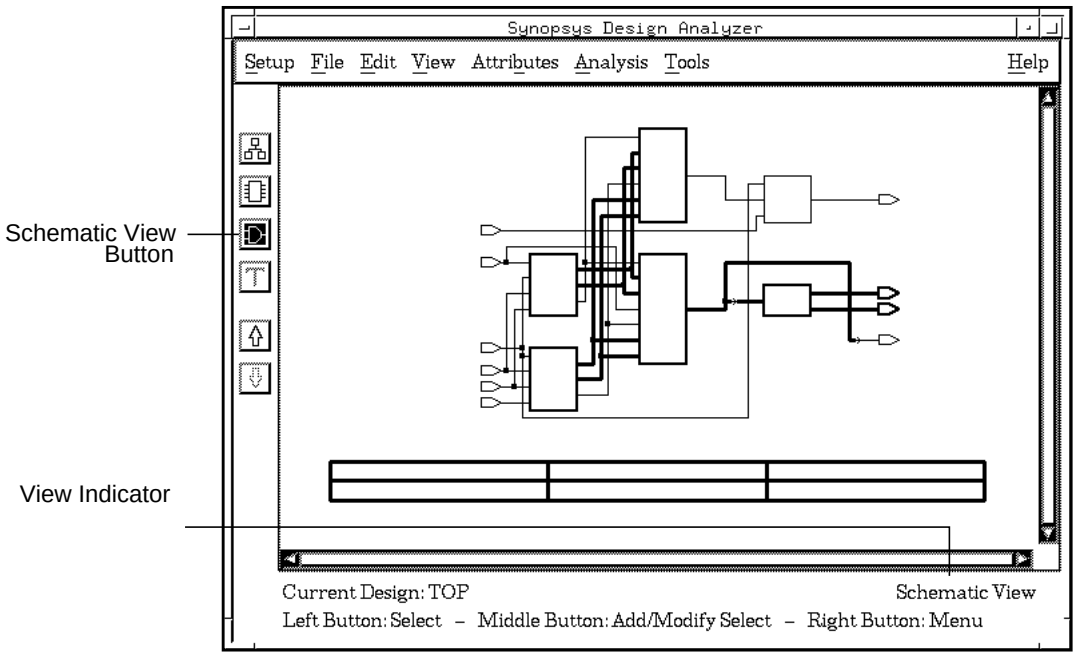
The TOP design has six input ports and four output ports. Notice that the Symbol View button (upper left) is highlighted.

If a design already has a schematic generated when you push into it, you see its Schematic View rather than its Symbol View. To see the Symbol View, select View > Change View > Symbol from the menu or click the Symbol View button.

Schematic View

Select View > Change View > Schematic from the menu to see the Schematic View of the TOP design, as shown in Figure 2-12.

Figure 2-12 Schematic View



The current design name (TOP) appears in the bottom margin. If the schematic has more than one sheet, the schematic sheet number (for example, Sheet: 1 of 2) also appears in the bottom margin. The Schematic View shows both low-level logic (gates) and subdesigns (boxes).

To get to a subdesign, push into its cell. For example, if you push into cell ALARM_BLOCK, you can get design the ALARM_BLOCK Hierarchy View, Symbol View, or Schematic View.

Note:

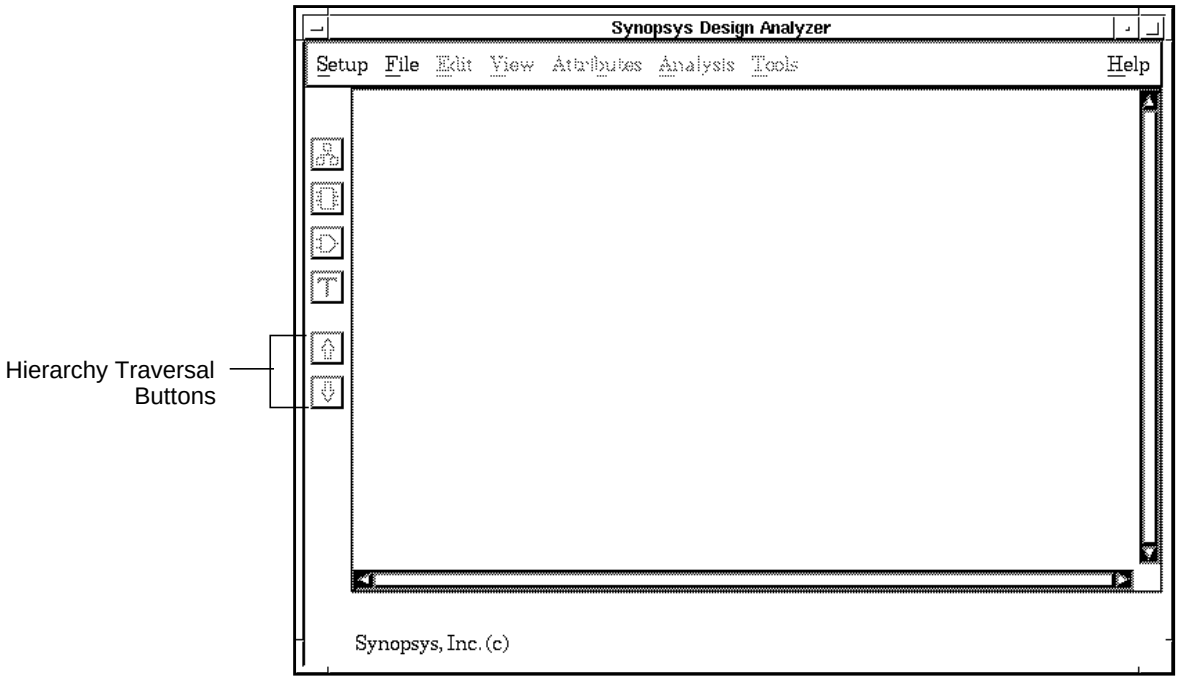
By default, DesignWare components appear in a different color than other cells. Change the color of the designware_layer components by using View > Style.

Traversing a Design Hierarchy

Design Analyzer uniquely treats each instance of a design in a hierarchy. This allows you to add attributes or explore the timing of instances of designs without affecting the referenced design.

The up-arrow button and the down-arrow button are hierarchy traversal buttons as shown in Figure 2-13. If a design is currently selected or being viewed, these two buttons enable you to move up and down the design hierarchy.

Figure 2-13 Hierarchy Traversal Buttons



The up arrow reverts to the previous view. Repeatedly clicking the up-arrow button eventually returns you to the Designs View.

The down arrow moves into the currently selected design or subdesign (subdesigns appear as boxes in a schematic). The down arrow stays within the current view if possible. For example,

- If you are in the Hierarchy View, you get the selected design's Hierarchy View (if one exists) or its Symbol View. A design does not have a Hierarchy View if it does not have subdesigns.
- If you are in the Symbol View, there are no subdesigns to select, so the down arrow is disabled.
- If you are in the Schematic View, you get the selected subdesign's Schematic View (if one has already been created) or its Symbol View. You can use the Schematic View button to create the Schematic View.

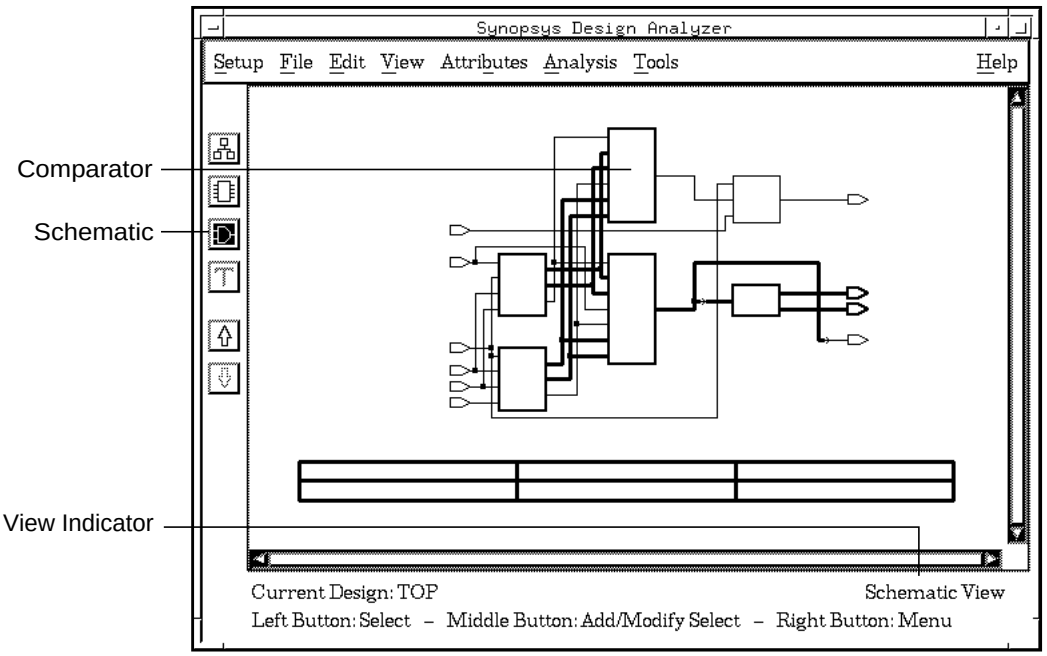
SHORTCUT

Double-clicking the left mouse button on a design or subdesign is equivalent to selecting it and clicking on the down arrow.

You can also use the View menu's Change Level submenu to move up and down the design hierarchy and to move to the top design (Designs View).

To view the schematic for U4, you would select the COMPARATOR block marked U4 in the TOP schematic view and click the down arrow key, shown in Figure 2-14. The text at the bottom of the Design Analyzer window indicates that the design is in TOP and the instance is U4 (COMPARATOR).

Figure 2-14 Design Analyzer Window: TOP Design



Executing Tasks

You can execute a task by either selecting an object or selecting a task.

Selecting Objects

You can select objects in the Design Analyzer window either graphically or by name and object type. Objects to select include designs, cells, nets, pins, ports, clocks, and constraint icons.

Selecting Objects Graphically

You can select objects directly or by area.

- Direct selection

Click the left or middle mouse button with the cursor on the object you want. The left mouse button selects just one object, deselecting all other objects. The middle mouse button toggles the select status of that object. If the object was not selected, it is selected and added to the current set of selected objects; if the object was previously selected, it becomes deselected.

To select a pin, zoom in (see Chapter 6, "View Menu"), then click the left or middle mouse button with the cursor directly over the pin. You can also select pins when you are not zoomed in by holding down the Shift key and clicking the middle mouse button. Continue clicking until you select the pin you want. Alternately, you can press Shift-Control along with the left mouse button to select a pin. The latter method also applies to systems having a single mouse button.

- Area selection

  Press and hold the left or middle mouse button and drag the select outline around the objects you want. The left mouse button selects all objects in the select outline, deselecting all other objects.

  The middle mouse button toggles the select status of the objects inside the select outline. If an object inside the select outline was not already selected, it is added to the existing set of selected objects (if any). If an object inside the select outline was already selected, it becomes deselected.

To deselect all selected objects,

1. Move the cursor into an empty part of the background.
2. Click the left mouse button (you select nothing).

Selecting Objects by Name and Type

Use the Edit menu's Select dialog box to select objects by name and by type. For example, you can select all input ports whose name begins with X. In addition, you can select a subset of objects that have a particular attribute value such as all nets with a fanout greater than three. See Chapter 5, "Edit Menu," for a complete description of the Edit menu's Select dialog box.

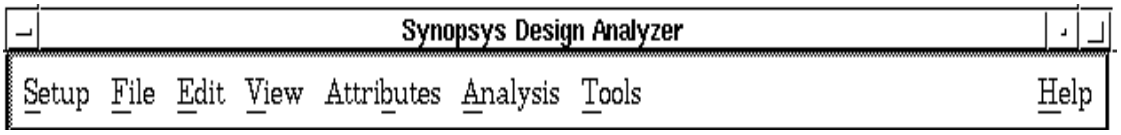
Selecting Tasks

You can select tasks in Design Analyzer using the menu bar or the pop-up menu.

Understanding the Menu Bar

The design flow through Design Analyzer displays in the order (left to right) of the seven top-level menus. Figure 2-15 shows the menu bar. The Help menu is located at the far right of the menu bar.

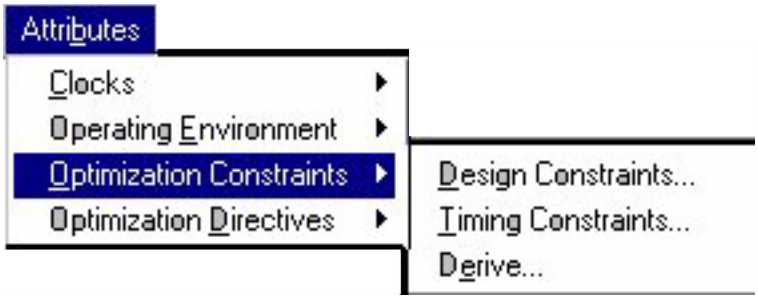
Figure 2-15 Menu Bar



Each pull-down menu contains a set of selections related to that topic that executes a command, displays a submenu, or displays a dialog box. Selections that execute commands have no punctuation. Selections that include a submenu are followed by a right-pointing arrow. Selections that display a dialog box are followed by an ellipsis (...).

When you select a menu title, such as Attributes, the associated submenu appears as in Figure 2-16.

Figure 2-16 Example Menu



In Figure 2-16, the Attributes menu has four selections: Clocks, Operating Environment, Optimization Constraints, and Optimization Directives. Each of these selections has a right-pointing arrow indicating that a submenu pops up when selected.

If you select Optimization Constraints, the illustrated submenu pops up. An ellipses follows two selections in this menu, indicating that each menu displays dialog boxes when selected.

Design Analyzer enables only the currently valid subset of actions. Unavailable actions still show on menus, but they appear in gray and you cannot select them. For example, if you have not selected a design, you cannot select Tools > Design Optimization. As another example, if your design is not a finite state machine, you cannot define the design's state vector.

Design Analyzer recognizes object-specific actions. For example, if you select a net then choose Set Values, a net-specific dialog box appears. If you select a pin, port, or clock, a different dialog box appears. The following information briefly describes the options in the Design Analyzer menu bar.

Setup

- Define the search path, link libraries, and target library.
- Set system variables.

- Get necessary tool licenses.
- Execute predefined and user-defined scripts.
- Display the Command Window.

File

- Read design description files.
- Analyze and elaborate HDL files and designs.
- Import timing and physical cluster information.
- Save designs in different formats.
- Write out timing information for external tools.
- Plot designs.
- Quit Design Analyzer.

Edit

- Find design objects with wildcard expressions.
- Insert pads in FPGA designs.
- Edit the design hierarchy, creating and deleting subdesigns.
- Uniquify the design instances.
- Remove all attributes and constraints.

View

- View the design hierarchy, its symbols showing the ports, and its schematics.
- Traverse the hierarchy.

- Change the view of a design.
- Change schematic sheets.
- Create a new view window.
- Change display properties.
- Re-create and refresh a schematic.

Attributes

- Specify clocks and their properties.
- Specify the following aspects of the design operating environment:
  - Input delay
  - Output delay
  - Drive strength
  - Load
  - Characterize
  - Operating conditions
  - Wire load
  - Timing range
- Specify design constraints (goals) including area, power, and speed.
- Characterize a subdesign in the context of the current design.
- Specify options and directives for the Design Compiler synthesis tools.

Analysis

- Link the current design.
- Check the current design for errors.
- Call the timing analyzer to update timing estimates.
- Show timing values.
- Highlight maximum, minimum, and critical timing paths.
- Get different kinds of reports about the current design.

Tools

- Synthesize and optimize a design.
- Create or optimize a finite state machine design.
- Create or optimize FPGA designs.)
- Add test structures to a design and get test-related reports.

Help

- Obtain descriptions of Design Analyzer features.
- Display Design Compiler man pages.
- View online documentation.

Selecting Tasks Using the Mouse

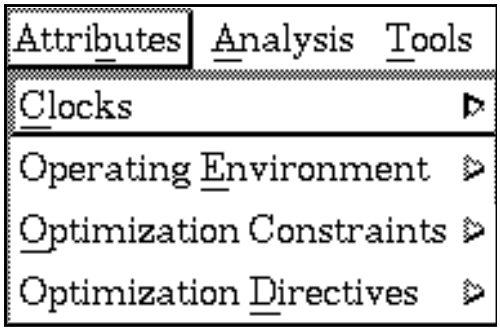
To outline the menu selection,

1. Holding down the left mouse button, drag the cursor arrow to the desired menu title

2. Release the left mouse button on that menu title.

See the highlighted selection in Figure 2-17.

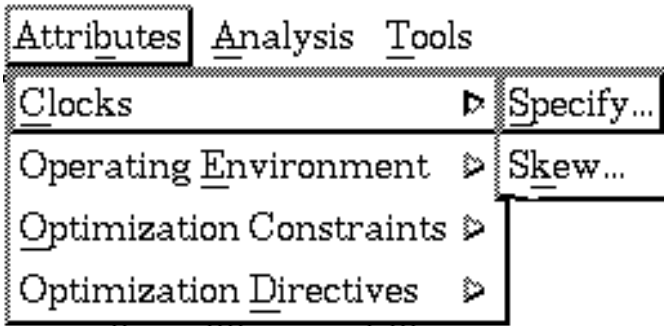
Figure 2-17 Attributes Menu with Selection Highlighted



To choose the outlined (default) selection, press the Return key. To choose any menu selection, click the selection with the left mouse button.

An arrow beside a selection indicates a submenu. For example, Figure 2-18 shows the Attributes > Clocks submenu. You interact with submenus just as you do with menus. Some submenus contain other submenus.

Figure 2-18 Menu and Submenu



Selecting Tasks Using the Keyboard

Most keyboards have a Meta key (also called Alt, Left, or Right). You can select a menu title by typing the underlined character in the title name along with this Meta key.

To select Attributes,

1. Type Meta-B.

   Then, to execute the Attributes selection Optimization Constraints,

2. Type O (without the Meta key).

   You can use either uppercase (B O) or lowercase (b o) letters.

Using the Pop-up Menu

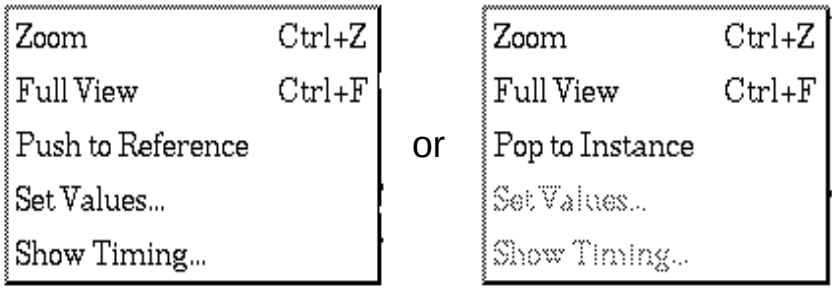
You can use the buttons on your mouse to immediately access the options available in the pop-up menu.

To use the pop-up menu,

1. Position the cursor in the main Design Analyzer window.
2. Press and hold down the right mouse button to see the pop-up menu.
3. Drag the cursor to the selection you want.
4. Release the mouse button.

The third menu item appears as Push to Reference or Pop to Instance depending on your location in a hierarchical design. Figure 2-19 shows an example of these two pop-up menus.

Figure 2-19 Pop-up Menus



The pop-up menu provides you with the following options:

Zoom

Zooms into a region. This selection changes the cursor to a plus sign (on a white background) or to an open plus sign (on a black background):

Drag an outline around the region you want to zoom into using the left mouse button. When you release the mouse button, the selected region is centered in the Design Analyzer viewing window and is shown as large as possible.

SHORTCUT

Press Control-z.

The View menu's Zoom In and Zoom Out selections double or halve the current zoom factor. For more information on zooming, see Chapter 6, "View Menu."

Full View

Makes the current schematic full size.

SHORTCUT

Press Control-f.

Push to Reference

Sets the current design to the design referenced by the selected instance.

Pop to Instance

Reverts to the instance of a design. This menu item is available only if you are pushed into the reference of a design.

Set Values

Shows and edits a selected object's attribute or constraint values.

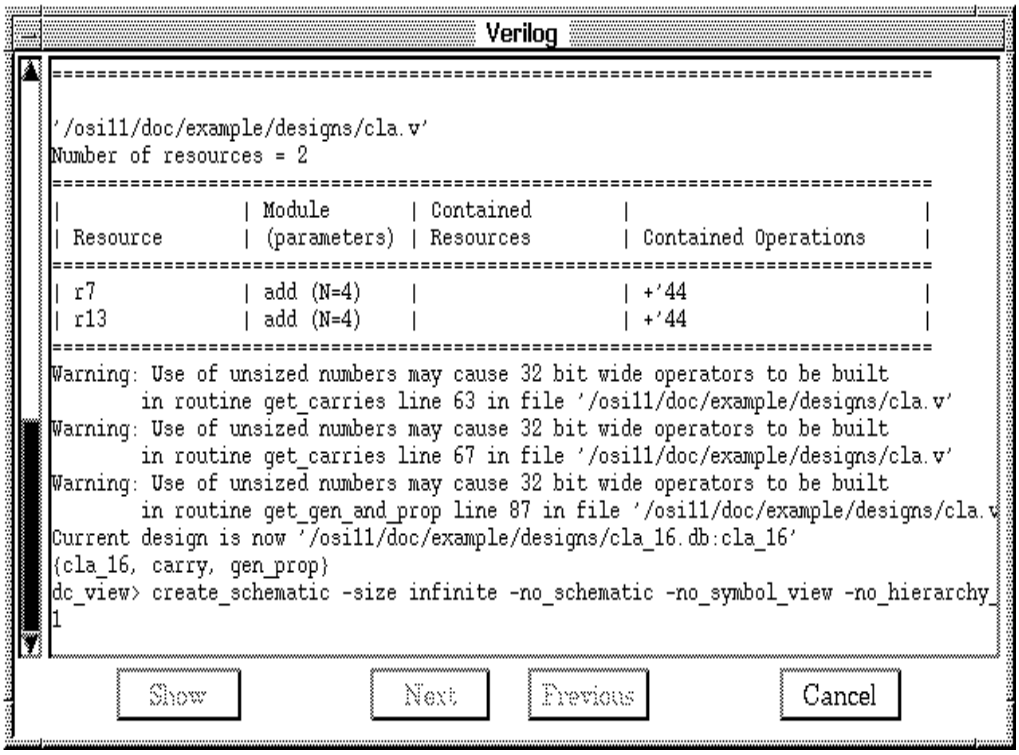
Show Timing

Shows the current timing values when you select a port, net, or pin. The timing analyzer derives timing values.

Monitoring Task Progress

You can monitor the progress of a task that you execute through a status window. This window has a text area with a scroll bar and four push buttons. Figure 2-20 shows the Status Window titled Verilog.

Figure 2-20 Status Window: Verilog Input Report



Find the following buttons along the bottom of a report window:

Show

Shows the object corresponding to a selected report line.

Next

Shows the object on the next report line.

Previous

Shows the object on the previous report line.

Cancel

Removes the report window.

To remove a status window, use the Cancel button. Use the Show, Next, and Previous buttons with linked status windows.

The following partial list of menu selections displays status windows with the indicated window names:

- Analysis > Link Design (Link Report)
- File > Read (Verilog or VHDL)
- Tools > Design Optimization (Compile Log)

Whether you enter commands through the menu interface or through the command-line interface, all commands are sent to Design Analyzer's command processor. For more information on dc_shell commands and syntax, see the Design Compiler Command-Line Interface Guide.

Note:

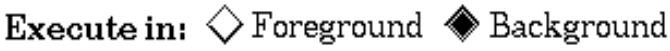
You can copy text from inside of the status window into a buffer by highlighting the text with the left mouse button. You can paste the contents of this buffer into the prompt line by moving the cursor into the prompt area and clicking the middle mouse button.

Some tasks started from Design Analyzer can take a long time to execute; for example,

- Compiling a circuit (Tools > Design Optimization selection; compile command)
- Compiling a finite state machine's circuit (Tools > Finite State Machines > Compile selection; compile command)
- Compiling test structures into a circuit (Tools > Test Synthesis > Insert Internal Scan Circuitry selection; insert_scan command)

When you start one of the previously listed tasks, a dialog box appears requesting more information. Among the information requested is whether you want to execute the task in the background or foreground. Figure 2-21 shows the buttons to choose foreground or background.

Figure 2-21 Foreground or Background Button



Foreground Tasks

When you run a task in the foreground, Design Analyzer suspends all user interaction until the task finishes. Upon completion, you can interact with the tool again.

Background Tasks

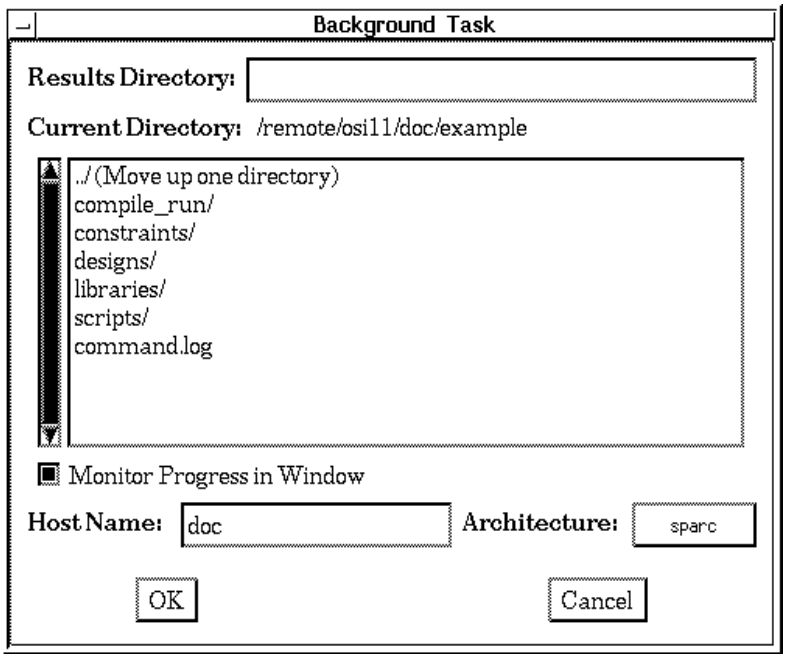
If you use node-locked software, background tasks execute on the current Design Analyzer node or on any other enabled node. If you use Synopsys Network Licensing, you can submit background tasks to any supported host in your network.

Design Analyzer continues to accept input and display results while a task window displays the current status of a background job. Later, a task completion dialog box appears to tell you when the background task is finished.

Background Task Dialog Box

Figure 2-22 shows the Background Task dialog box.

Figure 2-22 Background Task Dialog Box: Compilation



Click OK to execute the task on the displayed host, writing the resulting design or vector files into the displayed results directory. If you enable the Monitor Progress in Window option, a task monitor window is created. See “Background Task Monitor Window” later in this chapter.

Click Cancel to remove this dialog box without creating a background task.

The following sections describe the parts of the Background Task Window.

Results Directory

Enter the name of the directory where you want the files created by the task to be placed. Depending on the operation, the created files can be design database files or test vector files.

Monitor Progress in Window

Click this button to create a task monitor window.

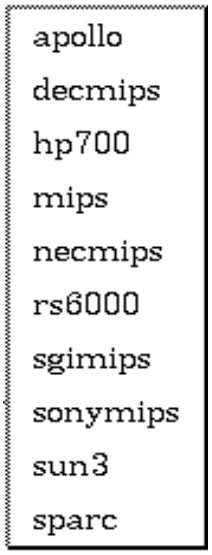
Host Name

Enter the name of the (possibly remote) host on which the background command executes in this text box.

Architecture

Click the Architecture button to open the Option Menu, shown in Figure 2-23, and choose the Host Name's architecture.

Figure 2-23 Supported Host Architectures

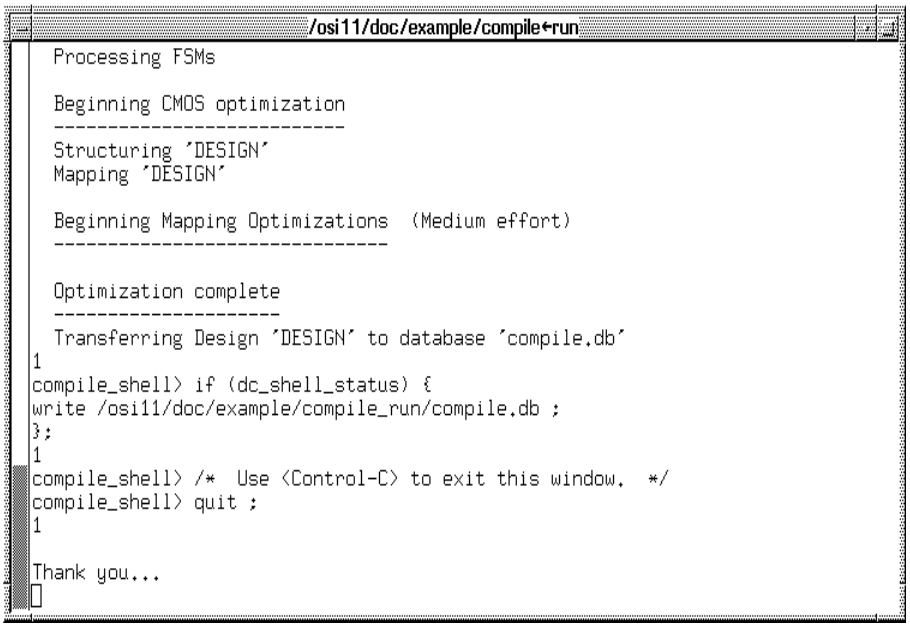


The dc_shell variable view_arch_types defines this list, which is subject to change. You can also customize this list to the available machine types on your network.

Background Task Monitor Window

Click the Monitor Progress in Window button to create a task monitor window. A task monitor window, shown in Figure 2-24, is a text window with a scroll bar. The name of the task window is the directory that contains the results.

Figure 2-24 Task Monitor Window: Compilation Report



To close a task monitor window on most platforms,

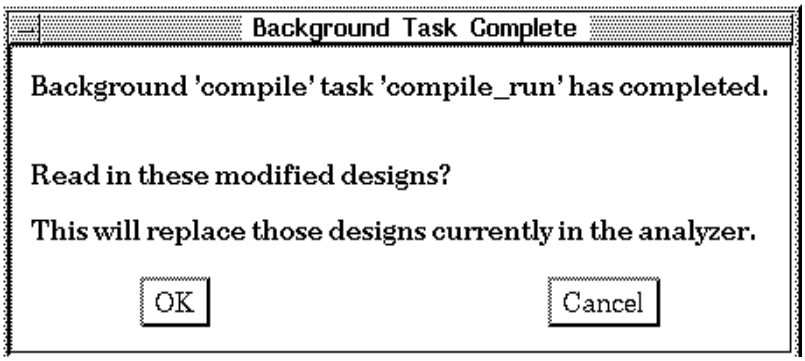
1. Move the cursor into the window.
2. Press Control-c.

For the interrupt to occur, you must invoke Design Analyzer as a foreground process (not as a background process using 'design_analyzer &').

Background Task Completion Dialog Box

When a design compilation background task finishes, you have the option of overwriting existing designs with the newly compiled designs. A dialog box, such as the one shown in Figure 2-25, appears.

Figure 2-25 Task Completion Dialog Box

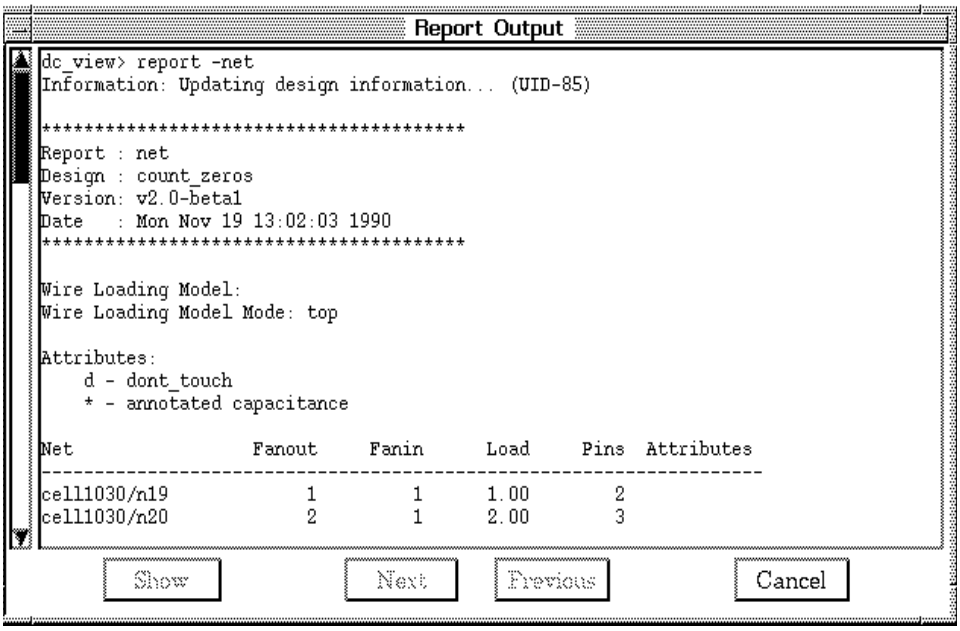


Click OK to replace (overwrite) the previous designs. Click Cancel to remove this dialog box without replacing any designs. In either case, the indicated directory, shown as compile_run in Figure 2-25, stores the newly completed versions.

Analyzing the Results

Linked report windows show the results of your analysis. The Analysis > Report and Tools > Test Synthesis > Display Reports selections create a linked report window that displays the selected reports. Figure 2-26 shows a sample report created by Analysis > Report with the Net option.

Figure 2-26 Report Output Window: Net Report



The next sections describe how to use the report window buttons with linked reports and show which reports and objects link to schematics.

Showing Linked Report Objects

To show an object in a linked report,

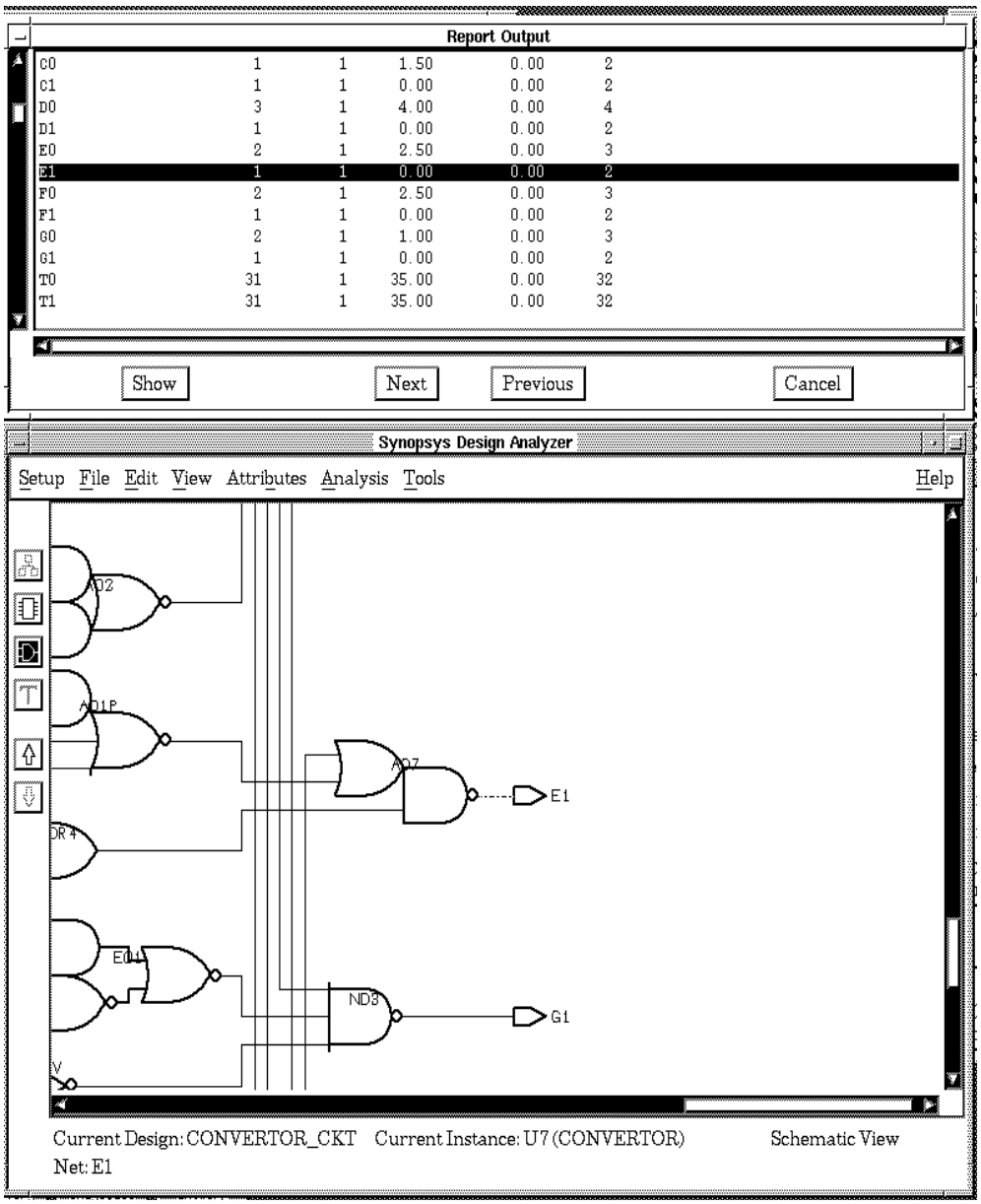
1. Select the name of the object in the report window.
2. Click Show.

This action generates a schematic (if it does not already exist) and shows the selected object centered in the Schematic View.

An object name (such as a design name) can be linked to multiple objects (such as its pins).

Figure 2-27 shows a selected net name in a net report (created by Analysis > Report with the Net option) and the corresponding net in a schematic.

Figure 2-27 Linked Report Window: Schematic Net Report, Net



To see the next object listed in a report window, click Next. To see the previous object listed in a report window, click Previous. If the report window contains more than one linked report, the next object can be a different type. For example, if you have both a cell and a net report in a report window, the Next object after the last cell name is the first net name.

Analysis and Test Reports Linked to Objects

Table 2-1 shows the various analysis and test reports available in Design Analyzer.

Table 2-1 Analysis and Test Reports

Menu Selection	Report Window Name	Report	Description
Analysis > Check Design	Design Errors	Check Design	Checks the design for obvious errors.
Analysis > Report	Report Output	All Attributes	Lists the attributes and their values for the selected object.
		Area	Lists area information and statistics on the current design.
		Bussing	Lists the bused ports and nets in the current design.
		Cell	Lists the cells in the current design and their cell attributes.
		Clock Skew	Lists the clock network skew information set on the design by the set_clock_skew command.
		Clock Tree	Lists the fanout network for the clock sources in the design.
		Clocks	Displays clock-related information on the current design.

Table 2-1 Analysis and Test Reports (Continued)

Menu Selection	Report Window Name	Report	Description
		Compile Options	Lists information about the compile options on the design.
		Constraints	Lists the constraints on the current design, their cost, weight, and weighted cost.
		Cross Ref	Lists a cross-reference of the schematic objects and the sheets where they appear.
		Design	Displays attributes on the current design.
		FPGA Resources	Shows FPGA vendor-specific information about the design. Useful for part selection.
		FSM	Lists the state-machine attributes and information on the current design.
		Hierarchy	Shows the selected design or subdesign. Does not show gates.
		Net	Displays net information for the design of the current instance if set; otherwise, displays the current design.
		Path Groups	Lists information about path groups in the current design.
		Point Timing	Lists point-to-point timing information for paths to the selected pin, or between two pins or ports.
		Port	Lists information about ports in the current design.
		Power	Lists information about the static power of the current design. ECL Compiler only.

Table 2-1 Analysis and Test Reports (Continued)

Menu Selection	Report Window Name	Report	Description
		Reference	Shows the selected design or subdesign reference. Does not show gate references.
		Resource	Lists the resources used in the current design.
		Selected	Lists the name and type of the selected object.
		Timing	Lists timing information for the current design.
		Timing Requirements	Lists timing path requirements and related information.
Tools > Test Synthesis >Check Design Rules	Design Rule Errors	Check Test	Checks the design for test design rule violations.
Tools > Test Synthesis > Display Reports or Analysis > Test Report	Test Report	Assertions	Lists the cell pins and design ports specified in set_test_assume, set_test_hold, set_test_initial, and set_test_isolate.
		Constraints	Lists any test constraints for the current design and indicates whether the constraints are met by DFT Compiler.
		JTAG	Lists the JTAG information for the current design.
		Methodology	Lists the details of the test scan style and methodology for the design.
		Ports	Lists the details of test ports for the current design.
		Scan Path	Lists every scan cell on the scan path for the current design.

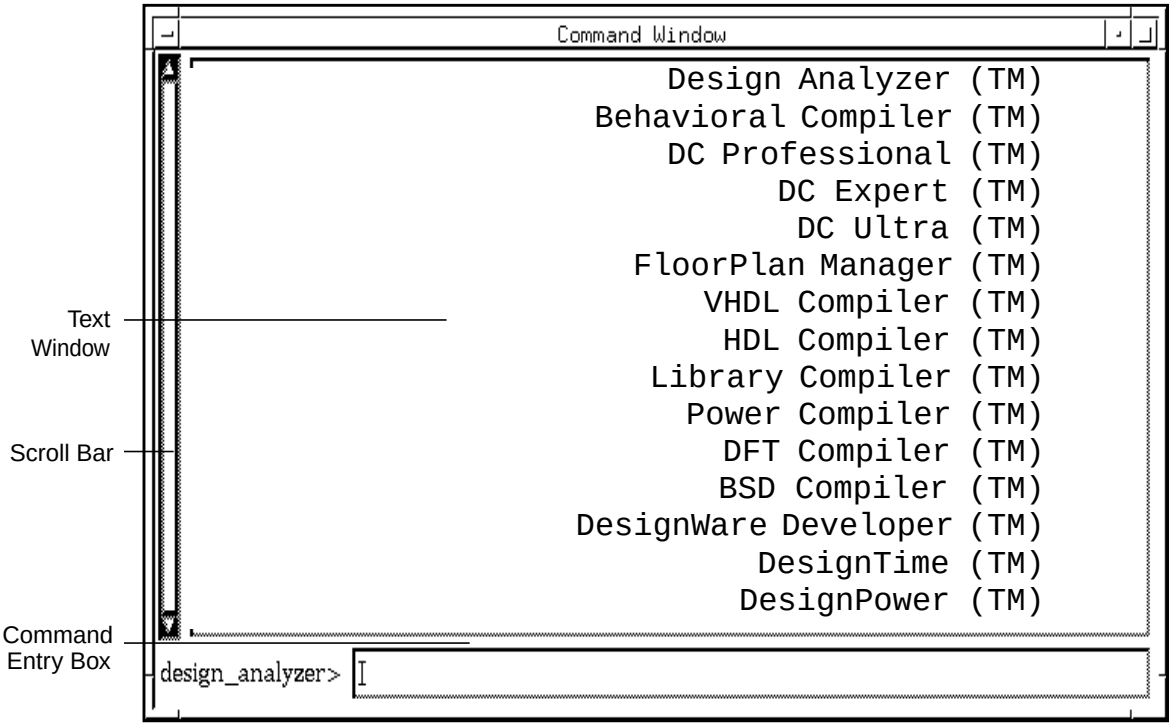
Using the Command-Line Interface

Design Analyzer's Command Window shows the command-line interface. All commands and reports generated by menu selections echo in the Command Window. You can type Design Compiler (dc_shell) commands in the command entry box.

To display the Command Window, select Setup > Command Window.

Figure 2-28 shows the Design Analyzer Command Window.

Figure 2-28 Command Window



The Command Window consists of a text window with a scroll bar and a command entry box, which includes the following parts:

Text window

Shows all Design Analyzer command input and text output. When you use a menu selection to perform an action, the corresponding command appears in this window. Status and error messages also display in this window.

Scroll bar

Scrolls through the displayed text. For more information, see Chapter 1, “Design Analyzer Overview.”

Command entry box

Allows you to type commands in the command entry box at the bottom of the Command Window, exactly as you type in the Design Compiler command-line interface. Each command you type echoes on a separate line in the command window itself.

To cut and paste text from the text window area into the command entry box,

1. Select an area of text with the left mouse button.
2. Paste with the middle mouse button.

Customizing the Design Analyzer Environment

Push buttons, toggle buttons, option menus, and some text boxes are preset to certain defaults. To view and change the default settings for the current Design Analyzer session, use Setup > Variables.

To change the defaults for Design Analyzer, edit the .synopsys_dc.setup file in your home or working directory. See the Design Compiler Reference Manual: Fundamentals for more information.

The graphical interface variables are in the view group. Use Setup > Variables to see their current values.

Two variables control whether Design Analyzer writes records of its actions and outputs the information to a file:

view_command_log_file

If you set this variable to a file name, all text written to the Design Analyzer Command Window is echoed to that file. If an error occurs during your session, this file can help determine the cause. If you find an error in the Synopsys software, keep this file and the related design or script files, and contact your Synopsys Applications Engineer. If you do not designate a filename, Design Analyzer creates a default file called view_command.log in the present working directory.

view_log_file

If you set this variable to a file name, the file contains a record of all Design Analyzer user-interface actions in the current session such as menu selections and mouse actions. If you encounter a repeatable error in the Design Analyzer user interface, use this variable to create a file and contact your Synopsys Applications Engineer. If you do not designate a file name, Design Analyzer does not create a file.

The following variables control the display and behavior of Design Analyzer:

default_schematic_options

Sets default options for all automatically generated schematics (create_schematic command options).

view_background

Sets background color of the main Design Analyzer window, either black or white. The default is black. To change the color to white, set this variable in your .synopsys_dc.setup file.

view_cache_images

Specifies whether bitmaps cache for fast schematic drawing. The default value is true.

view_command_win_max_lines

Specifies the maximum number of lines saved in the Design Analyzer command window. When this number of lines is exceeded, the older lines at the top of the list are removed. The default is 1,000 lines.

view_dialogs_modal

Before allowing you to enter other commands, requires acknowledgment of error and question (confirmation) dialog boxes if true. The default is true.

view_disable_cursor_warping

Does not “warp” (move) the cursor into dialog boxes, if true. The default is true.

view_disable_error_windows

Creates no errors if set to true. Error messages display in the Command Window. The default is false.

view_disable_output

Specifies whether output to the Design Analyzer Command Window is disabled. The default value is false.

view_error_window_count

Sets the maximum number of errors that Design Analyzer reports per command. If more than this number of errors occur, it informs you that additional errors occurred and you can view the errors in the command window. The error window suppresses until the end of the current command. The default is 6.

Set this variable to 0, which indicates to display all errors. Set it to a negative number (or set view_disable_error_windows to true) to indicate not to display errors.

view_on_line_doc_cmd

If you set this variable, it allows you to invoke the online documentation viewer from the optional menu item, Online Documentation, in the Help menu. Set the value of this variable to the UNIX command that invokes the online documentation view.

view_script_submenu_items

Allows you to add your own scripts to the Setup menu by placing this variable in the .synopsys_dc.setup file. The variable should contain a list of strings that are grouped into pairs. The first member of the pair is the text as it will appear in the submenu; the second member is the string that gets sent to the dc_shell command line for execution.

view_set_selecting_color

Specifies the name of an X Window System color to use for zooming and selecting box outlines. The default is white.

view_tools_menu_items

Allows you to add your own scripts to the Tools menu by placing this variable in the .synopsys_dc.setup file. The variable should contain a list of strings that are grouped into pairs. The first member of the pair is the text as it will appear in the submenu. The second member is the string that gets sent to the dc_shell command line for execution.

view_use_x_routines

A true value indicates that the workstation where the graphics display has a floating-point processor. A false value indicates the absence of a floating-point processor. Setting this variable to the correct value improves performance. The default is true.

The following variables determine the contents of various fields and lists:

view_analyze_file_suffix

Shows a list of file extensions that identify the files displayed in the File > Analyze dialog box.

view_arch_types

Shows a list of architecture types displayed in the Background dialog box Architecture list. See “Background Tasks” earlier in this chapter.

view_execute_script_suffix

Shows a list of file name extensions (file_name.ext). The file name list in the Setup > Execute Script dialog box displays only files with these extensions.

view_read_file_suffix

Shows a list of file name extensions. Only files with these extensions display in the file name list in the File > Read dialog box.

view_select_default_message

Defines the message that appears at the bottom of the Design Analyzer window.

view_select_separator

Defines the string that separates the selected object list on the bottom of the screen.

view_write_file_suffix

Shows a list of filename extensions. Only files with these extensions display in the filename list in the File > Save As dialog box.

The following set of variables relates to the X Window System:

view_use_small_cursor

Accommodates size limitations on some platforms. If true, the terminal only supports small (16-bit) cursors. The default is false.

x11_set_cursor_background

Names the X Window System color to use for the cursor's background.

x11_set_cursor_foreground

Names the color to use for the cursor's foreground.

x11_set_cursor_number

Designates the number of the default cursor. The number refers to standard cursor fonts. The default is a left-pointing arrow.

Design Analyzer sets the following variables before it reads the .synopsys_dc.setup files. (The initial values for these variables come from the UNIX environment and the X display itself.)

x11_is_color

Set to true if the X display supports color; otherwise, set false. The default is false.

x11_display_string

Set to the value of the UNIX environment DISPLAY variable, such as "machine5:0".

x11_vendor_version_number

Set to the version number of the X display.

x11_vendor_release_number

Set to the release number of the X display.

x11_vendor_string

Set to the first seven characters of the name of the maker of the X display.

Note:

The colors set by these variables refer to standard X11 color definitions. These color values are defined in /usr/lib/X11/rgb.txt.

You can put this last set of variables in your .synopsys_dc.setup file, for example:

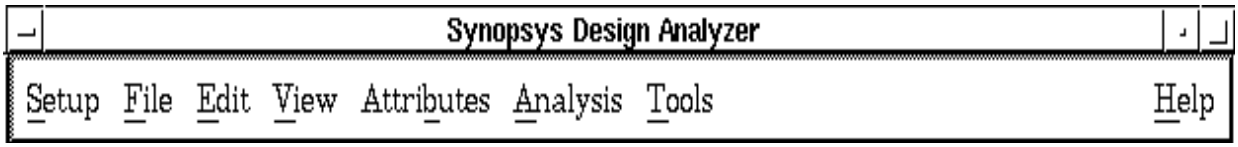
```
if( x11_vendor_string == ”Silicon” && \
    x11_is_color == ”true”) {
  x11_set_cursor_foreground = ”magenta” ;
  view_use_small_cursor = ”true” ;
  view_set_selecting_color = ”white” ;
}
```

For more information on view variables, use the Help > Commands menu.

Describing the Menu Bar

Figure 2-29 shows the design flow through Design Analyzer. Design Analyzer provides a Help menu at the far right of the menu bar. This manual presents the information in the sequence of the menu bar.

Figure 2-29 Menu Bar



The remaining chapters in this manual describe each Design Analyzer menu, submenu, and dialog box in the order presented in the menu bar:

- Setup menu
- File menu
- Edit menu
- View menu
- Attributes menu
- Analysis menu
- Tools menu
- Help menu

3

Setup Menu

This chapter describes all the items in the Setup menu and the submenus and dialog boxes you can access through it.

Use the Setup menu to obtain information about

- Defaults
- Variables
- License
- Execute Script
- Scripts
- Command Window

When you open the Setup menu, you can access the menu items and submenus shown in Figure 3-1.

Figure 3-1 Setup Menu and Submenus

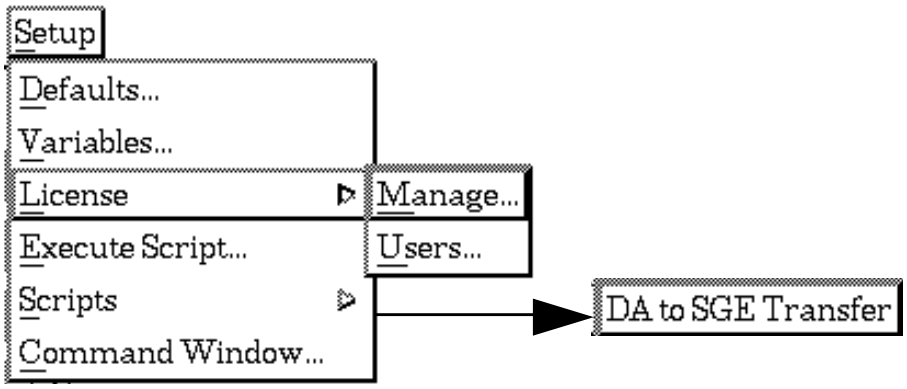


Table 3-1 and the following sections explain how to use the items in the Setup menu.

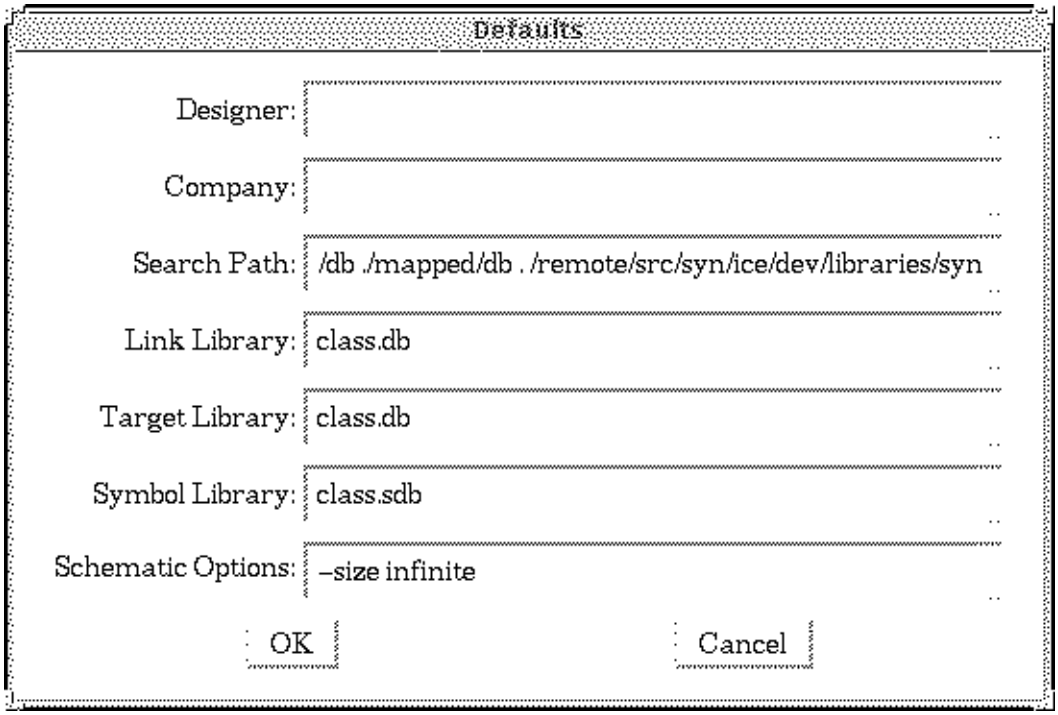
Table 3-1 Setup Menu Options

Option	Action	Equivalent Command
Defaults	Use to see and edit the current values of eight commonly used system variables.	variable_name = value
Variables	Use to query and edit the current values of system variables, and to create new variables.	variable_name = value
License	Use to query licensing information.	
Execute Script	Use to execute a dc_shell command script file.	include
Scripts	Use to run a predefined script in the .synopsys_setup file.	
Command Window	Use to display the Design Analyzer Command Window.	

Defaults

When you choose Defaults from the Setup menu, you see the Defaults dialog box shown in Figure 3-2.

Figure 3-2 Defaults Dialog Box



Click OK to change the variables' current values to the displayed values. Click Cancel to remove this dialog box.

Design Analyzer uses the Schematic Options variable (default_schematic_options) every time you create a schematic. When you call the create_schematic command, the Schematic Options variable's value is used for command options. By default, the value is -size infinite, meaning that each schematic is created on a single sheet of infinite size.

To create schematics using A-size sheets,

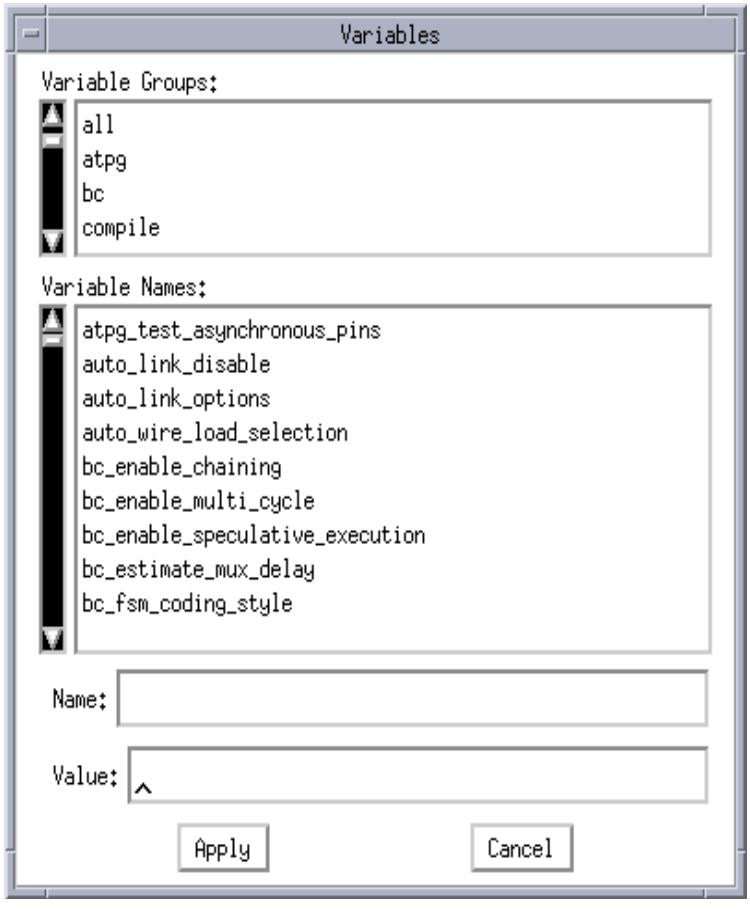
1. Change the Schematic Options value to -size A.
2. Click OK.

For a complete list of options to the create_schematic command, use the Help > Commands menu.

Variables

Figure 3-3 shows the Variables dialog box.

Figure 3-3 Variables Dialog Box



Click Apply to change the variable shown in the Name text box to the displayed Value. Click Cancel to remove this dialog box.

The following sections explain the parts of the Variable dialog box

Variable Groups

The Variable Groups list shows all predefined variable group names. Use the scroll bar, as necessary, to bring a variable group name into view.

When you click a variable group's name, its member variables appear in the Variable Names list.

The special variable group "all" contains all variables, including those not in any other group.

To create a new variable group, use the group_variable command in the Command Window's command line.

Variable Names

The Variable Names list shows all variable names in the currently selected variable group. Use the scroll bar, as necessary, to bring a variable name into view.

Name

Type a variable name in the Name text box, or choose a variable name from the list.

If you type a variable name that does not already exist and click Apply, that variable appears. The new variable is not placed in the current Variable Group. To see a newly created variable's value, look up the variable name in the "all" group. To add a newly created variable to an existing variable group, use the group_variable command in the Command Window's command line.

Value

Type the value you want in the Value text box.

If you choose a Variable Name from the current Variable Group, its current value appears in this text box. Edit the current value and click Apply.

When you click a variable name, the name and the variable's current value appear in the Name and Value text boxes.

License

When you select License from the Setup menu, you see the License submenu shown in Figure 3-4. If you need more information about Synopsys licensing, see the *Licensing Installation and Administration Guide*.

Figure 3-4 License Submenu

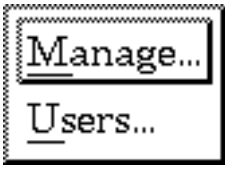


Table 3-2 explains how to use the options in the License submenu.

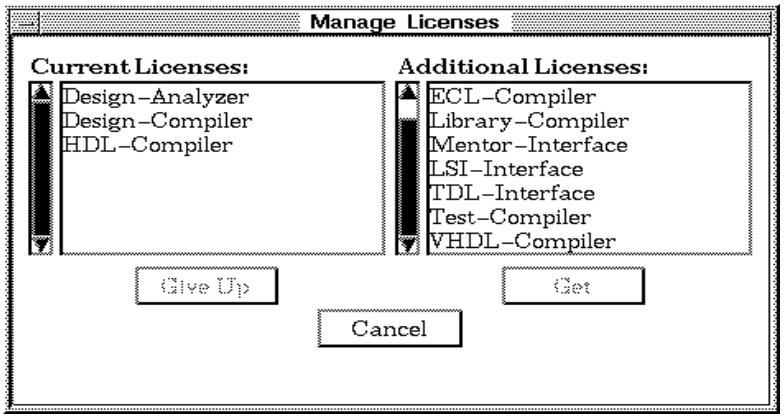
Table 3-2 License Submenu Options

Option	Action	Selection	Equivalent Command
Manage	Shows current licenses and available licenses		
	Allows you to give up a license	Give Up	remove_license
	Allows you to get a license	Get	get_license
Users	Shows all current users of your site's Synopsys licenses		license_users

Manage

When you select Manage from the License submenu, you see the Manage Licenses dialog box shown in Figure 3-5.

Figure 3-5 Manage Licenses Dialog Box



Click Cancel to remove this dialog box.

To give up one of the licenses you currently have (shown in the Current Licenses list in Figure 3-5),

1. Select the license name.
2. Click Give Up.

SHORTCUT

Double-click a current license name to give it up.

To get one of the available licenses (shown in the Additional Licenses list in Figure 3-5),

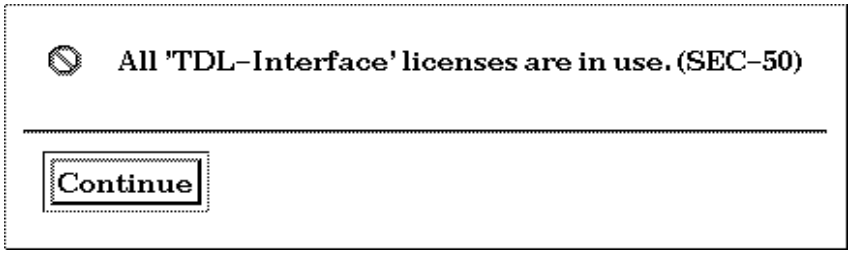
1. Select the license name.
2. Click Get.

SHORTCUT

Double-click an additional licence name to get it.

If you try to get a license when all available licenses are already taken, you receive an error message. For example, if all TDL interface licenses are already taken, you see a message similar to the one in Figure 3-6.

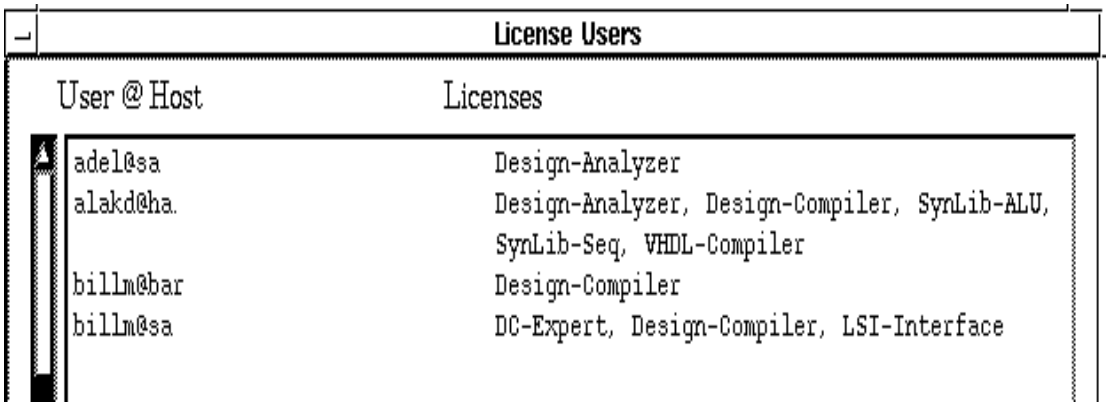
Figure 3-6 All Licenses in Use Message



Users

When you select Users from the License submenu, you see the License Users dialog box shown in Figure 3-7. You can have more than one license of a particular type, which means that you execute more than one copy of that tool.

Figure 3-7 License Users Dialog Box



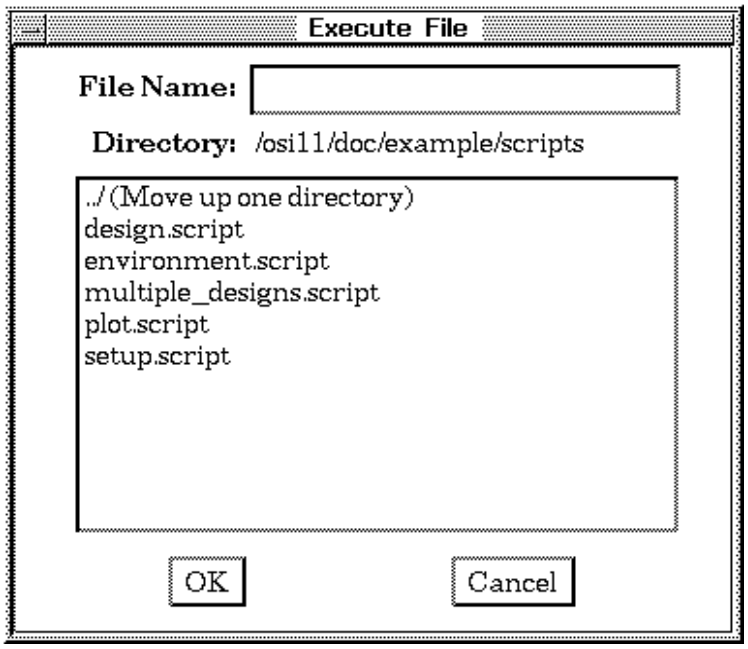
Click Cancel to remove this dialog box. Use Setup > License > Manage to get or give up a license.

The list of license users is a snapshot of the licenses in use. If you see that not all licenses of a particular type are in use but you can't get that license, someone else checked it out after the License Users list was created.

Execute Script

When you select Execute Script from the Setup menu, you see the Execute File dialog box shown in Figure 3-8.

Figure 3-8 Execute File Dialog Box



Click OK to read and execute the file whose name appears in the File Name text box. Click Cancel to remove this dialog box.

The list variable view_execute_script_suffix specifies which file suffixes display in this list.

Scripts

When you choose Scripts from the Setup menu, you see the Scripts submenu.

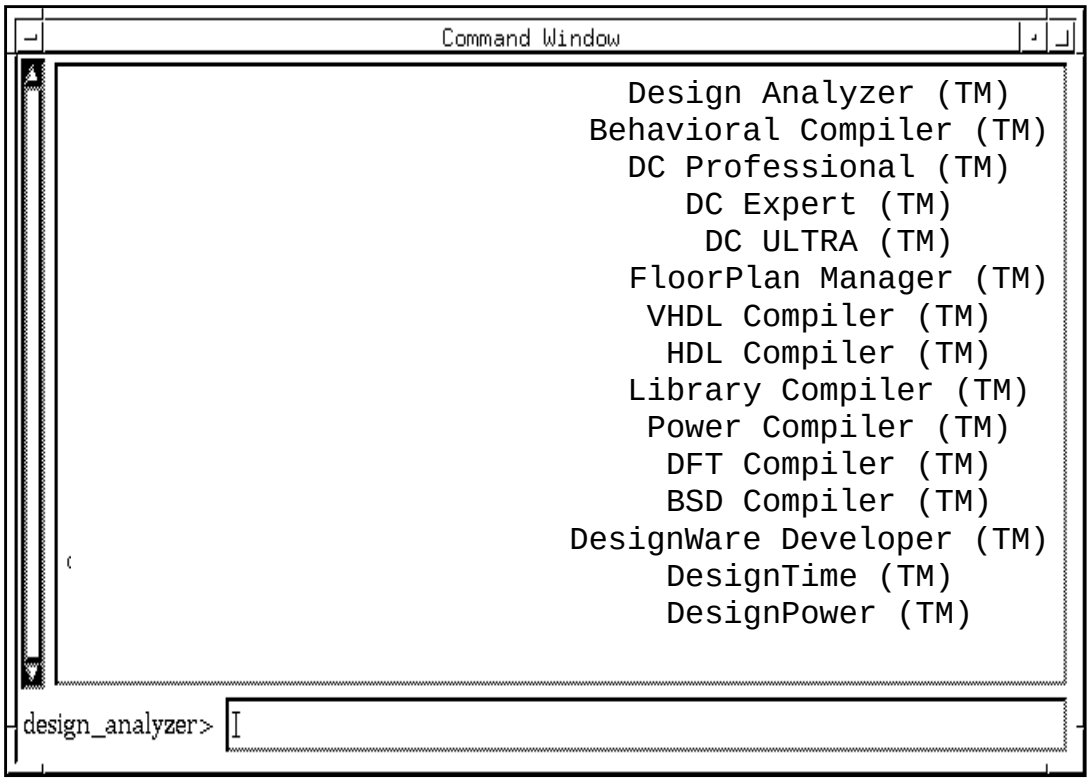
You can define up to ten scripts for the Setup > Scripts submenu. You add scripts with the following variable definition format:

```
view_script_submenu_items= {"cmd_title1",
"cmd_string1"..."cmd_title10","cmd_string10"}
```

Command Window

When you select Command Window from the Setup menu, you see the Command Window shown in Figure 3-9.

Figure 3-9 Command Window



Chapter 2, “Using Design Analyzer,” describes this window.

The value of the shell_prompt variable determines the prompt displayed in the Command Window. The default value is design_analyzer>.

You can use all Design Analyzer commands in the Command Window.

Whether you enter commands through the menu interface or through the command-line interface, all commands are sent to Design Analyzer's command processor.

4

File Menu

This chapter describes all the items in the File menu and the submenus and dialog boxes you can access through it.

Use the File menu to

- Read
- Analyze
- Elaborate
- Import
- Save
- Save As
- Save Info
- Plot
- Quit

When you open the File menu, you can access the menu items and submenus shown in Figure 4-1.

Figure 4-1 File Menu and Submenus

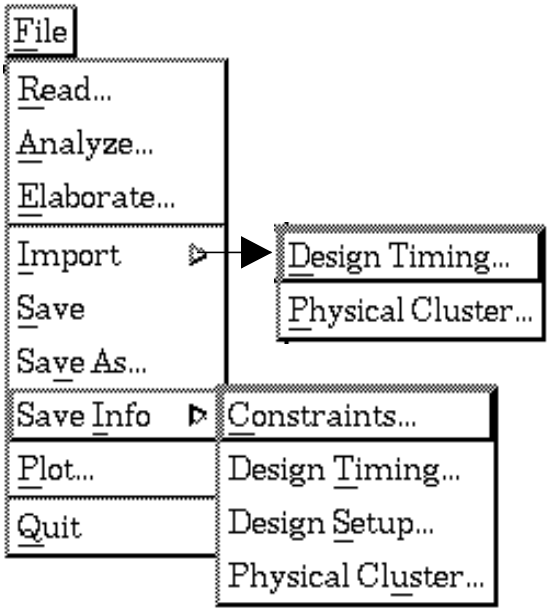


Table 4-1 and the following sections explain how to use the items in the File menu.

Table 4-1 File Menu Options

Option	Action	Equivalent Command
Read	Reads in one or more design description files	read
Analyze	Reads in HDL source file and creates HDL library objects	
Elaborate	Creates a design from the intermediate format of a Verilog module, a VHDL entity, or a VHDL configuration	
Import	Imports design timing or physical cluster information	

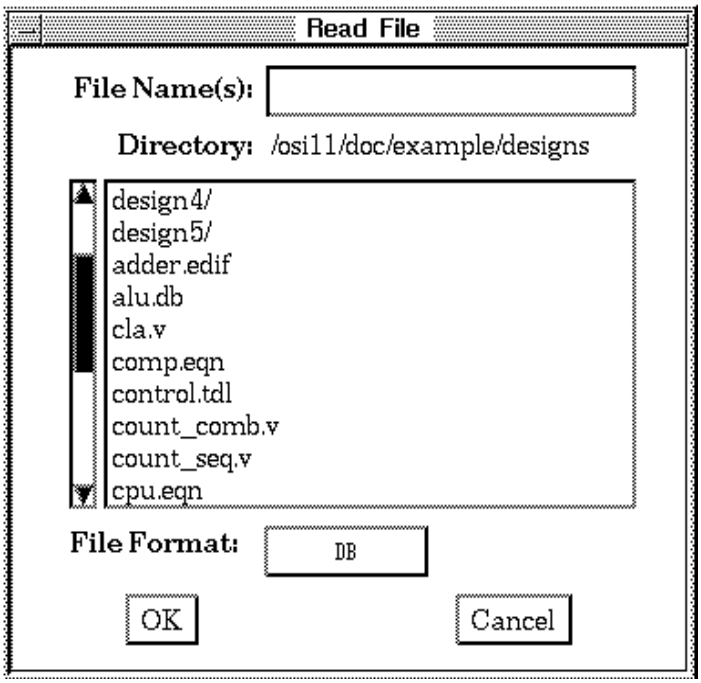
Table 4-1 File Menu Options (Continued)

Option	Action	Equivalent Command
Save	Saves the current design in Synopsys internal database (db) format as a file named design_name.db	write [-format db] -hierarchy
Save As	Saves selected designs or the design currently viewed under any file name	write [-format file_format] [-hierarchy] [-output output_filename]
Save Info	Writes timing or design setup information	
Plot	Writes a design symbol schematic view to a file or printer in PostScript format	plot
Quit	Closes a Design Analyzer window	exit, quit

Read

When you choose Read from the File menu, you see the Read File dialog box shown in Figure 4-2.

Figure 4-2 Read File Dialog Box



Click OK to read in the chosen File Name in the current File Format. Click Cancel to remove this dialog box without reading in a file.

File Name(s) and Directory

Type one or more file names in the File Names text box, separated by commas or spaces. If you type more than one file name, the files must be in the displayed Directory list and in the same format.

You can also choose file names by moving through directories, then clicking on the displayed name, as described in Chapter 1, “Design Analyzer Overview.” Clicking a file name with the left mouse button replaces the displayed file name with the file name you clicked. Clicking a file name with the middle mouse button adds that file name to the displayed set of file names. If you select more than one file name, they must all have the same format.

If you type a single name in the text box and that file name is not in the current directory, Design Analyzer searches for it in the Search Path directory. See Chapter 3, “Setup Menu,” for more information.

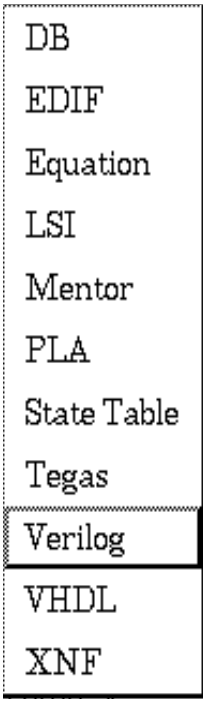
The name in the File Names text box is relative to the displayed Directory (in Figure 4-2, /osi11/doc/example/designs) unless you type a full path name or unless the name resides in the Search Path directory.

File Format

If you graphically select a file name, the File Format option menu automatically reflects the format corresponding to the selected design description file’s suffix. For example, a file name ending in .st is assumed to be in State Table format. Choose a different output format from the File Format option menu if needed.

If you type the file name, you must select the appropriate output format from the File Format option menu. Figure 4-3 shows the File Format option menu.

Figure 4-3 File Format Option Menu

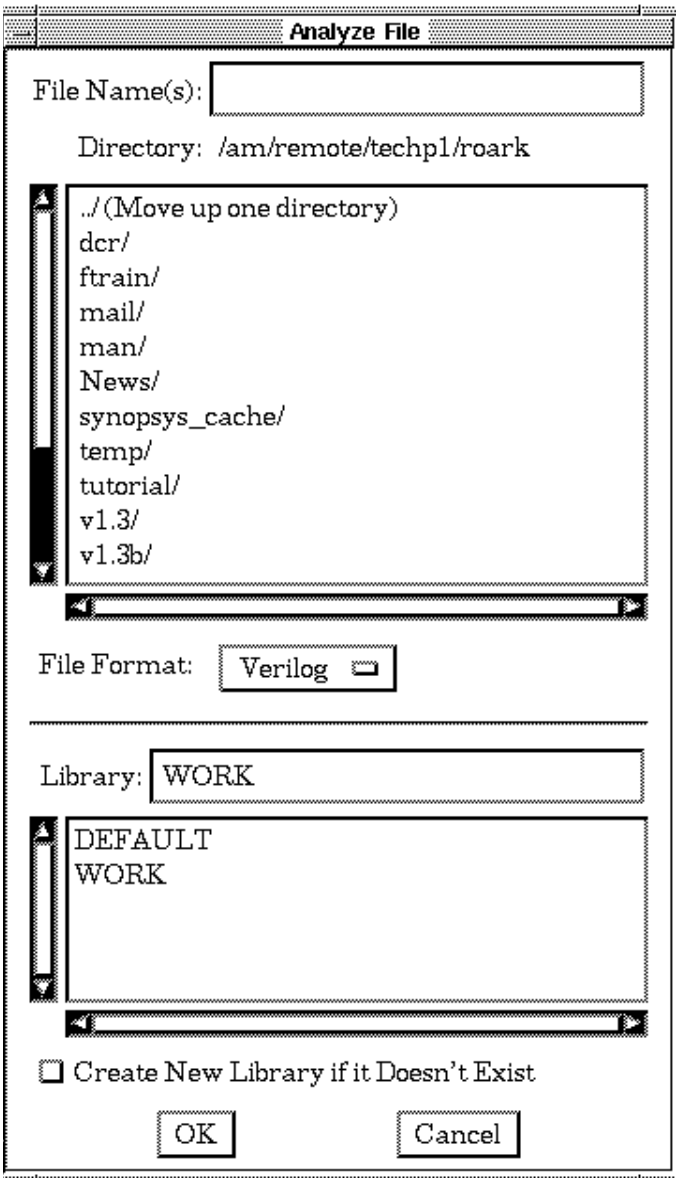


Your site licenses determine the available set of input formats.

Analyze

When you choose Analyze from the File menu, you see the Analyze File dialog box shown in Figure 4-4. After you make a change to an HDL source file, use the Analyze File dialog box to read in the file and check for errors.

Figure 4-4 Analyze File Dialog Box



The top portion of the Analyze File dialog box looks like the File > Read dialog box. However, only VHDL and Verilog files display in this file list. You use the File Format option menu below the files list to select VHDL or Verilog as the type of file you want to analyze.

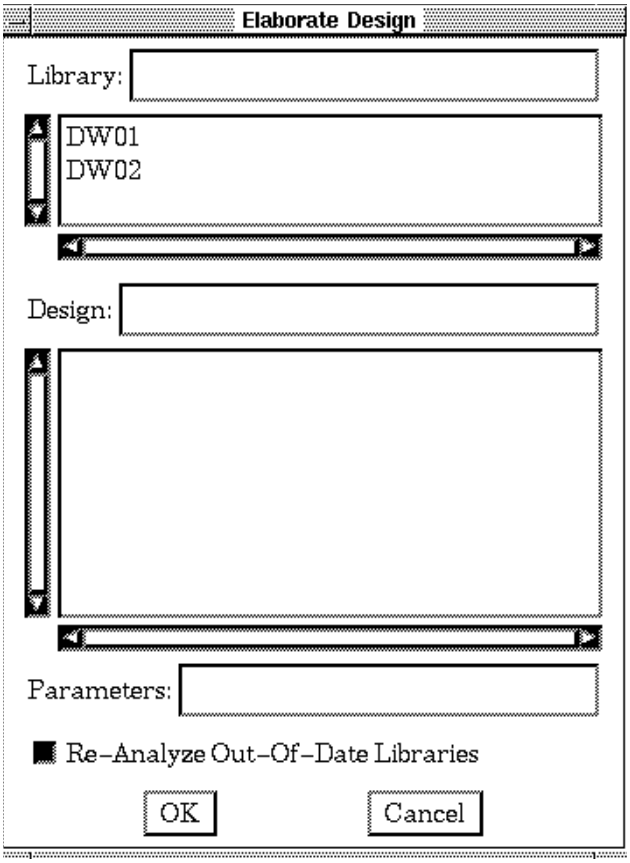
In the lower half of the dialog box, select the HDL library you want to use with the Analyze command. The WORK library is the default, and other available design libraries are displayed in the library list.

When you click OK, a report output window appears and displays messages.

Elaborate

When you choose Elaborate from the File menu, you see the Elaborate Design dialog box shown in Figure 4-5.

Figure 4-5 Elaborate Design Dialog Box



In the Elaborate Design dialog box, select a library from the library list. The Design list automatically fills in. You can select any design from the design list. The Parameters field automatically fills in if there are any parameters. You can edit this line to change the default parameter specification. Deselect the toggle button Re-Analyze Out-of-Date Libraries to prevent Design Analyzer from reanalyzing out-of-date libraries.

When you click OK, a report output window appears and displays messages from the Elaborate command. If the Elaborate command is successful, design icons appear in the Design Analyzer window.

Import

Figure 4-6 shows the Import submenu.

Figure 4-6 Import Submenu

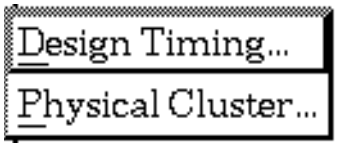


Table 4-2 and the following sections explain how to use the items in the Import submenu.

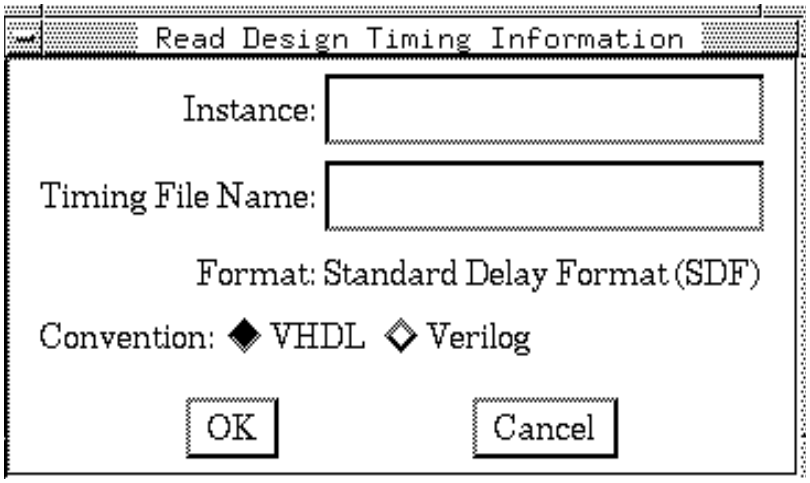
Table 4-2 Import Submenu Options

Option	Action	Equivalent Command
Design Timing	Use this dialog box to read and annotate design leaf cell and net timing information from a disk file onto the current design.	read_timing [-format sdf] [-design design_name] [-path path_name] [-context vhdl | verilog]
Physical Cluster	Use this dialog box to read in and annotate the physical cluster hierarchy associated with a design.	read_clusters cluster_file_name

Design Timing

Figure 4-7 is enabled whenever you have a fully mapped netlist defined as the current design. The timing file must be in SDF format.

Figure 4-7 Read Design Timing Information Dialog Box



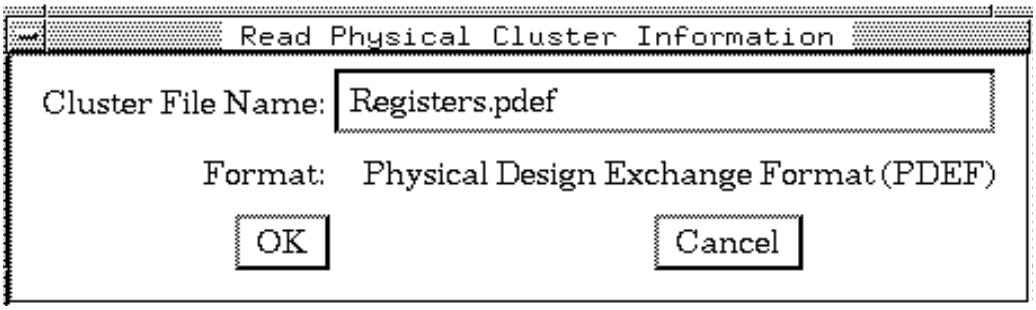
Use the Instance text field to specify an instance as the source of timing information. When reading the timing for a subdesign, you cannot annotate the net delays to the ports of the subdesign. Instance-specific pin-to-pin cell and net delays read from the file indicated in the Timing File Name text field and annotate on the current design. Select the appropriate Convention button to indicate the context for which the timing file is created.

Click OK to select the indicated information. Click Cancel to remove this dialog box without importing timing information.

Physical Cluster

Figure 4-8 is enabled only if you have a Floorplan-Management license available. The physical cluster hierarchy represents the partitioning of the cells in a design on a physical chip, and guides the reoptimize_design command in making convergent optimizations to the design.

Figure 4-8 Read Physical Cluster Information Dialog Box



Click OK to select the file shown in the Cluster File Name text field. Click Cancel to remove this dialog box without importing physical cluster information.

Save

The Save selection becomes available when you select or view a design. Save writes the current design and its subdesigns in Synopsys internal database format (.db) only. Use File > Save As to save the current design and its subdesigns under another file name or another output format.

Save As

Figure 4-9 shows the Save As dialog box.

Figure 4-9 Save Design Dialog Box

Click OK to save the current design (or the selected designs in Designs View) in the chosen File Name in the current File Format. Click Cancel to remove this dialog box without saving the selected designs.

You can use this file selection to view existing design file names in a selected directory.

File Name

Type a file name in this text box.

To choose a file name,

1. Scroll through directories.

2. Click on the displayed name.

Chapter 1, “Design Analyzer Overview” also describes how to choose a file name.

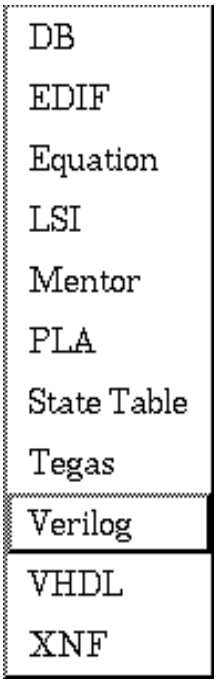
The name in the File Name field is relative to the displayed Directory (in Figure 4-9, /osi11/doc/example/designs) unless you enter a full path name.

File Format

If you graphically select a file name, the File Format option menu automatically reflects the format corresponding to the selected design description file’s suffix. For example, a file name ending in .st is assumed to be in State Table format. You can choose a different output format from the File Format option menu.

If you type the file name, you must select the appropriate file format from the option menu. When you select File Format from the Save Design dialog box, you see the File Format option menu shown in Figure 4-10.

Figure 4-10 File Format Option Menu



Your site licenses determine the available set of file formats.

Save All Designs in Hierarchy

The Save All Designs in Hierarchy option is relevant only when the selected designs are hierarchical. Enable the Save All Designs in Hierarchy button to save the selected designs and all subdesigns in the chosen File Name, in the current File Format. The equivalent command for this selection is write -hierarchy.

Save Info

When you choose Save Info from the File menu, you see the Save Info submenu shown in Figure 4-11.

Figure 4-11 Save Info Submenu

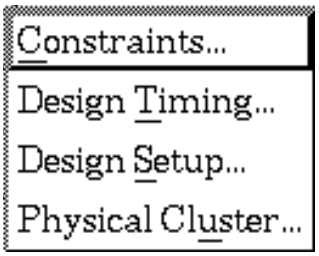


Table 4-3 and the following sections explain how to use the items in the Save Info submenu.

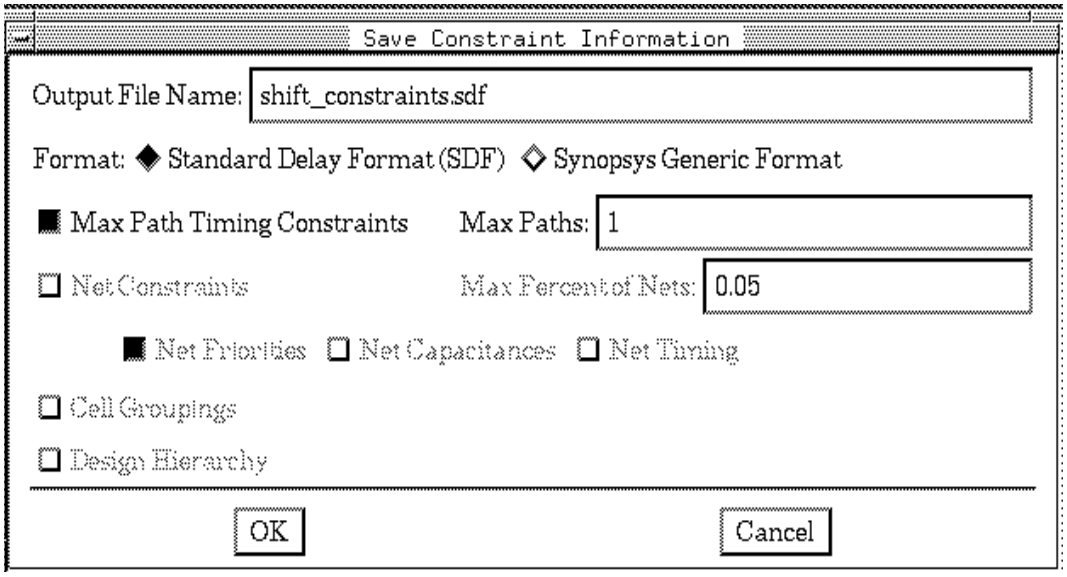
Table 4-3 Save Info Submenu Options

Option	Action	Equivalent Command
Constraints	Writes constraints from current design to a disk file	write_constraints [-format sdf | synopsys] [-max_path_timing] [-max_paths number] [-max_net number] [-by_input_pin_name] [-by_output_pin_name]
Design Timing	Writes leaf cell pin-to-pin timing information to a disk file	write_timing [-format format_name] [-design design_name] [-output file]
Design Setup	Saves the design attribute to the file name that you specify	write_script
Physical Cluster	Writes the physical cluster information annotated to a design to a disk file (only available if you have a Floorplan-Management license)	write_clusters [-output new_cluster_file_name]

Constraints

Use the dialog box shown in Figure 4-12 to write constraints for the current design to a disk file. This dialog box is always enabled.

Figure 4-12 Save Constraint Information Dialog Box



To save constraint information, enter a file name in the text box and select the write_constraints parameters you want to use.

Format

The SDF format is the default. The net constraints, cell groupings, and design hierarchy options are not available with the SDF format. If you select the Synopsys Generic Format, you can choose any of the options.

Max Path Timing Constraints

The default, Max Percent of Nets, is .05, meaning that 5 percent of all nets write to the constraints file. The Max Paths field defines the maximum number of timing paths selected. By default, one path is selected.

Net Constraints

If you select Net Constraints, the Net Priorities button is enabled by default. Use the Net Priorities, Net Capacitances, and Net Timing buttons to change the options.

Net Priorities

If you select Net Priorities, the nets along the selected paths are assigned a priority ranging between the minimum net priority and the maximum net priority. Design Compiler assigns net priorities on the basis of the difference between the required and actual arriving times at the endpoints of the selected path.

Net Capacitances

If you select Net Capacitances, the capacitance of each net along the selected paths is written.

Net Timing

If you select Net Timing, the actual delay for each net on the selected paths is written.

Cell Groupings

If you select Cell Groupings, the cells with the group_name attribute are written.

Design Hierarchy

If you select Design Hierarchy, all of the cells in each design hierarchy write to the constraints file.

To save constraint information,

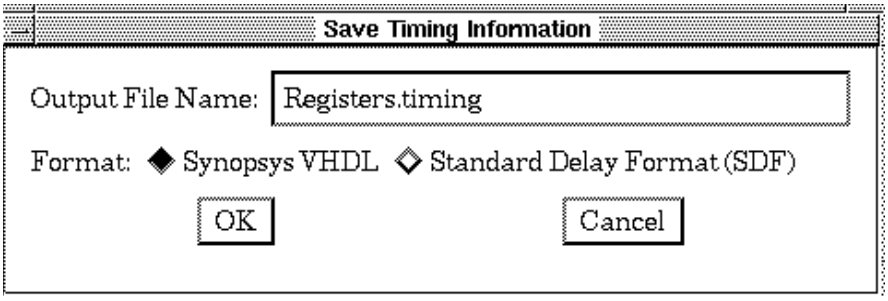
1. Type the output file name in the text box.
2. Select the format and options.
3. Click OK.

Click Cancel to remove this dialog box without writing constraint information.

Design Timing

When you choose Design Timing from the Save Info submenu, you see the Save Timing Information dialog box shown in Figure 4-13.

Figure 4-13 Save Timing Information Dialog Box



To save timing information,

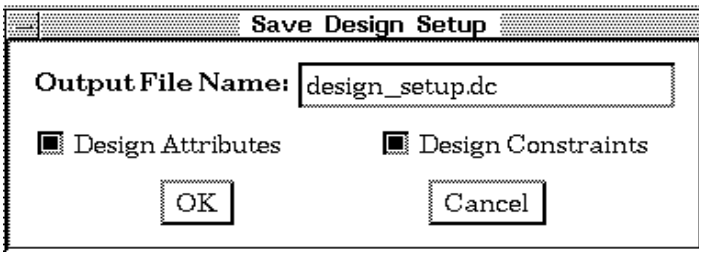
1. Type the file name in the text box.
2. Select the format.
3. Click OK.

You can write the timing information in Synopsys VHDL or SDF format; Synopsys VHDL is the default. Click Cancel to remove this dialog box without saving timing information.

Design Setup

When you choose Design Setup from the Save Info submenu, you see the Save Design Setup dialog box shown in Figure 4-14.

Figure 4-14 Save Design Setup Dialog Box



To save the design setup,

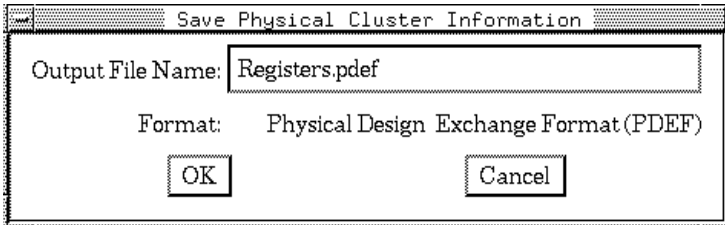
1. Type the file name in the text box.
2. Enable or disable Design Attributes and Design Constraints.
3. Click OK.

Click Cancel to remove this dialog box without saving setup information.

Physical Cluster

When you choose Physical Cluster from the Save Info submenu, you see the Save Physical Cluster Information dialog box shown in Figure 4-15.

Figure 4-15 Save Physical Cluster Information Dialog Box



To save physical cluster information,

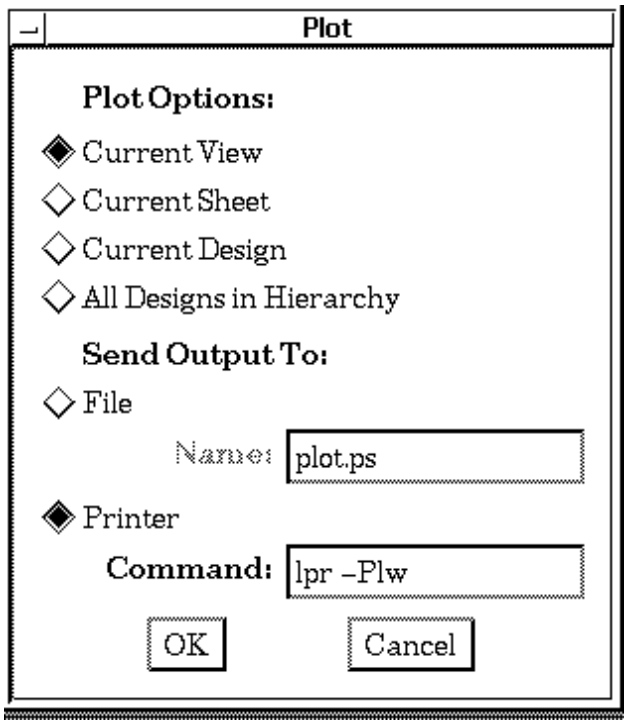
1. Type the output file name in the text box.
2. Click OK.

Click Cancel to remove this dialog box without writing the cluster information.

Plot

When you choose Plot from the File menu, you see the Plot dialog box shown in Figure 4-16.

Figure 4-16 Plot Dialog Box



Click OK to plot the design's schematic to the chosen file or printer. Click Cancel to remove this dialog box without plotting.

The selection in Plot Options plots symbols or any part of the schematic; you cannot plot a Hierarchy View or Design View.

Current View

Plots the currently visible symbols or portion of the schematic. Use this option when you zoom into a region.

Current Sheet

Plots the current sheet of the schematic or symbol. A large schematic can have more than one sheet; To change sheets, use View > Change Sheet.

Current Design

Plots the symbol view or the entire schematic, which can have more than one sheet.

All Designs in Hierarchy

Plots the symbols or the entire schematic, including subdesigns.

Only designs that have generated schematics can use the plot option. Design Analyzer generates schematics only for designs you viewed. To create schematics for the current design and all its subdesigns, type create_schematic -all in the Command Window (Setup > Command Window).

File

Writes the PostScript plot to the file name shown in the Name text box. You can type any file name in this text box; a typical suffix is .ps or .plot. Schematics write in PostScript format.

Printer

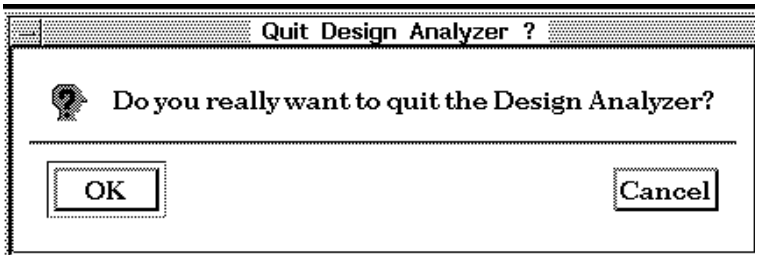
Uses the command in the Command text box to plot the schematic to a PostScript printer. The default command is the value of the plot_command variable set by Setup > Variables.

The lpr command is the UNIX command to print a file to a printer; its -P option names the printer.

Quit

Figure 4-17 shows the Quit Design Analyzer dialog box, which corresponds to the Quit information in Table 4-1. If only one Design Analyzer window is open, this selection also exits Design Analyzer.

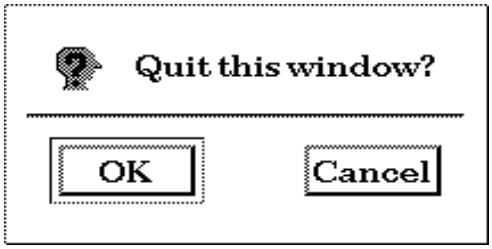
Figure 4-17 Quit Design Analyzer Dialog Box (Single Design Analyzer Window)



Click OK to quit Design Analyzer. Click Cancel to remove this dialog box.

When multiple Design Analyzer windows are open, you see the Quit dialog box shown in Figure 4-18. This Quit selection closes only the calling Design Analyzer window.

Figure 4-18 Quit Dialog Box



5

Edit Menu

This chapter contains a summary of the Edit menu and the submenus and dialog boxes you can access through it.

Use the Edit menu to

- Delete
- Insert Pads
- Select
- Unselect All
- Group
- Ungroup
- Uniquify
- Reset

When you choose Edit from the menu bar, you see the Edit menu and its submenus shown in Figure 5-1.

Figure 5-1 Edit Menu and Submenus

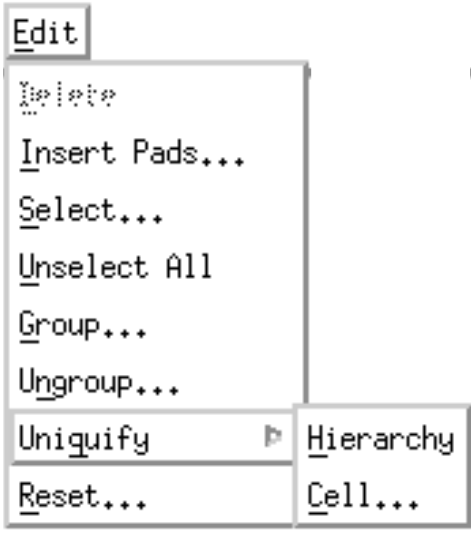


Table 5-1 and the following sections explain how to use the options in the Edit menu.

Table 5-1 Edit Menu Options

Option	Action	Equivalent Commands
Delete	Deletes the currently selected clocks or design icons.	remove_clock clock_name, remove_design (designs)
Insert Pads	Displays the Insert Pads dialog box. Refer to the “FPGA Compiler” section in Chapter 9, for a description.	insert_pads
Select	Selects objects by name, by type, and optionally by values; shows the total number of selected objects.	
Unselect All	Unselects all selected objects in all designs.	

Table 5-1 Edit Menu Options

Option	Action	Equivalent Commands
Group	Groups all currently selected cells.	group -design_name design_name
Ungroup	Ungroups all the currently selected cells.	ungroup
Uniquify	Makes unique all or some of the subdesigns in the current design.	
Reset	Resets the current design.	reset_design

Delete

You enable the Delete menu item when you select a design in the Symbol view or a clock in the Symbol or Schematic View. When you choose Delete, you delete the currently selected clocks or design icons.

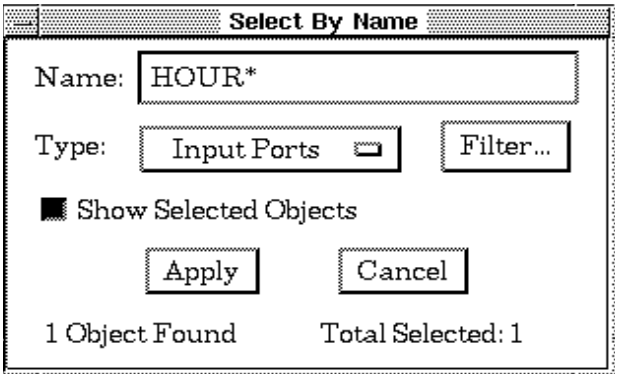
Insert Pads

When you choose Insert Pads from the Edit menu, you see the Insert Pads dialog box as shown in Figure 9-12. See the "FPGA Compiler" section in Chapter 9, for instructions about this dialog box.

Select

When you choose Select from the Edit menu, you see the Select By Name dialog box shown in Figure 5-2.

Figure 5-2 Select by Name Dialog Box



The example Select By Name dialog box shown in Figure 5-2 indicates that one input port whose name begins with HOUR was found and selected, bringing the total of selected objects to 1.

When you click Apply, Design Analyzer displays the number of objects found and updates the total number of selected objects. Click Cancel to remove this dialog box.

Table 5-2 explains how to use the options in the Select By Name dialog box.

Table 5-2 Select By Name Dialog Box Options

Option	Action	Equivalent Command
Name	Type the name of the object or objects you want in the text box. The wildcard character, * (an asterisk), can be used to match any number of characters. It can also be used by itself to match all names.	
Type	Open the Option menu and choose Input Ports, Output Ports, I/O Ports, Cells, Pins, or Nets.	find
Filter	Click the Filter button to open the Select Filter dialog box. Use this dialog box to filter the list of names that match the values in the Name and Type text boxes.	filter

Table 5-2 Select By Name Dialog Box Options

Option	Action	Equivalent Command
Show Selected Objects	Use this button to zoom in on all selected objects.	

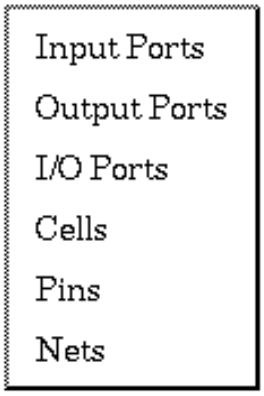
Name

You can type the name of the object or objects you want in the Name text box. The wildcard character matches all names.

Type

When you open the Type option menu, you can choose one of the menu items shown in Figure 5-3.

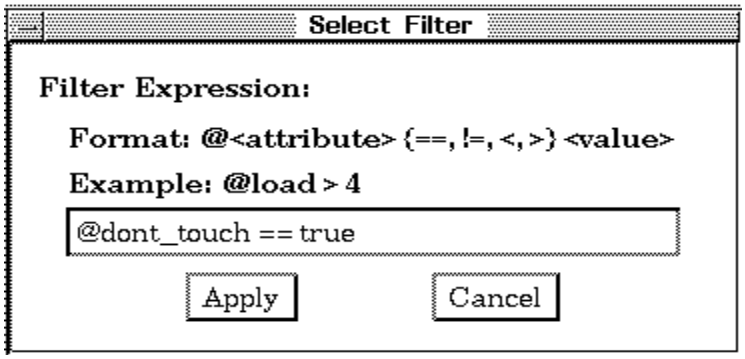
Figure 5-3 Type Option Menu



Filter

When you click the Filter button, you see the Select Filter dialog box shown in Figure 5-4.

Figure 5-4 Select Filter Dialog Box



The filter expression is a logical combination of attribute relationships. The example filter expression in Figure 5-4 allows any selected object whose dont_touch attribute is true. The dialog box describes filter expressions and lists all default attribute names and values. You can also use user-defined attributes in filter expressions.

Click Apply to perform the filter operation. Click Cancel to remove this dialog box and return to the Select By Name dialog box.

Show Selected Objects

When you enable the Show Selected Objects button, you zoom in on all selected objects.

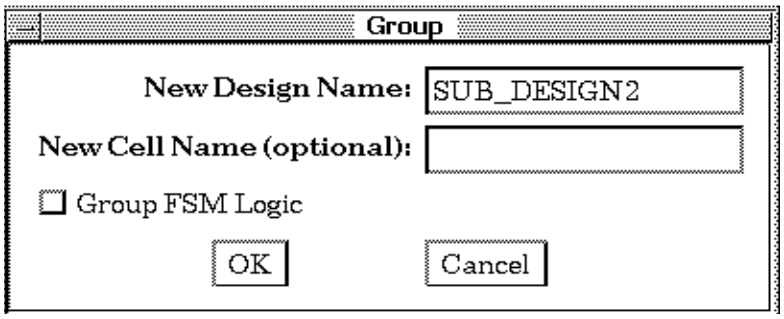
Unselect All

When you choose Unselect All from the Edit menu, you unselect all selected objects in all designs. To unselect only objects selected in the current sheet of the current view, click the left mouse button on the background. To clear highlighting, use Analysis > Highlight > Clear.

Group

When you choose Group from the Edit menu, you see the Group dialog box shown in Figure 5-5. You can select objects graphically with the mouse or by using Edit > Select.

Figure 5-5 Group Dialog Box



To group the selected objects,

1. Type the new design name in the text box.
2. Click OK.

Click Cancel to remove this dialog box.

Table 5-3 explains how to use the options in the Group dialog box.

Table 5-3 Group Dialog Box Options

Option	Action	Equivalent Command
New Design Name	Type the new design name.	
New Cell Name (optional)	Type the new design's cell name in the box; this is optional. If you do not enter a cell name, a unique name is automatically generated in the Unnn format.	group -cell_name cell_name

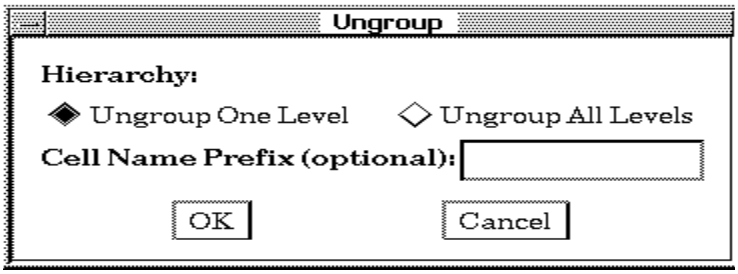
Table 5-3 Group Dialog Box Options

Option	Action	Equivalent Command
Group FSM Logic	Click this option after you select a flip-flop or latch, to group together all cells in the transitive fan-in and fan-out of the selected cells, which then creates an FSM design.	group -fsm, set_fsm_state_vector

Ungroup

When you choose Ungroup from the Edit menu, you see the Ungroup dialog box shown in Figure 5-6.

Figure 5-6 Ungroup Dialog Box



You can select objects graphically with the mouse or by using Edit > Select.

Table 5-4 explains how to use the options in the Ungroup dialog box.

Table 5-4 Ungroup Dialog Box Options

Option	Action	Equivalent Com-mand
Ungroup One Level	Ungroups just the selected cells' first level of subdesigns.	ungroup

Table 5-4 Ungroup Dialog Box Options

Option	Action	Equivalent Command
Ungroup All Levels	Recursively ungroups all the selected cells' subdesigns and their subdesigns.	ungroup -flatten
Cell Name Prefix (optional)	Type a prefix value that is added to the beginning of each ungrouped cell's name.	ungroup -prefix

Uniquify

Figure 5-7 shows the Uniquify submenu.

Figure 5-7 Uniquify Submenu

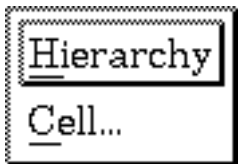


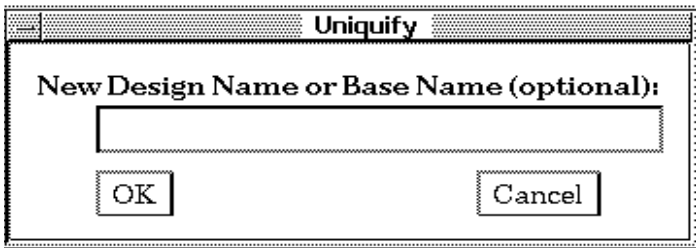
Table 5-5 explains how to use the options in the Uniquify submenu.

Table 5-5 Uniquify Submenu Options

Option	Action	Equivalent Command
Hierarchy	Makes unique all subdesigns in the current design	uniquify
Cell	Becomes available when you select one or more hierarchical cells and makes unique the currently selected cells, optionally specifying how they should be renamed	uniquify -new_name -base_name

Figure 5-8 shows the Uniquify dialog box.

Figure 5-8 Uniquify Dialog Box



You can select cells graphically with the mouse or by using Edit > Select.

Click OK to uniquify the selected cells. Click Cancel to remove this dialog box.

If you select one cell, type a new design name for the uniquified cell in the New Design Name or Base Name (optional) text box.

If you select two or more cells, type a base name used to generate a new name for each uniquified cell. A new cell name generates by concatenating a unique number onto the base name, as specified by the uniquify_naming_style variable (set with the Setup > Variables dialog box).

If you do not specify a name, each uniquified cell's name generates by concatenating a unique number onto the existing cell name, as specified by the uniquify_naming_style variable.

Reset

When you choose Reset from the Edit menu, you reset the current design.

6

View Menu

This chapter describes all the items in the View menu and the submenus and dialog boxes you can access through it.

Use the View menu to change the current view of a design or schematic. With this menu, you can

- Full View
- Zoom In
- Zoom Out
- Change Sheet
- Change View
- Change Level
- Push to Reference

- New View
- Style
- Refresh
- Recreate

When you open the View menu, you can access the menu items and submenus shown in Figure 6-1.

Figure 6-1 View Menu and Submenus

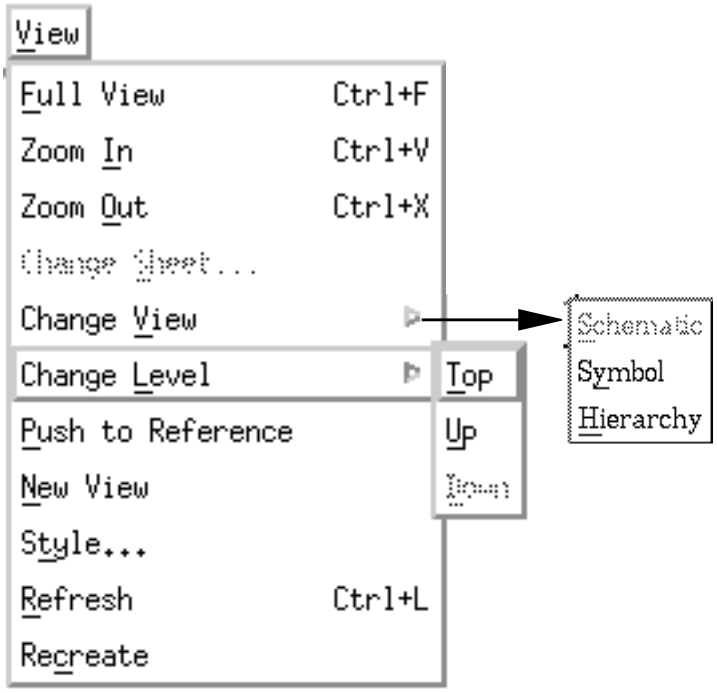


Table 6-1 and the following sections explain how to use the options in the View menu.

Table 6-1 View Menu Options

Option	Action	Equivalent Command or Short-cut
Full View	Resets the current magnification factor and redraws the current schematic sheet to fit in the current window.	Press Control-f.
Zoom In	Doubles the displayed size of a symbol or schematic, providing a close-up view of the central part.	Press Control-v.
Zoom Out	Zooms the display out by a factor of 2.	Press Control-x.
Change Sheet	Views different sheets of a multiple-sheet schematic.	Double-click a sheet number to see that sheet.
Change View	Allows you to change the current view of a design among Hierarchy View, Symbol View, and Schematic View.	Use the buttons on the left side of the Design Analyzer window.
Change Level	Allows you to move between levels of a hierarchical design.	current_design = design_name current_instance = instance_name
Push to Reference	Sets the current design to the design referenced by the selected instance.	
New View	Creates a duplicate copy of the current Design Analyzer window, viewing the same database.	
Style	Changes the values of the various drawing layers.	set_layer
Refresh	Refreshes the Design Analyzer's window. Just repaints the window; View > Recreate recreates the current view from the database.	Press Control-l.

Table 6-1 View Menu Options (Continued)

Option	Action	Equivalent Command or Short-cut
Recreate	Recreates the current view from the database using the current parameters.	

Full View

When you choose Full View from the File menu, you can reset the current magnification factor.

Zoom In

Graphically set the zoom region and magnification by using the pop-up menu's Zoom selection (or press Control-z), then drag a rectangle around the area. The Zoom In submenu is disabled during Designs and Hierarchy View.

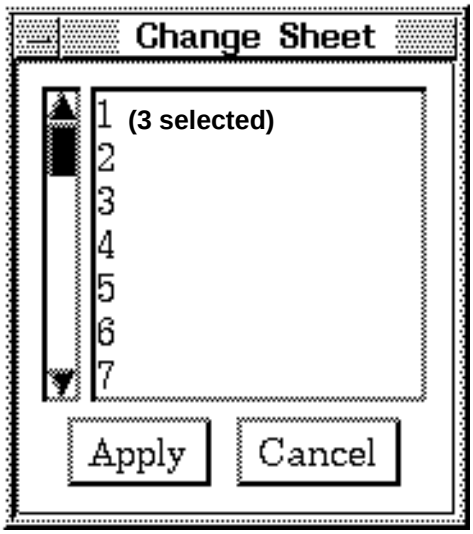
Zoom Out

The Zoom Out option is disabled in the Designs and Hierarchy View.

Change Sheet

If objects are selected on a sheet, the number of selected objects appears in parentheses next to the sheet number. The Change Sheet option becomes available only when viewing a design with a multiple-sheet schematic in Schematic View. Figure 6-2 shows the Change Sheet dialog box.

Figure 6-2 Change Sheet Dialog Box

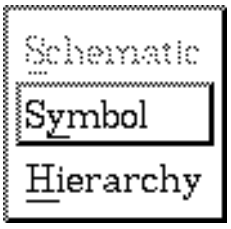


Choose a sheet number, then click Apply to see that sheet. Click Cancel to remove this dialog box.

Change View

When you select Change View from the View menu, you see the Change View submenu shown in Figure 6-3.

Figure 6-3 Change View Submenu



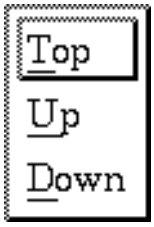
The name of the current view is disabled (grayed out). If the current design has no hierarchy, the Change View submenu's Hierarchy selection is disabled.

You can also use the view buttons on the left side of the Design Analyzer Window to change your view.

Change Level

When you select Change Level from the View menu, you see the Change Level submenu shown in Figure 6-4.

Figure 6-4 Change Level Submenu



Top

The Top submenu moves you to the top of the current design.

Up

The Up submenu moves you up one level of hierarchy. This selection is available when the current instance is part of a larger design.

Down

The Down submenu moves you down one level of hierarchy into a subdesign. This selection is available when a single subdesign is selected.

You can also use the level buttons on the left side of the Design Analyzer Window.

Push to Reference

Push to Reference sets the current design to the design referenced by the selected instance.

New View

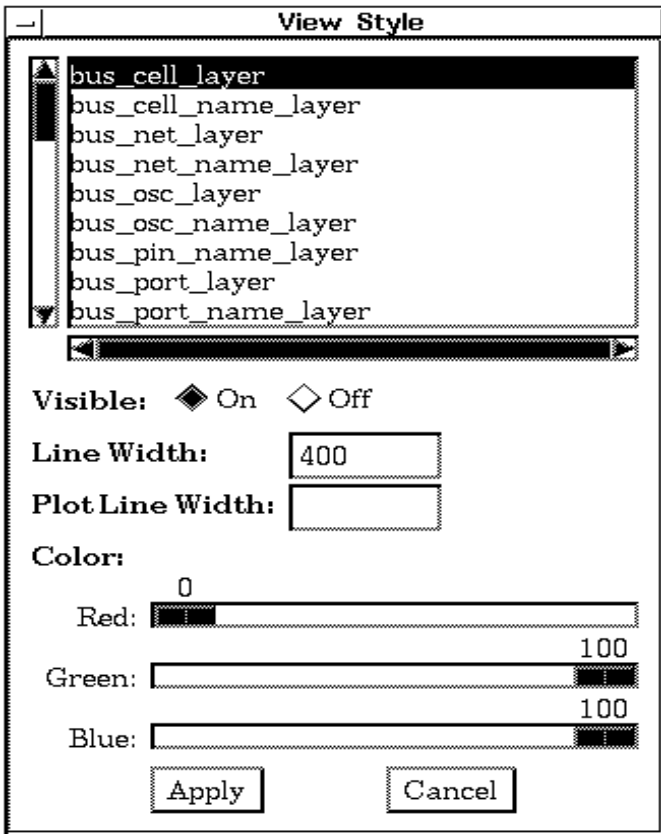
Any changes made to a given database reflect in all Design Analyzer windows viewing that database. The New View option is useful for viewing different views of a design at the same time.

To close a Design Analyzer window, use File > Quit.

Style

Figure 6-5 shows the View Style dialog box.

Figure 6-5 View Style Dialog Box



Click Apply to change the selected layer to the displayed values. Click Cancel to remove this dialog box.

Each layer represents some type of graphic information. For example, cell_layer shows the outline of each cell in a schematic, cell_name_layer shows each cell's name (such as U45), and cell_ref_name_layer shows each cell's reference name (such as AND3).

Layer Name List

Click the layer name whose values you want to see or change. Use the scroll bars as necessary.

To create a new layer, use the set_layer command from the Command Window's command line. Layers that you create will not appear in the View Style list.

Visible

Click On to make the selected layer visible. Click Off to make the selected layer invisible.

Line Width

Type the line width you want in pixel equivalents.

Plot Line Width

If you want a different plot line width from the line width displayed on your screen, type the plot line width in this text box. If you leave the Plot Line Width field empty, the plot line width is the same as Line Width.

Color

Drag the sliders to the color saturation you want for Red, Green, and Blue. A value of 0 indicates no color, while a value of 100 indicates full saturation. Black corresponds to 0,0,0, and white corresponds to 100,100,100.

For example, to make the selected layer bright purple, set both Red and Blue to 100, and set Green to 0.

The colors displayed depend on your workstation's palette.

Refresh

The Refresh option refreshes the Design Analyzer's window.

Recreate

The Recreate option recreates the current view from the database using the current parameters.

7

Attributes Menu

This chapter describes all the items in the Attributes menu and the submenus, and dialog boxes you can access through it.

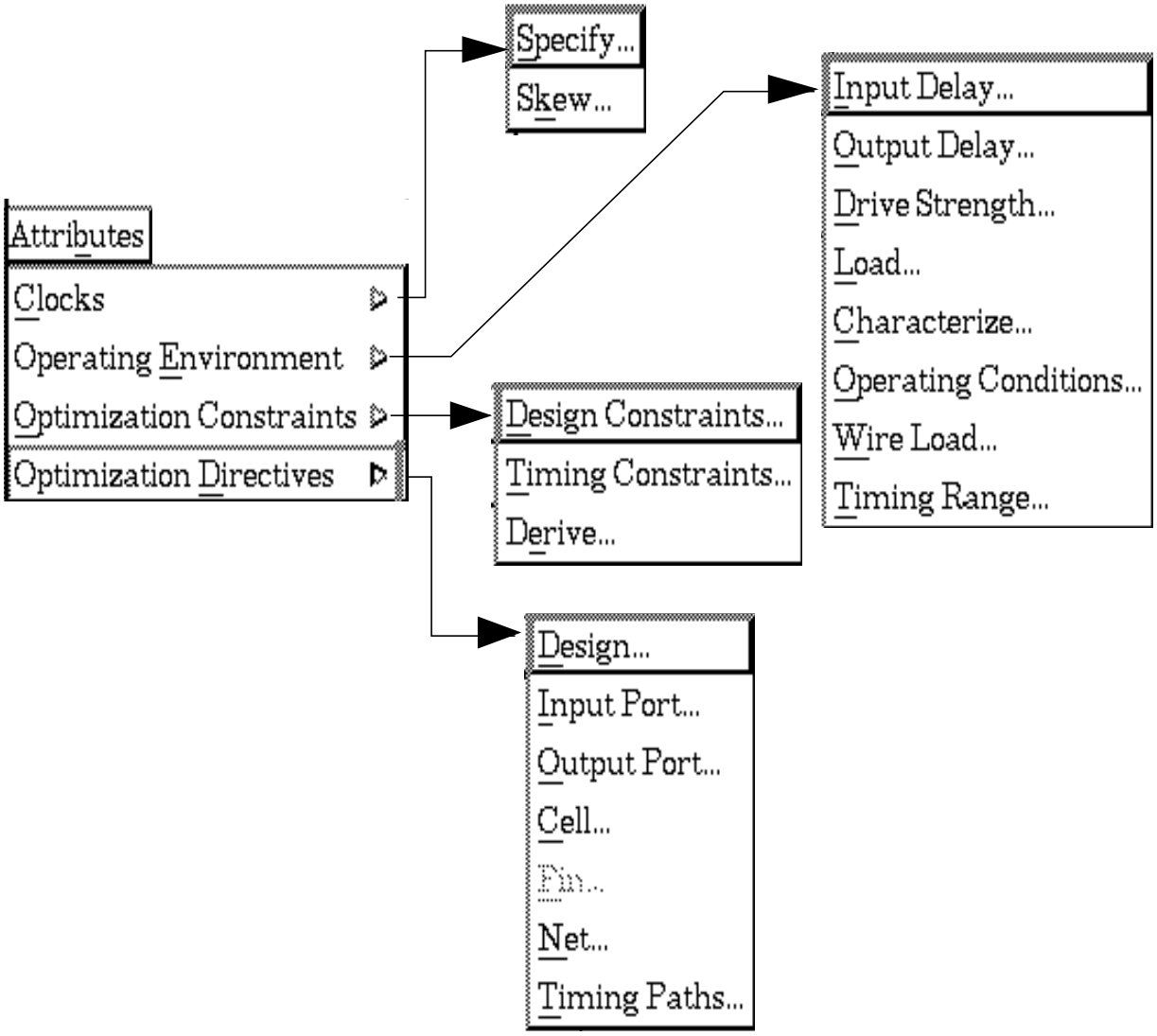
Use the Attributes menu to see and change attribute values for selected objects. This menu has four sections:

- Clocks
- Operating Environment
- Optimization Constraints
- Optimization Directives

The order of these sections reflects a typical flow for setting attributes for a design.

When you open the Attributes menu, you can access the menu items and submenus shown in Figure 7-1.

Figure 7-1 Attributes Menu and Submenus



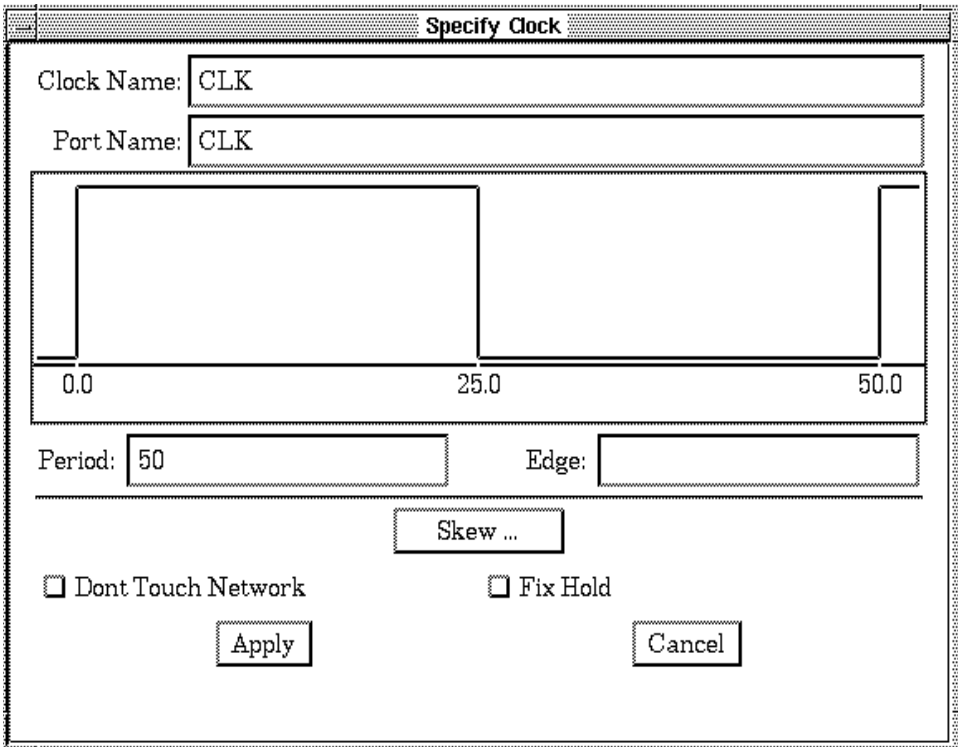
Clocks

Use the Clocks menu to see and change the values of a clock's attributes.

Specify

You can select an input port or pin before or after displaying the Specify Clock dialog box as shown in Figure 7-2. If you select an object that is not the clock source but is on the clock network, the waveform appears but with the Apply button inactive (grayed out). In this case, a line of text below the Don't Touch Network button displays the polarity of the clock at the selected object.

Figure 7-2 Specify Clock Dialog Box



Click Apply to set the values as shown. Click Cancel to remove this dialog box.

Table 7-1 and the following sections explain how to use the options in the Specify Clock dialog box.

Table 7-1 Specify Clock Dialog Box Options

Option	Action	Equivalent Command
Clock Name	Displays the clock's name, if you selected one	
Port Name	Displays the name of the object connected to the clock	
Don't Touch Network	Preserves the clock fanout network during compilation	set_dont_touch_network
Fix Hold	Creates hold constraints for the current clocks in the design	set_fix_hold
Message Area	Displays messages pertaining to the waveform above the Apply and Cancel buttons	
Skew	Sets skew attributes on a\ clock	set_clock_skew [-ideal | -rise_delay number | -fall_delay number | -plus_uncertainty | -minus_uncertainty]

The following sections provide additional information about the selections available in the Specify Clock dialog box.

Clock Name

If you select more than one clock, the Clock Name field shows the name of the last clock selected. If you select an object that is not a clock, the name of the object appears in the Clock Name field. Entered values are set for all selected clocks.

Port Name

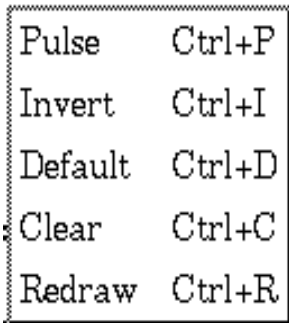
Design Compiler Reference Manual: Fundamentals describes clocks and clock objects.

The clock waveform appears below the Port Name field. The default waveform has a half duty cycle pulse with a rising edge at time 0 and a falling edge at time T/2, where T is the clock period. You edit the waveform by selecting a clock edge with the left mouse button, then dragging this edge to the location you want on the time axis. A scale below the waveform displays the time at each edge. If you want to define an edge more accurately, enter a smaller edge transition time in the Edge field. The number you enter applies to the selected edge.

The default waveform appears even if there is no clock associated with the selected object.

You display the waveform display pop-up menu by pressing the third mouse button with the cursor in the waveform display area. Figure 7-3 shows the menu selections.

Figure 7-3 Waveform Display Pop-up Menu



Pulse

Creates a pulse where the mouse button is pressed. You can also create a pulse by double-clicking the middle mouse button.

Invert

Inverts the waveform.

Default

Reverts to a 50 percent duty cycle default waveform.

Clear

Clears the waveform and creates a straight line at logic level 0.

Redraw

Redraws the waveform.

Don’t Touch Network

Preserves the clock fanout network during compilation.

Fix Hold

Creates the hold constraints for the current clocks in the design.

Message Area

Displays messages pertaining to the waveform above the Apply and Cancel buttons.

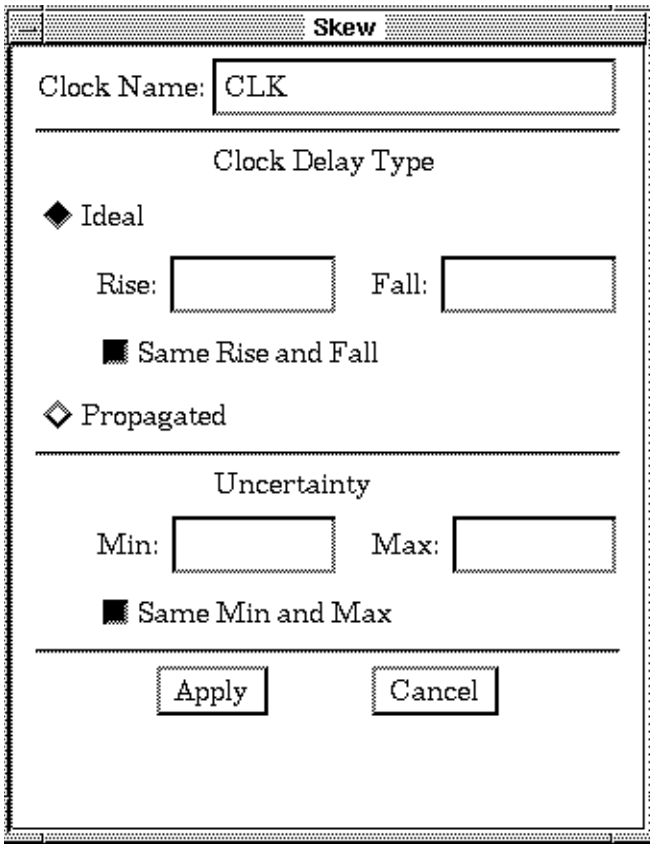
Skew

You can display this dialog box from Specify Clock dialog box (Attributes > Clocks > Specify) or the Attributes menu. The following section describes the Skew option further.

Skew

When you choose Clocks from the Attributes menu, then choose Skew from the submenu, you see the Skew dialog box shown in Figure 7-4. You can also click the skew button in the Specify Clock dialog box.

Figure 7-4 Skew Dialog Box



Enable the Ideal button to specify an ideal clock network. Enable the Propagated button to propagate clock delay times through the network. The default is Ideal. When Same Rise as Fall is toggled on, the Rise and Fall text boxes display the same text, so you do not have to type the same number twice. The same principle applies to the Same Min and Max button.

Clock Name

Displays the clock name.

Rise

Type the clock rise time into this box.

Fall

Type the clock fall time into this box.

Min

Type the minimum clock uncertainty into this box.

Max

Type the maximum clock uncertainty into this box.

After entering your selections, click Apply or Cancel.

Operating Environment

Use this menu to set constraints and define the external environment for a design. Table 7-2 and the following sections explain how to use the items in the Operating Environment submenu.

Table 7-2 Operating Environment Submenu Options

Option	Action	Equivalent Command
Input Delay	Shows the current attribute settings for the selected input ports, in/out ports, and pins	
Output Delay	Shows the current attribute setting for the selected output ports, in/out ports, and pins	
Drive Strength	Shows the current attribute setting for the selected input or in/out ports	
Load	Shows the current attribute settings for the selected ports or nets	
Characterize	Allows you to capture and assign cell environment information as attributes on designs linked to the cell	

Table 7-2 Operating Environment Submenu Options (Continued)

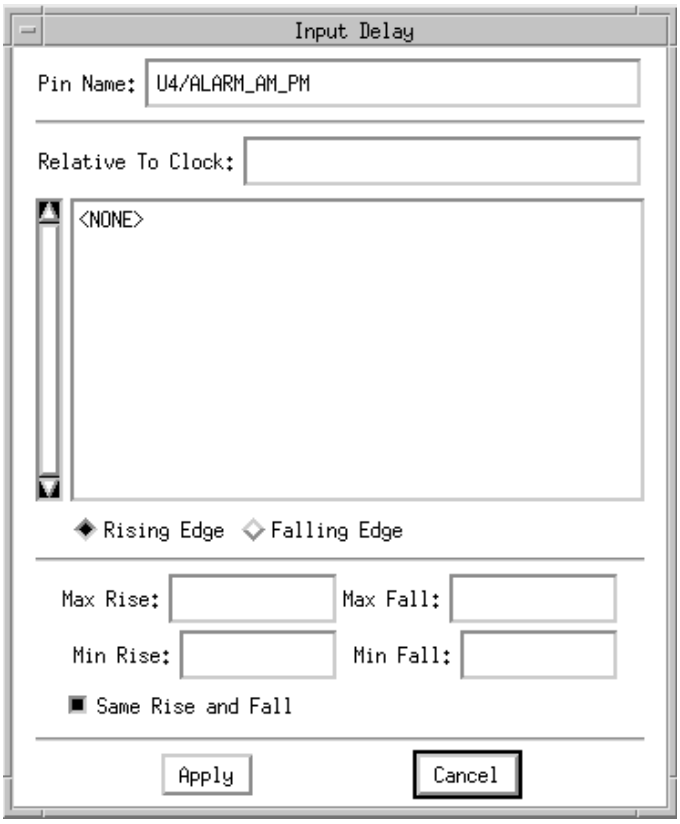
Option	Action	Equivalent Command
Operating Conditions	Allows you to define environmental characteristics of a design	set_operating_conditions -library lib_name op_condition
Wire Load	Allows you to specify a wire load model for the current design	set_wire_load wire_load_model -library lib_name
Timing Range	Allows you to set timing ranges for the current design	set_timing_ranges

Input Delay

If you select more than one port or pin, the text fields appear blank. However, the values that you set apply to all of the selected ports and pins. If you select only one port or pin, its name appears in the Pin Name text field and the current rise and fall values display in the corresponding text fields.

When you choose the Input Delay from the Operating Environment submenu, you see the Input Delay dialog box shown in Figure 7-5.

Figure 7-5 Input Delay Dialog Box



To delete or change the current values,

1. Select the affected text.

   Click the left mouse button to place the cursor in the text. Double-click the left mouse button to select all of the text in a box.

2. Type the new values.

3. Click Apply to set the values.

Click Cancel to close this dialog box without changing the current values.

Table 7-3 explains how to use the options in the Input Delay dialog box.

Table 7-3 Input Delay Dialog Box Options

Option	Action	Equivalent Command
Pin Name	Specify the pin on which the action is performed	
Relative To Clock	Use to specify delays relative to a clock edge	set_input_delay -clock clock_name
Rising Edge	Set to mark the pin on its rising edge	
Falling Edge	Set to mark the pin on its falling edge	
Max Rise and Min Rise	Use to define the rise characteristics for signal edges	set_input_delay [-add_delay -max -rise number -min -rise number]
Max Fall and Min Fall	Use to define the fall characteristics for signal edges	set_input_delay [-add_delay -max -fall number -min -fall number]
Same Rise and Fall	Use to set Rise and Fall text boxes with the same text, so you don't have to retype information	

The following sections provide additional information about the selections available in the Input Delay dialog box.

Relative To Clock

Displays the selected clock from a list of clocks in the design. Clock names appear in the scroll list below the Relative To Clock field. Select the clock name you want from the scroll list using the left mouse button. Select <NONE> to clear the field.

Max Rise and Min Rise

Defines the rise characteristics for signal edges.

Max Fall and Min Fall

Defines the fall characteristics for signal edges.

Same Rise and Fall

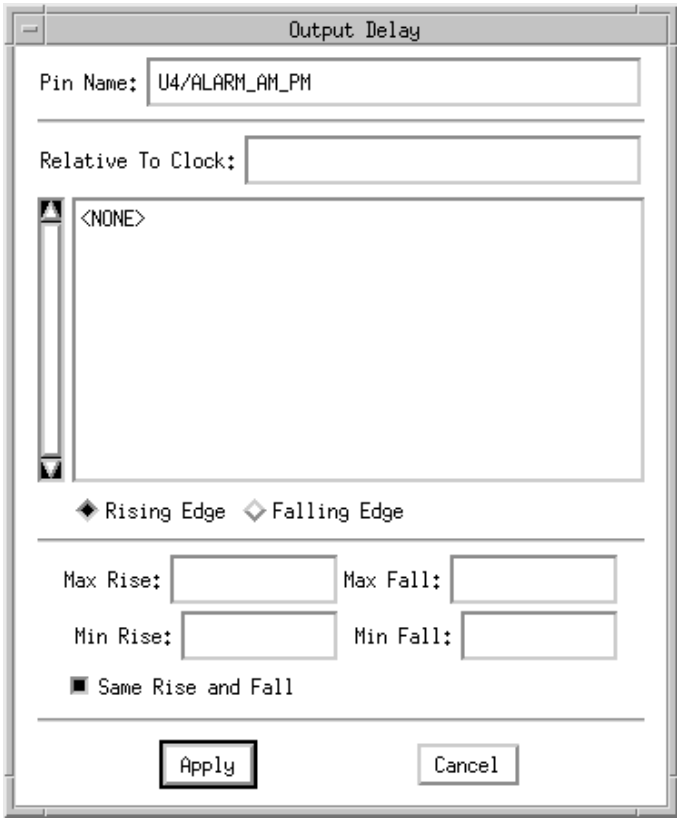
Sets the Rise and Fall text boxes with the same text, so you don’t have to retype information.

Click Apply to set the values as shown. Click Cancel to remove this dialog box.

Output Delay

If you select more than one port or pin, the text fields appear blank. However, the values that you set apply to all of the selected ports and pins. If you selected only one port or pin, its name appears in the Pin Name text field and the current rise and fall values display in the corresponding text fields. Choosing the Output Delay submenu selection displays the dialog box in Figure 7-6.

Figure 7-6 Output Delay Dialog Box



To delete or change the current values,

1. Select the affected text.

   Click the left mouse button to place the cursor in the text. Double-click the left mouse button to select all of the text in a box.

2. Type the new values.

3. Click Apply to set the values.

Click Cancel to close this dialog box without changing the current values.

Table 7-4 and the following sections explain how to use the options in the Output Delay dialog box.

Table 7-4 Output Delay Dialog Box Options

Option	Action	Equivalent Command
Relative To Clock	Use this text field to specify delays relative to a clock edge.	set_output_delay -clock clock_name
Max Rise and Min Rise	Use these text fields to define the rise characteristics for signal edges.	set_output_delay [-add_delay -max -rise number -min -rise number]
Max Fall and Min Fall	Use these text fields to define the fall characteristics for signal edges.	set_output_delay [-add_delay -max -fall number -min -fall number]
Same Rise and Fall	Use to set Rise and Fall text boxes with the same text so you don't have to retype information.	

Relative To Clock

Displays the selected clock from a list of clocks in the design. Clock names appear in the scroll list below the Relative To Clock field. Select the clock name you want from the scroll list using the left mouse button. Select <NONE> to clear the field.

Max Rise and Min Rise

Defines the rise characteristics for signal edges.

Max Fall and Min Fall

Defines the fall characteristics for signal edges.

Same Rise and Fall

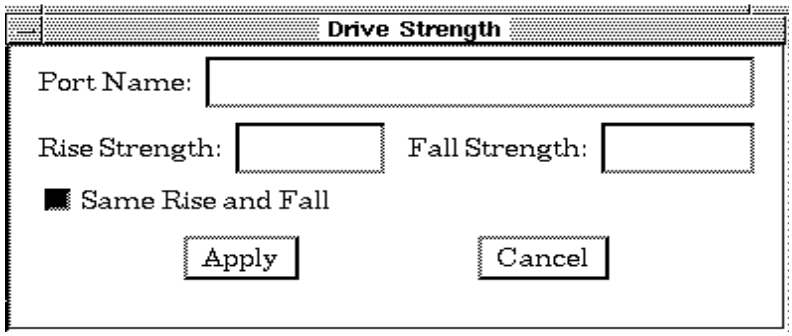
Sets the Rise and Fall text boxes with the same text, so you don't have to retype information.

Click Apply to set the values as shown. Click Cancel to remove this dialog box.

Drive Strength

If you did not select a port or you selected more than one port, the text fields in the Drive Strength dialog box appear blank. However, the values that you set apply to all of the selected ports. If you selected only one port, its name appears in the Port Name text field and the current rise and fall strengths display in the Rise Strength and Fall Strength text fields. Choosing the Drive Strength submenu selection displays the dialog box in Figure 7-7.

Figure 7-7 Drive Strength Dialog Box



To delete or change the current values,

1. Select the affected text.

   Click the left mouse to place the cursor in the text. Double-click the left mouse button to select all of the text in a box.

2. Type the new values.

3. Click Apply to set the values.

Click Cancel to close this dialog box without changing the current values.

Rise Strength and Fall Strength

Type the rise and fall drive strengths, in technology library load units.

Same Rise and Fall

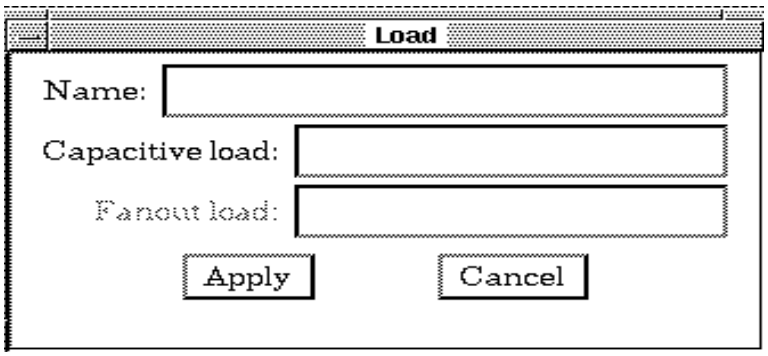
When you select the Same Rise and Fall button, the Rise and Fall text boxes display the same text, so you don’t have to retype the number.

Click Apply to set the values as shown. Click Cancel to remove this dialog box.

Load

If you did not select a net or port or if you selected more than one, the text fields in the Load dialog box are initially blank. However, the values that you set apply to all of the selected ports. If you selected only one port, its name appears in the Name text field and the current rise and fall strengths display in the Capacitive load and Fanout load text fields. Choosing the Load submenu selection displays the dialog box in Figure 7-8.

Figure 7-8 Load Dialog Box



To delete or change the current values,

1. Select the affected text.

   Click the left mouse to place the cursor in the text. Double-click the left mouse button to select all of the text in a box.

2. Type the new values.

3. Click Apply to set the values.

Click Cancel to close this dialog box without changing the current values.

Table 7-5 explains how to use the options in the Load dialog box.

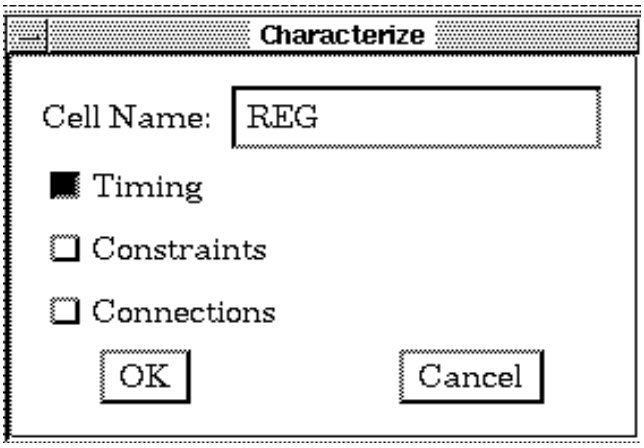
Table 7-5 Load Dialog Box Options

Option	Action	Equivalent Command
Capacitive load	Type the load incurred by this port or net in technology library load units.	set_load capacitive_load
Fanout load	Type the maximum fanout load that can be driven by this port or net in technology library load units.	set_fanout_load fanout_load

Characterize

When you choose Characterize from the Operating Environment submenu, you see the Character dialog box shown in Figure 7-9.

Figure 7-9 Characterize Dialog Box



The Cell Name text field shows the name of the selected cell. If you select more than one cell, the Cell Name field initially appears blank; however, the values that you set apply to all of the cells you select.

Click OK to characterize the current design using the displayed options. Click Cancel to remove this dialog box.

Table 7-6 explains how to use the options in the Characterize dialog box.

Table 7-6 Characterize Dialog Box Options

Option	Action	Equivalent Command
Timing	Enable this button to generate timing information for the characterized cell. Enabled by default.	characterize {cell_name}
Constraints	Enable this button to record constraint information for the characterized cell.	characterize -no_timing -constraints cell_name

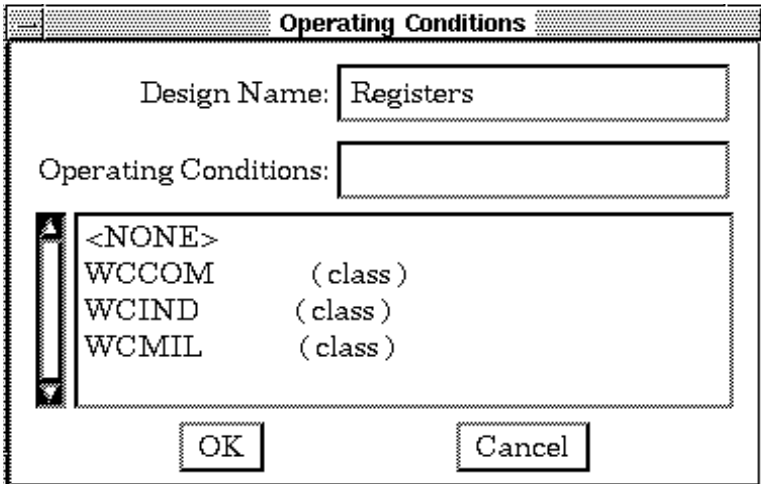
Table 7-6 Characterize Dialog Box Options (Continued)

Option	Action	Equivalent Command
Connections	Enable this button to generate logical connection (port) information for the characterized cell.	characterize -no_timing -connections cell_name

Operating Conditions

The Operating Conditions characteristics are defined in a technology library. In the Operating Conditions dialog box, the class library contains definitions for worst-case commercial (WCCOM), worst-case industrial (WCIND), and worst-case military (WCMIL) environmental conditions. Choosing the Operating Conditions submenu selection displays the dialog box in Figure 7-10.

Figure 7-10 Operating Conditions Dialog Box



The Design Name field shows the name of the top design. Click OK to set the operating conditions to the highlighted Operating Conditions name.

To change operating conditions,

1. Select the operating conditions name you want from the list.
2. Click OK.

Note:
You can issue this dialog box only at the level of the top design.

To clear (reset) the current operating conditions,

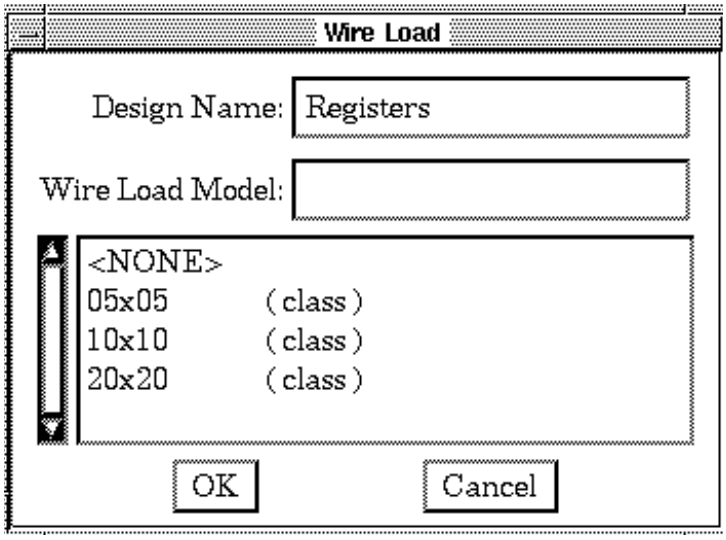
1. Select <NONE>.
2. Click OK.

To remove this dialog box without making any changes, click Cancel.

Wire Load

When you select Wire Load from the Operating Environment submenu, you see the Wire Load dialog box shown in Figure 7-11.

Figure 7-11 Wire Load Dialog Box



The Design Name field shows the name of the top design. Click OK to set the wire load model to the highlighted Wire Load Model. (Wire load models are defined in a technology library.)

You can issue this dialog box only at the level of the top design.

To change wire load models,

1. Select the wire load model's name you want from the list.
2. Click OK.

To clear (reset) the current wire load model,

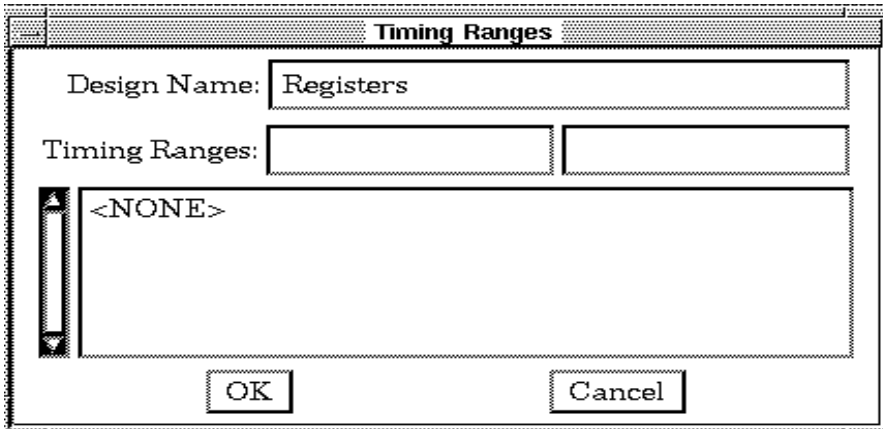
1. Select <NONE>.
2. Click OK.

To remove this dialog box without making any changes, click Cancel.

Timing Range

Timing range defines scaling factors used to scale timing path totals. Choosing the Timing Range submenu selection from the Operating Environment submenu displays the Timing Ranges dialog box shown in Figure 7-12.

Figure 7-12 Timing Ranges Dialog Box



The Design Name field shows the name of the top design. Click OK to set the timing ranges to the displayed Timing Ranges names. To change timing ranges, click the timing range name or names you want. You can choose one or two timing ranges. (Timing ranges are defined in a technology library.)

You can issue this dialog box only at the level of the top design.

Click <NONE> to erase the displayed Timing Ranges. Click Cancel to remove this dialog box without making any changes.

To clear (reset) the current timing ranges,

1. Click <NONE>.
2. Click OK.

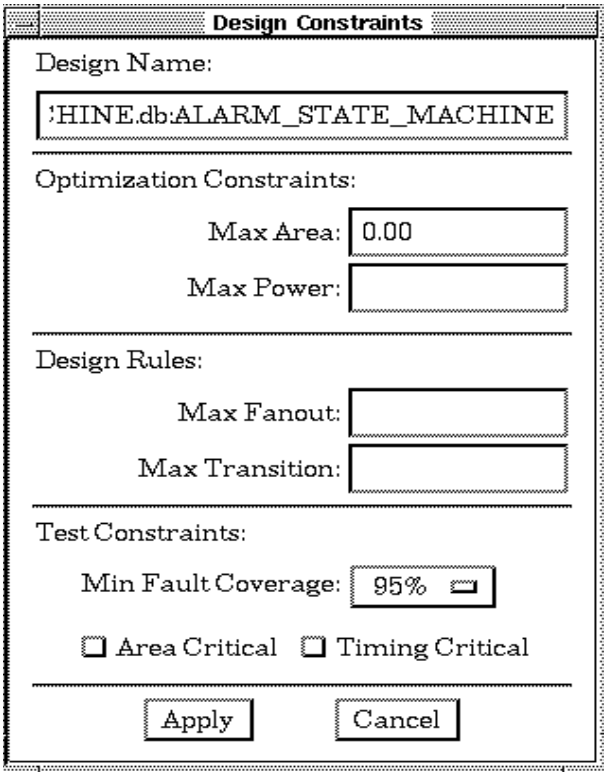
Optimization Constraints

Use this menu to set design and timing constraints.

Design Constraints

Use the Design Constraints dialog box, shown in Figure 7-13, to set design objectives for the top level of a design. The name of the top level appears in the Design Name field.

Figure 7-13 Design Constraints Dialog Box



Click Apply to set the values as shown. Click Cancel to remove this dialog box.

Table 7-7 explains how to use the options in the Designs Constraints dialog box.

Table 7-7 Design Constraints Dialog Box Options

Option	Action	Equivalent Command
Max Area	Type the maximum allowable area constraint, in technology library area units.	set_max_area number
Max Power	Type the maximum allowable power constraint, in technology library power units.	set_max_power number
Max Fanout	Type the maximum fanout load that can be driven by any port or pin in this design, in technology library load units.	set_max_fanout
Max Transition	Type the maximum transition time for any transitioning net in this design, in technology library time units.	set_max_transition
Min Fault Coverage	Select a number from the available list using the left mouse button.	set_min_fault_coverage number [-area_critical | -timing_critical]

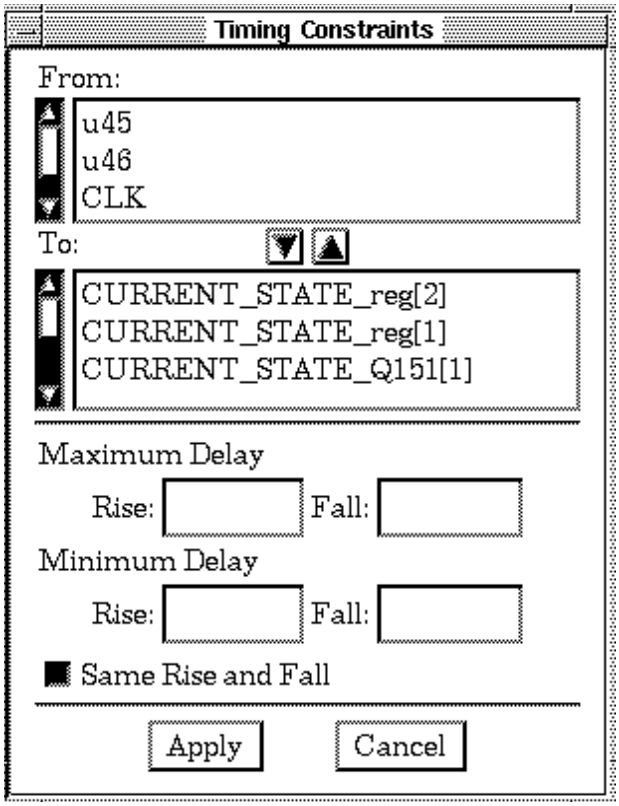
By default, fault coverage takes precedence over area and timing considerations. If area takes precedence over fault coverage, enable the Area Critical button. If timing takes precedence over fault coverage, enable the Timing Critical button.

Timing Constraints

When you choose Timing Constraints from the Optimization Constraints submenu, you see the Timing Constraints dialog box shown in Figure 7-14. You use the options in this dialog box to define delay objectives for combinational circuits. The top portion of the

dialog box has a From list and a To list. These lists display the names of the selected ports, pins, or cells. You can move object names from one list to the other by using the arrow buttons.

Figure 7-14 Timing Constraints Dialog Box



Click Apply to set constraints between each member of the From list and To list. Click Cancel to remove this dialog box. Table 7-8 explains how to use the options in the Timing Constraints dialog box.

Table 7-8 Timing Constraints Dialog Box Options

Option	Action	Equivalent Command
Maximum Delay	Type the maximum rise and fall times. To delete or change the current values, select the affected text and type new values.	set_max_delay number -rise -to object_name -fall -to object_name

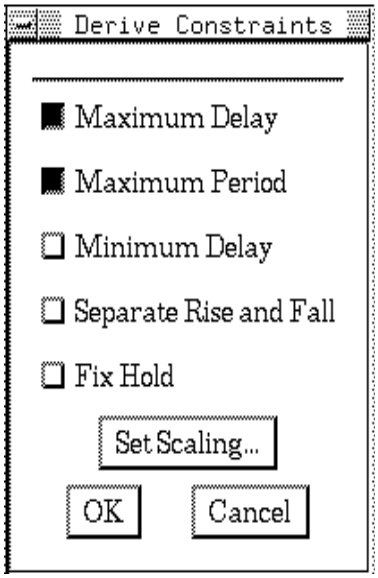
Table 7-8 Timing Constraints Dialog Box Options (Continued)

Option	Action	Equivalent Command
Minimum Delay	Type the minimum rise and fall times. To delete or change the current values, select the affected text and type new values.	set_min_delay number -rise -to object_name -fall -to object_name
Same Rise and Fall	Enable to set Rise and Fall text boxes with the same text so you don't have to retype information.	

Derive

When you choose Derive... from the Optimization Constraints submenu, you see the Derive Constraints dialog box shown in Figure 7-15. Use the Derive Constraints dialog box to derive timing constraints for a design.

Figure 7-15 Derive Constraints Dialog Box



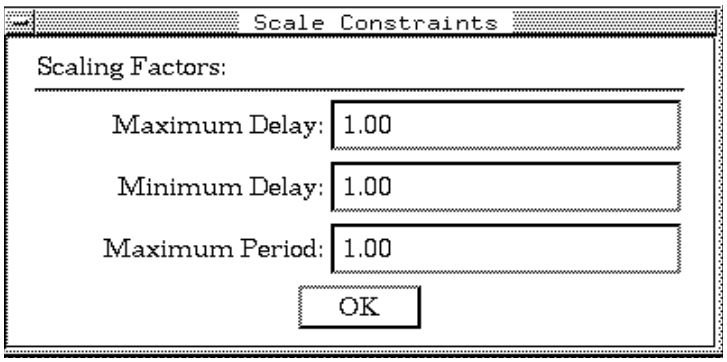
Click OK to derive the selected constraints. Click Cancel to remove this dialog box. Table 7-9 explains how to use the items in the Derive Constraints dialog box.

Table 7-9 Derive Constraints Dialog Box Options

Option	Action	Equivalent Commands
Maximum Delay	Derives maximum delay constraints for combinational paths in the design	derive_timing_constraints
Maximum Period	Derives maximum period constraints for the clock in the design	derive_timing_constraints
Minimum Delay	Derives minimum delay constraints for unconstrained combination paths	derive_timing_constraints -min_delay
Separate Rise and Fall	Derives separate rise and fall constraints for each combinational timing endpoint	derive_timing_constraints -separate_rise_fall
Fix Hold	Creates hold constraints for unconstrained clocks in the design	derive_timing_constraints -fix_hold
Set Scaling	Allows you to type the maximum delay, minimum delay, and maximum period scaling factors	derive_timing_constraints [-max_delay_scale scale_factor] [-min_delay_scale scale_factor] [-period_scale scale_factor]

Clicking the Set Scaling button from the Derive Constraints dialog box, brings up the Scale Constraints dialog box shown in Figure 7-16.

Figure 7-16 Scale Constraints Dialog Box

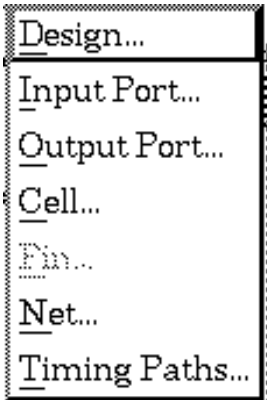


You use this dialog box to set the scaling factors in the design.

Optimization Directives

When you choose Optimization Directives from the Attributes menu, you see the Optimization Directives submenu shown in Figure 7-17. Use the Optimization Directives option menu to set attributes on design objects that control or influence optimization.

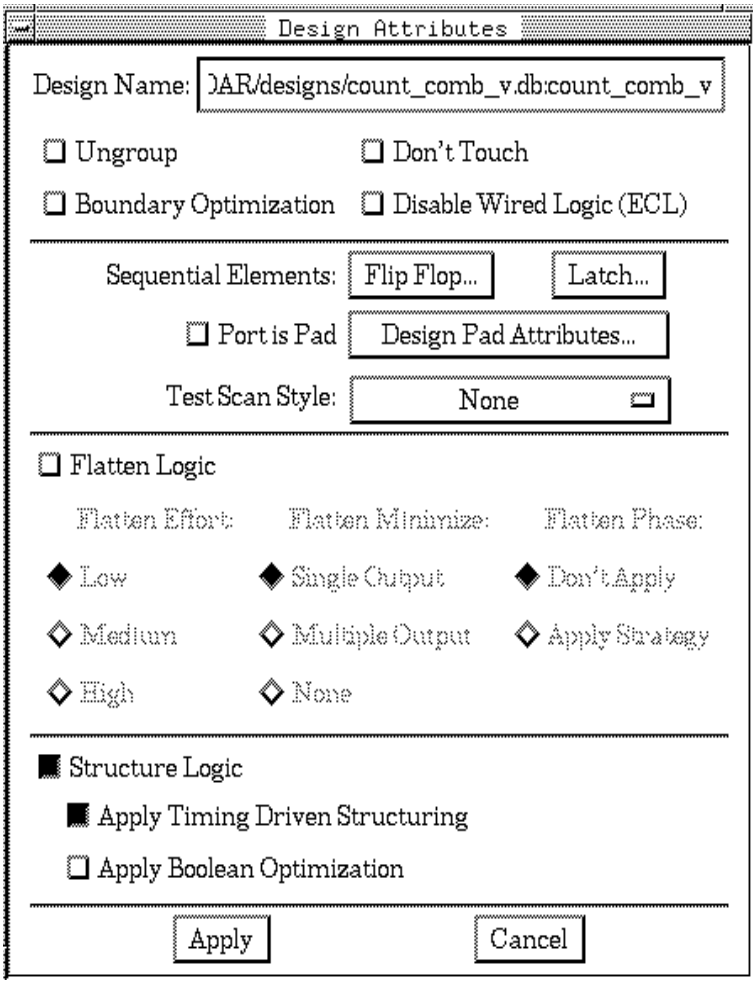
Figure 7-17 Optimization Directives Option Menu



Design

Use the Design Attributes dialog box, shown in Figure 7-18, to set attributes that control optimization on the top-level design. To set design attributes on an instance, traverse the hierarchy to the instance you want, as described in Chapter 2, “Using Design Analyzer.”

Figure 7-18 Design Attributes Dialog Box



Click Apply to set the values as shown. Click Cancel to remove this dialog box. Table 7-10 explains how to use the options in the Design Attributes dialog box.

Table 7-10 Design Attributes Dialog Box Options

Option	Action	Equivalent Command
Ungroup	Ungroups the current design during compilation	set_ungroup
Boundary Optimization	Allows boundary optimization during compilation, allowing logic optimization to occur across hierarchical boundaries	set_boundary_optimization
Don't Touch	Preserves the design during compilation.	set_dont_touch
Disable Wired Logic	Allows Design Compiler to use wired logic where appropriate (only used with ECL designs)	set_wired_logic_disable
Flip-Flop	Allows you to see and change the preferred flip-flop type used during compilation	set_register_type -flip_flop type [-exact]
Latch	Allows you to see and change the preferred latch type used during compilation	set_register_type -latch type [-exact]
Port is Pad	Places the port_is_pad attribute on the input ports in the design	set_port_is_pad
Design Pad Attributes	Allows you to define threshold, minimum, and maximum pad voltage levels for the design	set_pad_type [-vil value] [-vih value] [-vimin value] [-vimax value]
Test Scan Style	Obsolete command—use `set_scan_configuration -style` instead)	
Flatten Effort	Allows you to choose the flatten effort level (available when the Flatten Logic button is enabled)	set_flatten true -design design_name effort [low | medium | high]

Table 7-10 Design Attributes Dialog Box Options (Continued)

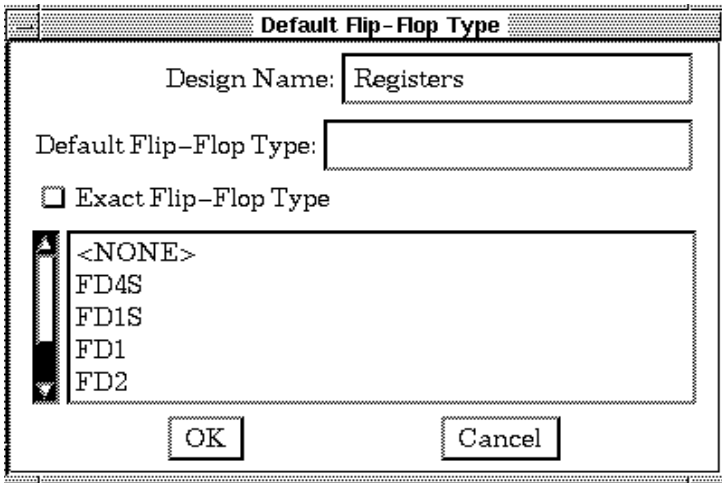
Option	Action	Equivalent Command
Flatten Minimize	Allows you to choose the minimization strategy (available when the Flatten Logic button is enabled)	set_flatten true -design design_name -minimize [single_output | multiple_output | none]
Flatten Phase	Allows you to choose the phase assignment strategy (available when the Flatten Logic button is enabled)	set_flatten true -design design_name -phase [false | true]
Apply Timing Driven Structuring	Allows you to use timing-driven structuring on this design (available when the Structure Logic button is enabled)	set_structure true -design design_name -boolean false -timing true
Apply Boolean Optimization	Allows you to use Boolean optimization on this design (available when Structure Logic button is enabled)	set_structure true -design design_name -boolean true -timing true

The following sections provide additional information for some of the selections in the Design Attributes dialog box.

Flip-flop

When you click the Flip-Flop button in the Design Attributes dialog box, you see the Default Flip-Flop Type dialog box shown in Figure 7-19.

Figure 7-19 Default Flip-Flop Type Dialog Box



Click OK to set the default flip-flop type as shown in the text box. To change the default flip-flop type, click the flip-flop type you want in the list.

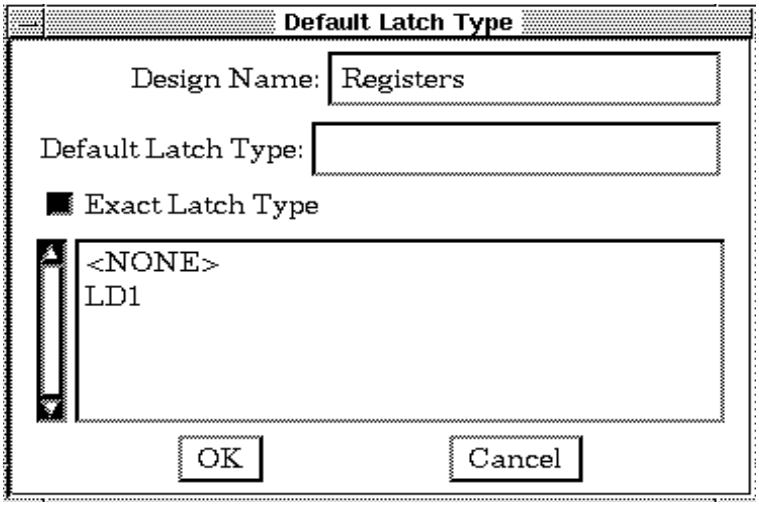
Click <NONE> to clear the name displayed in the Default Flip-Flop Type text box. Click Cancel to remove this dialog box.

Enable the Exact Flip-Flop Type button if you want an exact mapping to the specified flip-flop type during compile. The technology library defines flip-flops.

Latch

When you click the Latch button in the Design Attributes dialog box, you see the Default Latch Type dialog box shown in Figure 7-20.

Figure 7-20 Default Latch Type Dialog Box



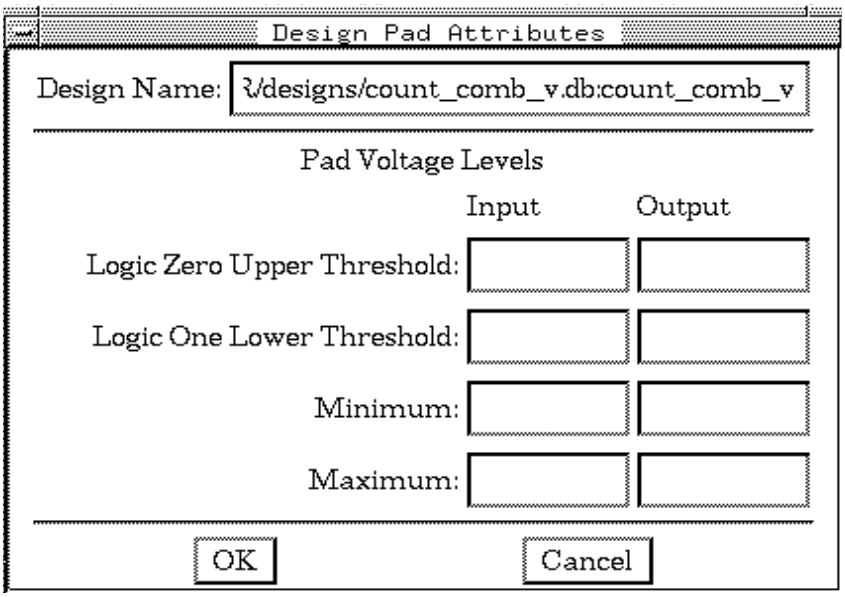
Click OK to set the default latch type as shown in the text box. To change the default latch type, click the latch type you want in the list.

Click <NONE> to clear the name displayed in the Default Latch Type text box. Click Cancel to remove this dialog box.

Enable the Exact Latch Type button if you want an exact mapping to the specified latch type during compilation. The technology library defines latches.

When you click the Design Pad Attributes button in the Design Attributes dialog box, you see the Design Pad Attributes dialog box shown in Figure 7-21.

Figure 7-21 Design Pad Attributes Dialog Box



Click OK to set the indicated voltage levels. Click Cancel to remove this dialog box.

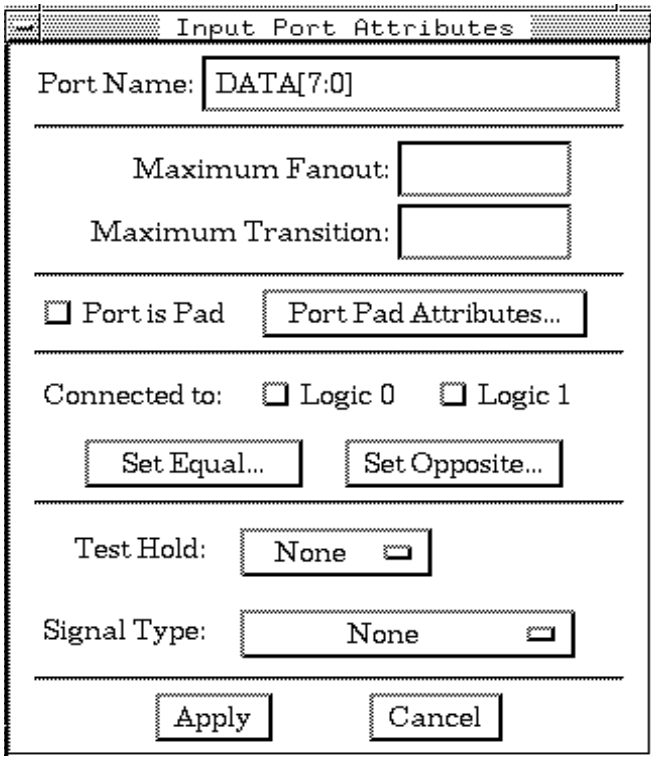
Test Scan Style

This command is obsolete. Instead, use the `set_scan_configuration -style` command.

Input Port

When you choose Input Port from the Optimization Directives submenu, you see the Input Port dialog box shown in Figure 7-22. This dialog box displays the current attribute settings for the selected input ports.

Figure 7-22 Input Port Attributes Dialog Box



SHORTCUT

Double-click an input port to display this dialog box.

If you select more than one port, the text fields appear blank. However, the values that you set apply to all of the selected ports. If you select only one port, its name appears in the Port Name text field and the dialog box indicates its current attribute status.

To delete or change the current values,

1. Select the affected text.

   Click the left mouse to place the cursor in the text. Double-click the left mouse button to select all of the text in a box.

2. Type the new values.

3. Click Apply to set the values.

Click Cancel to close this dialog box without changing the current values.

Table 7-11 explains how to use the items in the Input Port Attributes dialog box.

Table 7-11 Input Port Dialog Box Options

Option	Action	Equivalent Command
Maximum Fanout	Type the maximum fanout load that can be driven by this input port. Use technology library load units.	set_max_fanout number
Maximum Transition	Type the maximum transition time for the signal arriving at this input port. Use technology library time units.	set_max_transition number
Port is Pad	Enable this button to place the port_is_pad attribute on the selected input ports.	set_port_is_pad
Port Pad Attributes	Enable this button to use the Port Pad Attributes dialog box.	
Connected to	Click Logic 0 if this input port is connected o logic 0; otherwise, click Logic 1.	set_logic_one, set_logic_zero
Set Equal	Click this button, and type the equal port in the Port 2 text box if this input port is logically equal to another port.	set_equal port_1 port_2
Set Opposite	Click this button, and type the equal port in the Port 2 text box if this input port is logically opposite to another port.	set_opposite port_1 port_2
Test Hold	Use this menu to place a test_hold attribute on the specified input port.	set_test_hold hold_type

Table 7-11 Input Port Dialog Box Options

Option	Action	Equivalent Command
Signal Type	Choose a signal type from the option menu. If this is a test cell, specify the type from the submenu.	set_signal_type [-clocked_on_also | test_scan_in | test_scan_enable | test_scan_enable_inverted | test_scan_clock | test_scan_clock_a | test_scan_clock_b | test_clock | jtag_tdi | jtag_tms | jtag_tck | jtag_trst}

Maximum Fanout

Allows you to choose the maximum fanout load that can be driven by this input port. Use technology library load units.

Maximum Transition

Allows you to choose the maximum transition time for the signal arriving at this input port. Use technology library time units.

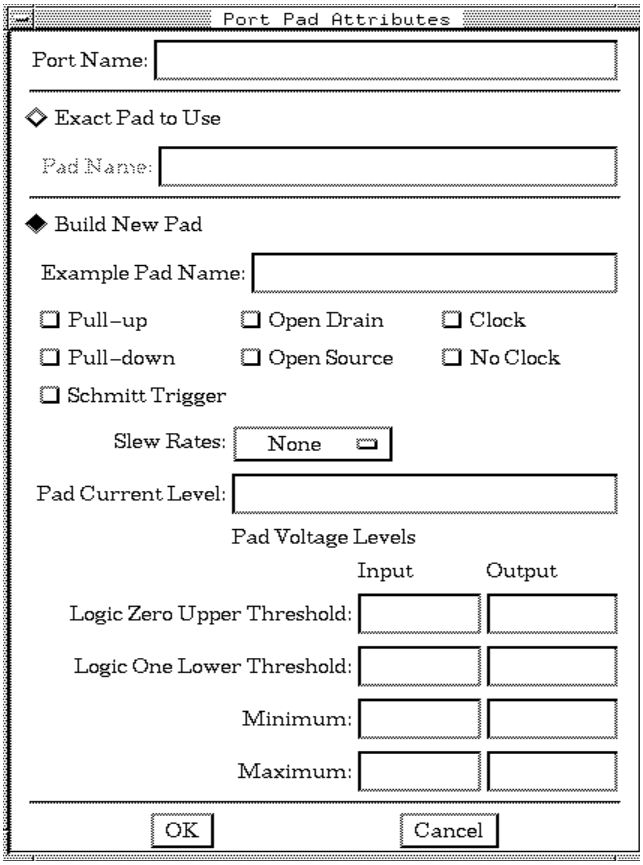
Port is Pad

Places the port_is_pad attribute on the selected input ports.

Port Pad Attributes

When you choose Port Pad Attributes from the Input Port dialog box, you see the Port Pad Attributes dialog box shown in Figure 7-24.

Figure 7-23 Port Pad Attributes Dialog Box



Use this dialog box to define the pad cell type, pad cell characteristics, slew rate, and pad current and voltage levels for a port. Click OK to set the options and values as shown. Click Cancel to remove this dialog box.

Table 7-12 explains how to use the options in the Port Pad Attributes dialog box.

Table 7-12 Port Pad Attributes Dialog Box Options

Option	Action	Equivalent Command
Port Name	View the port name in the dialog box. If you select more than one port or you do not select a port, the text box is blank.	

Table 7-12 Port Pad Attributes Dialog Box Options (Continued)

Option	Action	Equivalent Command
Pad Name	Enable the Exact Pad to Use button, and type the pad cell name to define the exact I/O pad cell to be instantiated at selected ports.	set_pad_type [-exact exact_pad]
Example Pad Name	Enable the Build New Pad button, and type the name of the pad example to define the nonfunctional characteristics of the pad by inference from the library information of a pad example.	set_pad_type [-example example_pad]
Pad Characteristics Buttons	Use these buttons to select characteristics of the pad. Options are pull-up, pull-down Schmitt Trigger, Open Drain, Open Source, Clock, and No Clock.	set_pad_type [-opendrain] [-opensource] [-pulldown] [-pullup] [-schmitt] [-clock] [-no_clock]
Slew Rate	Use the Slew Rates option to set the slew rate of the pad.	set_pad_type [-slewrate low | medium | high]
Pad Current Level	Type the minimum current rating (mA) for the pad in this text box.	set_pad_type [-currentlevel value]
Pad Voltage Levels	Use the text boxes to define pad voltage levels.	set_pad_type [-vih value] [-vil value] [-vimax value] [-vimin value] [-voh value] [-vol value] [-vomax value] [-vomin value]

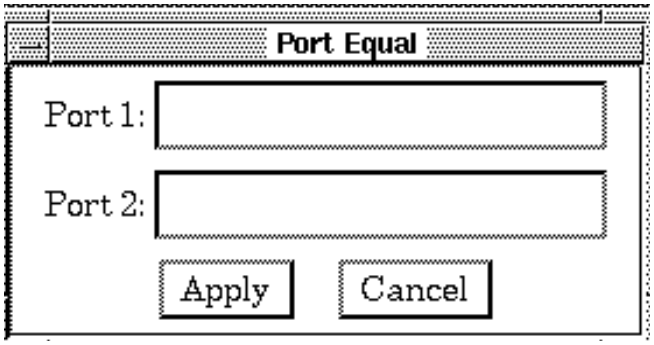
Connected to

Click Logic 0 if this input port is connected to logic 0; otherwise, click Logic 1.

Set Equal

When you choose Set Equal from the Input Port Attributes dialog box, you see the Port Equal dialog box shown in Figure 7-24.

Figure 7-24 Port Equal Dialog Box

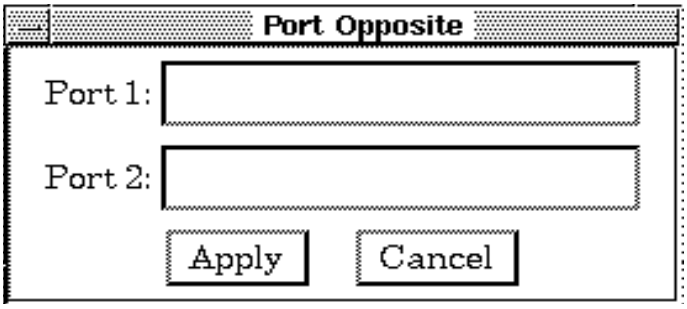


Click Apply to define the given ports as logical equivalents. Click Cancel to remove this dialog box.

Set Opposite

When you choose Set Opposite from the Input Port Attributes dialog box, you see the Port Opposite dialog box shown in Figure 7-25.

Figure 7-25 Port Opposite Dialog Box

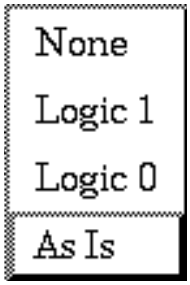


Click Apply to define the given ports as logical opposites. Click Cancel to remove this dialog box.

Test Hold

When you choose Test Hold from the Input Port Attributes dialog box, you see the Test Hold option menu shown in Figure 7-26.

Figure 7-26 Test Hold Option Menu

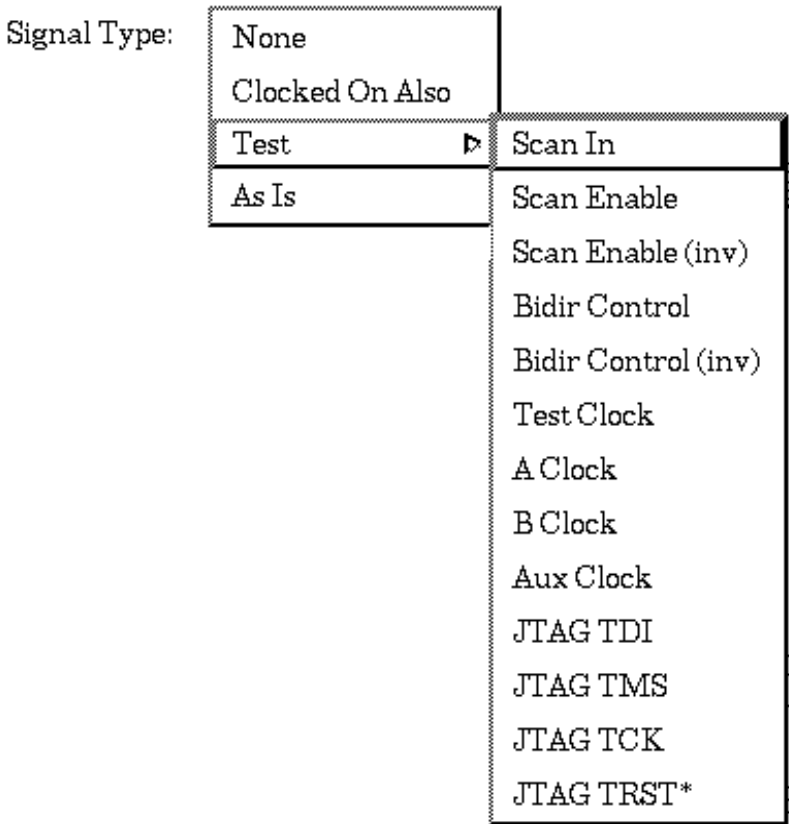


Use this option menu to place a test_hold attribute on the specified input port.

Signal Type

When you choose Signal Type from the Input Port Attributes dialog box, you see the Signal Type option menu shown in Figure 7-27.

Figure 7-27 Signal Type Option Menu

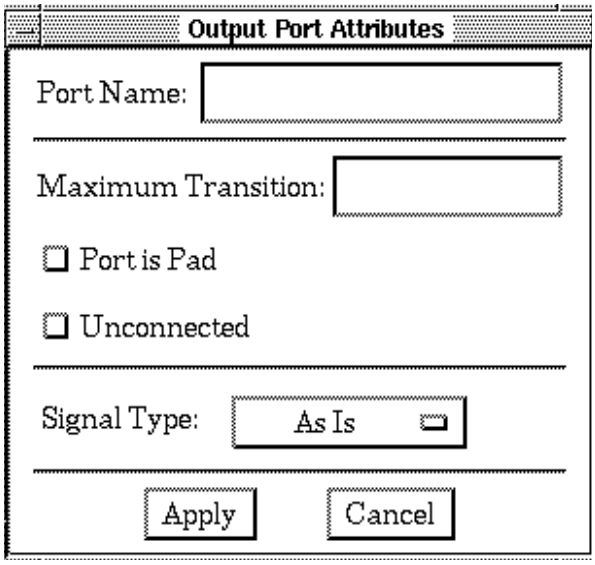


Use this submenu to select the type of signal for the specified input port.

Output Port

When you select Output Port from the Optimization Directives submenu, you see the Output Port Attributes dialog box shown in Figure 7-28. This dialog box displays the current attribute settings for the selected output ports.

Figure 7-28 Output Port Attributes Dialog Box



SHORTCUT

Double-click an output port to display this dialog box.

If you select more than one port, the text fields appear blank. However, the values that you set apply to all of the selected ports. If you select only one port, its name appears in the Port Name text field and the dialog box indicates its current attribute status.

To delete or change the current text values,

1. Select the affected text.

   A click with the left mouse places the cursor in the text. A double-click with the left mouse button selects all of the text in a box.

2. Type the new values.

3. Click Apply to set the values as shown.

Click Cancel to remove this dialog box.

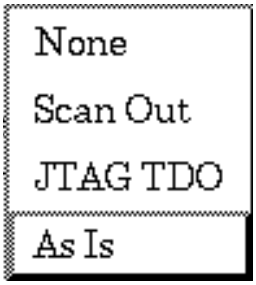
Table 7-13 explains how to use the options in the Output Port Attributes dialog box.

Table 7-13 Output Port Attributes Dialog Box Options

Option	Action	Equivalent Command
Maximum Transition	Type the maximum transition time for the signal arriving at this output port, in technology library time units.	set_max_transition number
Port is Pad	Enable this button to place the port_is_pad attribute on the selected output ports.	set_port_is_pad
Unconnected	Enable this button if this output is not connected.	set_unconnected
Signal Type	Choose a signal type from the option menu. If this is not a scan cell, select None.	set_signal_type [test_scan_out | jtag_tdo]

When you choose Signal Type from the Output Port Attributes dialog box, you see the Signal Type option menu shown in Figure 7-29.

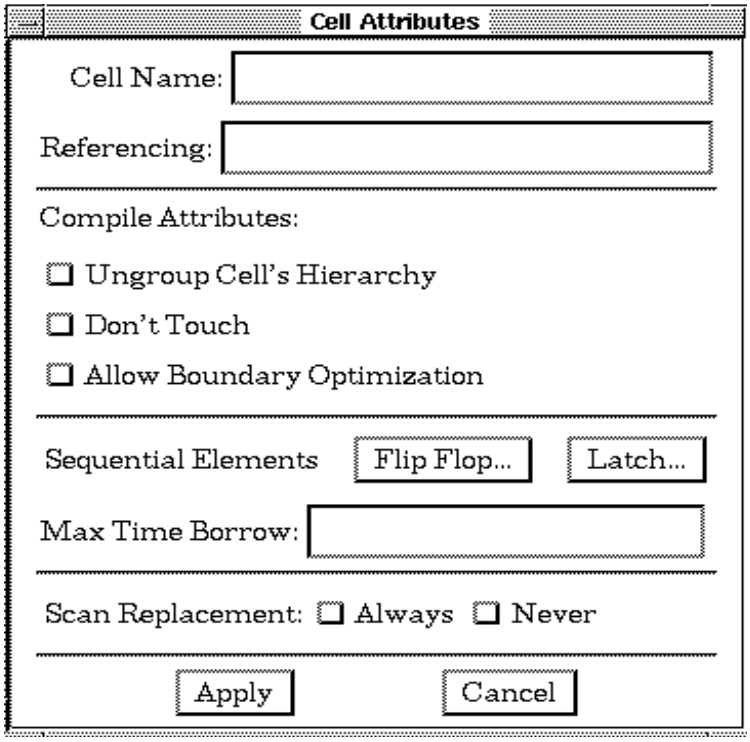
Figure 7-29 Signal Type Option Menu



Cell

When you select Cell from the Optimization Directives menu, you see the Cell Attributes dialog box shown in Figure 7-30. You can use this dialog box to set instance-specific cell attributes throughout the design hierarchy.

Figure 7-30 Cell Attributes Dialog Box



You can select objects graphically with the mouse, or by using Edit > Select. If you select more than one cell, the text fields appear blank. However, the values that you set apply to all of the selected cells. If you select only one cell, its name appears in the Cell Name text field and the dialog box indicates its current attribute status.

To delete or change the current values,

1. Select the affected text.

   Click the left mouse to place the cursor in the text. Double-click the left mouse button to select all of the text in a box.

2. Type the new values.

3. Click Apply to set the values.

Click Cancel to close this dialog box without changing the current values.

Table 7-14 Cell Attributes Dialog Box Options

Option	Action	Equivalent Command
Referencing	Display the name of the cell's reference, either a library cell name or a subdesign name.	
Ungroup Cell's Hierarchy	Enable this button if the cell is a subdesign that is to be ungrouped during compilation.	set_ungroup
Don't Touch	Enable this button to skip the cell during compilation.	set_dont_touch
Allow Boundary Optimization	Enable this button to allow boundary optimization during compilation, which allows logic optimization to occur across hierarchical boundaries.	set_boundary_optimization
Flip-Flop	Click to see and change the preferred flip-flop type used during compilation.	set_register_type -flip_flop type [-exact]
Latch	Click to see and change the preferred latch type used during compilation.	set_register_type -latch type [-exact]
Max Time Borrow	Type the amount of time borrowing possible for sequential elements.	set_max_time_borrow number

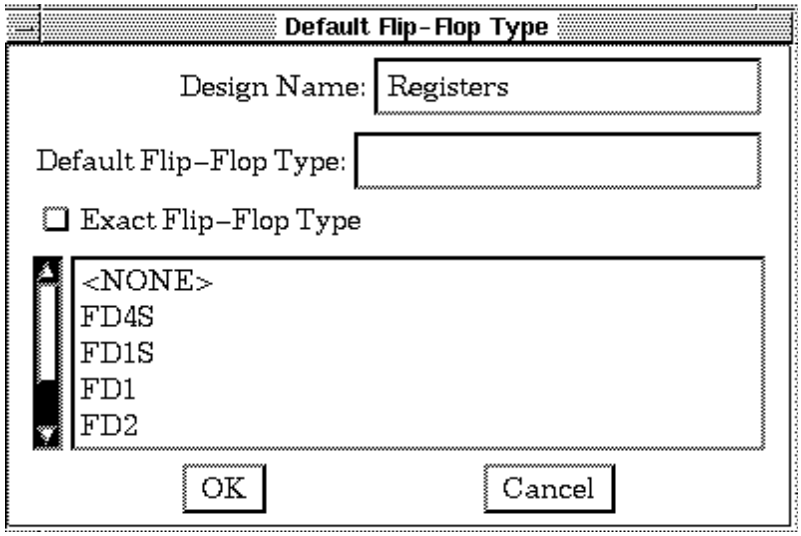
Table 7-14 Cell Attributes Dialog Box Options (Continued)

Option	Action	Equivalent Command
Scan Replacement	Obsolete command—do not use	

The following sections provide additional information about some of the options from the Cell Attributes dialog box.

When you choose Flip-Flop from the Cell Attributes dialog box, you see the Default Flip-Flop Type dialog box shown in Figure 7-31.

Figure 7-31 Default Flip-Flop Type Dialog Box



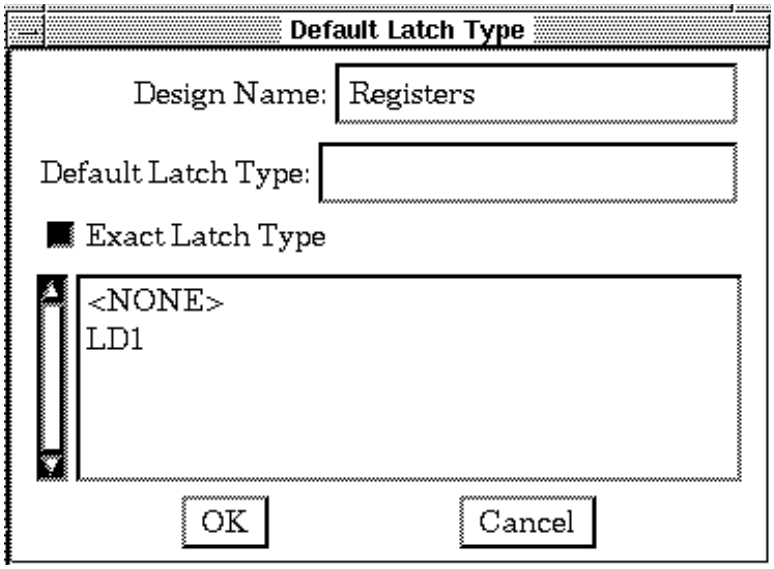
Click OK to set the default flip-flop type as shown in the text box. To change the default flip-flop type, click the flip-flop type you want from the list.

Click <NONE> to erase the name displayed in the Default Flip-Flop Type text box. Click Cancel to remove this dialog box.

Enable the Exact Flip-Flop Type button if you want an exact mapping to the specified flip-flop type during compile. A technology library defines flip-flops.

When you choose Latch from the Cell Attributes dialog box, you see the Default Latch Type dialog box shown in Figure 7-32.

Figure 7-32 Default Latch Type Dialog Box



Click OK to set the default latch type shown in the text box. To change the default latch type, click the latch type you want from the list.

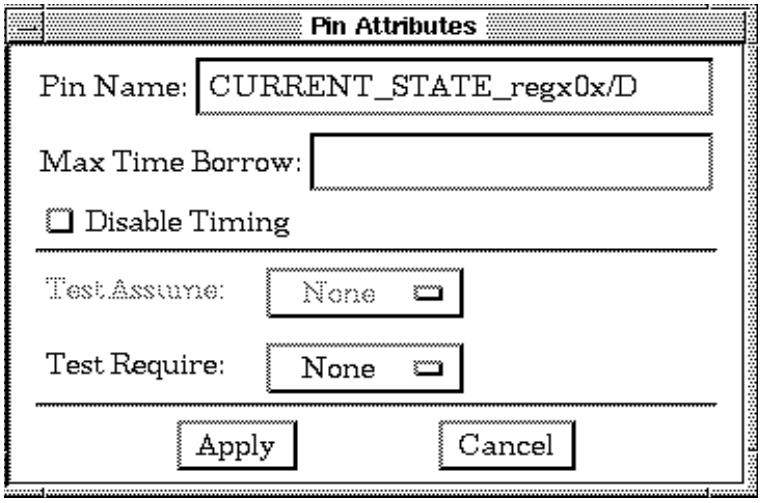
Click <NONE> to erase the name displayed in the Default Latch Type text box. Click Cancel to remove this dialog box.

Enable the Exact Latch Type button if you want an exact mapping to the specified latch type during compile. Latches are defined in a technology library.

Pin

When you choose Pin from the Optimization Directives menu, you see the Pin Attributes dialog box shown in Figure 7-33. You can use this dialog box to set instance-specific pin attributes throughout the design hierarchy. You can select objects graphically with the mouse or by using Edit > Select.

Figure 7-33 Pin Attributes Dialog Box



To select a pin graphically,

1. Zoom in.
2. Click the left or middle mouse button with the cursor directly over the pin.

To select pins when you are not zoomed in,

1. Select the instance.
2. Press the Shift key.
3. Continue clicking with the middle mouse button until you select the pin you want.

If you select more than one pin, the displayed attributes values are set for all selected pins.

If you select more than one pin, the text fields appear blank. However, the values that you set apply to all of the selected pins. If you select only one pin, its name appears in the Pin Name text field and the dialog box indicates its current attribute status.

To delete or change the current values,

1. Select the affected text.

   Click the left mouse to place the cursor in the text. Double-click the left mouse button to select all of the text in a box.

2. Type the new values.

3. Click Apply to set the values.

Click Cancel to close this dialog box without changing the current values.

SHORTCUT

Double-click a pin to display this dialog box.

Table 7-15 explains how to use the options in the Pin Attributes dialog box.

Table 7-15 Pin Attributes Dialog Box Options

Option	Action	Equivalent Command
Max Time Borrow	Type a number to define the maximum allowable time borrowing for the pin.	set_max_time_borrow number
Disable Timing	Enable this button to disable all timing arcs approaching the pin.	set_disable_timing

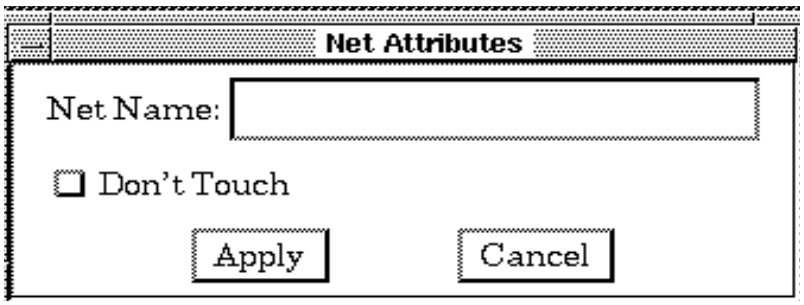
Table 7-15 Pin Attributes Dialog Box Options (Continued)

Option	Action	Equivalent Command
Test Assume	Choose the appropriate option to specify a fixed, assumed value at the selected cell output pin.	set_test_assume value
Test Require	Obsolete command—do not use	

Net

When you choose Net from the Optimization Directives menu, you see the Net Attributes dialog box shown in Figure 7-34. Use this dialog box to set instance-specific net attributes throughout the design hierarchy.

Figure 7-34 Net Attributes Dialog Box



If you select more than one net (or bus member) and any of them does not have the dont_touch attribute set, this dialog box shows the attribute as not set. Any change you make to the attribute value applies to all the selected nets.

To delete or change the current values,

1. Select the affected text.

Click the left mouse to place the cursor in the text. Double-click the left mouse button to select all of the text in a box.

2. Type the new values.
3. Click Apply to set the values.

Click Cancel to close this dialog box without changing the current values.

SHORTCUT

Double-click a net to display this dialog box.

Don’t Touch

Enable this button to preserve the net during compilation. The equivalent command to this selection is

```
set_dont_touch
```

Timing Paths

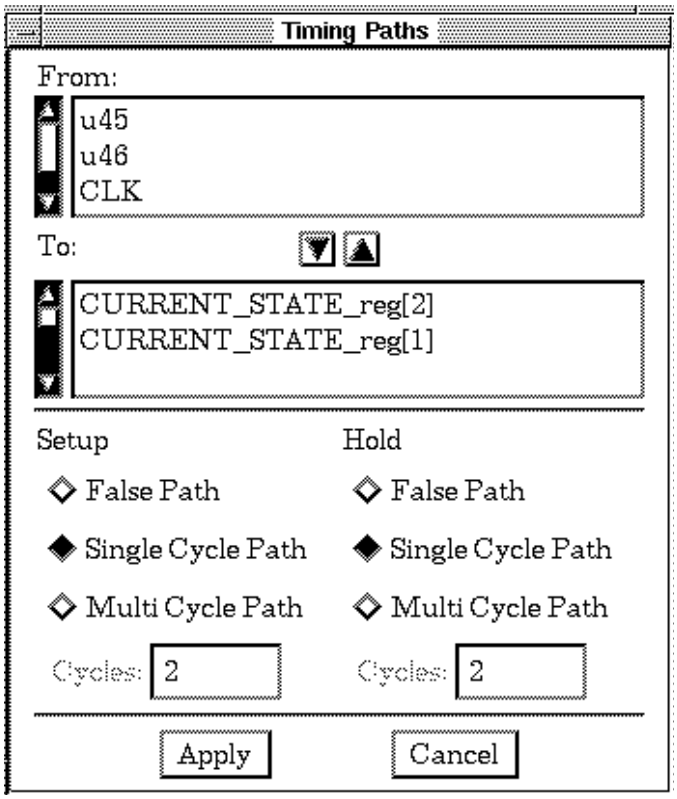
When you select Timing Paths from the Optimization Directives menu, you see the Timing Paths dialog box shown in Figure 7-35. Use the Timing Paths dialog box to specify both MultiCycle Paths and False Paths. This dialog box does not have a corresponding graphical object in the schematic window. The report window links the dialog box to the design. Each line you want written in the multicycle delay report corresponds to a delay setting in the design. When you click the Apply button in the report window, this dialog box appears with the relevant information.

To remove the information in this dialog box,

1. Click the Single Cycle Path button.
2. Click Apply.

Doing this overwrites the multicycle information with single cycle (default) settings.

Figure 7-35 Timing Paths Dialog Box



Select source points in the From list, and select destination points in the To list.

To move points from one list to the other,

1. Select one or more lines in the scrollable list.

2. Click the appropriate arrow button between the lists.

Use the buttons under Setup and Hold to define setup and hold relationships. The equivalent command to this selection in the dialog box is

```
[reset_path | set_false_path | set_multicycle_path] [-setup
| -hold] -to destination -from source
```

8

Analysis Menu

This chapter describes all the items in the Analysis menu and the submenus and dialog boxes you can access through it.

Use the Analysis menu to

- Link Design
- Check Design
- Time Design
- Show Timing
- Show Net Load
- Highlight
- Test Report
- Report

Table 8-1 explains how to use the options in the Analysis menu.

Table 8-1 Analysis Menu Options

Option	Action	Equivalent Command
Link Design	Links a library to the current design.	search_path = .tutorial/ library..., link_library = link_lib.db, link
Check Design	Checks the current design for errors.	check_design, check_timing
Time Design	Runs the Timing Analyzer on the current design.	update_timing
Show Timing	Displays the maximum and minimum rise and fall times for the selected ports.	
Show Net Load	Displays the net name, capacitance, and resistance of the highlighted net.	
Highlight	Highlights timing paths in the current design.	
Test Report	Generates and displays test reports for the current design.	
Report	Generates and displays various reports for the current design.	

The following sections provide additional information about the selections available in the Analysis Menu.

Link Design

When you choose Link Design from the Analysis menu, you see the Link Design dialog box shown in Figure 8-1. Click OK to link using the displayed search and link paths.

Figure 8-1 Link Design Dialog Box

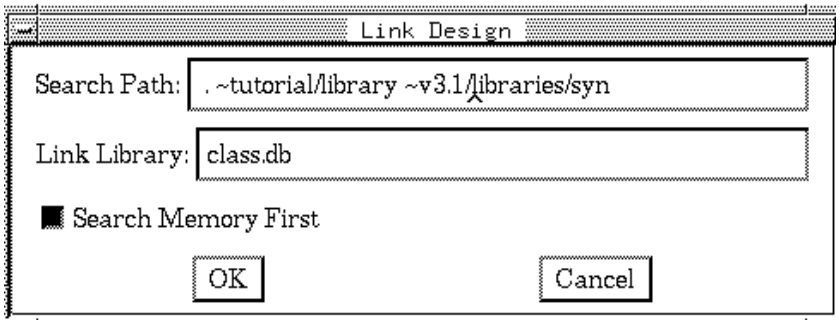


Table 8-2 explains how to use the options in the Link Design dialog box.

Table 8-2 Link Design Dialog Box Options

Option	Action	Equivalent Command
Search Path	Type the search path directories in the text box.	search_path = /search/ path
Link Library	Type the path file names in the text box.	link_library = link libraries
Search Memory First	Enable this button to search for referenced subdesigns in memory before searching the link path files.	search_path = . ~tutorial/ library..., link_library = * link_lib.db, link

Check Design

Figure 8-2 shows the Check Design dialog box. Click OK to check the current design using the displayed options. Click Cancel to remove this dialog box.

Figure 8-2 Check Design Dialog Box

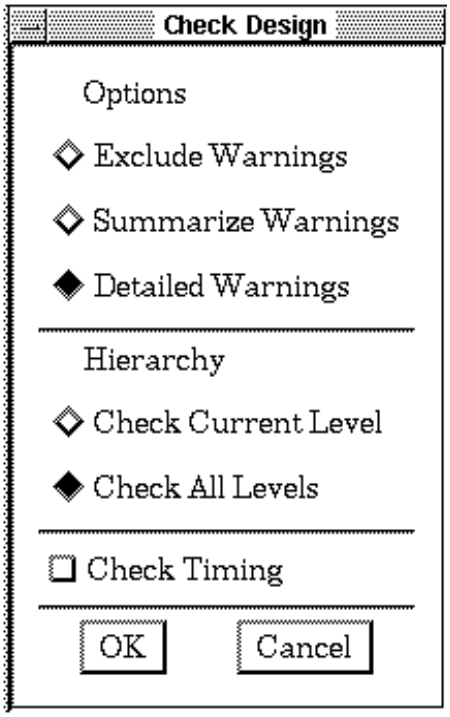


Table 8-3 explains how to use the options in the Check Design dialog box.

Table 8-3 Check Design Dialog Box Options

Option	Action	Equivalent Command
Options	Select the level of warning message desired: none (Exclude Warnings), summaries only (Summarize Warnings), or all (Detailed Warnings).	check_design, [-no_warnings] [-summary]

Table 8-3 Check Design Dialog Box Options (Continued)

Option	Action	Equivalent Command
Hierarchy	Choose which levels of the current design to check: the current level (Check Current Level) or all levels (Check All Levels).	check_design [-one_level]
Check Timing	Enable this button to check the timing attributes placed on the current design.	check_timing

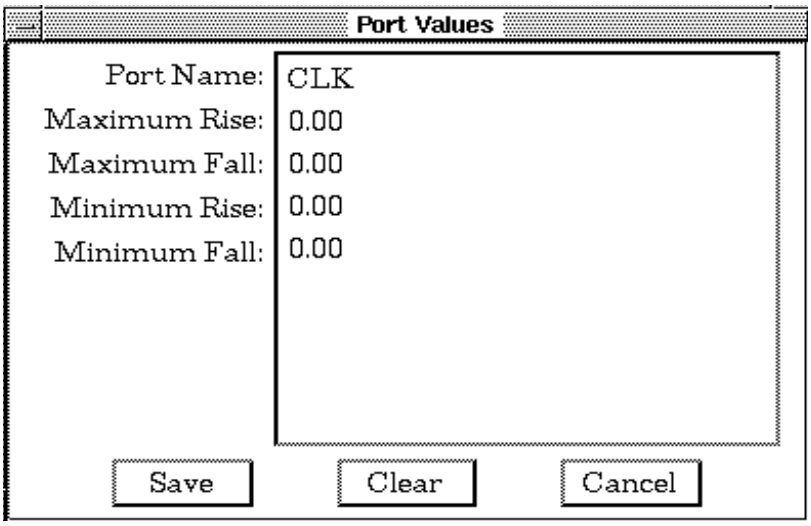
Time Design

Design Analyzer automatically runs the timing analyzer when necessary. However, when you change a design's timing attribute values, the timing analyzer is not automatically called until needed (such as for a timing report). In this case, use the Time Design selection to rederive timing values before using the pop-up menu's Show Timing selection or the Analysis > Show Timing selection.

Show Timing

When you select Show Timing for ports from the Analysis menu, you see the Port Values box shown in Figure 8-3. This dialog box displays the maximum and minimum rise and fall times for the selected port. A similar dialog box exists for selected pins.

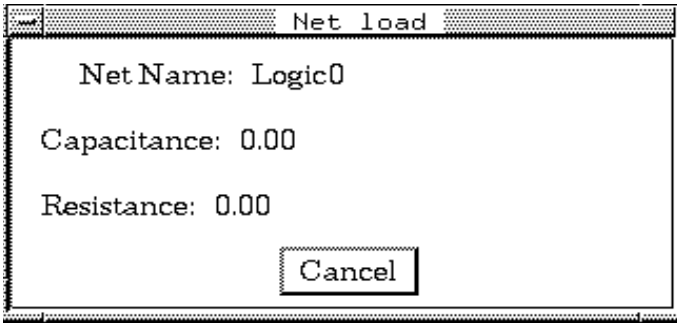
Figure 8-3 Port Values Box



Show Net Load

When you choose Show Net Load from the Analysis menu, you see the Net Load box shown in Figure 8-4. This box displays the net name, capacitance, and resistance of the highlighted net.

Figure 8-4 Net Load Box



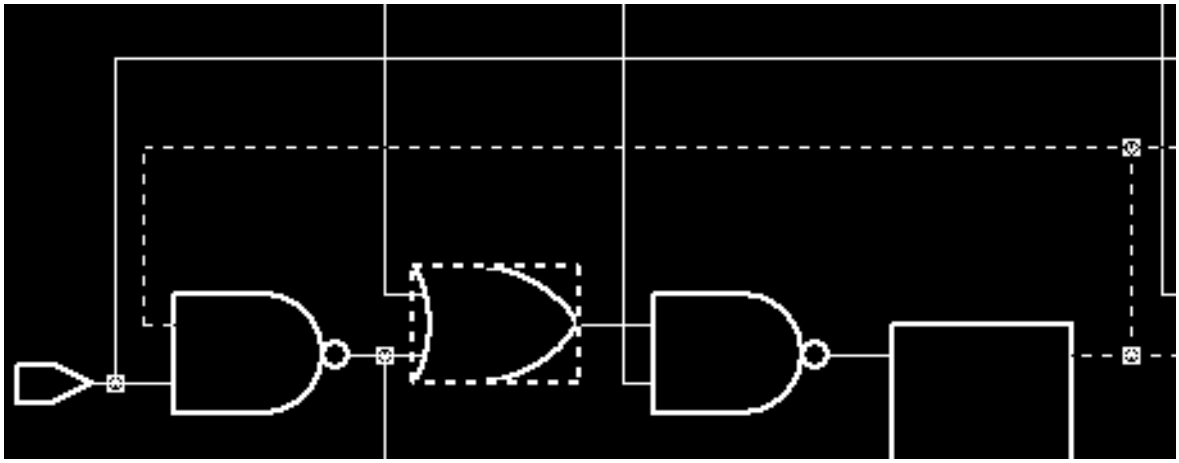
Click Cancel to remove this box.

Highlight

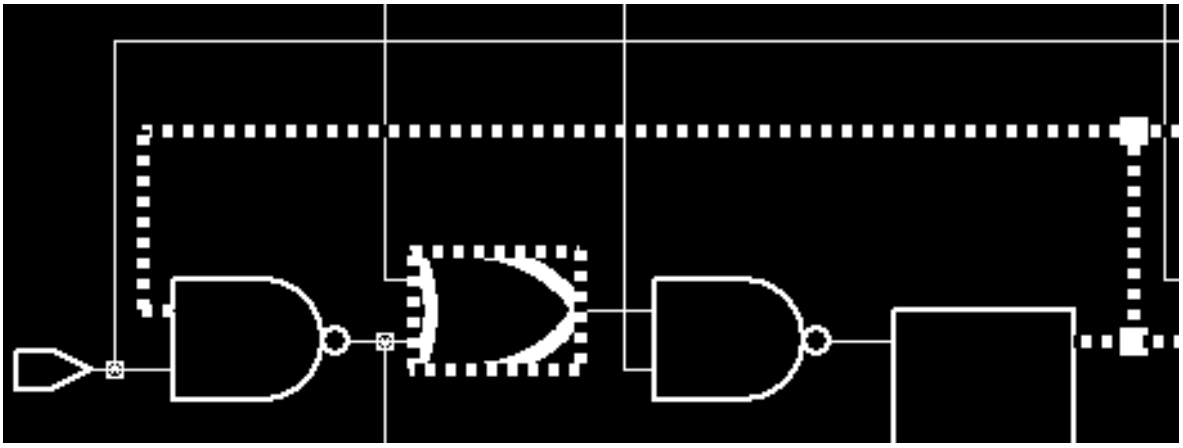
A highlighted symbol or net displays thicker lines, or in a different color, depending on the current settings of the layer highlight_layer. Use the View > Style dialog box to see and change the current settings of the highlight_layer.

To see and change the current settings,

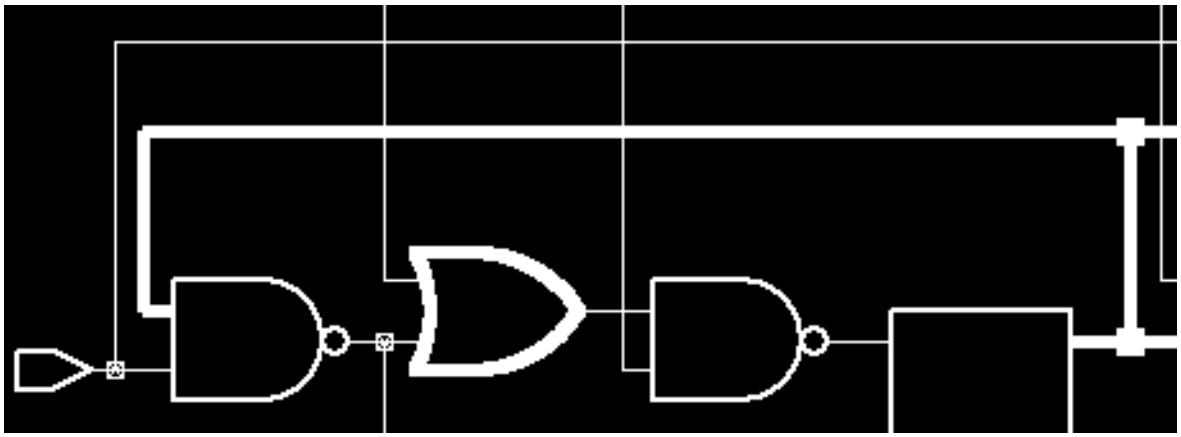
1. Select a cell and a net using the middle mouse button (the middle mouse button lets you select multiple objects).



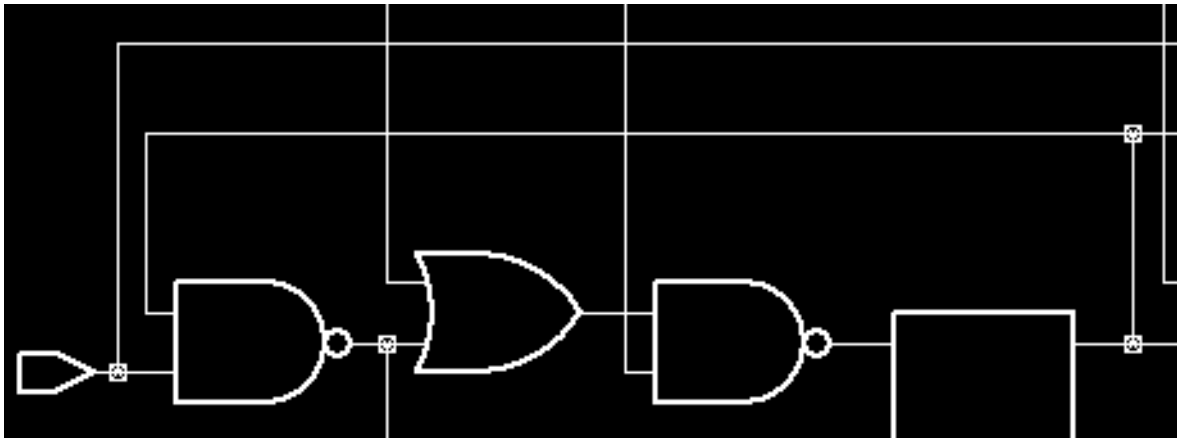
2. Use Analysis > Highlight > Selected to highlight the cell and net.



3. Deselect the cell and net by clicking the left mouse button on the background; the highlighting changes to solid lines.



4. To clear all highlighting, use Analysis > Highlight > Clear.



When you choose Highlight from the Analysis menu, you see the Highlight submenu shown in Figure 8-5.

Figure 8-5 Highlight Submenu

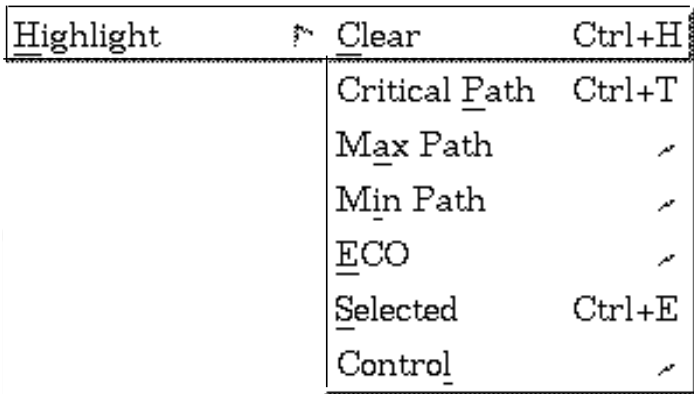


Table 8-4 explains how to use the options in the Highlight submenu options.

Table 8-4 Highlight Submenu Options

Option	Action	Equivalent Command
Clear	Clears any currently highlighted paths.	remove_highlighting -all -hier
Critical Path	Highlights the critical path.	highlight_path -critical_path
Max Path	Highlights the maximum path to the selected pin, port, net, or cell.	highlight_path find (port, {selected_item}) [-max | -max_rise | -max_fall]
Min Path	Highlights the minimum path to the selected pin, port, net, or cell.	highlight_path find (port, {selected_item}) [-min | -min_rise | -min_fall]
ECO	Highlights the old, recycled, new, spare, or obsolete cells in a design.	
Selected	Highlights the selected objects in a schematic.	
Control	Allows you to control the different highlight layers.	

The following sections provide additional information about the selections available in the Highlight option.

Clear

The Clear option clears any currently highlighted paths.

Critical Path

The Highlight option highlights the critical path.

Max Path

Using the Max Path option, you can choose

- The path with the largest overall delay (Max Path)
- The path with the largest rise delay (Max Rise)
- The path with the largest fall delay (Max Fall)

Min Path

Using the Min Path option, you can choose

- The path with the smallest overall delay (Min Path)
- The path with the smallest rise delay (Min Rise)
- The path with the smallest fall delay (Min Fall)

ECO

The ECO option is only available if you have an ECO Compiler license. For further information on ECO Compiler, see the ECO Compiler User Guide.

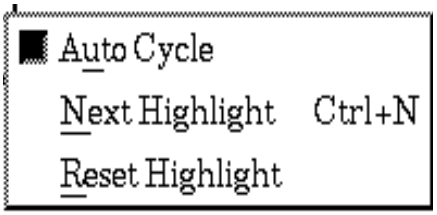
Selected

The Selected option highlights the selected objects in a schematic.

Control

When you choose Control from the Highlight submenu, you see the Control submenu shown in Figure 8-6.

Figure 8-6 Control Submenu



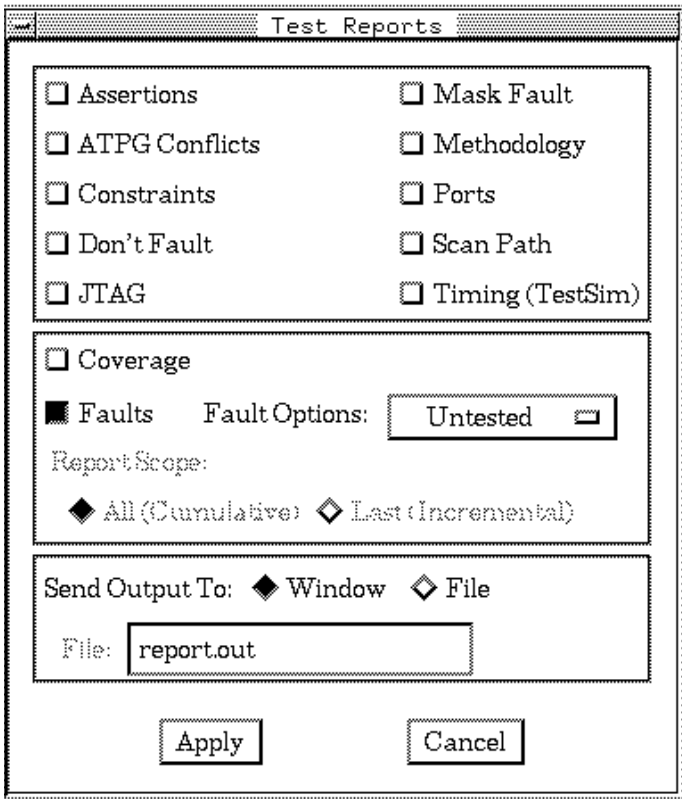
Using this submenu you to control the different highlight layers (layers named highlight_layerN, for N = 0, 1, 2, ... 9) that appear. You can cycle between the layers, which can be different colors or widths. The Auto Cycle toggle button, when set, displays each successive path in the next highlight_layer style. When all layers are displayed, the next layer is the first one defined. If Auto Cycle is not set, all displays are in the same highlight_layer style.

Next, Highlight forces the display in the next highlight_layer, even if the Auto Cycle button is not set. Reset Highlight activates the first highlight_layer defined.

Test Report

When you choose Test Report from the Analysis menu, you see the Test Reports dialog box shown in Figure 8-7.

Figure 8-7 Test Reports Dialog Box

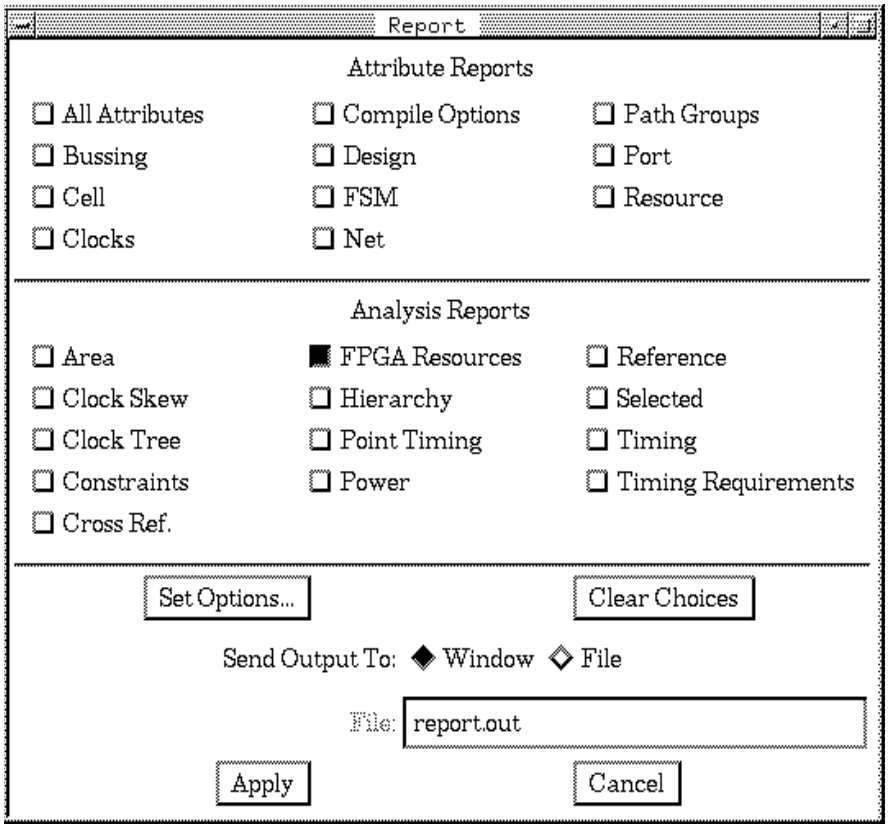


See the Tools > Test Synthesis > Display Reports description in Chapter 9, “Tools Menu,” for a description of this dialog box.

Report

When you choose Report from the Analysis menu, you see the Report dialog box shown in Figure 8-8.

Figure 8-8 Report Dialog Box



Click Apply to generate and display the chosen reports. Click Cancel to remove this dialog box.

Use the Analysis > Test Report selection to get test-related reports (report_test command).

Attribute Reports

This section of the Report dialog box contains toggle buttons corresponding to a variety of attribute reports. Table 8-5 explains how to use the options available under Attribute Reports.

Table 8-5 Attribute Reports Options

Option	Action	Equivalent Command
All Attributes	Lists the attributes and their values for all objects.	report_attributes
Bussing	Gets a report of all bused ports and bused nets in the current design.	report_bus
Cell	Gets a report of all cells in the current design and their cell attributes.	report_cell
Clocks	Gets a report of all clocks in the current design and their clock attributes. In this report, each clock links with all the schematic objects that are its sources.	report_clock -attributes
Compile Options	Gets a report of the current compile command options for the current design.	report_compile_options
Design	Gets the following current design information: target library, flip-flop types, constraints, operating conditions, wire load model and mode, timing ranges, any defined internal arrival times, and any disabled timing arcs.	report_design
FSM	Gets a report of the FSM clock name and sense, reset signal name and type, state encoding length and style, state vector flip-flops, and state encoding values and ordering.	report_fsm
Net	Gets a report of all nets in the current design; their net attributes; and their current fanout, fanin, load values, resistance, and pins.	report_net

Table 8-5 Attribute Reports Options (Continued)

Option	Action	Equivalent Command
Path Groups	Gets a report of the path groups in the current design.	report_path_group
Port	Gets a report of all ports in the current design; their port attributes; their direction; and their load, drive, arrival, transition time, and fanout values.	report_port
Resource	Gets a report of resources used in the current design.	report_resources

Analysis Reports

This section of the Report dialog box contains toggle buttons corresponding to a variety of analysis reports. Table 8-6 explains the options available in Analysis Reports.

Table 8-6 Analysis Reports Options

Option	Action	Equivalent Command
Area	Gets a report of the current design's technology library; number of ports, nets, cells, and references; and the total areas of the combination cells, noncombinational cells, nets, and the entire circuit.	report_area
Clock Skew	Gets a report on the clock network skew of the current design.	report_clock -skew
Clock Tree	Gets a report of all clock networks.	report_transitive_fanout -clock_tree
Constraints	Gets a report of all constraints set for the current design. (Set Options offers additional options.)	report_constraints

Table 8-6 Analysis Reports Options (Continued)

Option	Action	Equivalent Command
Cross Ref.	Gets a cross-reference report of the schematic objects and the sheets where they appear.	report_xref
FPGA Resources	Gets information on FPGA resource usage for Xilinx 4000 series designs.	report_fpga
Hierarchy	Gets an indented hierarchical report of all subdesigns in the current design, including subdesign names and references. (Set Options offers additional options.)	report_hierarchy
Point Timing	Lists point-to-point timing information for the selected path to the selected pin, or between two ports or pins (with only one port specified, the report reflects the point back to its source).	report_timing -path full -delay max -max_paths 1 -nworst 1 -to find(object)
Power	Gets a report of the current design's technology library, total cell power, total pin power, and total circuit power (generated only with ECL designs).	report_power
Reference	Gets a report of all references in the current design, their reference attributes, the referenced cells' technology library and area, the number of times each reference is used, and the total referenced cells' total area.	report_reference
Selected	Gets a report of the name and type of the selected objects.	report_selected
Timing	Gets a report of the timing paths' fanout and delay times. (Set Options offers additional options.)	report_timing -path full -delay max -max_paths 1 -nworst 1
Timing Requirements	Shows timing constraints, in pairs of a From object to a To object and each line is linked with a pair of schematic objects.	report_timing_requirements

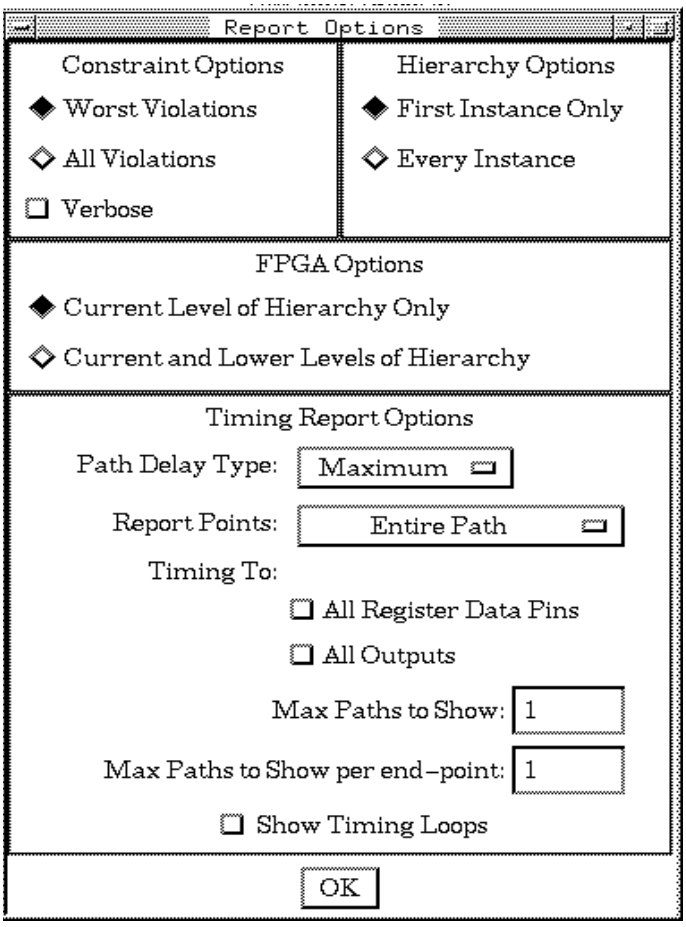
Note:

The FPGA Resources report applies only to Xilinx 4000 series designs that contain CLB and IOB cells. See the Help > Commands menu for a complete description of the report_fpga command.

Set Options

Click the Set Options button in the Report dialog box to set options for the following Analysis Reports: Constraints, Hierarchy, and Timing. The Report Options dialog box, shown in Figure 8-9, appears.

Figure 8-9 Report Options Dialog Box



Click OK to set the options as shown.

You can use the options in this dialog box only when you apply the parent (Analysis > Report) settings.

Table 8-7 explains how to use the options in the Report Options dialog box.

Table 8-7 Report Options Dialog Box Options

Option	Action	Equivalent Command
Constraint Options	Enable either the Worst Violations or All Violations.	report_constraints [-all_violators]
Verbose	Enable the Verbose button to report constraint calculations.	report_constraints -verbose
Hierarchy Options	Enable First Instance Only or Every Instance to specify how to report subdesigns referenced more than once.	report_hierarchy [-full]
FPGA Options	Enable the appropriate button to specify how you want to report FPGA resources.	report_fpga [-one_level]
Path Delay Type	Select an option from the submenu to determine what type of delay information lists in the timing report.	report_timing -delay [min | min_rise | min_fall | max | max_rise | max_fall]
Report Points	Select an option from the submenu to show information on the endpoints, the startpoints and endpoints, the entire timing path, or the path through hierarchy.	report_timing -path [end | short | full]
Timing To	Enable either button to define how to report the timing information.	
Max Paths to Show	Type the maximum number of path delays to be reported.	report_timing -max_paths number
Max Paths to Show per end-point	Type the number of paths to be reported per endpoint.	report_timing -nworst number
Show Timing Loops	Enable this button if you want only the timing loops in the design reported.	report_timing -loops

When you open the Path Delay Type option menu in the Report Options dialog box, you see the option menu shown in Figure 8-10.

Figure 8-10 Path Delay Type Option Menu

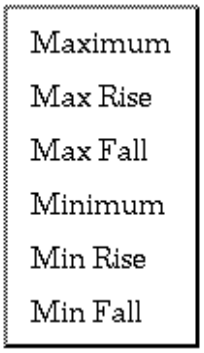
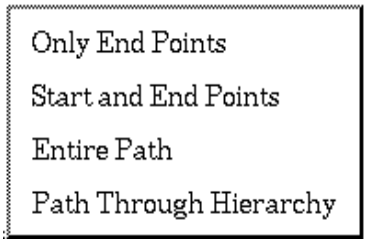


Figure 8-11 shows the option menu that appears when you select Report Points from the Report Options dialog box.

Figure 8-11 Report Points Option Menu



9

Tools Menu

This chapter describes the items in the Tools menu and the display boxes you access through it.

Using the Tools menu you can access

- Design Optimization
- Finite State Machines
- FPGA Compiler
- Test Synthesis

When you open the Tools menu, you can access the menu items shown in Figure 9-1.

Figure 9-1 Tools Menu

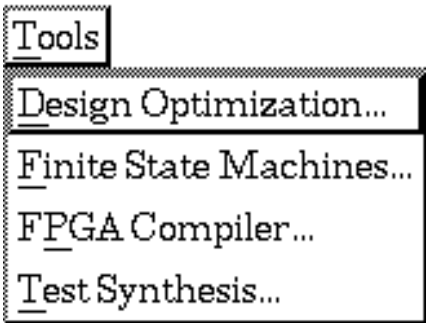


Table 9-1 explains how to use the options in the Tools menu.

Table 9-1 Tools Menu Options

Option	Action	Equivalent Command
Design Optimization	Compiles the current design.	compile
Finite State Machines	Creates a state table representation of an FSM from the current netlist-format design, or optimizes an existing FSM	
FPGA Compiler	Produces and optimizes an FPGA netlist provided it meets certain criteria	
Test Synthesis	Allows you to insert test structures into the current design	create_testsim_model, falut_simulate -eval_probables drop, read_test_protocol, report_test -inst, set_test_assume, set_test_initial, set_test_isolate, write_test_protocol, write_testsim_lib

The following sections provide additional information about the selections available in the Tools menu.

Design Optimization

When you select Design Optimization from the Tools menu, you see the Design Optimization dialog box shown in Figure 9-2.

Figure 9-2 Design Optimization Dialog Box

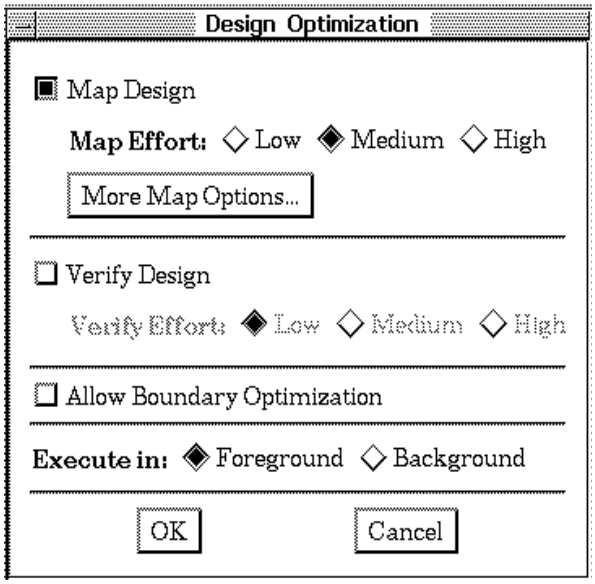


Table 9-2 explains how to use the options in the Design Optimization dialog box.

Table 9-2 Design Optimization Dialog Box Options

Option	Action	Equivalent Command
Map Design	Maps the circuit to the current technology library during compilation.	compile [-map_effort | -no_map]
Map Effort	Sets the map effort to low, medium, or high.	
More Map Options	Sets additional mapping options for the compile command if the Map Design option is enabled.	

Table 9-2 Design Optimization Dialog Box Options (Continued)

Option	Action	Equivalent Command
Verify Design	Verifies that the logical behavior of the circuit is the same before and after compilation.	compile -verify
Verify Effort	Allows you to choose the verification effort level you want enabled. (This selection is available when Verify Design is enabled.)	compile -verify_effort
Allow Boundary Optimization	Allows boundary optimization during compilation.	compile -boundary_optimization
Execute in	Allows you to specify whether the compile command runs in the foreground or background.	

The following sections provide additional information about the selections available in the Design Optimization dialog box.

Map Design

The Map Design option maps the circuit to the current technology library during compilation.

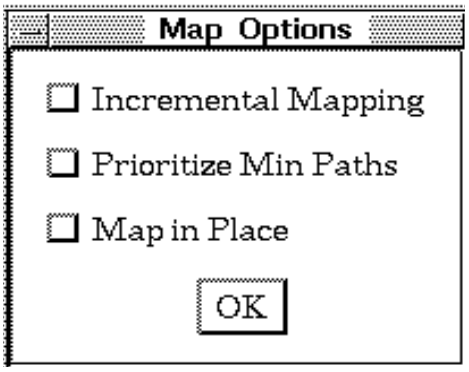
Map Effort

The Map Effort option sets the map effort to low, medium, or high.

More Map Options

Figure 9-3 shows the dialog box that appears when you select More Map Options from the Design Optimization dialog box.

Figure 9-3 Map Options Dialog Box



Click OK to set the options as shown. Table 9-3 describes the Map Options dialog box.

Table 9-3 Map Options Dialog Box Options

Option	Action	Equivalent Command
Incremental Mapping	Maps the circuit using only local mapping transformations that improve the circuit.	compile -incremental_mapping
Prioritize Min Paths	Gives priority to minimum path delays during mapping.	compile -prioritize_min_paths
Map in Place	Maps the circuit in place. See the Design Compiler Reference Manual: Fundamentals for details on in-place optimization.	compile -in_place

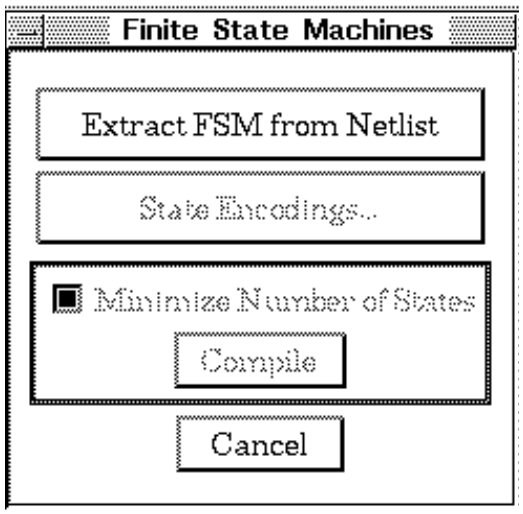
Execute in

Using the Execute in option you can specify whether the compile command runs in the foreground or background.

Finite State Machines

When you choose Finite State Machines from the Tools menu, you see the Finite State Machines dialog box shown in Figure 9-4.

Figure 9-4 Finite State Machines Dialog Box



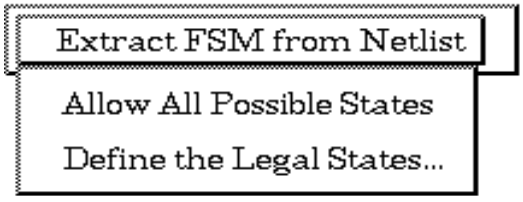
To create a subdesign containing only the finite state machine related logic,

1. Select the state vector flip-flops.
2. Use Edit > Group with the Group FSM Logic toggle button enabled.
3. Click Cancel to remove this dialog box.

Extract FSM from Netlist

Click the Extract FSM from Netlist button to extract a finite state machine (FSM) from the current design. The menu options, shown in Figure 9-5, appear. Extract all possible states or define the legal subset of states using this netlist menu option.

Figure 9-5 Extract FSM from Netlist Option Menu



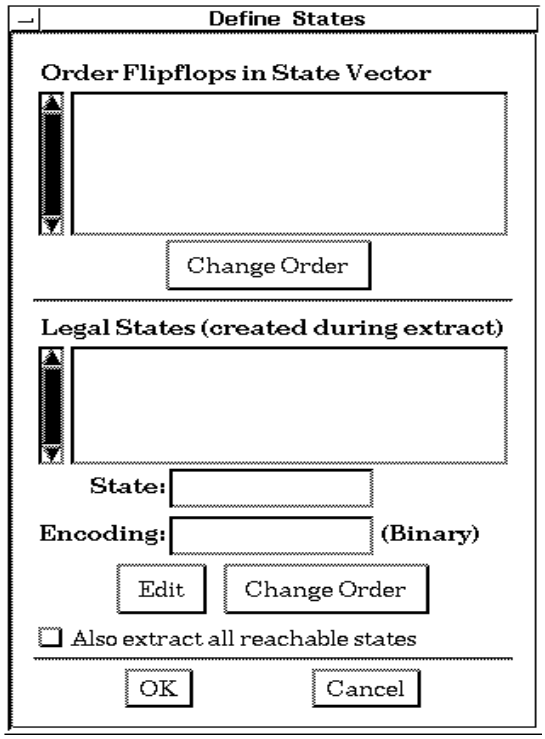
Allow All Possible States

Use this option to extract an FSM 2n (n = number of flip-flops) automatically encoded states. (If the design has 3 flip-flops, Allow All Possible States creates 8 states.)

Define the Legal States

Use the dialog box in Figure 9-6 to define the valid subset of the possible states.

Figure 9-6 Define States Dialog Box



Click OK to define the state vector flip-flops, order of the flip-flops, and state names and encoding values, as shown. Click Cancel to remove this dialog box.

Table 9-4 and the information in the following sections explain how to use the options in the Define States dialog box.

Table 9-4 Define States Dialog Box Options

Option	Action	Equivalent Commands
Order Flip-Flops in State Vector	Shows the names of all flip-flops in the current design.	set_fsm_state_vector
Legal States	Shows all legal states and allows you to add, delete, or reorder states.	set_fsm_encoding, set_fsm_order
Also extract all reachable states	Allows you to specify that any state that can be reached from a legal state is considered legal and is extracted.	extract -reachable

Order Flip-Flops in State Vector

Each of the flip-flops holds one bit of the FSM state vector. Use the Change Order dialog box to define the order of the state vector flip-flops, from MSB (top) to LSB (bottom).

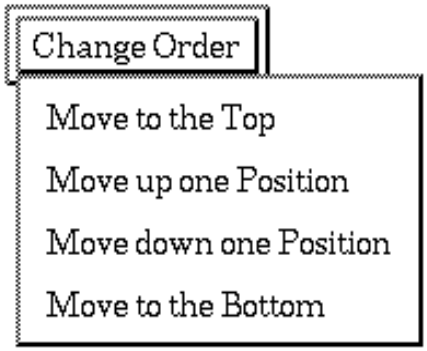
To change the relative position of a flip-flop,

1. Click a state vector flip-flop name.
2. Click Change Order.

   When you select Change Order from the Define States dialog box, you see the option menu in Figure 9-7.

   The order of state names is relevant only when using automatic encoding. For more information, see the following section, “State Encodings” on page 9-11.

Figure 9-7 Change Order Option Menu



Legal States

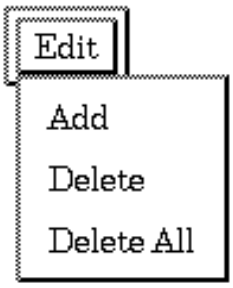
Use the Define States dialog box to define the state names and encoding values.

To add a state,

1. Type its name in the State text box and its binary encoding in the Encoding text box.
2. Select Edit > Add.

   When you select Edit from the Define dialog box, you see the option menu shown in Figure 9-8.

Figure 9-8 Edit Option Menu



To remove a state,

1. Click the state name.

2. Select Edit > Delete.

To remove all states, select Edit > Delete All.

To change a state's order,

1. Click the state name.
2. Click Change Order and specify its new position.

Also extract all reachable states

Using this option, you can specify that any state that can be reached from a legal state is considered legal and is extracted.

State Encodings

When you click State Encodings in the Finite State Machine dialog box, you see the Encode States dialog box shown in Figure 9-9.

Figure 9-9 Encode States Dialog Box

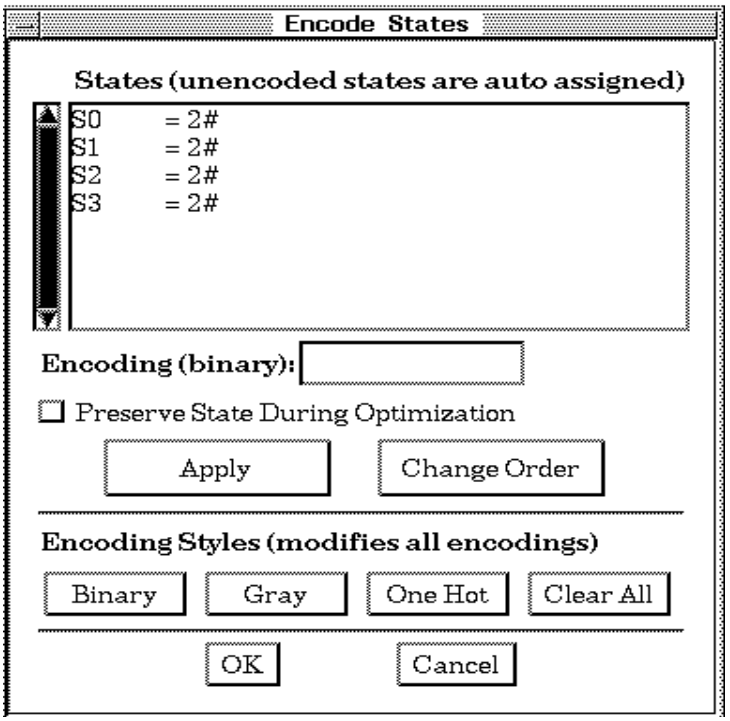


Table 9-5 and the information in the following sections explain how to use the options in the Encode States dialog box.

Table 9-5 Encode States Dialog Box

Selection	Description	Equivalent Command
Encoding	Changes a state's encoding	set_fsm_encoding
Preserve State During Optimization	Preserves a state during optimization	set_fsm_preserve_state
Change Order	Changes a state's order	set_fsm_order
Encoding Styles	Assigns encoding styles for states	

Encoding

To change a state's encoding,

1. Select the state name.
2. Edit its binary encoding value.
3. Click Apply.

Preserve State during Optimization

To Preserve a state during optimization,

1. Select the state name.
2. Enable the Preserve State During Optimization button.
3. Click Apply.

Change Order

To specify a new position,

1. Select the state name.
2. Click Change Order.

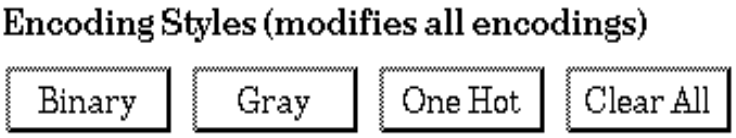
   See Figure 9-7 on page 9-10 to view the dialog box that appears when you select Change Order.

   The ordering of state names is relevant only when using automatic encoding (see "State Encodings" on page 9-11).

Encoding Styles

Click one of the buttons, shown in Figure 9-10, to automatically assign all state encodings.

Figure 9-10 Encoding Style Options



The Binary, Gray, and One Hot encoding styles generate encodings for all states and display these encodings in the States list. You can then edit the states' ordering and encodings as previously described.

The Clear All button clears all state encodings. During compilation, any unencoded states encode using auto encoding.

Minimize Number of States

Enable the Minimize Number of States button in the Finite State Machines dialog box to minimize the number of states during compilation. Equivalent or redundant states are collapsed. An equivalent command to this option is set_fsm_minimize set to true.

Compile

Click the Compile button in the Finite State Machine dialog box to compile an FSM (state table format) into an optimized circuit. The Design Optimization dialog box appears.

FPGA Compiler

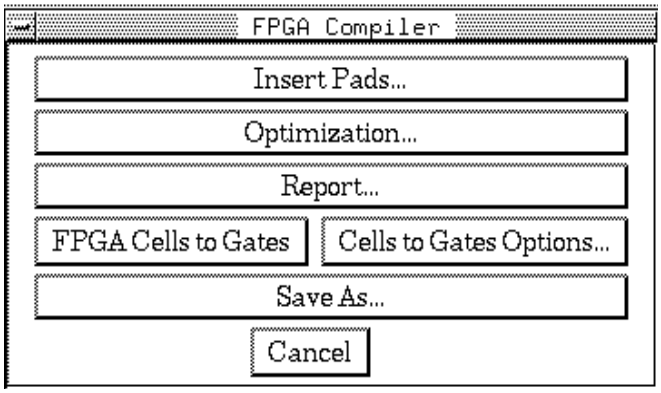
FPGA devices consist of programmable logic cells and programmable interconnects. The FPGA Compiler can produce and optimize an FPGA netlist provided that

- The technology of the target library is FPGA.
- The security key for the FPGA product is enabled.

For most FPGA designs, the compile command produces a netlist that references macrocells for the target vendor's FPGA technology. However, for a Xilinx FPGA design (4000 series devices), the compile command produces a netlist that references only CLB, IOB, TBUF, and a limited number of special cells in an FPGA library. By explicitly representing CLBs and IOBs in the netlist, the FPGA Compiler can provide improved estimations of area and delay as well as improved algorithms for optimizing FPGA designs. See the Design Compiler Reference Manual: Fundamentals for more details.

When you choose FPGA Compiler from the Tools menu, you see the FPGA Compiler dialog box shown in Figure 9-11.

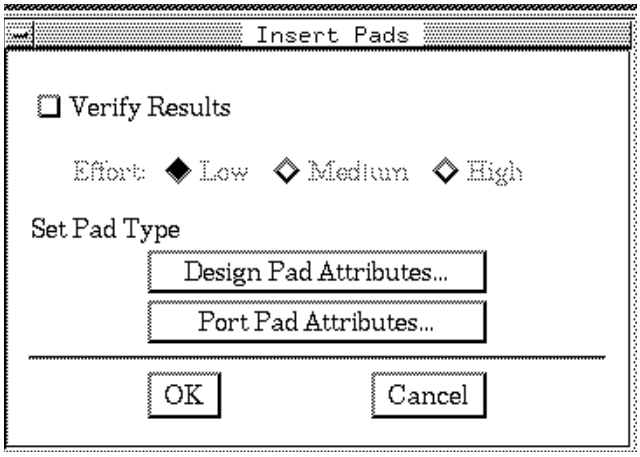
Figure 9-11 FPGA Compiler Dialog Box



Insert Pads

Click the Insert Pads button to display the Insert Pads dialog box illustrated in Figure 9-12. This dialog box is also available from the Edit menu (Edit > Insert Pads).

Figure 9-12 Insert Pads Dialog Box



Use this dialog box to

- Turn verification on or off.
- Select the verification effort.
- Set pad types.

Click OK to set the options and values as shown. Click Cancel to remove the dialog box.

Table 9-6 and the following sections describe the options available in the Insert Pads dialog box.

Table 9-6 Insert Pads Dialog Box Options

Option	Action	Equivalent Command
Verify Results	Enable this button to verify that the logical behavior of the circuit is the same before and after pads are inserted.	insert_pads -verify
Effort	Choose the verification level. Buttons become available when Verify Results is enabled.	insert_pads [-verify_effort effort]
Design Pad Attributes	Click this button to display the Design Pad Attributes dialog box.	
Port Pad Attributes	Click this button to display the Port Pad Attributes dialog box.	

Verify Results

Enable the Verify results button to verify that the logical behavior of the circuit is the same before and after pads are inserted.

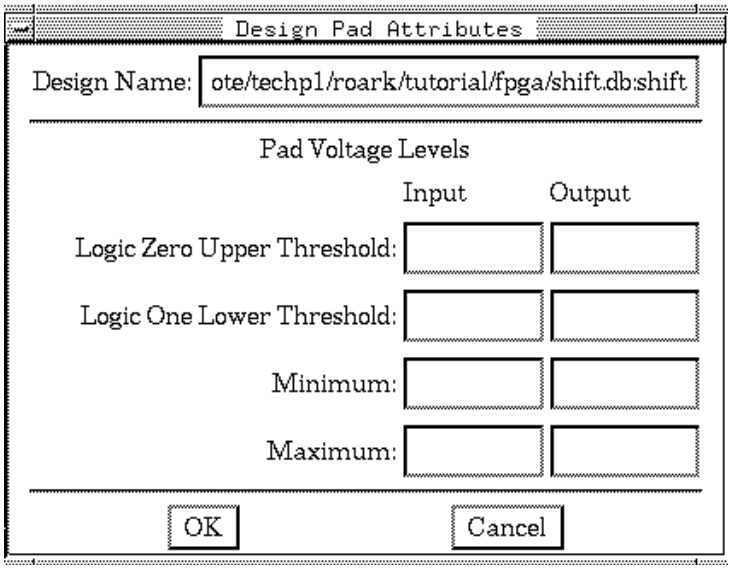
Effort

Choose the verification level. Buttons become available when Verify Results is enabled.

Design Pad Attributes

Figure 9-13 shows the dialog box that appears when you choose the Design Pad Attributes option.

Figure 9-13 Design Pad Attributes Dialog Box



Use this dialog box to define the input and output voltage levels for the pads in a design. Click OK to set the options and values as shown. Click Cancel to remove this dialog box.

Table 9-7 explains how to use the options in the Design Pad Attributes dialog box.

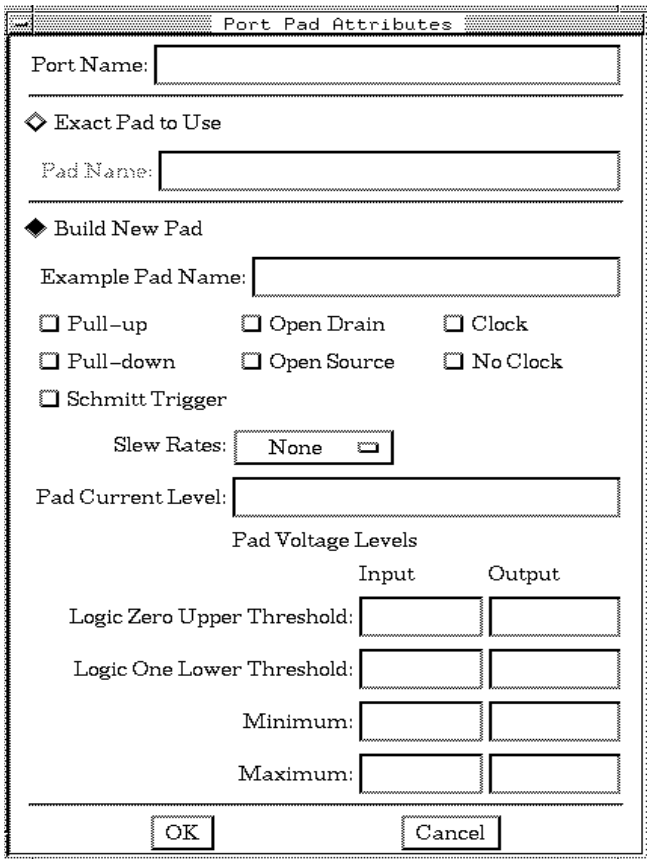
Table 9-7 Design Pad Attributes Dialog Box Options

Option	Action	Equivalent Commands
Design Name	View the name of the current design.	
Pad Voltage Levels	Use these text boxes to define the pad voltage levels for a design.	set_pad_type [-vih value] [-vil value][-vimax value] [-vimin value][-voh value] [-vol value][-vomax value] [-vomin value]

Port Pad Attributes

When you choose Port Pad Attributes from the Insert Pads dialog box, you see the Port Pad Attributes dialog box shown in Figure 9-13.

Figure 9-14 Port Pad Attributes Dialog Box



Use this dialog box to define the pad cell type, pad cell characteristics, slew rate, pad current level, and pad voltage levels for a port. Click OK to set the options and values as shown. Click Cancel to remove this dialog box.

Table 9-8 explains how to use the options in the Port Pad Attributes dialog box.

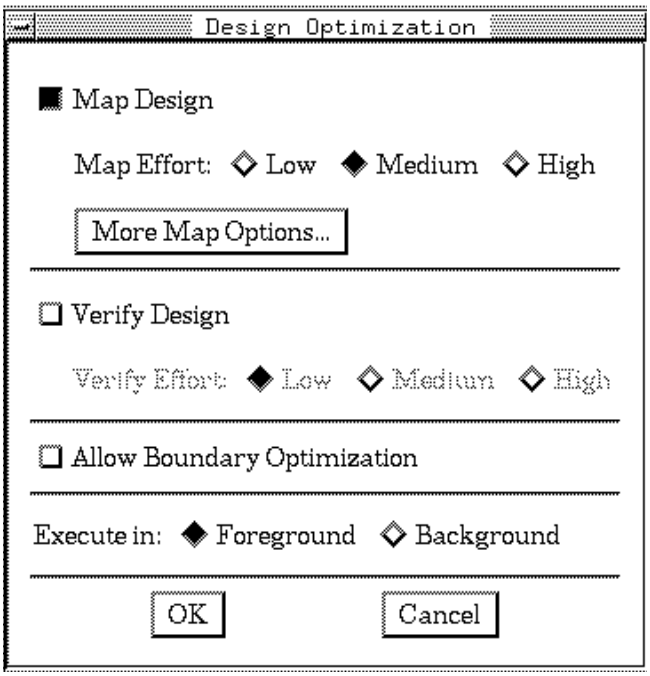
Table 9-8 Port Pad Attributes Dialog Box Options

Option	Action	Equivalent Command
Port Name	View the port name if a single port is already selected; if more than one port is selected or you don't select a port, the field is blank.	
Pad Name	Define a pad name by turning on the Exact Pad to Use button, and type the pad cell name.	set_pad_type [-exact exact_pad]
Example Pad Name	Define nonfunctional characteristics of the pad by inference of library information of a pad example by turning on the Build New Pad button, and type the pad example name.	set_pad_type [-example example_pad]
Pad Characteristic Buttons	Use these buttons to select characteristics of the pad such as pull-up or pull-down resistors, Schmitt trigger, clock, and so on.	set_pad_type [-opendrain] [-opensource] [-pulldown] [-pullup] [-schmitt] [-clock] [-no_clock]
Slew Rates	Use this button to set the slew rate of the pad.	set_pad_type [-slewrate low | medium | high]
Pad Current Level	Type the minimum current rating (mA) for the pad in this text box.	set_pad_type [-currentlevel value]
Pad Voltage Levels	Use these text boxes to define pad voltage levels.	set_pad_type [-vih value] [-vil value] [-vimax value] [-vimin value] [-voh value] [-vol value] [-vomax value] [-vomin value]

Optimization

When you click the Optimization button in the FPGA Compiler dialog box, you see the Design Optimization dialog box shown in Figure 9-15.

Figure 9-15 Design Optimization Dialog Box



Click OK to compile the current design using the displayed options. Click Cancel to remove this dialog box.

Table 9-9 and the following sections explain how to use the options in the Design Optimization dialog box.

Table 9-9 Design Optimization Dialog Box Options

Option	Action	Equivalent Command
Map Design	Maps the circuit to the current technology library during compilation.	compile [-map_effort | -no_map]

Table 9-9 Design Optimization Dialog Box Options (Continued)

Option	Action	Equivalent Command
Map Effort	Sets the map effort to low, medium, or high.	
More Map Options	Sets additional mapping options for the compile command.	
Verify Design	Verifies that the logical behavior of the circuit is the same before and after compilation.	compile_verify
Verify Effort	Allows you to choose the verification level (available when the Verify Design button is enabled).	compile [-verify_effort effort]
Allow Boundary Optimization	Allows boundary optimization during compile.	compile [-boundary_optimization]
Execute in	Allows you to define whether the compile command is to run in the foreground or background.	

Map Design

Maps the circuit to the current technology library during compilation.

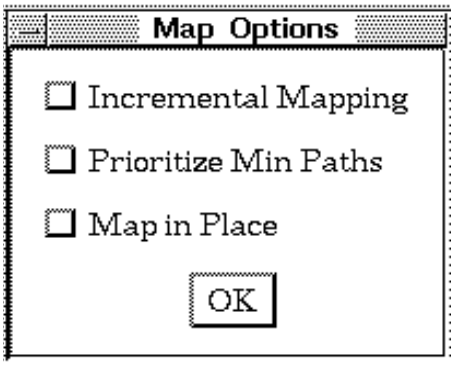
Map Effort

You use these toggle buttons to set the map effort to low, medium, or high.

More Map Options

You can use the dialog box shown in Figure 9-16 to set additional mapping options for the compile command.

Figure 9-16 Map Options Dialog Box



Click OK to set the options as shown. Table 9-10 explains how to use the options in the Map Options dialog box.

Table 9-10 Map Options Dialog Box Options

Option	Action	Equivalent Command
Incremental Mapping	Enable this button to map the circuit using only local mapping transformations that improve the circuit.	compile -incremental_mapping
Prioritize Min Paths	Enable this button to give priority to minimum path delays during mapping.	compile -prioritize_min_paths
Map in Place	Enable this button to map the circuit in place. See the Design Compiler Reference Manual: Fundamentals for information on in-place optimization.	compile -in_place

Verify Design

Using the Verify Design option from the Design Optimization dialog box, you can verify that the logical behavior of the circuit is the same before and after compilation.

Verify Effort

Using the Verify Effort option from the Design Optimization dialog box, you can choose the verification level. This option is available only when the Verify Design button is enabled.

Allow Boundary Optimization

Using the Allow Boundary Optimization option from the Design Optimization dialog box, you allow boundary optimization during compile.

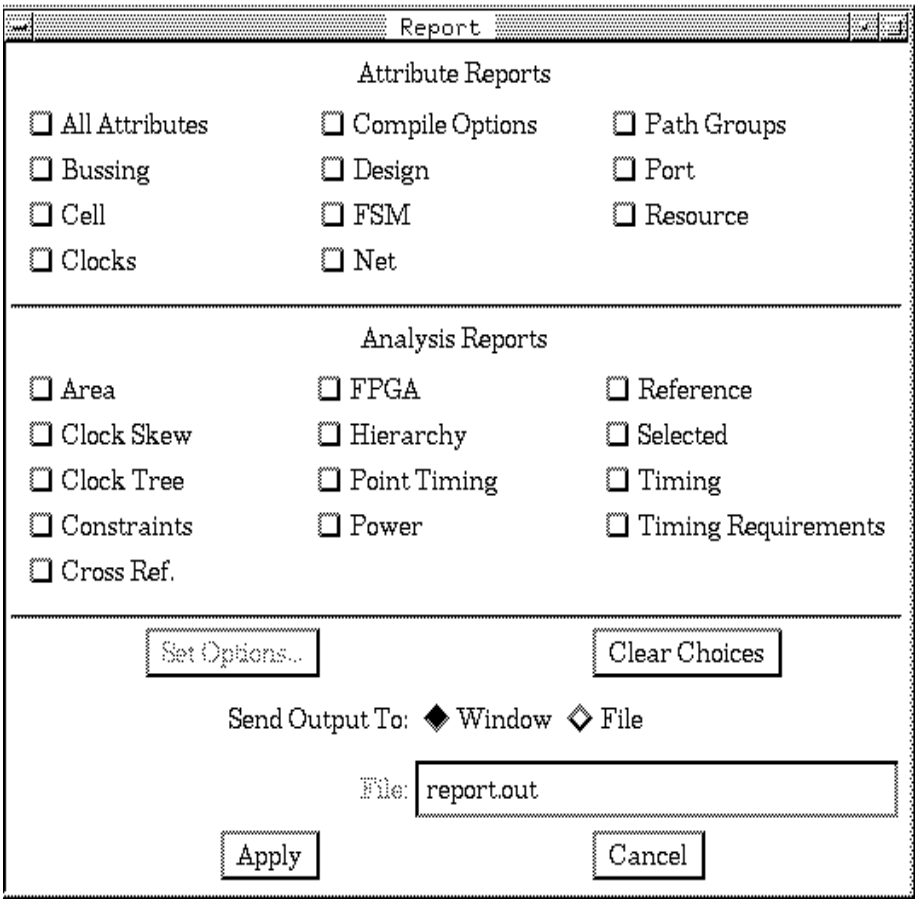
Execute in

Using the Execute in option from the Design Optimization dialog box, you can define whether the compile command is to run in the foreground or background.

Report

When you click the Report button in the FPGA Compiler dialog box, you see the Report dialog box shown in Figure 9-16. You can also open this dialog box by choosing Report from the Analysis menu.

Figure 9-17 Report Dialog Box

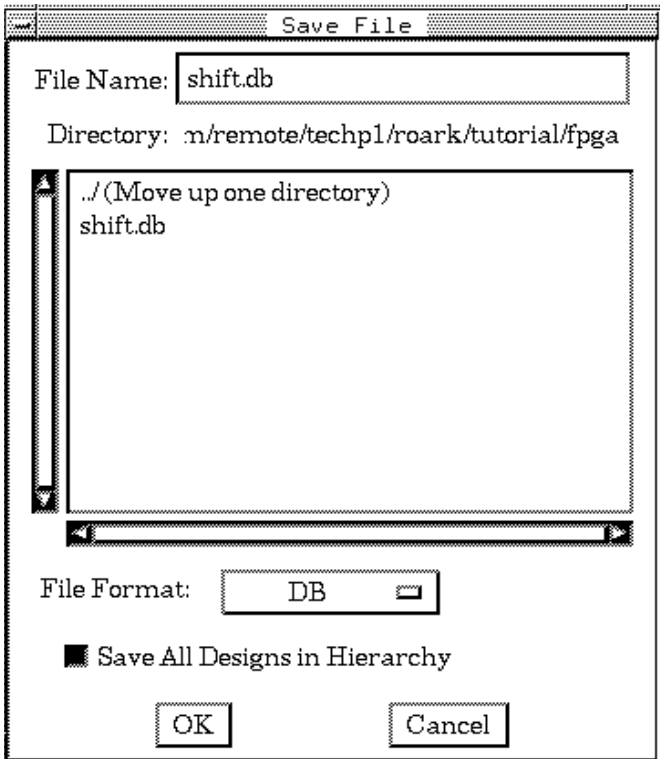


Click Apply to generate and display the chosen reports. Click Cancel to remove this dialog box. See Chapter 8, “Analysis Menu,” for more information on the Report dialog box.

Save As

Click the Save As button to display the dialog box illustrated in Figure 9-18.

Figure 9-18 Save File Dialog Box

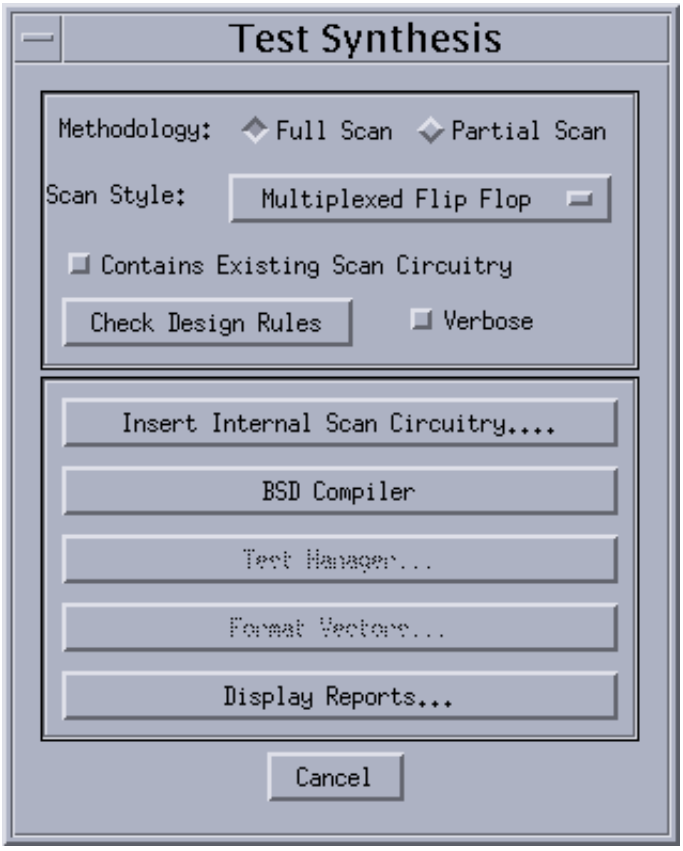


Click OK to set the options and values as shown. Click Cancel to remove this dialog box. See Chapter 4, “File Menu,” for more information on the Save File dialog box.

Test Synthesis

With this dialog box, shown in Figure 9-19, you can insert test structures into the current design.

Figure 9-19 Test Synthesis Dialog Box



Click Cancel to remove this dialog box.

The following commands are available only through the Command Window's command-line interface:

```
create_testsim_model, read_test_protocol, report_test
-inst, set_test_assume, set_test_initial, set_test_isolate,
set_test_unmask_fault, write_test_protocol,
write_testsim_lib.
```

Table 9-11 and the following sections explain how to use the options in the Test Synthesis dialog box.

Table 9-11 Test Synthesis Dialog Box Options

Option	Action	Equivalent Command
Methodology	Obsolete command—use `set_scan_configuration -methodology` instead)	
Scan Style	Obsolete command—use `set_scan_configuration -style` instead)	
Contains Existing Scan Circuitry	Obsolete command—use `set_scan_configuration -methodology` instead)	
Check Design Rules	Click this button to check the design for test design-rule violations.	check_test
Verbose	Select this option to get a detailed report from Check Design Rules.	check_test -verbose
Insert Internal Scan Circuitry	Click this button to display the Insert Internal Scan Circuitry dialog box, in which you define how to insert test scan cells and route the test scan path.	
BSD Compiler	Click this button to display the BSD Compiler dialog box, in which you set up, generate, optimize, check, and save ANSI/IEEE Std 1149.1-compliant boundary-scan circuitry.	
Test Manager	This option is obsolete.	
Format Vectors	This option is obsolete.	
Display Reports	Click this button to create test reports for the current design.	

Methodology

This command is obsolete. Instead, use the `set_scan_configuration -methodology` command.

Scan Style

This command is obsolete. Instead, use the `set_scan_configuration -style` command.

Contains Existing Scan Circuitry

This command is obsolete. Instead, use the `set_scan_configuration -methodology` command.

Check Design Rules

Enable the Verbose toggle button to get a report listing each design-rule violation. A linked report window named Design Rule Errors is created, listing all types of design-rule violations found. Click a TEST warning or error message, then click the report window's Show button to see a schematic with the affected cell, pin, or port selected. For more information, see Chapter 2, "Using Design Analyzer."

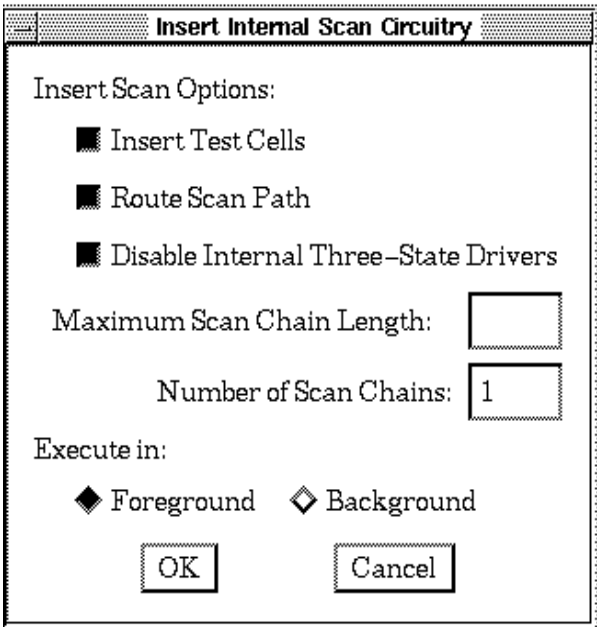
Verbose

Enable the Verbose button to get a detailed report from Check Design Rules.

Insert Internal Scan Circuitry

When you click Insert Internal Scan Circuitry in the Test Synthesis dialog box, you see the Insert Internal Scan Circuitry dialog box shown in Figure 9-20. Use this dialog box to define how to insert test scan cells and route the test scan path.

Figure 9-20 Insert Internal Scan Circuitry Dialog Box



Click OK to compile in test structures as shown. Click Cancel to remove this dialog box.

Table 9-12 explains how to use the options in the Insert Internal Scan Circuitry dialog box.

Table 9-12 Insert Internal Scan Circuitry Dialog Box Options

Option	Action	Equivalent Command
Insert Scan Options	Enable these buttons to build the scan path, route the scan path, and disable three-state logic.	set_scan_configuration -replace true -route true -disable true

Table 9-12 Insert Internal Scan Circuitry Dialog Box Options (Continued)

Option	Action	Equivalent Command
Maximum Scan Chain Length	This option is obsolete.	
Number of Scan Chains	Type the number of scan chains to create.	iset_scan_configuration -chain_count
Execute in	Choose whether the insert_scan command is run in the foreground or background.	

BSD Compiler

When you click BSD Compiler in the Test Synthesis dialog box, you see the BSDS Compiler dialog box shown in Figure 9-21.

Figure 9-21 BSD Compiler Dialog Box

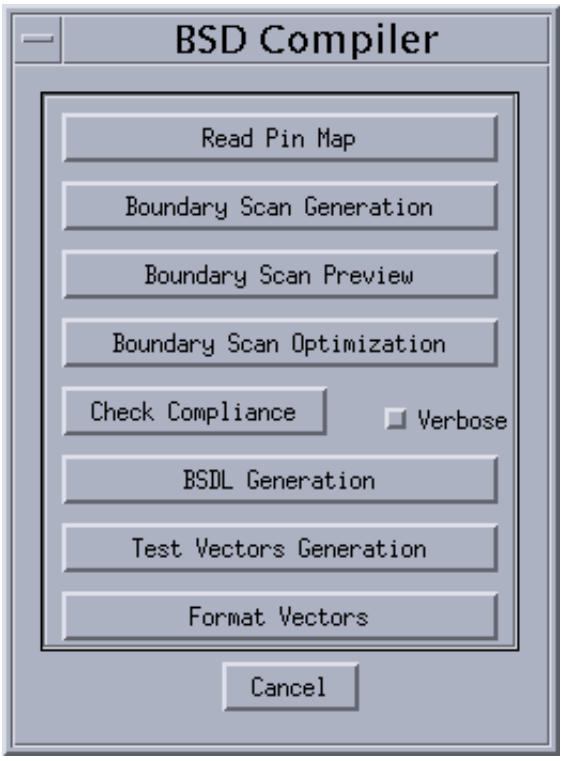


Table 9-13 and the following section explains how to use the options in the BSD Compiler dialog box.

Table 9-13 BSD Compiler Dialog Box Options

Option	Action	Equivalent Command
Read Pin Map	Click to open the BSDL Generation dialog box, in which you specify the pin map file name.	
Boundary Scan Generation	Click to open the Boundary Scan Generation dialog box, which you use to set up and generate the boundary scan circuitry for the current design.	

Table 9-13 BSD Compiler Dialog Box Options (Continued)

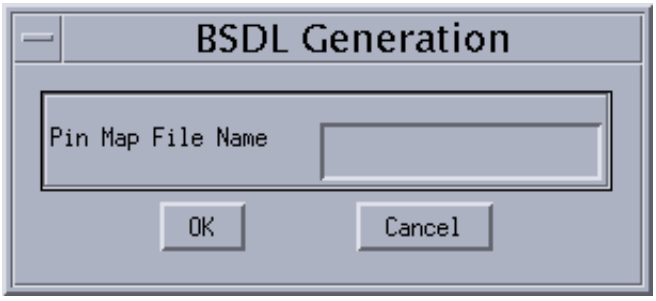
Option	Action	Equivalent Command
Boundary Scan Preview	Click to open the Boundary Scan Preview dialog box, which you can use to preview the boundary scan circuitry for the current design.	
Boundary Scan Optimization	Click to open the Boundary Scan Optimization dialog box, which you use to optimize the boundary-scan circuitry for the current design.	
Check Compliance	Click this button to check the boundary-scan implementation in the current design for compliance with ANSI/IEEE standard 1149.1.	check_bsd
Verbose	Enable this button to get a detailed report from Check Compliance.	check_bsd -verbose
BSDL Generation	Click to open BSDL Generation dialog box, which you use to generate an output file containing the boundary-scan description for the current design.	
Test Vector Generation	Click to open the Test Vector Generation dialog box, which you use to generate a test program file containing the boundary-scan test patterns for the current design.	
Format Vectors	Click to open the Format Vectors dialog box, which you use to assemble the scan and functional test patterns generated for the current design into a series of test program files that are suitable for use with automated test equipment (ATE) or simulators.	

After you setup, generate, and optimize the boundary-scan circuitry, click the Check Compliance button to check the boundary-scan implementation. If you want to get a detailed report from Check Compliance, select the Verbose option.

Read Pin Map

When you click the Read Pin Map button in the BSD Compiler dialog box, you see the BSDL Generation dialog box shown in Figure 9-22.

Figure 9-22 BSDL Generation Dialog Box



Enter the name of the file that contains the port-to-pin mapping for the current design and click the OK button.

Boundary Scan Generation

When you click this button in the BSD Compiler dialog box, you see the Boundary Scan Generation dialog box shown in Figure 9-23. Use this dialog box to synthesize ANSI/IEEE Std 1149.1-compliant boundary-scan circuitry, based on DesignWare macro cells, for the current design.

Figure 9-23 Boundary Scan Generation Dialog Box

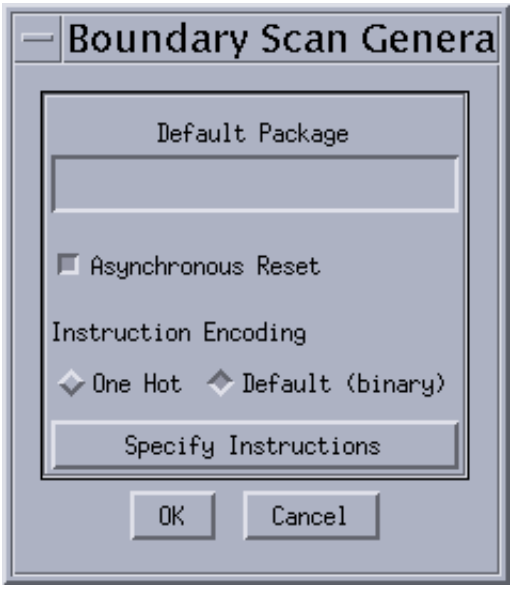


Table 9-14 explains how to use the options in the Boundary Scan Generation dialog box.

Table 9-14 Boundary Scan Generation Dialog Box Options

Option	Action	Equivalent Command
Default Package	Enter the name of the correspondence package to use as the reference. This package name must correspond to one of the packages in the pin map file.	set_bsd_configuration -default_package package_name
Asynchronous Reset	Enable this option if you want the synthesized boundary-scan circuitry to include an asynchronous test logic reset port. If this option is disabled, you must provide a power-up reset mechanism.	set_bsd_configuration -asynchronous_reset [true | false]
One Hot	Select this option to use the one hot encoding method, which encodes each operation code with one bit set to 1 and the other bits set to 0.	set_bsd_configuration -instruction_encoding one_hot

Table 9-14 Boundary Scan Generation Dialog Box Options (Continued)

Option	Action	Equivalent Command
Default (binary)	Select this option to use the default encoding method, which encodes the instructions with a minimum number of bits.	set_bsd_configuration -instruction_encoding default
Specify Instructions	Click to open the Specify Instructions dialog box, which you can use to add or remove instructions.	set_bsd_instruction instruction_list

When you click the Specify Instructions button in the Insert Boundary Scan Generation dialog box, you see the Specify Instructions dialog box. To add an instruction, select it and click the Add button. To remove and instruction, select it and click the Delete button.

Boundary Scan Preview

When you click this button in the BSD Compiler dialog box, you see the Boundary Scan Preview dialog box shown in Figure 9-24. Use this dialog box to set up and generate a preview report of the boundary-scan circuitry specified for the current design.

Figure 9-24 Boundary Scan Preview Dialog Box

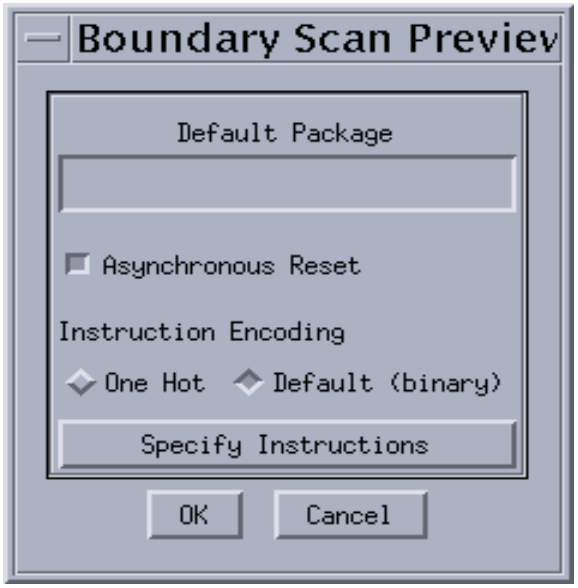


Table 9-15 explains how to use the options in the Boundary Scan Preview dialog box.

Table 9-15 Boundary Scan Preview Dialog Box Options

Option	Action	Equivalent Command
Default Package	Enter the name of the correspondence package to use as the reference. This package name must correspond to one of the packages in the pin map file.	set_bsd_configuration -default_package package_name
Asynchronous Reset	Enable this option if you want the synthesized boundary-scan circuitry to include an asynchronous test logic reset port. If this option is disabled, you must provide a power-up reset mechanism.	set_bsd_configuration -asynchronous_reset [true | false]
One Hot	Select this option to use the one hot encoding method, which encodes each operation code with one bit set to 1 and the other bits set to 0.	set_bsd_configuration -instruction_encoding one_hot

Table 9-15 Boundary Scan Preview Dialog Box Options (Continued)

Option	Action	Equivalent Command
Default (binary)	Select this option to use the default encoding method, which encodes the instructions with a minimum number of bits.	set_bsd_configuration -instruction_encoding default
Specify Instructions	Click to open the Specify Instructions dialog box, which you can use to add or remove instructions.	set_bsd_instruction instruction_list

When you click the Specify Instructions button in the Insert Boundary Scan Generation dialog box, you see the Specify Instructions dialog box. To add an instruction, select it and click the Add button. To remove and instruction, select it and click the Delete button.

Boundary Scan Optimization

When you click this button in the BSD Compiler dialog box, you see the Boundary Scan Optimization dialog box shown in Figure 9-25. Use this dialog box to optimize ANSI/IEEE Std 1149.1-compliant boundary-scan circuitry, based on DesignWare macro cells, for the current design.

Figure 9-25 Boundary Scan Optimization Dialog Box

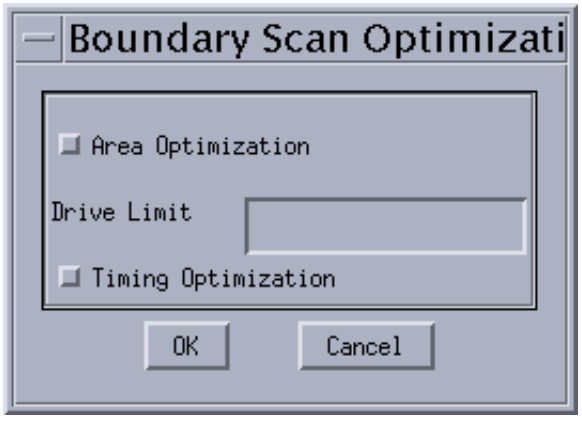


Table 9-16 explains how to use the options in the Boundary Scan Optimization dialog box.

Table 9-16 Boundary Scan Optimization Dialog Box Options

Option	Action	Equivalent Command
Area Optimization	Enable this option to optimize the allocation of boundary-scan register (BSR) control cells during area optimization. This option takes affect only if the design contains maximum area constraint violations.	test_bsd_optimize_control_cell
Drive Limit	Enter the drive limit value you want to use to allocate BSR cells during area optimization when the Area Optimization option is enabled.	test_bsd_control_all_drive_limit

Table 9-16 Boundary Scan Optimization Dialog Box Options (Continued)

Option	Action	Equivalent Command
Timing Optimization	Enable this option to optimize BSR control cells on the critical path if that path is from a port to a register or from a register to a port. This option takes affect only when the design contains maximum delay constraint violations.	test_bsd_allow_tolerable_violations

Check Compliance

After you setup, generate, and optimize the boundary-scan circuitry, click the Check Compliance button in the BSD Compiler dialog box to check the boundary-scan implementation.

Verbose

Enable this option in the BSD Compiler dialog box if you want to get a detailed report from Check Compliance.

BSDL Generation

When you click this button in the BSD Compiler dialog box, you see the BSDL Generation dialog box shown in Figure 9-26. Use this dialog box to generate a file containing the boundary-scan description for the current design.

Figure 9-26 BSDL Generation Dialog Box

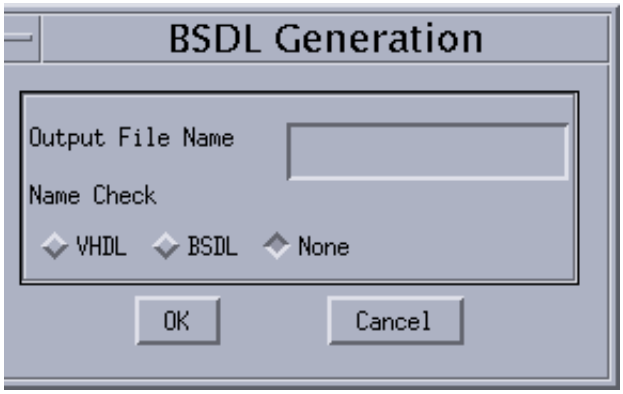


Table 9-17 explains how to use the options in the BSDL Generation dialog box.

Table 9-17 BSDL Generation Dialog Box Options

Option	Action	Equivalent Command
Output File Name	Enter the name of the BSDL output file. The default file is top_level_design_name.bsdl in the current directory.	write_bsdl -output file_name
VHDL	Select this option to check the BSDL output file for both VHDL and BSDL reserved words.	write_bsdl -naming_check [VHDL]
BSDL	Select this option to check the BSDL output file for BSDL reserved words.	write_bsdl -naming_check [BSDL]
None	Select this option if you do not want to perform reserved word checking on the BSDL output file.	write_bsdl -naming_check [none]

Test Vectors Generation

When you click this button in the BSD Compiler dialog box, you see the Test Vector Generation dialog box shown in Figure 9-27. Use this dialog box to generate a file containing the boundary-scan test patterns for the current design.

Figure 9-27 Test Vector Generation Dialog Box

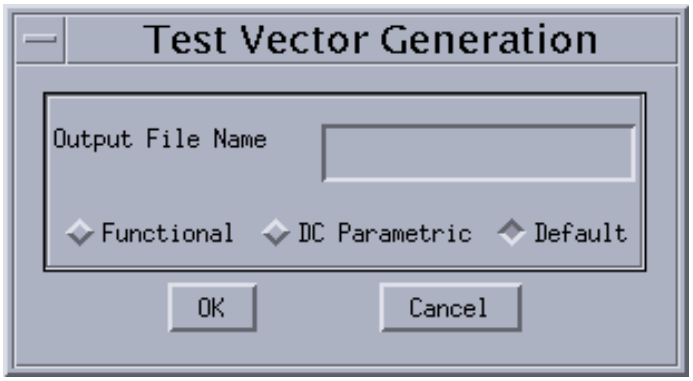


Table 9-18 explains how to use the options in the Test Vector Generation dialog box.

Table 9-18 Test Vector Generation Dialog Box Options

Option	Action	Equivalent Command
Output File Name	Enter the name of a test program file that contains the Synopsys pattern database for generated test patterns and fault status information. The default file name is the design name with the .vdb extension, and the file is located in the current directory.	create_bsd_patterns -output test_program_name
Functional	Select this option to generate functional vectors (bsr, tap, tdr, and resetr) that test all functions of the boundary scan.	create_bsd_patterns -type [functional]

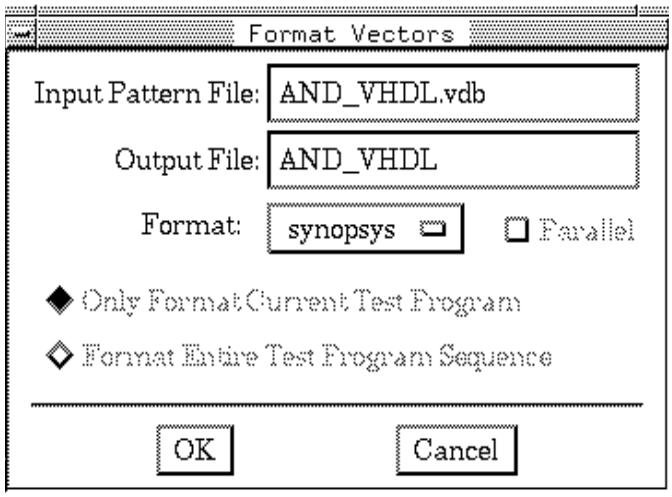
Table 9-18 Test Vector Generation Dialog Box Options (Continued)

Option	Action	Equivalent Command
DC Parametric	Select this option to generate leakage vectors that test the parametrics of the boundary scan.	create_bsd_patterns -type [dc_parametric]
Default	Select this option to generate both functional and leakage vectors.	create_bsd_patterns -type [all]

Format Vectors

When you click this button in the BSD Compiler dialog box, you see the Format Vectors dialog box shown in Figure 9-28. Use this dialog box to format an existing test vector file.

Figure 9-28 Format Vectors Dialog Box



Click OK to format the test vectors as shown. Click Cancel to remove this dialog box.

Table 9-19 and the following sections explain how to use the options ins the Format Vectors dialog box.

Table 9-19 Format Vectors Dialog Box Options

Option	Action	Equivalent Command
Input Pattern File	Type the name of the file that contains the Synopsys-generated test patterns, which must be in Synopsys vector format (.vdb).	write_test -input
Output File	Type the name of the file receiving the formatted test vectors. It creates a new file if one doesn't already exist or overwrites the existing file.	write_test -output
Format	Choose an output file format from the Format option menu.	write_test_format
Parallel	Enable this to write the test program in parallel mode.	write_test_parallel
Only Format Current Test Program or Format Entire Test Program Sequence	Choose one of these mutually exclusive options to determine the scope of the test program formatting.	write_test [-cumulative]

Input Pattern File

Type the name of the file that contains the Synopsys-generated test patterns, which must be in Synopsys vector format (.vdb).

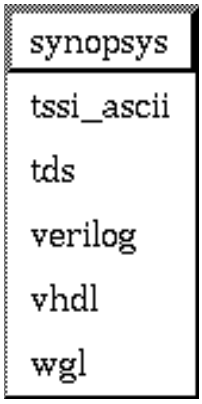
Output File

Type the name of the file receiving the formatted test vectors. It creates a new file if one doesn't already exist or overwrites the existing file.

Format

Choose the output file format that you want from the Format option menu shown in Figure 9-29.

Figure 9-29 Format Options Menu



This figure illustrates the default formatting option. The value of the write_test_formats variable in the .synopsys_dc.setup file controls the options that display.

Parallel

Enable the Parallel option to write the test program in parallel mode.

Only Format Current Test Program,
Format Entire Test Program Sequence

The Only Format Current Test Program and Format Entire Test Program Sequence options become available only if the value of the multi_pass_test_generation variable is true. Format Entire Test Program Sequence turns on the -cumulative option to the write_test command.

Display Reports

Click this button to create test reports for the current design. Figure 9-30 shows the Test Reports dialog box that appears when you select Display Reports from the Test Synthesis dialog box.

This selection generates and displays test reports for the current design.

Figure 9-30 Test Reports Dialog Box

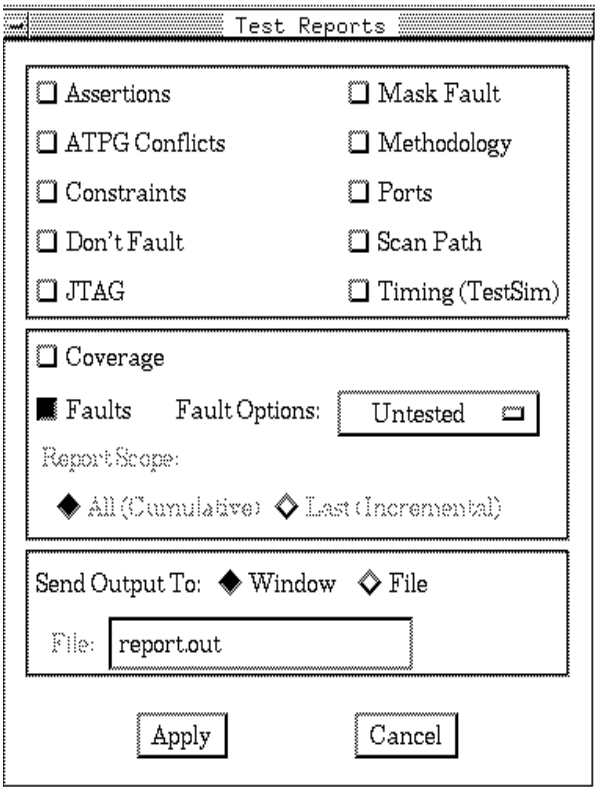


Table 9-20 and the following sections explain how to use the options in the Test Reports dialog box.

Table 9-20 Test Reports Dialog Box Options

Option or Button	Action	Equivalent Command
Assertions	Enable this button to list the cell pins and design ports.	report_test -assertions
ATPG Conflicts	Obsolete option—do not use.	
Constraints	Enable this button to list any test constraints for the current design and to indicate whether the constraints have been met by DFT Compiler.	report_test -constraints
Don't Fault	Obsolete option—do not use.	
JTAG	Enable this button to list the JTAG information for the current design.	report_test -jtag
Mask Fault	Obsolete option—do not use.	
Methodology	Enable this button to list the test-scan style and methodology for the current design.	report_test -methodology
Ports	Enable this button to list the details of the test ports for the current design.	report_test -port
Scan Path	Enable this button to report the test-scan path's cells and routing.	report_test -scan_path
Timing (TestSim)	Obsolete option—do not use.	
Coverage	Obsolete option—do not use.	
Faults	Obsolete option—do not use.	

Table 9-20 Test Reports Dialog Box Options (Continued)

Option or Button	Action	Equivalent Command
Report Scope	Obsolete option—do not use.	
Send Output To	Click Window to display the chosen reports in a new report window. Click File to put the chosen reports in a file.	

Assertions

Lists the cell pins and design ports specified in set_test_assume, set_test_hold, set_test_initial, and set_test_isolate. These commands assert logical conditions that must be met at the specified pins and ports during test generation.

ATPG Conflicts

This report option is obsolete.

Constraints

Lists any test constraints for the current design and indicates whether the constraints have been met by the DFT Compiler.

Don’t Fault

This report option is obsolete.

JTAG

This information is relevant only after JTAG circuitry has been added with the insert_jtag command.

Mask Fault

This report option is obsolete.

Methodology

Lists the test-scan style and methodology for the current design.

Ports

Lists the details of the test ports for the current design.

Scan Path

If you enable the Send Output To: Window button, you can Show the scan path’s ports and cells.

Timing (TestSim)

This report option is obsolete.

Coverage

This report option is obsolete.

Faults

This report option is obsolete.

Report Scope

This report option is obsolete.

Send Output To

Creates a linked report window named Test Report.

Click File to write the chosen reports to the file named in the File text box. The file is created if it does not exist, and is appended to if it does exist.

If you click the Send Output To: Window button, you can show either an individual pin (or port) or all pins in a fault class (such as Detected). Individual pins appear in the Faults report as INSTANCE_NAME/PIN_NAME pin. Ports appear as PORT_NAME port. For each design, fault classes appear as Detected, Redundant, and so on. When you show a fault class, all affected pins in that design are selected and shown in a schematic.

If you click Send Output To: Window button, a linked report window named Test Report is created, containing all the generated reports. For example, to see a schematic with a tested pin selected, click a pin name in the Faults report, then click the Test Report window's Show button. For more information, see Chapter 2, "Using Design Analyzer."

10

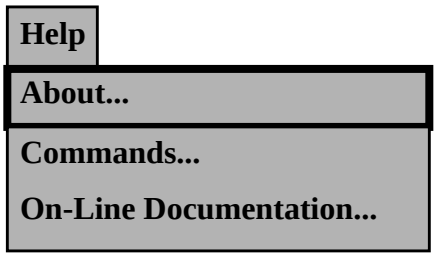
Help Menu

Use the Help menu to get information regarding

- About
- Commands
- Online Documentation

Figure 10-1 shows the Help menu.

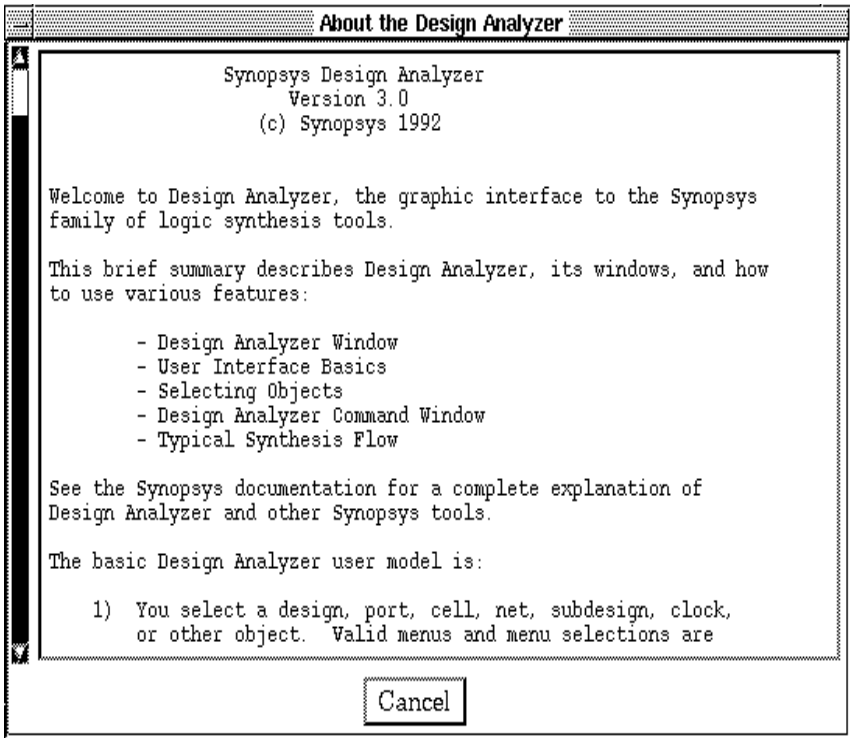
Figure 10-1 Help Menu



About

The About submenu, shown in Figure 10-2, provides a summary information dialog box about Design Analyzer describing how to use menus, dialog boxes, the Command Window, and other features.

Figure 10-2 About the Design Analyzer Dialog Box



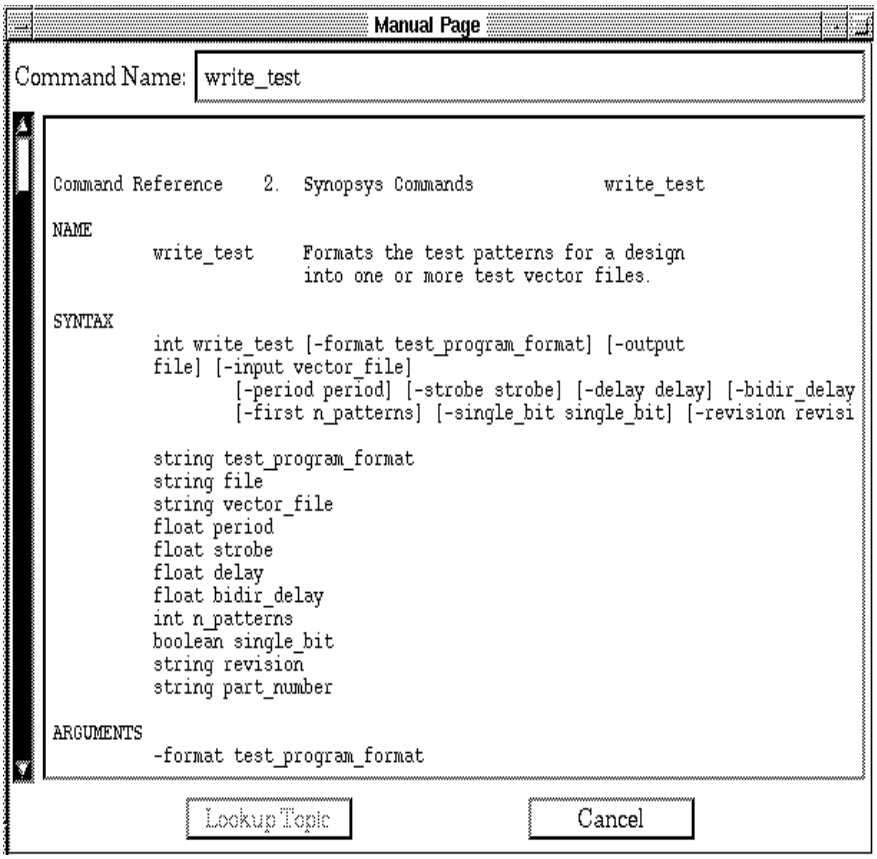
Click Cancel to remove this dialog box. Use the scroll bar to move through the text.

Commands

When you choose the commands submenu, the Manual page window appears. Use this window to access information about Design Analyzer commands, variables, and errors that have man pages.

Figure 10-3 displays information about the write_test command.

Figure 10-3 Man Page Dialog Box



To access information about a command,

1. Type the command name in the text field at the top of the dialog box.

2. Choose the Lookup Topic button.

Click Cancel to remove this dialog box. Use the scroll bar to move through the text.

Online Documentation

The On-line Documentation submenu invokes the online documentation viewer. To use the On-line Documentation option, set the view_on_line_doc_cmd variable in your .synopsys_dc.setup file to the UNIX command that invokes the online documentation viewer.

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