**Department of Computer Engineering**
Digital Hardware Systems
*CpE 3104 - Microprocessors*

# Laboratory Report

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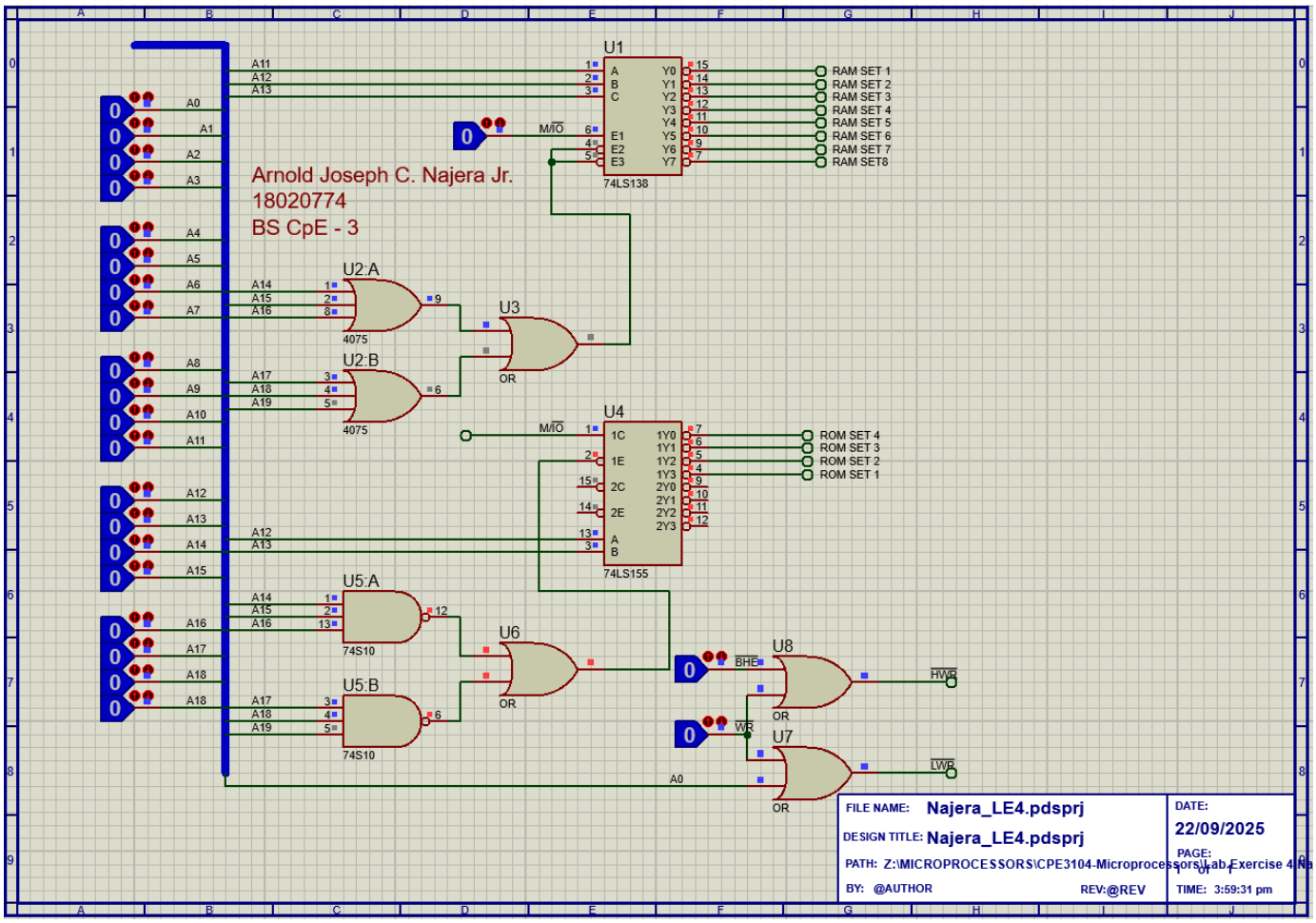
|---|---|---|---|
| **Laboratory Exercise No.:** | 4 | **Date Performed:** | Sept. 22, 2025 |
| **Laboratory Exercise Title:** | Memory Interfacing | | |
| **Name of Student:** | Arnold Joseph C. Najera Jr. | **Document Version:** | 1 |

## Activity #1



**Simulated address decoding and RAM write/read data.**

| Address ($A_{19}$…$A_0$) | | M/IO | WR | BHE | Memory Set Enabled | HWR | LWR | Observations |
|---|---|---|---|---|---|---|---|---|
| 0000 0000 1111 0000 0001 | 00F01H | 1 | 0 | 0 | RAM Set 2 | 0 | 1 | High bank 8 bit transfer (write) |
| 1111 1100 0110 1000 0010 | FC680H | 1 | 0 | 1 | ROM Set 4 | 1 | 0 | Low bank 8 bit transfer (write) |
| 0000 0101 1010 0111 1100 | 05A7CH | 1 | 1 | 0 | none | 1 | 1 | Address out of range |
| 1111 1111 0000 0000 0010 | FF002H | 0 | 0 | 0 | **none** | **0** | **1** | **Accessing isolated** |
| 0000 0001 1111 1111 1111 | 01FFFH | 1 | 1 | 1 | **RAM set 4** | **1** | **1** | **Read from memory** |
| 0000 0000 0000 0000 0001 | 00001H | 1 | 1 | 0 | **RAM set 1** | **1** | **1** | **Read from memory** |
| 1111 1011 1111 0000 0011 | FBF03H | 1 | 0 | 0 | **none** | **0** | **1** | **Address out of range** |
| 0000 0000 1111 1100 1110 | 00FCEH | 0 | 1 | 1 | **none** | **1** | **1** | **Accessing isolated** |
| 0000 0100 0000 0000 0000 | 04000H | 1 | 0 | 0 | **none** | **0** | **1** | **Address out of range** |
| 0000 0010 0110 0101 1001 | 02659H | 1 | 0 | 1 | **RAM set 5** | **1** | **1** | **No bank enabled** |

a. How many RAM and ROM chips are used?

There are:

- RAM chips = Number of sets * 2 banks = 8 * 2 = **16 chips**
- ROM chips = Number of sets * 2 banks = 4 * 2 = **8 chips**

b. What is the chip size of the RAM and ROM?
- The RAM chip size is **2K x 8**
- The ROM chip size is **4K x 8**

c. Determine the address range of the RAM and ROM

RAM chip size: **2K = 007FFH**

| Set # | Start Address (Previous End + 1) | End Address (Current Start + Previous End) | Address Range (Start Address - End Address) |
|---|---|---|---|
| 1 | 00000H | 00000H + 007FFH = 007FFH | 00000H – 007FFH |
| 2 | 007FFH + 1 = 00800H | 00800H + 007FFH = 00FFFH | 00800H – 00FFFH |
| 3 | 00FFFH + 1 = 01000H | 01000H + 007FFH = 017FFH | 01000H – 017FFH |

| | | | |
|---|---|---|---|
| 4 | 017FFH + 1 = 01800H | 01800H + 007FFH = 01FFFH | 01800H – 01FFFH |
| 5 | 01FFFH + 1 = 02000H | 02000H + 007FFH = 027FFH | 02000H – 027FFH |
| 6 | 027FFH + 1 = 02800H | 02800H + 007FFH = 02FFFH | 02800H – 02FFFH |
| 7 | 02FFFH + 1 = 03000H | 03000H + 007FFH = 037FFH | 03000H – 037FFH |
| 8 | 037FFH + 1 = 03800H | 03800H + 007FFH = 03FFFH | 03800H – 03FFFH |

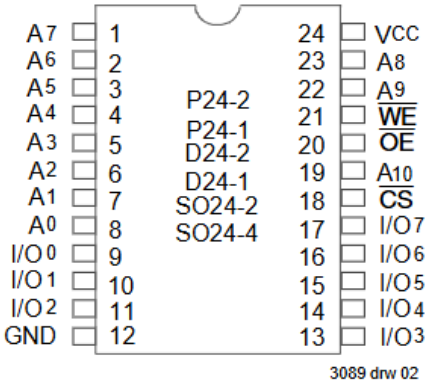
ROM chip size: **4K = 00FFFH**

| **Set #** | **Start Address (Current End - Chip Size)** | **End Address (Previous Start - 1)** | **Address Range (Start Address - End Address)** |
|---|---|---|---|
| 1 | FFFFFH – 00FFFH = FF000H | FFFFFH | FF000H – FFFFFH |
| 2 | FEFFFH – 00FFFH = FE000H | FF000H – 1 = FEFFFH | FE000H – FEFFFH |
| 3 | FDFFFH – 00FFFH = FD000H | FE000H – 1 = FDFFFH | FD000H – FDFFFH |
| 4 | FCFFFH – 00FFFH = FC000H | FD000H – 1 = FCFFFH | FC000H – FCFFFH |

a. Suggest an actual RAM (static RAM) and ROM (EPROM) integrated circuit (IC) with the same size as determined in (b).

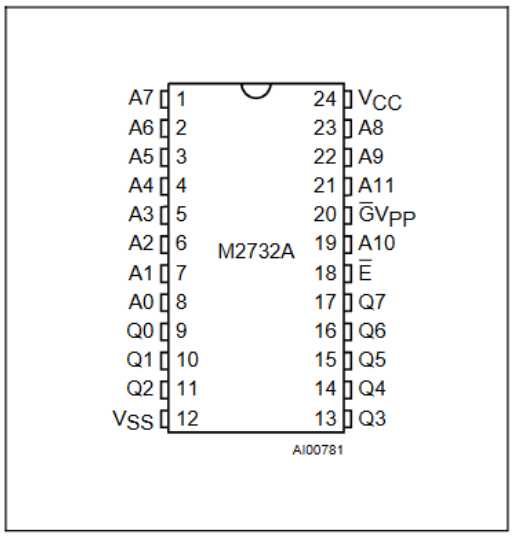
- RAM 16K = 2K x 8 = **IDT6116SA CMOS Static RAM 16K (2K x 8-Bit)**

**Pin Configurations**



- ROM 32K = 4K x 8 = **M2732A NMOS 32K (4K x 8) UV EPROM**

**Figure 2. DIP Pin Connections**




**References:**

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