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Heterogeneous Managed Runtime Systems: A Computer Vision Case Study

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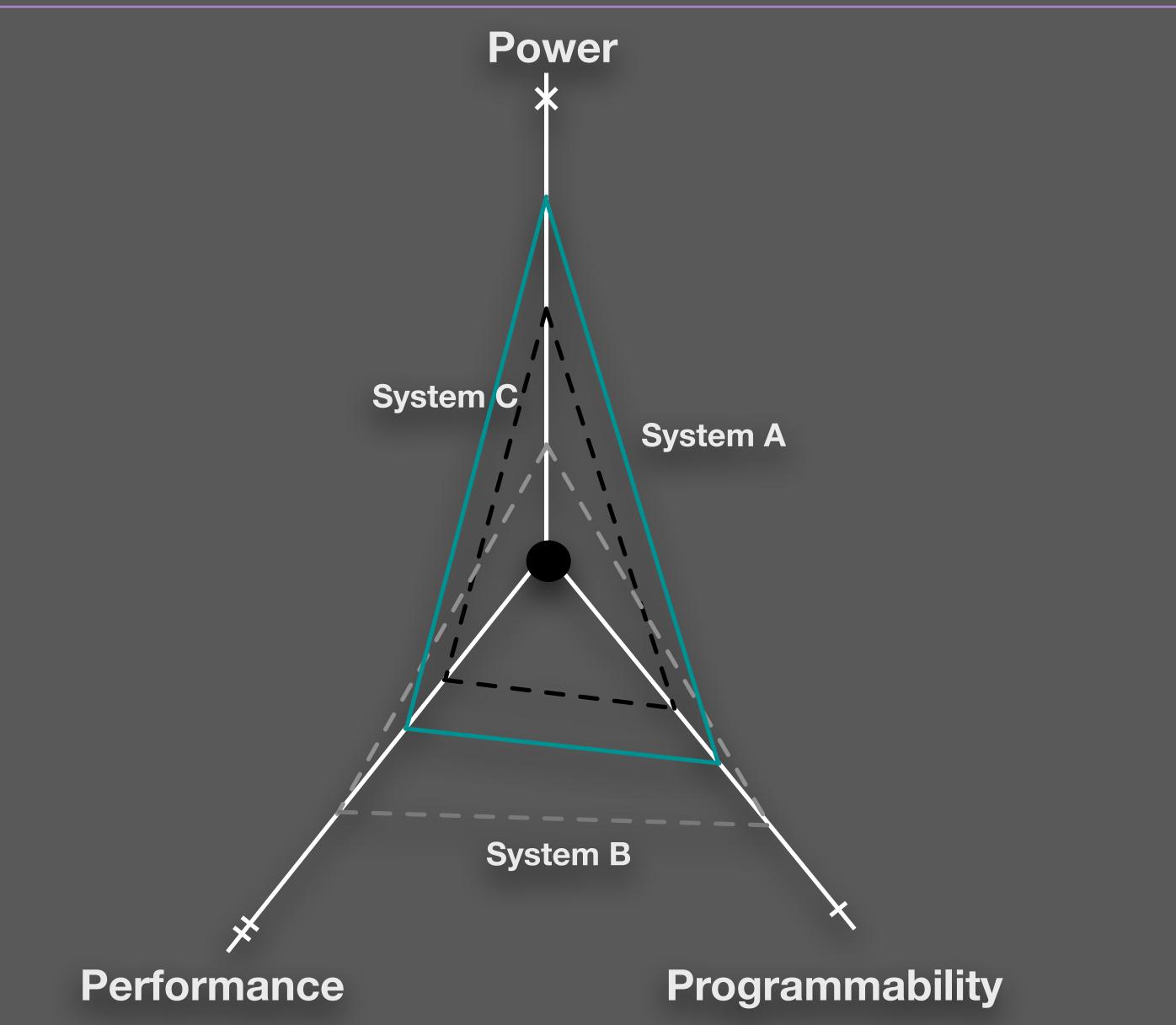
Computing Challenges

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- More performance
- Less power
- Complex applications (NN, CV, etc.)
- Diversity of:
 - Hardware devices
 - Programming models
 - Programming languages

Pareto-optimal Point





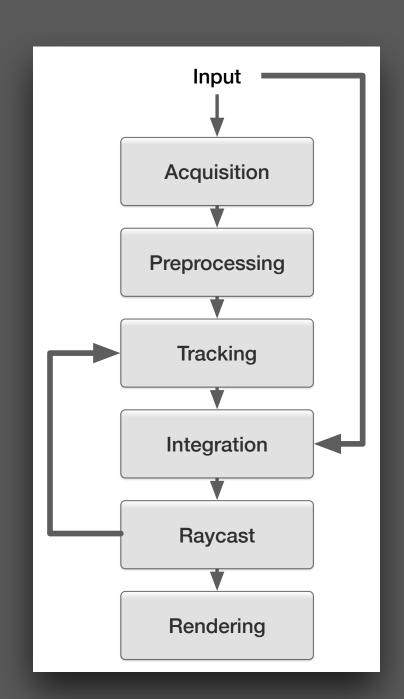
Challenge Accepted

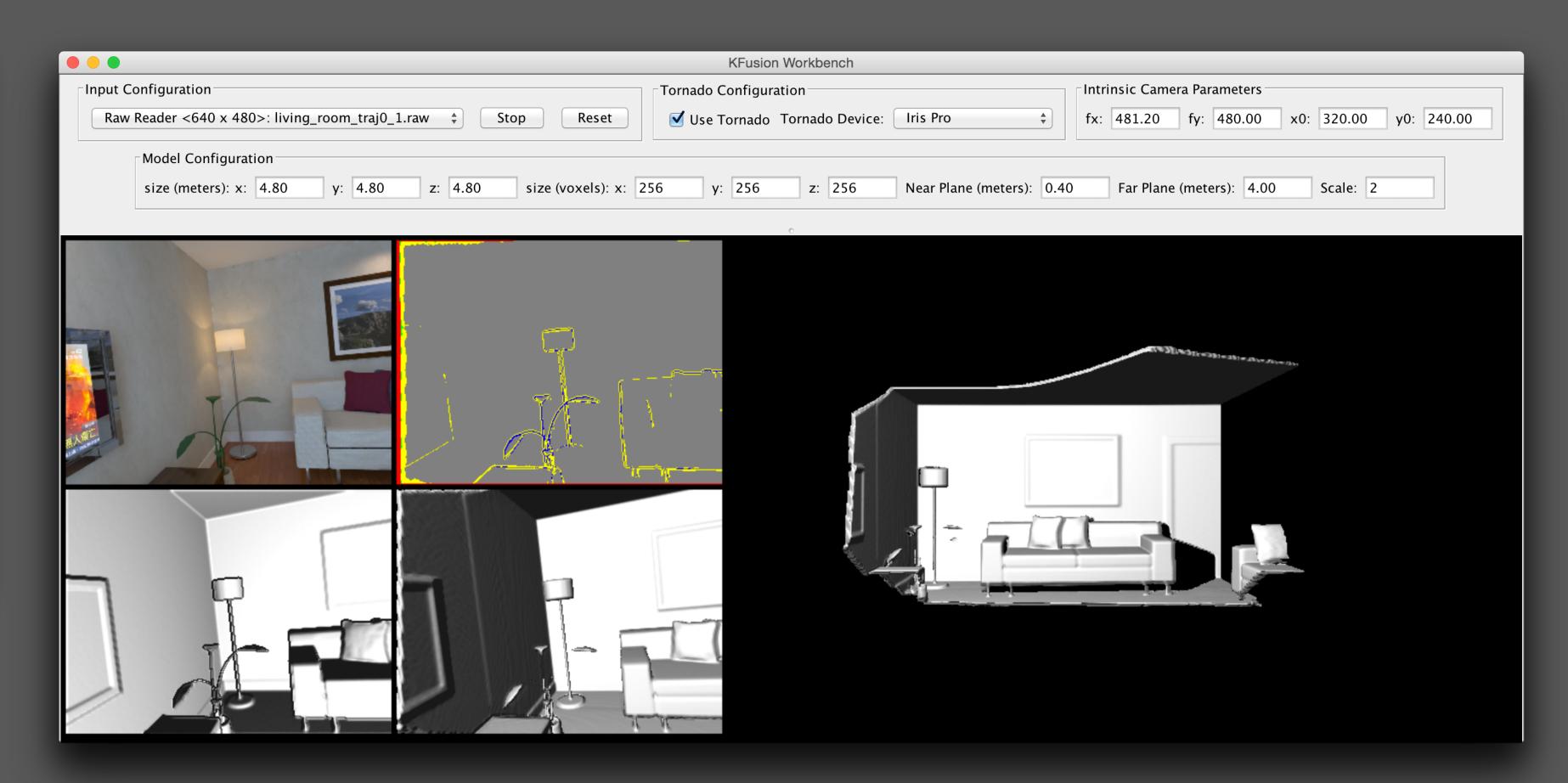
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- "Write-once-run-everywhere"
- Exploit heterogeneous hardware
- Choose a demanding application
- Meet the QoS of selected application
- Generalize solution

- 3D space reconstruction (RGB-D)
- Complex multi-kernel pipeline
 - 540-1620 kernels/second
 - SLA of 30 FPS
- Cutting edge robotics application
- Deploy across many combinations of platforms and accelerators

Kinect Fusion



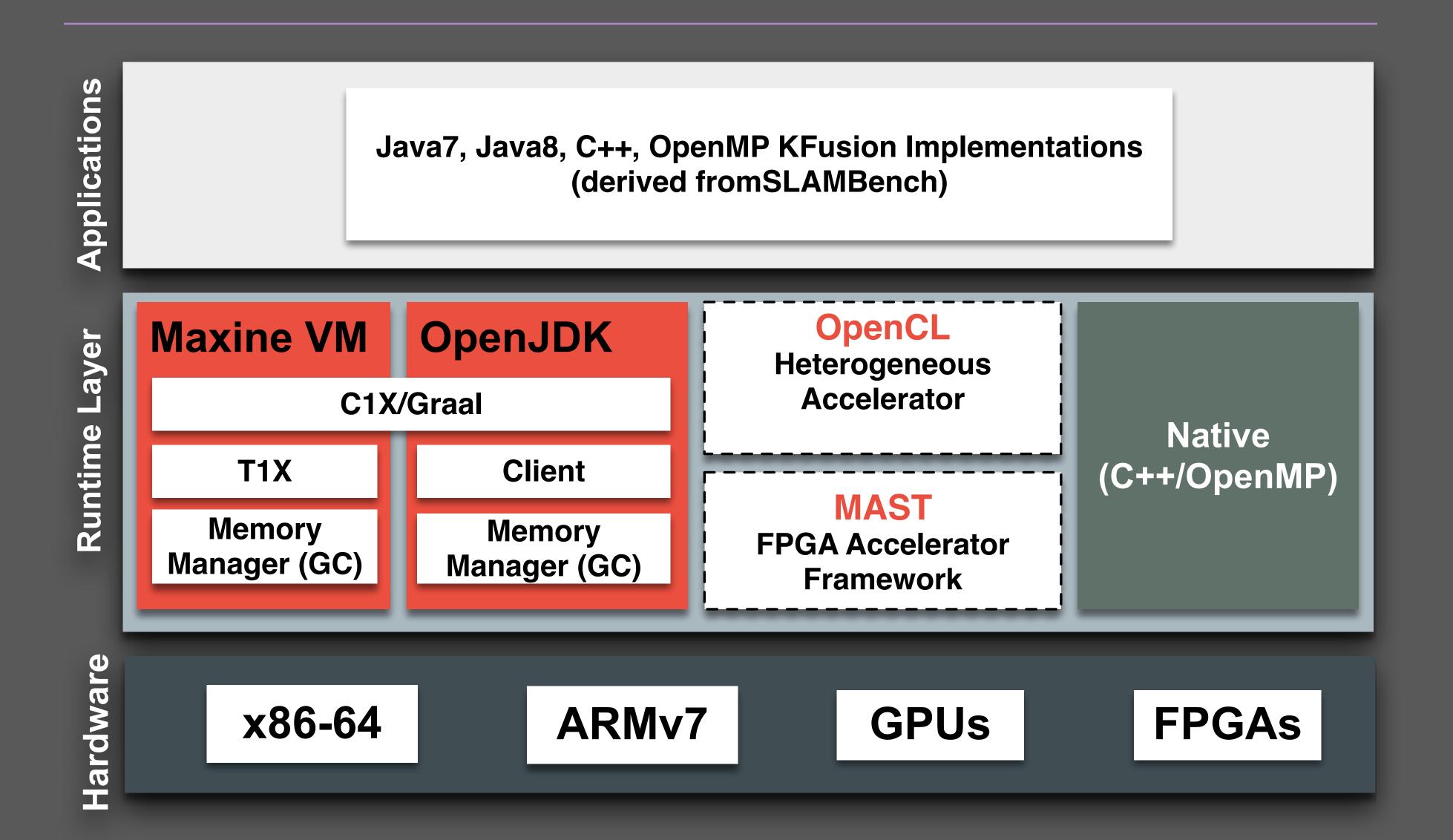


Platform I Objectives

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- Application portability
- Increased productivity
- Hardware / Device diversity
- High performance
- Easy experimentation and prototyping

Platform I Floor Plan



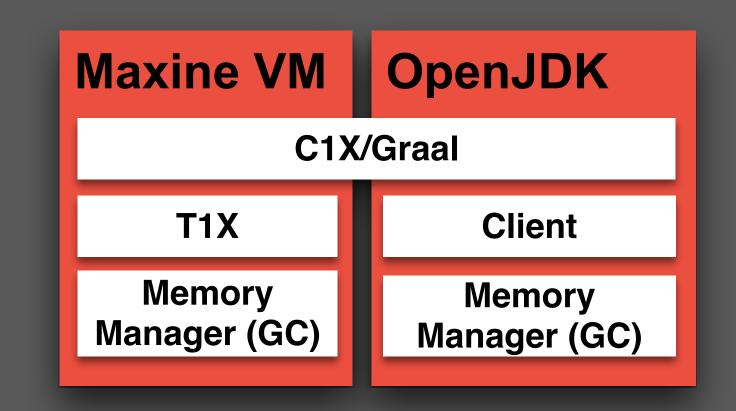
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Platform I Maxine VM and OpenJDK



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- Graal Integration and Interoperability
- Research vs. Industrial VMs
- Flexibility vs. Performance



Maxine VM Improvements

- Enable Profile-guided Optimisations
- ARM Port (32bit transition)
- Stability and Performance Improvements
- x86-64: 1.64x over baseline Maxine VM 0.57x over HotSpot C2
- ARMv7: SpecJVM2008, KFusion 100% passrate 2.3x and 3.3x slower against HotSpot C1 and C2

Platform I OpenCL Acceleration



- OpenCL Acceleration Module
- Based on Graal/OpenJDK
- API, Compiler, Runtime
- Exploits any OpenCL Compatible Device
- Successor of JACC [1]

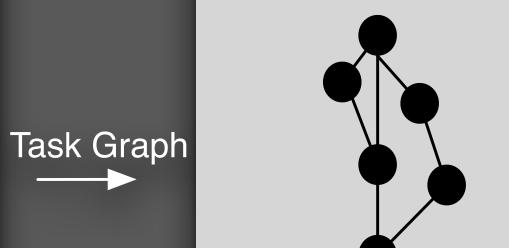
Platform I OpenCL Acceleration



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OpenCL/Java API

- Users create Task Graphs with our OpenCL API.

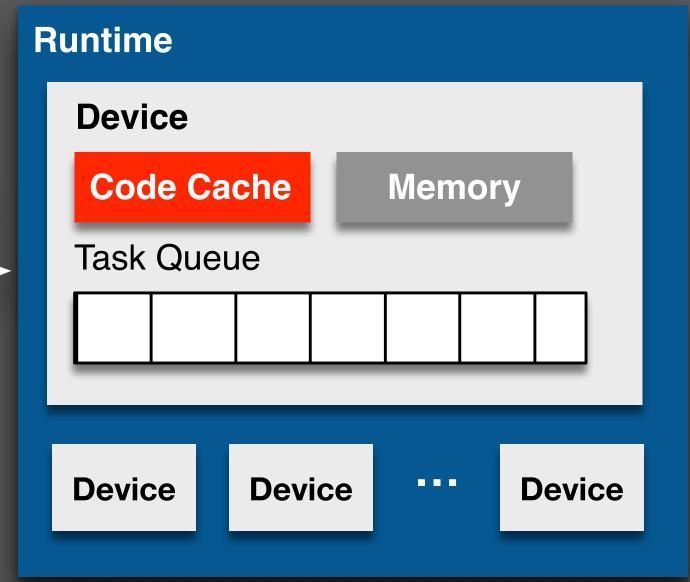


- The compiler expands graphs to include data movement.

Graph Optimizer

- Graph is optimized to remove redundant data transfers.

Optimized Graph



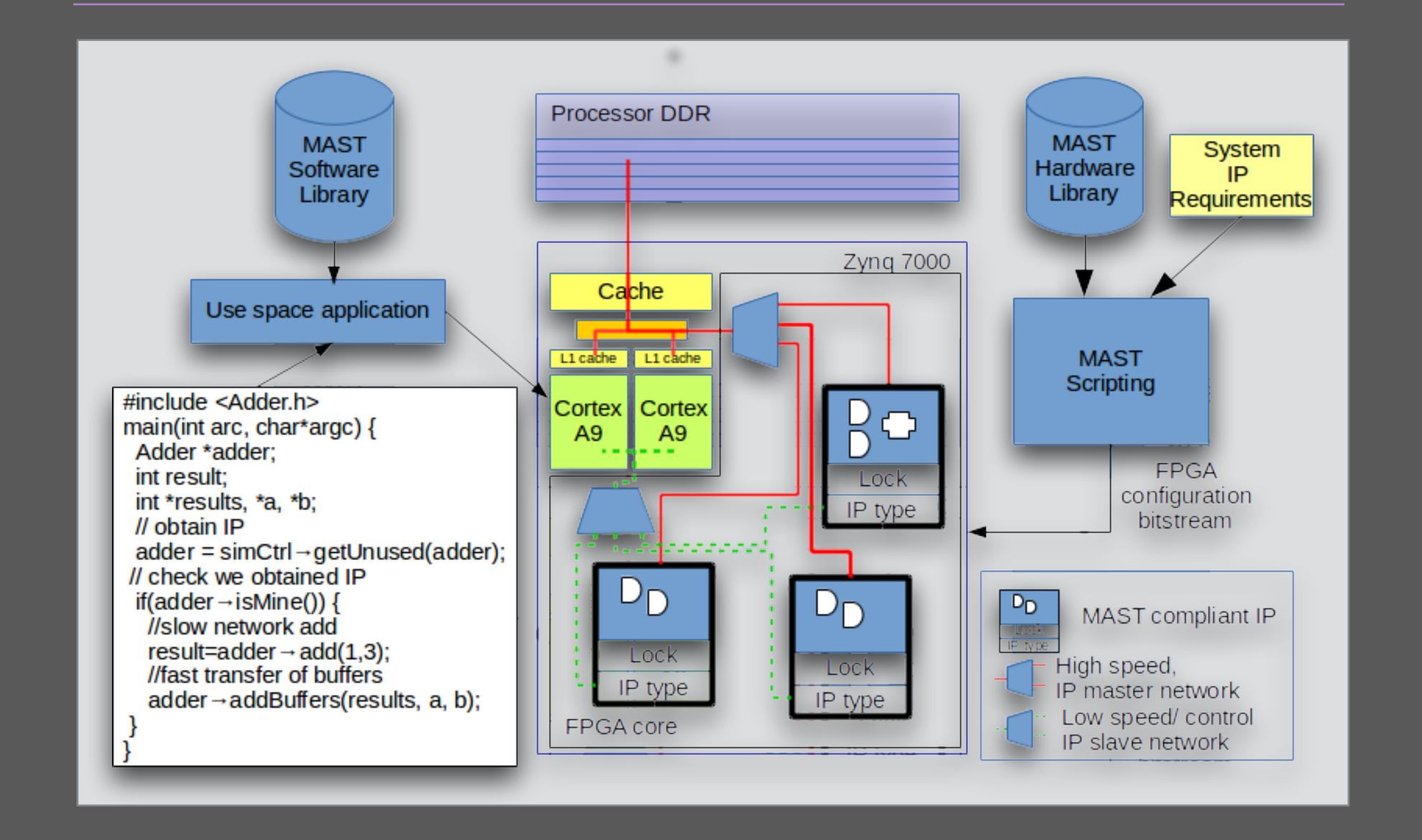
- Runtime schedules tasks on devices.

Platform I FPGA Acceleration



- MAST: Modular Accelerator and Simulation Technology
- HW/SW Libraries for FPGA Acceleration (C++, BlueSpec)
- Thread, Process, OS Concurrency
- Acceleration through IP Blocks
- Simulation [2] via MAMBO [3] Dynamic Binary Instrumentation
- Currently Implemented in ARMv7 Xilinx Zynq SoC

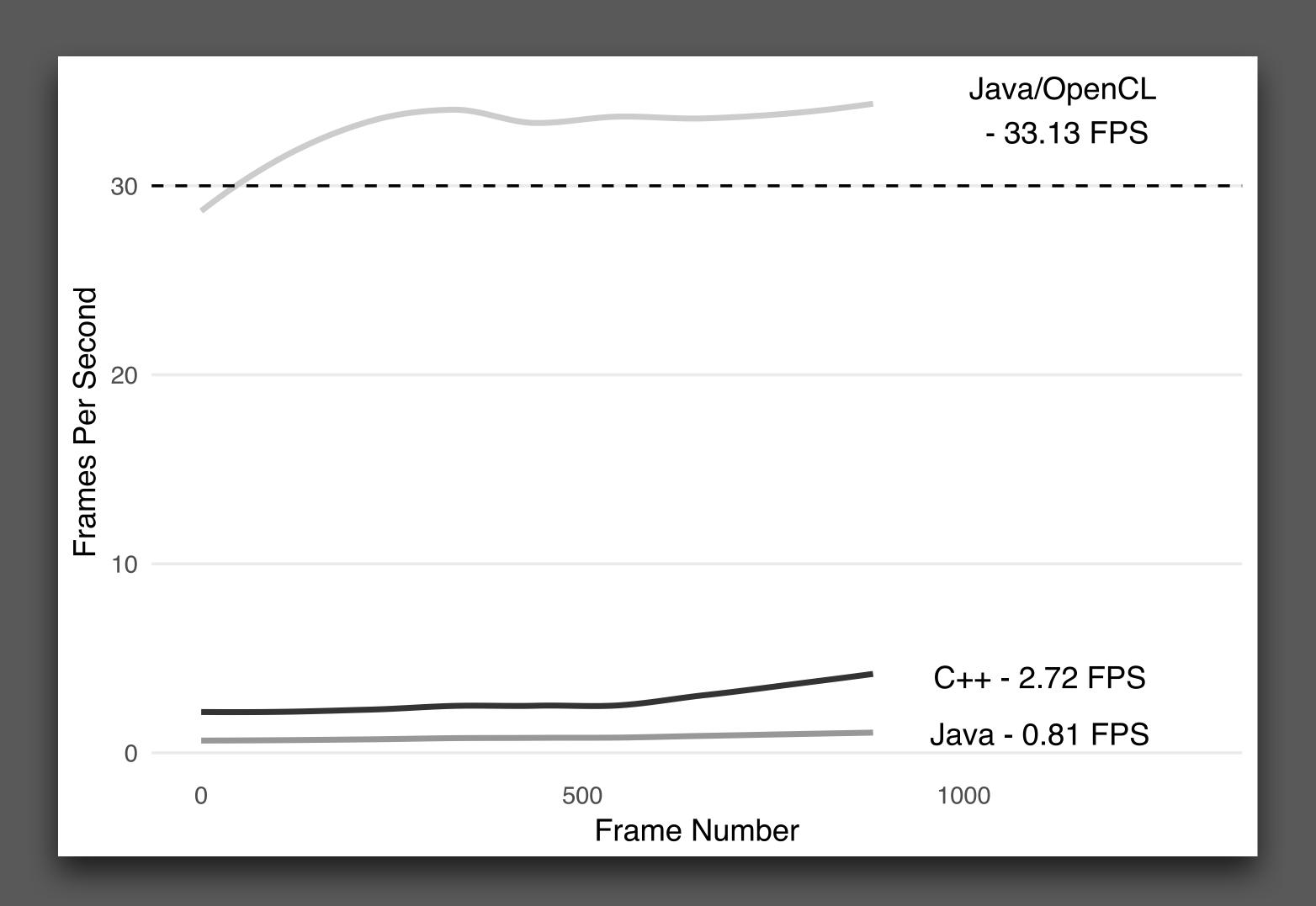
Platform I FPGA Acceleration



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Results I OpenCL Acceleration





Results I FPGA Acceleration



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- Targeting preprocessing stage
 - Image scaling from mm to meters
 - Bilateral filter to produce a filtered scaled image
- Merging of two kernels

VM	No FPGA Acceleration	With FPGA Acceleration	Speedup
Maxine VM	2.20	0.05	43x
OpenJDK	0.66	0.03	22x

OpenJDK/Maxine,Xilinx Zynq 706, ARMv7 Cortex A9, 1GB RAM, MAST FPGA

Conclusions

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Future Challenges of Computing

- Performance I Power I Programmability I +++
- Is there a Magic Bullet?

VM Approach

- "Write-once-run-everywhere"
- Extend VMs for the heterogeneous world

Our Approach

- Demonstrate feasibility with proof-of-concept
- Target both Industrial and Research VMs
- High Performance through OpenCL/FPGA Acceleration
- Use complex CV application as a driver

Future Work

- Device Diversity
- Join Mast and OpenCL Accelerator
- Extend API through more real-world use cases

Thank you!

Questions?

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