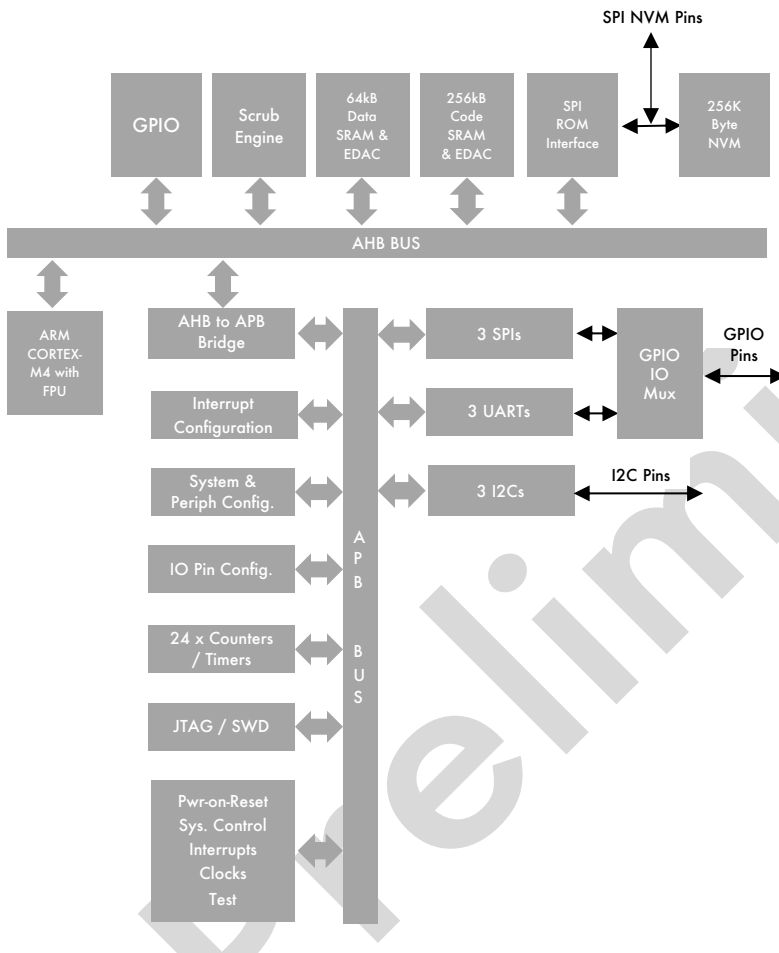


Radiation Hardened VA416X7 32-Bit Arm® Cortex®-M4 (with FPU) microcontroller manufactured with HARDSIL® technology offering best in class radiation performance and latch-up immunity.



MEMORY CONFIGURATION OPTIONS

- Internal NVM (VA41637 only)
- External SPI NVM (for code boot)

RADIATION HARDENED PERFORMANCE

- VA41627 Total Ionizing Dose (TID) > 300 krad (Si)
- VA41637 Total Ionizing Dose (TID) > 200 krad (Si)
- Soft Error Rate (SER) < $1e^{-15}$ errors / bit-day
- Single-Event Latch-Up (SEL) immunity to LET > 110 MeVcm² / mg

KEY FEATURES

- Manufactured with HARDSIL technology
- RAD hardened Registers with Triple-Module Redundancy (TMR)
- 32-bit Arm Cortex-M4 processor
 - Single-Precision Floating-Point Unit (FPU)
 - SWD based debug interface
- Operating voltages
 - GPIO 3.3 ± 10% V
 - Optional 1.5 V core supply voltage
 - Includes on-chip LDO regulator
- Clock rate up to 100 MHz
 - Internal 20 MHz oscillator for fail-safe clocking
- Memory
 - 64 Kbyte on-chip data and 256 Kbyte on-chip program memory SRAM
 - 256 Kbyte SPI NVM (VA41637 only)
 - Error Detection and Correction (EDAC)
 - Built in Scrub Engine
- Peripherals
 - 104 Configurable GPIO pins
 - 3 UART interfaces
 - 3 I²C interfaces
 - 3 SPI interfaces
 - DMA controller
- Timer System
 - 24 configurable 32-bit counters / timers
 - Input capture, Output compares
 - PWMs, Pulse Counters, Watchdog timer
- Package
 - 196 BGA (12 mm x 12 mm)

SUPPORT

- PEB1 development board
- Keil™ Microcontroller Development Kit

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Features

- **Performance**
 - 100 MHz Arm Cortex-M4 processor with Single-Precision Floating-Point Unit (FPU)
- **On-Chip Memory**
 - 256 Kbyte Non-Volatile Memory (NVM) (VA41637 only)
 - 256 Kbyte Program SRAM
 - 64 Kbyte Data SRAM
 - On-chip Error Detection and Correction (EDAC) and Scrub Engine
- **General-purpose I/O (GPIO) pins**
 - Configurable direction
 - Configurable pull-up/down resistors
 - Configurable as edge or level sensitive interrupt sources
- **24 General-purpose counter/timers**
 - Configurable interrupt sources
 - Can be triggered from multiple sources (GPIO or other counter/timers)
 - Each counter/timer has an independent 32-bit counter
 - Configurable as PWM, capture or compare
- **3 x UARTS**
 - Internal FIFO
 - Transmit or receive interrupt source
- **3 x Serial Peripheral Interface (SPI) ports**
 - Internal FIFO
 - Transmit or receive interrupt source
 - Multiple chip select outputs
- **3 x I²C ports**
 - Internal FIFO
 - Master and Slave mode on all ports
 - Standard and Fast mode support
- **System-level Triple Modular Redundancy (TMR) on critical internal registers**
- **Random Number Generator**
- **Serial Wire Debug (SWD) based debug controller**
- **3.3 V single rail supply or configurable for dual supplies**

1 Functional Description

The VA416X7 is optimized for radiation environments and consists of an Arm Cortex-M4 CPU core and a related set of peripherals. It includes Error Detection and Correction (EDAC) logic on the internal memories. The program space EDAC is 16-bit word-based for optimum performance and reliability. The data space EDAC is 8-bit to allow reliable byte size data manipulation. In addition, the VA416X7 includes Triple-Mode Redundancy (TMR) with voting on select internal flip-flop storage elements.

1.1 Related Documentation

The following associated documents will help understand this device:

- Arm Documents (Available from <http://infocenter.arm.com>)
 - Cortex-M4 Generic User Guide
 - Cortex-M4 Technical Reference Manual
 - AMBA® 3 AHB-Lite™ Protocol Specification
 - AMBA® 3 APB Protocol Specification
 - Arm® TrustZone® True Random Number Generator Technical Reference Manual
 - Arm® PrimeCell® External Bus Interface Technical Reference Manual
 - Arm® PrimeCell® DMA Technical Reference Manual
- NXP Documents (Available from <http://www.nxp.com>)
 - I²C-bus Specification and User Manual
- Cypress Documents (Available from <http://cypress.com>)
 - FM25V20A FRAM Datasheet
- VORAGO Documents
 - VA416XX Programmer's Guide

1.2 Feature Summary

- Processor Core
 - Arm Cortex-M4 processor
 - Up to 100 MHz operation
 - SysTick Counter
 - Single Cycle Multiply-and-accumulate
 - Hardware divide (2 to 12 cycles)
 - Single-precision IEEE 754 compliant HW Floating Point Unit (FPU)
 - Bit-Banding region for registers and data SRAM
 - Arm Cortex-M4 built-in Nested Vectored Interrupt Controller (NVIC)
 - 240 Interrupt sources with a unique 8-bit priority level (176 of these are used)
 - Tail chaining supported

- Arm CoreSight™ debug and trace technology
 - SWD: Serial Wire Debug
 - DAP: Debug Access Port
 - SWV: Serial Wire Viewer
 - Four Breakpoint Comparators
 - Two Data Watch Point Comparators
- Memory
 - 64 Kbyte SRAM Data Memory (32 Kbyte on Data bus and 32 Kbyte on System bus)
 - Byte-level Error Detection and Correction (EDAC) logic on Data memory
 - 256 Kbyte SRAM Instruction Memory
 - Loaded from Serial Peripheral Interface (SPI) based memory
 - Configurable boot delay, boot speed, and error checking
 - 16-bit level EDAC on instruction memory
 - Programmable Scrub Engine for both Data and Instruction memory
 - Utility peripheral
 - Provides means of injecting single and multi-bit errors to check error handling routines.
 - 256 Kbyte serial NVM in package (VA41637 only)
- System Integration Peripherals
 - System Configuration
 - Memory Control
 - Data memory clear on reset
 - Code memory reload on reset
 - Code memory write protect
 - Code/Data memory Scrub rate
 - Code/Data memory SBE/MBE counters
 - Code/Data memory SBE/MBE Interrupt control
 - GPIO Glitch Filter rate control
 - Peripheral Configuration
 - Clock gating and Reset control of individual peripherals
 - Interrupt Router
 - Maps interrupt sources to timers and DMA for flexible event triggers
 - Four-Channel DMA
 - Allows CPU independent data movement from memory to memory, peripherals to memory, or memory to peripherals.

- Serial Communication Peripherals
 - Three UARTs
 - 16 word Transmit and Receive FIFOs
 - Fractional baud rate generation
 - Supports baud rates up to 115200 with system clocks above 2MHz
 - Supports:
 - 5, 6, 7, 8 and 9 bits
 - Even, Odd and None parity
 - Stop Bits 1 or 2
 - Break generation and detection
 - Error detection
 - FIFO overflow
 - Framing error
 - Parity error
 - Break detection
 - Configurable Interrupt generation
 - FIFO level (fully configurable)
 - Receive Timeout
 - Error
 - Three SPI Ports (Fourth SPI used only to program Boot SPI NVM)
 - Supports all four modes of SPI operation
 - Data size of 4 to 16 bits
 - 16 word Transmit and Receive FIFOs
 - Block mode support for larger Frame sizes
 - Master-mode clock rates up to 1/8 System clock (1.56 Mbit/s)
 - Slave-mode clock rates up to 1/24 System clock (520 kbit/s)
 - Configurable Interrupt generation for transmitting and receiving
 - FIFO level (fully configurable)
 - FIFO Overflow
 - Receive Timeout
 - Three I²C Ports
 - Standard (NXP UM10204) I²C-compliant bus interface
 - Dedicated open-drain pins supporting I²C Fast mode
 - Configurable as Master or Slave
 - 16-byte Transmit and Receive FIFOs
 - Configurable Interrupt generation
 - FIFO level (fully configurable)

- System Connection Peripherals
 - GPIO
 - Seven GPIO Ports with up to 104 pins total
 - 16-bit ports A-F
 - 8-bit port G
 - Configurable direction control of individual bits
 - Bit-level mask register allows single instruction setting or clearing of any bits in one port.
 - Configurable interrupt generation on ports A-F
 - Level or Edge sensitive
 - Configurable Pulse mode on individual bits
 - Configurable (0 to 3) cycle delay filtering on individual bits
 - I/O Configuration
 - Manages programmable function selects of each pin to allow peripherals to be mapped to GPIO
 - Sets electrical parameters:
 - Glitch filters
 - Pull-up/Pull-down resistors
 - Signal inversion
 - Pseudo open-drain
 - Timers
 - Twenty-four 32-bit timers
 - Advanced trigger modes using cascade feature
 - Separate Start/Stop based on other timers or interrupt signals
 - Multiple trigger sources from GPIO or other timers
 - Configurable output event
 - One cycle pulse when timer equal to zero detected
 - Active mode
 - Divide by two for square wave creation
 - Two PWM modes: single edge and double edge detection (supports center alignment)
- Power supplies
 - Can be configured for use with a single 3.3 V supply
 - Can be configured for use with dual supplies
 - 3.3 V for I/O
 - 1.5 V for logic
 - Selectable with an external input pin (EXT15_SEL)

- **Radiation Hardness**
 - Latch-up immunity in extreme environments
 - Built to be resistant to Single Event Upsets (SEU)
 - Built with VORAGO proprietary HARDSIL technology
 - Designed with Dual-Interlocked Storage Cells (DICE) and Triple Mode Redundancy (TMR) on key register elements.

1.3 Power-Up Sequence

The VA416X7 auto-detects the Power-Up condition and begins operation by loading the internal SRAM code memory from an NVM memory located in the same package via an internally connected Serial Peripheral Interface (VA41637 only) or from an external NVM memory via the ROM_SPI interface pins. After loading the code memory, the processor follows a typical Arm Cortex-M4 start sequence. The clock source for boot operation is a 20 MHz internally generated oscillator

1.4 Resets

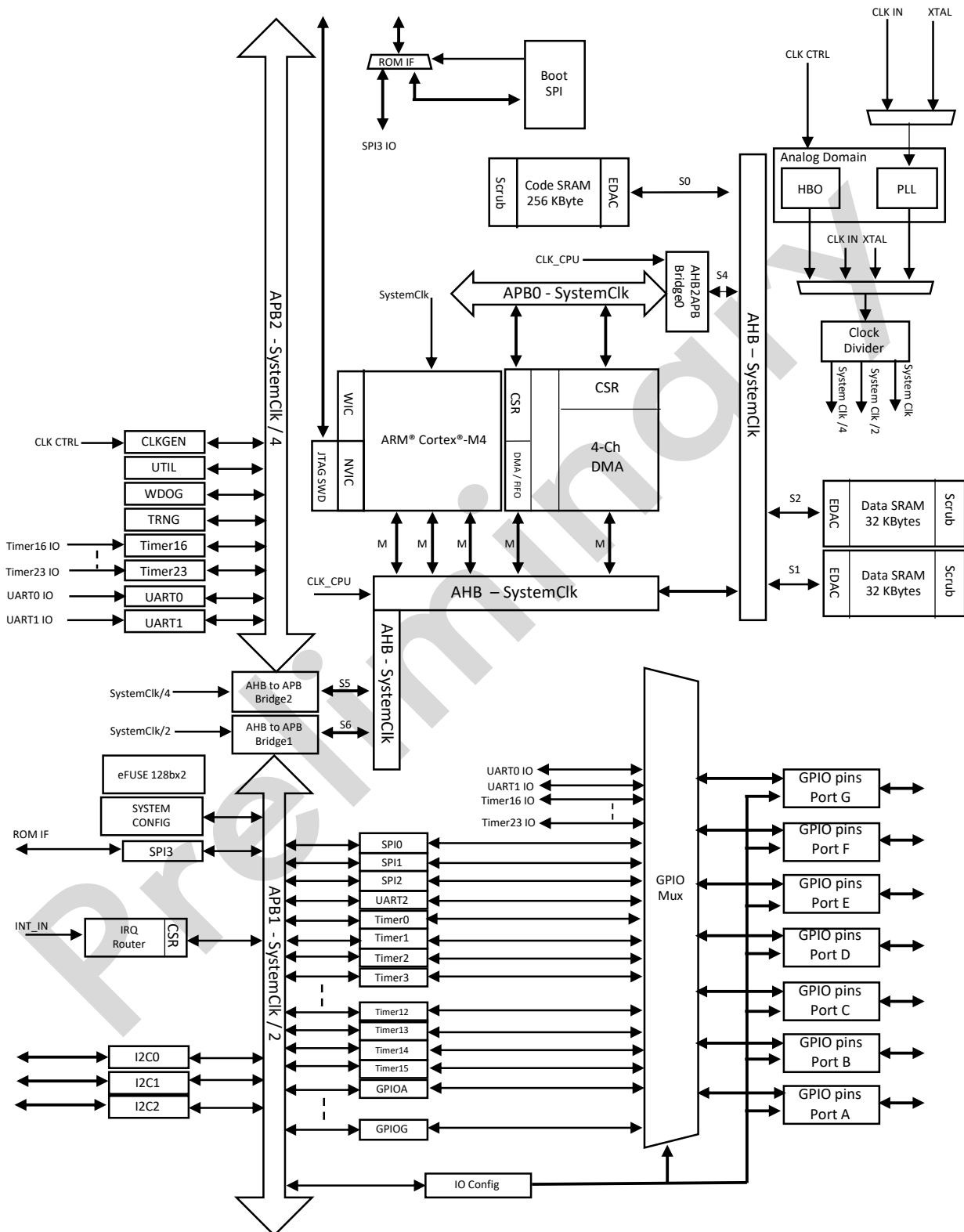
In addition to the Power-on reset, the device can be reset from other events:

- EXTRESETn pin
- SYSRESETREQ from software
- Hardware events configured by IRQ Selector Peripheral or the System Controller Peripheral:
 - Processor Lockup
 - Watchdog Timer
 - Memory Errors (Single or Multi-bit errors from the EDAC memory controller)

1.5 Inter-Integrated Circuit (I²C) pins

The VA416X7 contains three sets of dedicated I²C pins and related I²C controllers. Each controller can act as both an I²C master and an I²C slave simultaneously. These interfaces are capable of operating up to 100 kbps in Standard mode and up to 400 kbps in Fast mode.

2 Block Diagram



3 Pinout

The VA416X7 is available in a 196-pin plastic BGA

3.1 196-Pin Plastic BGA Ball-Map diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	PF15	NC	SRXSN	SRXN	STXSN	STXN	SDA0	PG01	PG05	NC	XTALp	AN7	AN3	VREFH
B	PF11	PF14	SRXSP	SRXP	STXSP	SCL0	PG00	PG04	NMI	XTALn	A3V3	AN4	AN0	DAC0
C	TRST	TDO	PF13	STXP	NC	CRX0	PG03	PG07	1V5n	A1V5	AN5	AN1	DAC1	VSS
D	PF08	TMS	TCK	PF12	CTX0	PG02	PG06	RST	VDDQ	AN6	AN2	PA03	PA01	PA00
E	PF04	PF07	3V3	TDI	1V5	VSS	3V3	1V5	VSS	3V3	PA09	PA06	PA04	PA02
F	SCK	PF03	PF06	PF09	VSS	VSS	3V3	1V5	VSS	VSS	PA13	PA10	PA07	PA05
G	PF01	CSn	MOSI	PF05	1V5	1V5	VSS	VSS	3V3	3V3	PB01	PA14	PA11	PA08
H	PE13	PF00	F_SO	MISO	3V3	3V3	VSS	VSS	1V5	1V5	PB04	NC	PA15	PA12
J	VSS	WPn	PE15	PF02	VSS	VSS	1V5	3V3	VSS	VSS	PB08	PB05	PB02	PB00
K	PE10	PE12	TM	PE14	3V3	VSS	1V5	3V3	VSS	1V5	PB12	PB09	PB06	PB03
L	PE08	PE09	PE11	PE01	PD13	PD09	PD05	PD01	PC13	PC10	PC00	PB13	PB10	PB07
M	PE06	PE07	PE02	PD14	PD10	PD06	PD02	PC14	NC	PC07	PC04	SDA1	PB14	PB11
N	PE05	PE03	PD15	PD11	PD07	PD03	PC15	PC11	PC08	PC05	PC02	SCL2	SCL1	PB15
P	PE04	PE00	PD12	PD08	PD04	PD00	PC12	PC09	PC06	PC03	PC01	SDA2	CTX1	CRX1

3.1.1 Ball-Map

Ball No.	Ball Name	Datasheet Name	Ball No.	Ball Name	Datasheet Name
A01	PF15	PORTF[15]	D01	PF08	PORTF[8]
A02	NC	NC	D02	TMS	TMS/SWDIO
A03	NC	NC	D03	TCK	TCK/SWCLK
A04	NC	NC	D04	PF12	PORTF[12]
A05	NC	NC	D05	NC	NC
A06	NC	NC	D06	PG02	PORTG[2]
A07	SDA0	I2C0_SDA	D07	PG06	PORTG[6]
A08	PG01	PORTG[1]	D08	RST	EXTRESETn
A09	PG05	PORTG[5]	D09	VDDQ	VDDQ
A10	NC	NC	D10	NC	NC
A11	XTALp	XTAL_P	D11	NC	NC
A12	NC	NC	D12	PA03	PORTA[3]
A13	NC	NC	D13	PA01	PORTA[1]
A14	3V3	VDD33	D14	PA00	PORTA[0]
B01	PF11	PORTF[11]	E01	PF04	PORTF[4]
B02	PF14	PORTF[14]	E02	PF07	PORTF[7]
B03	NC	NC	E03	PF10	PORTF[10]
B04	NC	NC	E04	TDI	TDI
B05	NC	NC	E05	1V5	VDD15
B06	SCL0	I2C0_SCL	E06	VSS	VSS
B07	PG00	PORTG[0]	E07	3V3	VDD33
B08	PG04	PORTG[4]	E08	1V5	VDD15
B09	NMI	NMI	E09	VSS	VSS
B10	XTALn	XTAL_N	E10	3V3	VDD33
B11	3V3	VDD33	E11	PA09	PORTA[9]
B12	NC	NC	E12	PA06	PORTA[6]
B13	NC	NC	E13	PA04	PORTA[4]
B14	NC	NC	E14	PA02	PORTA[2]
C01	TRST	TRSTn	F01	SCK	ROM_SCK
C02	TDO	TDO	F02	PF03	PORTF[3]
C03	PF13	PORTF[13]	F03	PF06	PORTF[6]
C04	NC	NC	F04	PF09	PORTF[9]
C05	NC	NC	F05	VSS	VSS
C06	NC	NC	F06	VSS	VSS
C07	PG03	PORTG[3]	F07	3V3	VDD33
C08	PG07	PORTG[7]	F08	1V5	VDD15
C09	1V5n	EXT15_SEL	F09	VSS	VSS
C10	1V5	VDD15	F10	VSS	VSS
C11	NC	NC	F11	PA13	PORTA[13]
C12	NC	NC	F12	PA10	PORTA[10]
C13	NC	NC	F13	PA07	PORTA[7]
C14	VSS	VSS	F14	PA05	PORTA[5]

G01	PF01	PORTF[1]	K01	PE10	PORTE[10]
G02	CSn	ROM_CSn	K02	PE12	PORTE[12]
G03	SO	ROM_MOSI	K03	TM	TEST_MODE
G04	PF05	PORTF[5]	K04	PE14	PORTE[14]
G05	1V5	VDD15	K05	3V3	VDD33
G06	1V5	VDD15	K06	VSS	VSS
G07	VSS	VSS	K07	1V5	VDD15
G08	VSS	VSS	K08	3V3	VDD33
G09	3V3	VDD33	K09	VSS	VSS
G10	3V3	VDD33	K10	1V5	VDD15
G11	PB01	PORTB[1]	K11	PB12	PORTB[12]
G12	PA14	PORTA[14]	K12	PB09	PORTB[9]
G13	PA11	PORTA[11]	K13	PB06	PORTB[6]
G14	PA08	PORTA[8]	K14	PB03	PORTB[3]
H01	PE13	PORTE[13]	L01	PE08	PORTE[8]
H02	PF00	PORTF[0]	L02	PE09	PORTE[9]
H03	F_SO	FRAM_MISO	L03	PE11	PORTE[11]
H04	SI	ROM_MISO	L04	PE01	PORTE[1]
H05	3V3	VDD33	L05	PD13	PORTD[13]
H06	3V3	VDD33	L06	PD09	PORTD[9]
H07	VSS	VSS	L07	PD05	PORTD[5]
H08	VSS	VSS	L08	PD01	PORTD[1]
H09	1V5	VDD15	L09	PC13	PORTC[13]
H10	1V5	VDD15	L10	PC10	PORTC[10]
H11	PB04	PORTB[4]	L11	PC00	PORTC[0]
H12	NC	NC	L12	PB13	PORTB[13]
H13	PA15	PORTA[15]	L13	PB10	PORTB[10]
H14	PA12	PORTA[12]	L14	PB07	PORTB[7]
J01	VSS	VSS	M01	PE06	PORTE[6]
J02	WPn	FRAM_PROTn	M02	PE07	PORTE[7]
J03	PE15	PORTE[15]	M03	PE02	PORTE[2]
J04	PF02	PORTF[2]	M04	PD14	PORTD[14]
J05	VSS	VSS	M05	PD10	PORTD[10]
J06	VSS	VSS	M06	PD06	PORTD[6]
J07	1V5	VDD15	M07	PD02	PORTD[2]
J08	3V3	VDD33	M08	PC14	PORTC[14]
J09	VSS	VSS	M09	NC	NC
J10	VSS	VSS	M10	PC07	PORTC[7]
J11	PB08	PORTB[8]	M11	PC04	PORTC[4]
J12	PB05	PORTB[5]	M12	SDA1	I2C1_SDA
J13	PB02	PORTB[2]	M13	PB14	PORTB[14]
J14	PB00	PORTB[0]	M14	PB11	PORTB[11]

N01	PE05	PORTE[5]	P01	PE04	PORTE[4]
N02	PE03	PORTE[3]	P02	PE00	PORTE[0]
N03	PD15	PORTD[15]	P03	PD12	PORTD[12]
N04	PD11	PORTD[11]	P04	PD08	PORTD[8]
N05	PD07	PORTD[7]	P05	PD04	PORTD[4]
N06	PD03	PORTD[3]	P06	PD00	PORTD[0]
N07	PC15	PORTC[15]	P07	PC12	PORTC[12]
N08	PC11	PORTC[11]	P08	PC09	PORTC[9]
N09	PC08	PORTC[8]	P09	PC06	PORTC[6]
N10	PC05	PORTC[5]	P10	PC03	PORTC[3]
N11	PC02	PORTC[2]	P11	PC01	PORTC[1]
N12	SCL2	I2C2_SCL	P12	SDA2	I2C2_SDA
N13	SCL1	I2C1_SCL	P13	NC	NC
N14	PB15	PORTB[15]	P14	NC	NC

3.2 Pin Descriptions

Pin Type	Description	Type	Internal Pull-up/down
System Pins			
XTAL_P	Crystal Oscillator Output	Out	None
XTAL_N	Crystal Oscillator Input	In	None
EXTRESETn	External System Reset, active low. Resets the processor and all peripherals. This signal is internally synchronized before being used. Any reset will cause this pin to pull low during the reset sequence.	ASync In / Open drain Out	Pull-up
NMI	Non-maskable Interrupt – active high	ASync In	None
EXT15_SEL	When high, this signal disables the internal 1.5 V regulator, and 1.5 V must be applied externally to all VDD15 pins and A_VDD15.	In	None
NVM_PROTn	When low, this signal inhibits programming of the internal NVM (VA41637 only).	In	None
TEST_MODE	For factory use only. Must be tied to VSS with a 10k resistor.	In	None
General-Purpose I/O Pins			
PORTA[15:0]	Software configurable general-purpose I/O pins. Software configurable for direction, interrupt sources, and counter/timer triggers. These pins are configurable as UART, SPI, and Timers pins.	Sync I/O	Software configurable
PORTB[15:0]	Software configurable general-purpose I/O pins. Software configurable for direction, interrupt sources, and counter/timer triggers. These pins are configurable as UART, SPI, and Timers pins.	Sync I/O	Software configurable

Pin Type	Description	Type	Internal Pull-up/down
PORTC[15:0]	Software configurable general-purpose I/O pins. Software configurable for direction, interrupt sources, and counter/timer triggers. These pins are configurable as UART, SPI, and Timers pins.	Sync I/O	Software configurable
PORTD[15:0]	Software configurable general-purpose I/O pins. Software configurable for direction, interrupt sources, and counter/timer triggers. These pins are configurable as UART, and Timers pins.	Sync I/O	Software configurable
PORTE[15:0]	Software configurable general-purpose I/O pins. Software configurable for direction, interrupt sources, and counter/timer triggers. These pins are configurable as UART, SPI, and Timers pins.	Sync I/O	Software configurable
PORTF[15:0]	Software configurable general-purpose I/O pins. Software configurable for direction, interrupt sources, and counter/timer triggers. These pins are configurable as UART, SPI, and Timers pins.	Sync I/O	Software configurable
PORTG[7:0]	Software configurable general-purpose I/O pins. Software configurable for direction, interrupt sources, and counter/timer triggers. These pins are configurable as UART, SPI, and Timer pins.	Sync I/O	Software configurable
SPI ROM pins			
ROM_SCK	SPI Clock to Boot ROM.	Sync Out	Pull-down
ROM_SS	SPI Chip Select to Boot ROM (Active Low).	Sync Out	Pull-up
ROM_MOSI	SPI Data Out to Boot ROM.	Sync Out	Pull-down
ROM_MISO	SPI Data In from Boot ROM (must be tied to VSS for VA41637 devices with an internal NVM).	Sync In	None
I²C Pins			
I2C0_SCL	I ² C0 Clock	Open drain	None
I2C0_SDA	I ² C0 Data	Open drain	None
I2C1_SCL	I ² C1 Clock	Open drain	None
I2C1_SDA	I ² C1 Data	Open drain	None
I2C2_SCL	I ² C2 Clock	Open drain	None
I2C2_SDA	I ² C2 Data	Open drain	None

JTAG/SWD Pins			
TCK/SWCK	Test Clock/Serial Wire Debug Clock	Clock	None
TMS/SWDIO	Test Mode Select/Serial Wire Debug Data IO	Sync In/Out	Pull-up
TRSTn	Test Reset, active low	Sync In	Pull-up
TDI	Test Data In	Sync In	Pull-up
TDO	Test Data Out	Sync Out	None
Power/Ground pins			
VDD15	1.5 V Core power (must be supplied externally if EXT15_SEL=1)	Power	N/A
VSS	Ground	Ground	N/A
VDD33	3.3 V IO power	Power	N/A
VDDQ	For factory use only. Must be tied to VSS	Power	N/A

3.3 GPIO Pin Alternative Functions

GPIO pins can be configured for various peripherals on the VA416X7 MCU. The default configuration is for all the pins to be assigned as GPIO. Please refer to the VA416XX Programmer's Guide for more information about the usage of GPIO pins and their alternative functions.

Port pin default function	Alternative function 1	Alternative function 2	Alternative function 3
PORTA[0]	TIM[0]	SPI2_SS4	UART0_RTS
PORTA[1]	TIM[1]	SPI2_SS3	UART0_CTS
PORTA[2]	TIM[2]	SPI2_SS2	UART0_TX
PORTA[3]	TIM[3]	SPI2_SS1	UART0_RX
PORTA[4]	TIM[4]	SPI2_SS0	Not assigned
PORTA[5]	TIM[5]	SPI2_SCK	Not assigned
PORTA[6]	TIM[6]	SPI2_MISO	Not assigned
PORTA[7]	TIM[7]	SPI2_MOSI	Not assigned
PORTA[8]	Not assigned	SPI2_SS6	TIM[8]
PORTA[9]	Not assigned	SPI2_SS5	Not assigned
PORTA[10]	Not assigned	TIM[23]	Not assigned
PORTA[11]	Not assigned	TIM[22]	Not assigned
PORTA[12]	Not assigned	TIM[21]	Not assigned
PORTA[13]	Not assigned	TIM[20]	Not assigned
PORTA[14]	Not assigned	TIM[19]	Not assigned
PORTA[15]	Not assigned	TIM[18]	Not assigned
PORTB[0]	Not assigned	TIM[17]	SPI1_SS7
PORTB[1]	Not assigned	TIM[16]	SPI1_SS6

Port pin default function	Alternative function 1	Alternative function 2	Alternative function 3
PORTB[2]	Not assigned	TIM[15]	SPI1_SS5
PORTB[3]	Not assigned	TIM[14]	SPI1_SS4
PORTB[4]	Not assigned	TIM[13]	SPI1_SS3
PORTB[5]	Not assigned	TIM[12]	SPI1_SS2
PORTB[6]	Not assigned	TIM[11]	SPI1_SS1
PORTB[7]	Not assigned	TIM[10]	SPI1_SS0
PORTB[8]	Not assigned	TIM[9]	SPI1_SCK
PORTB[9]	Not assigned	TIM[8]	SPI1_MISO
PORTB[10]	Not assigned	TIM[7]	SPI1_MOSI
PORTB[11]	SPI0_SS3	TIM[6]	Not assigned
PORTB[12]	SPI0_SS2	TIM[5]	UART1_RTS
PORTB[13]	SPI0_SS1	TIM[4]	UART1_CTS
PORTB[14]	SPI0_SS0	TIM[3]	UART1_TX
PORTB[15]	SPI0_SCK	TIM[2]	UART1_RX
PORTC[0]	SPI0_MISO	TIM[1]	Not assigned
PORTC[1]	SPI0_MOSI	TIM[0]	Not assigned
PORTC[2]	Not assigned	UART0_RTS	Not assigned
PORTC[3]	Not assigned	UART0_CTS	Not assigned
PORTC[4]	Not assigned	UART0_TX	Not assigned
PORTC[5]	Not assigned	UART0_RX	Not assigned
PORTC[6]	Not assigned	Not assigned	Not assigned
PORTC[7]	Not assigned	SPI1_SS1	Not assigned
PORTC[8]	Not assigned	SPI1_SS0	Not assigned
PORTC[9]	Not assigned	SPI1_SCK	Not assigned
PORTC[10]	Not assigned	SPI1_MISO	Not assigned
PORTC[11]	Not assigned	SPI1_MOSI	Not assigned
PORTC[12]	Not assigned	UART2_RTS	Not assigned
PORTC[13]	Not assigned	UART2_CTS	Not assigned
PORTC[14]	Not assigned	UART2_TX	Not assigned
PORTC[15]	Not assigned	UART2_RX	Not assigned
PORTD[0]	Not assigned	TIM[0]	Not assigned
PORTD[1]	Not assigned	TIM[1]	Not assigned
PORTD[2]	Not assigned	TIM[2]	Not assigned
PORTD[3]	Not assigned	TIM[3]	Not assigned
PORTD[4]	Not assigned	TIM[4]	Not assigned
PORTD[5]	Not assigned	TIM[5]	Not assigned
PORTD[6]	Not assigned	TIM[6]	Not assigned

Port pin default function	Alternative function 1	Alternative function 2	Alternative function 3
PORTD[7]	Not assigned	TIM[7]	Not assigned
PORTD[8]	Not assigned	TIM[8]	Not assigned
PORTD[9]	Not assigned	TIM[9]	UART1_RTS
PORTD[10]	Not assigned	TIM[10]	UART1_CTS
PORTD[11]	Not assigned	TIM[11]	UART1_TX
PORTD[12]	Not assigned	TIM[12]	UART1_RX
PORTD[13]	Not assigned	TIM[13]	Not assigned
PORTD[14]	Not assigned	TIM[14]	Not assigned
PORTD[15]	Not assigned	TIM[15]	Not assigned
PORTE[0]	Not assigned	TIM[16]	UART0_RTS
PORTE[1]	Not assigned	TIM[17]	UART0_CTS
PORTE[2]	Not assigned	TIM[18]	UART0_TX
PORTE[3]	Not assigned	TIM[19]	UART0_RX
PORTE[4]	Not assigned	TIM[20]	Not assigned
PORTE[5]	Not assigned	TIM[21]	SPI1_SS7
PORTE[6]	Not assigned	TIM[22]	SPI1_SS6
PORTE[7]	Not assigned	TIM[23]	SPI1_SS5
PORTE[8]	Not assigned	SPI1_SS4	TIM[16]
PORTE[9]	Not assigned	SPI1_SS3	TIM[17]
PORTE[10]	Not assigned	SPI1_SS2	TIM[18]
PORTE[11]	Not assigned	SPI1_SS1	TIM[19]
PORTE[12]	Not assigned	SPI1_SS0	TIM[20]
PORTE[13]	Not assigned	SPI1_SCK	TIM[21]
PORTE[14]	Not assigned	SPI1_MISO	TIM[22]
PORTE[15]	Not assigned	SPI1_MOSI	TIM[23]
PORTF[0]	Not assigned	SPI2_SS4	TIM[0]
PORTF[1]	Not assigned	SPI2_SS3	TIM[1]
PORTF[2]	SPI1_SS0	SPI2_SS2	TIM[2]
PORTF[3]	SPI1_SCK	SPI2_SS1	TIM[3]
PORTF[4]	SPI1_MISO	SPI2_SS0	TIM[4]
PORTF[5]	SPI1_MOSI	SPI2_SCK	TIM[5]
PORTF[6]	UART2_RTS	SPI2_MISO	TIM[6]
PORTF[7]	UART2_CTS	SPI2_MOSI	TIM[7]
PORTF[8]	UART2_TX	Not assigned	TIM[8]
PORTF[9]	UART2_RX	Not assigned	TIM[9]
PORTF[10]	UART1_RTS	Not assigned	TIM[10]
PORTF[11]	UART1_CTS	Not assigned	TIM[11]

Port pin default function	Alternative function 1	Alternative function 2	Alternative function 3
PORTF[12]	UART1_TX	Not assigned	TIM[12]
PORTF[13]	UART1_RX	TIM[19]	Not assigned
PORTF[14]	UART0_RTS	TIM[20]	Not assigned
PORTF[15]	UART0_CTS	TIM[21]	Not assigned
PORTG[0]	UART0_TX	TIM[22]	Not assigned
PORTG[1]	UART0_RX	TIM[23]	Not assigned
PORTG[2]	TIM[9]	SPI1_SS0	Not assigned
PORTG[3]	TIM[10]	SPI1_SCK	Not assigned
PORTG[4]	SPI1_SS3	SPI1_MISO	Not assigned
PORTG[5]	SPI1_SS2	Not assigned	Not assigned
PORTG[6]	SPI1_SS1	TIM[12]	Not assigned
PORTG[7]	Not assigned	Not assigned	Not assigned

4 Peripheral Summary

4.1 Serial Peripheral Interface (SPI)

The VA416X7 contains three general purpose Serial Peripheral Interface (SPI) blocks. A fourth SPI is dedicated to the boot memory and uses a dedicated set of pins. The other three use pins shared with various GPIOs. Please refer to the VA416XX Programmer's Guide for more information about the usage of the SPI.

The SPI peripheral supports the following features:

- Master mode
- Slave mode
- Buffered RX/TX operation with dual four entry FIFOs
- Serial clock (SCK) with programmable polarity (SPO) and phase (SPH)
- SPI0 has up to 4 chip selects
- SPI1 has up to 8 chip selects
- SPI2 has up to 7 chip selects
- SPI3 is Master only and shares its pins with the SPI ROM pins (ROM_SCK, ROM_MOSI, ROM_MISO, ROM_SS)
- Interrupt conditions:
 - TX FIFO is at least half empty (TXIM)
 - RX FIFO is at least half full (RXIM)
 - RX Timeout (RTIM)
 - RX FIFO overrun (RORIM)

4.2 Universal Asynchronous Receiver/Transmitter (UART)

The VA416X7 contains three Universal Asynchronous Receiver/Transmitter (UART) interface blocks with an independent Transmit and Receive section, each with a 16-byte FIFO. The UART pins are shared with various GPIO pins. Please refer to the VA416XX Programmer's Guide for more information about the usage of the UART.

The UART peripheral supports the following features:

- Selectable even, odd or no parity
- Selectable one or two stop bits
- Word sizes from 5 to 8 bits
- 9-bit address mode
- Baud rates from 300 to 115,200 bps (or up to 2 Mbps)
- 16-byte RX and TX FIFO
- Detection of Framing, Parity and Overrun errors
- Full Duplex or Half Duplex operation
- Break signal generation and detection

- Interrupt conditions:
 - Receive FIFO at least half full (IRQ_RX)
 - Receive FIFO overflow, receive frame error, receive parity error, or receive break condition (IRQ_RX_STATUS)
 - Receive timeout (IRQ_RX_TO)
 - Transmit FIFO at least half empty (IRQ_TX)
 - Transmit FIFO overflow (IRQ_TX_STATUS)
 - Transmit FIFO empty (IRQ_TX_EMPTY)
 - Transmitter interrupt when CTSn changes value (IRQ_TX_CTS)

4.3 Inter-Integrated Circuit (I²C)

The VA416X7 contains three Inter-Integrated Circuit (I²C) interface blocks. Please refer to the VA416XX Programmer's Guide for more information about the usage of the I²C.

The I²C peripheral supports the following features:

- Standard I²C-compliant bus interface
- Configurable as Master or Slave
- Dedicated open-drain pins
- 16-word FIFO for both transmit and receive
- Programmable clock rate for standard 100 kHz mode or 400 kHz mode
- Interrupt conditions:
 - TX FIFO ready (TXREADY)
 - TX FIFO empty (TXEMPTY)
 - TX FIFO overflow (TXOVERFLOW)
 - RX FIFO full (RXFULL)
 - RX FIFO ready (RXREADY)
 - RX FIFO overflow (RXOVERFLOW)
 - Clock low timeout (CLKLOTO)
 - I²C Status (STATUS)

4.4 General Purpose 4-Channel DMA

The VA416X7 supports a single DMA interface to allow the MCU to transfer data from a peripheral to memory or memory to peripheral, independent of the Arm CPU. Please refer to the VA416XX Programmer's Guide for more information about the usage of the DMA.

The DMA controller implements the following features:

- Each DMA channel has dedicated handshake signals
- Each DMA channel has a programmable priority level
- Each priority level arbitrates using a fixed priority that is determined by the DMA channel
- Support for multiple transfer types:
 - Memory-to-memory
 - Memory-to-peripheral
 - Peripheral-to-memory
- Support for multiple DMA transfer data widths
- The number of transfers in a single DMA cycle is programmable from 1 to 1024

Typical use cases for the DMA are listed below:

- SPI/UART emptying own FIFO into RAM buffer or vice versa

4.5 Timers/Counters (TIM)

The VA416X7 contains 24 general-purpose Timer/Counter interface blocks. These can be configured as timers or event counters. They can be free-running or triggered by system events. Timer pins are shared with various GPIO pins. Please refer to the VA416XX Programmer's Guide for more information about the usage of the Timers.

Timer feature summary

- Advanced trigger modes
 - Start/Stop based on other Counter/Timers or GPIO signals
 - Multiple trigger sources
- Configurable output event
 - One cycle zero detect when timer equal to zero is detected
 - Active mode
 - Divide by two for square wave generation
 - Two PWM modes: Single edge and double edge detection

4.6 General-Purpose Input/Output Ports (GPIO)

The VA416X7 contains seven GPIO banks providing a total of 104 GPIO pins. GPIO pins can be configured as inputs or outputs. Please refer to the VA416XX Programmer's Guide for more information about the usage of the GPIO.

- PORTA[15:0]
- PORTB[15:0]
- PORTC[15:0]
- PORTD[15:0]
- PORTE[15:0]
- PORTF[15:0]
- PORTG[7:0]
- Interrupt capability on Ports A to F
- Selectable edge or level interrupts
- Programmable pull-up or pull-down resistors
- Programmable output inversion
- Selectable input filtering
- Pseudo open-drain capability
- Alternative functions available on many GPIO pins

4.7 True Random Number Generator (TRNG)

The Arm TrustZone TRNG offers these two components:

- The TRNG that conforms to the following standards and drafts:
 - NIST SP800-90B
 - NIST SP800-22
 - FIPS 140-2
 - BSI AIS-31
- A software-implemented Deterministic Random Bit Generator (DRBG) which follows NIST SP 800-90A (making the entire RNG flow SP 800-90C compliant)

For more detailed information, see the Arm TrustZone True Random Number Generator, Technical Reference Manual.

5 DC Electrical Characteristics

5.1 Absolute Maximum Ratings

Symbol	Rating	Hi-Rel	Unit
V _{DD33}	DC supply voltage (I/O)	-0.3 to 3.8	V
V _{I/O}	Voltage on any pin	-0.3 to 3.8	V
T _{CASE}	Operating temperature	-55 to 125	°C
T _{BIAS}	Temperature under bias	-55 to 125	°C
T _{STG}	Storage temperature	-55 to 125	°C

5.2 Recommended Supply Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V _{DD33}	I/O supply voltage	2.97	3.3	3.63	V
V _{DD15}	Core supply voltage (if supplied externally)	1.35	1.5	1.65	V
V _{SS}	Ground	-	0	-	V
V _{ramp}	V _{DD33} voltage ramp time ¹	2.0	-	-	μs
V _{PROFF}	V _{DD33} level at which the Power-on reset is released ²	2.5	2.7	2.9	V
V _{PRON}	V _{DD33} level at which the Power-on reset is activated ³	0.5	0.7	0.9	V

Notes:

1. V_{Ramp} time is the time from V_{DD} at 0 V until it reaches the operating range.
2. V_{PROFF} is the voltage at which the internal Power-on reset is released when power is rising.
3. V_{PRON} is the voltage at which the internal Power-on reset is activated.

5.3 DC Current Consumption

Core Supply Current (VDD15)

The core supply current is approximately 1.2mA/MHz.

Run I _{DD}	25 MHz	50 MHz	100 MHz	Units
CPU only	32	60	120	mA
Worst case (maximum activity)	50	100	200	mA

Notes:

1. Maximum activity is measured with all internal counters running at the maximum rate, all I²C interfaces active in Fast mode and loopback mode, all SPI interfaces active in master mode at 16x clock divide rate, all UARTs active in loopback mode at 1 MHz Baud rate, and the CPU running multiply operations.
2. Minimum activity (CPU only) is measured with all peripheral clocks disabled.
3. Measured at nominal VDD and 25°C.

I/O Supply Current (V_{DD33}) I_{DD33}

Run I_{DD}^1	Max	Units
Overall maximum I/O current	200	mA
Maximum I/O current per side of the device	100	mA

Notes:

- Although each GPIO can drive up to 8mA, the maximum current allowed per package side of the device is 100mA.

Deep-sleep Supply Current (V_{DD33})

Sleep I_{DD}^1	25 MHz	50 MHz	100 MHz	Units
CPU only	TBD	TBD	TBD	mA
Worst case (maximum activity)	TBD	TBD	TBD	mA

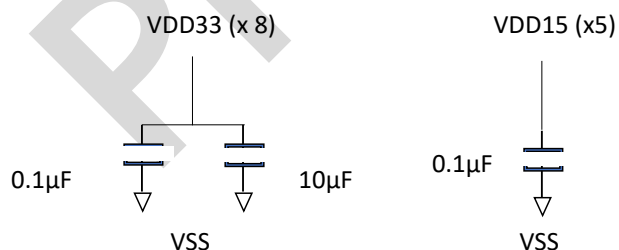
Notes:

- During deep sleep, the internal 1.5V supply is disabled, and the current consumption of the 1.5V circuitry is only due to leakage. The 3.3V supply is enabled along with a configurable 1MHz oscillator used as the wake-up counter. Deep sleep cannot be used if an external 1.5V supply is being supplied to the MCU (EXT15_SEL=1).

5.4 Power Supply Decoupling

Each power supply pair (V_{DD33}/V_{SS} , V_{DD15}/V_{SS}) must be decoupled with filtering ceramic capacitors, as shown. These capacitors must be placed as close as possible to the corresponding supply pins to ensure proper operation of the MCU. Capacitors can also be placed on the bottom side of a PC board for convenience.

Digital Supplies



5.5 Electrostatic Discharge (ESD)

ESD testing is done in conformance with MIL-PRF-38534 and applies to all pads.

Parameter	Test Conditions	Value	Unit
ESD for Human Body Model (HBM)	All pins	2000	V
ESD for field-induced Charged Device Model (CDM)	All pins	500	V

5.6 Signal Pads Operating Conditions

Input/Output and Input-Only Pads

Symbol	Parameter	Test Conditions	Min	Typ ¹	Max	Unit
V_{IL}	Input Low Voltage		-0.3	-	$0.3 \times V_{DD33}$	V
V_{IH}	Input High Voltage		$0.7 \times V_{DD33}$	-	$V_{DD33} + 0.3$	V
V_{hys}	Hysteresis of Schmitt trigger		300	450	600	mV

Notes:

1. Typ for -55° to 125°C measured at 25°C
2. The following input buffers have Schmitt Trigger Inputs: TCK, TRSTn, TDI, TMS, ROM_MISO, NVM_PROTn, TEST_MODE, NMI, CAN0_RX, CAN1_RX, EBI_BOOT, and all GPIO

Input/Output and Output-Only Pads

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OL}	Output voltage (Low)	Load I = 8 mA $V_{DD33} = \text{Min}$	-	0.25	$0.4 \times V_{DD33}$	V
V_{OH}	Output voltage (High)	Load I = -8 mA $V_{DD33} = \text{Min}$	$0.8 \times V_{DD33}$	3.0	-	V

Leakage Current Input/Output and Input-Only Pads (At Temperature -55 to 125°C)

Symbol	Parameter	Pins	Test Condition	Min	Typ	Max
I_{in}	Input leakage current (V_{in} low)	Pins with configurable pull-up or pull-down	$V_{in} = 0\text{ V}$	-1 μA	10 nA	-
		Pins with internal pull-down always enabled	$V_{in} = 0\text{ V}$	-65 μA	-50 μA	-
		Tri-state Pins	$V_{in} = 0\text{ V}$	-1 μA	10 nA	-
	Input leakage current (V_{in} high)	Pins with configurable pull-up or pull-down	$V_{in} = V_{DD33}$	-	10 nA	1 μA
		Pins with internal pull-down always enabled	$V_{in} = V_{DD33}$	-	10 nA	1 μA
		Tri-state Pins	$V_{in} = V_{DD33}$	-	10 nA	1 μA

Notes:

1. TYP for -55° to 125°C measured at 25°C
2. See Section 3.1 Pin Descriptions for more information

Open Drain I²C Pads

Open Drain I²C pad specifications apply to pads: I2C0_SCL, I2C0_SDA, I2C1_SCL, I2C1_SDA, I2C2_SCL, and I2C2_SDA

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IL}	Input low voltage		-0.3		$0.3 \times V_{DD33MAX}$	V
V_{IH}	Input high voltage		$0.7 \times V_{DD33MIN}$		$V_{DD33} + 0.3$	V
V_{hys}	Hysteresis of Schmitt trigger		300		600	mV
I_{in}	Input leakage current (high)	$V_{in} = V_{DD33}$	-1 μA	10 nA	1 μA	
V_{OL}	Output voltage (low)	Load I = -8 mA, $V_{DD33} = \text{Min}$	-	0.25	$0.4 \times V_{DD33}$	V

5.7 Low-Voltage Detect Circuit

Refer to the VA416XX Programmer's Guide for more information.

Low-Voltage Detect Level	LVL_SLCT Value	Min	Max	Units
Low-voltage detect rising	00	2.85	2.95	V
	01	2.95	3.05	V
	10	3.05	3.15	V
	11	3.15	3.25	V
Low-voltage detect falling	00	2.75	2.85	V
	01	2.85	2.95	V
	10	2.95	3.05	V
	11	3.05	3.15	V

Notes:

1. LVL_SLCT is set to the lowest possible setting on power-up to keep the low voltage detect circuit from resetting the device.

5.8 Internal Pull-up/Pull-down Resistors

	Typ Value	Units
Pull-up	60	k Ω
Pull-down	60	k Ω

Notes:

1. Pins with dedicated Pull-ups: TMS, TRSTn, TDI, ROM_SS, EXTRESETn, ROM_SCK
2. Pins with dedicated Pull-downs: ROM_MOSI
3. Pins with software configurable pulls: All GPIO pins

5.9 Pin Capacitance

Symbol	Parameter	Conditions	Max	Unit
C_{IN}^1	Input Capacitance	$V_{in} = 3.3\text{ V}$	6	pF
$C_{I/O}^2$	I/O Capacitance	$V_{out} = 3.3\text{ V}$	10	pF

Notes:

1. Input only pins: XTAL_N, ROM_MISO, TCK, TRSTn, TDI, CAN0_RX, CAN1_RX, NMI, EBI_BOOT, NVM_PROTn, EXT15_SEL
2. Bidirectional pins: PORTA[15:0], PORTB[15:0], PORTC[15:0], PORTD[15:0], PORTE[15:0], PORTF[15:0], PORTG[7:0], TMS/SWDIO
3. Open-drain pins: EXTRESETn, I2C0_SCL, I2C0_SDA, I2C1_SCL, I2C1_SDA, I2C2_SCL, and I2C2_SDA.

6 AC Electrical Characteristics

6.1 AC Timing Conditions

V_{DD33}	3.3 V ± 10%
Input swing levels	0 to 3.3 V
Input rise/fall times	1 / 4 ns ¹
Input timing reference levels	1.65 V
Output timing reference levels	1.65 V
AC test load	15 pF

Notes:

1. Rise/Fall times are measured from 20% to 80% of V_{DD33}

6.2 Internal 20 MHz Oscillator

The internal 20 MHz oscillator is used for boot and Power-Up delay timing. If the system clock drops below 1 MHz, the system clock will automatically switch over to the internal 20 MHz oscillator as a system fail-safe mechanism.

Parameter	Description	Min	Typ	Max	Unit
t _{CYC}	Clock cycle time	40	50	66.7	ns
t _{FREQ}	Clock frequency	15	20	25	MHz
-	Cycle time accuracy	-25	-	25	%

6.3 Internal 1 MHz Oscillator

The internal 1 MHz oscillator is used during deep-sleep to wake up the device. Please refer to the VA416XX Programmer's Guide for more information about entering and exiting deep-sleep mode.

Parameter	Description	Min	Typ	Max	Unit
t _{CYC}	Clock cycle time	0.82	1	1.28	μs
t _{FREQ}	Clock frequency	0.78	1	1.22	MHz
-	Cycle time accuracy	-28	-	28	%
t _{WAKE-UP}	Deep-sleep wake-up time ¹	256	-	1024	mA

Notes:

1. Wake-up time is software programmable and can be disabled to allow for hardware wake-up only.

6.4 Clock Signals

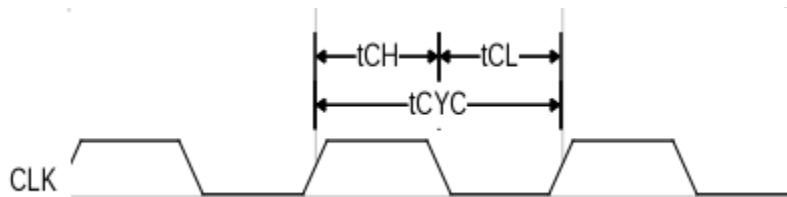
The VA416X7 can be clocked in several different ways.

- Internal oscillator
- 4 to 10 MHz external crystal oscillator with PLL or without PLL enabled
- 4 to 10 MHz external square wave with PLL enabled
- 0 to 100 MHz external square wave without PLL enabled

External Clock Signal

An external clock can be used to drive the XTAL_N input with the XTAL_P pin left unconnected. The clock signal must adhere to the following table.

Parameter	Description	Time	Unit
t_{CYC}	Clock cycle time (min)	10	ns
t_{CH}	Clock high (min)	4	ns
t_{CL}	Clock low (min)	4	ns



External Crystal Oscillator

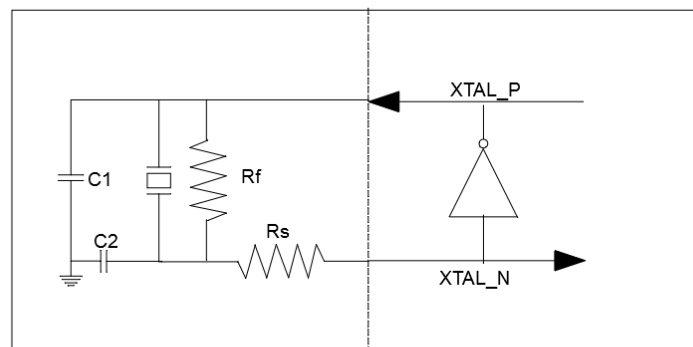
If an external crystal oscillator circuit is used, please refer to the crystal oscillator manufacturer's data sheet for exact values of resistors and capacitors for proper oscillation at the fundamental frequency, reliable start-up, and to maximize stability.

Parameter	Description	Min	Typ	Max	Unit
t_{CYC}	Clock cycle time (min)	-	-	100	ns
f_{XTAL}	Crystal frequency	4	-	10	MHz
R_F	Feedback resistor	-	1M	-	Ω
R_S	Series resistor	1k	-	20k	Ω
t_S	Start-up time	-	10	15	ms

Notes:

1. PC board trace lengths for the oscillator circuit should be as short as possible

External Crystal Circuit



R_F = Feedback resistor

R_S = Series resistor

C1, C2 = Load capacitors

6.5 Phased Locked Loop (PLL)

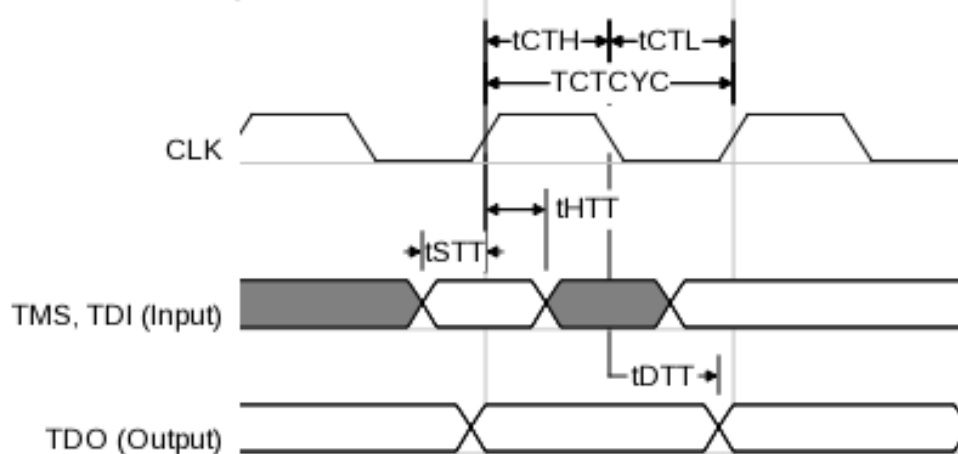
The VA416X7 contains an internal PLL circuit that can be used to generate internal frequencies higher than the input clock (either driven by an external clock or an external crystal oscillator). The PLL clock can be used as the MCU system clock. Please refer to the VA416XX Programmer's Guide for more information on the usage of the PLL.

Parameter	Description	Typ	Max	Unit
f_{in}	Input frequency	4	10	MHz
f_{out}	Output frequency	50	100	MHz
t_{LOCK}	PLL lock time	10	100	μ s
Jitter	PLL clock jitter (percentage of input frequency)	3	-	%
t_{CL}	Clock low (min) ¹	4	-	ns

6.6 Serial Wire Debug (SWD)

The Serial Wire Debug interface allows access to the Arm Debug Access Port (DAP). The TMS/SWDIO pin is bi-directional data, and the TCK/SWCLK pin is a clock input to the VA416X0.

Parameter	Description	Min	Typ	Max	Unit
t_{TCCYC}	TCK/SWCLK cycle time (min) ²	60	-	-	ns
t_{CTH}	TCK/SWCLK high (min) ²	20	-	-	ns
t_{CTL}	TCK/SWCLK low (min) ²	20	-	-	ns
t_{DTT}	SWDIO/TDO output change from TCK/SWCLK fall ³	3.0	9	14	ns
t_{STT}	TMS/SWDIO and TDI setup time to TCK/SWCLK rise	2.0	-	-	ns
t_{HTT}	TMS/SWDIO and TDI hold time to TCK/SWCLK rise	6.0	-	-	ns



7 Radiation Hardened Performance Targets

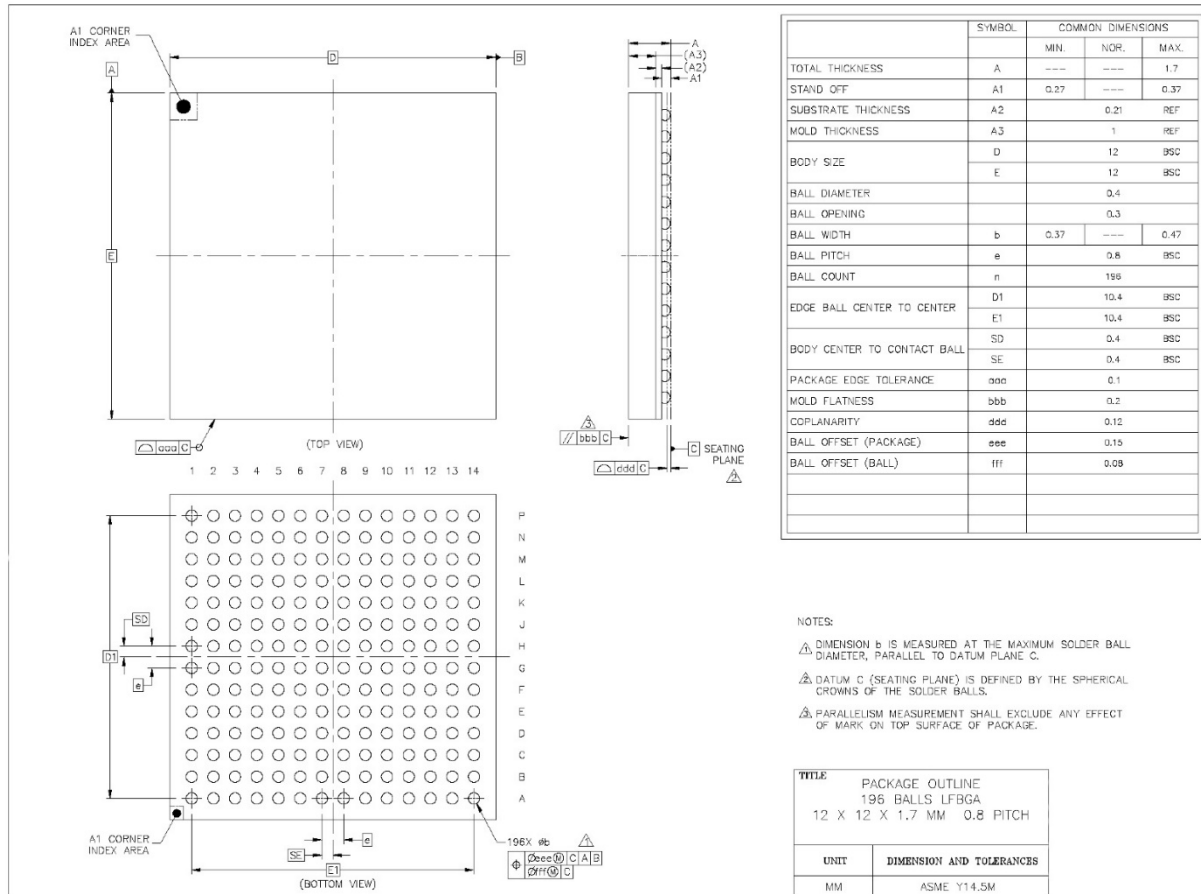
Parameter	Description	Min	Typ	Max	Unit
TID	Total ionizing dose (VA41627)	-	-	300	krad (Si) ¹
TID	Total ionizing dose (VA41637)	-	-	200	krad (Si) ¹
SER	Soft error rate (EDAC enabled)	-	1e ⁻¹⁵	-	errors / bit / day ^{1,2}
LET	Linear energy transfer (latch-up immunity)	110	-	-	MeV / cm ² / mg ¹

Notes:

1. Along with EDAC, the Scrub Engine should also be enabled and running at an appropriate frequency to prevent the accumulation of errors in the memory to achieve consistently low SER over time.
2. In geosynchronous orbit, solar min, and 100 mils of aluminum shielding.

8 Package Mechanical Information

8.1 196-Pin Plastic BGA Package Dimensions (mm)



9 Ordering Information

Part Number	Package	NVM	Qualification
VA41627-PG196F0EAA	Plastic 196 BGA	256 Kbyte on-chip FRAM	Engineering Sample
VA41637-PG196F0EAA	Plastic 196 BGA	External NVM (parallel or SPI)	Engineering Sample

10 Development Kit Ordering Information

Description	Part number	Features
Development Board	PEB1-VA41630	Supported by Keil™ MDK-Arm Microcontroller Software Kit Board Support Package (BSP) includes example software for peripherals Segger J-Link OB
Development Board	PEB1-VA41620	Supported by Keil™ MDK-Arm Microcontroller Software Kit Board Support Package (BSP) includes example software for peripherals Segger J-Link OB

11 Revision History

Date	Version	Page Locations	Description
08/7/2020	0.98	All	Initial Release
9/15/2020	0.99	10 - 15	Added pins VDDQ and TEST_MODE

The use of this product is subject to the manufacturer's standard terms and conditions available on the manufacturer's website [here](#).

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