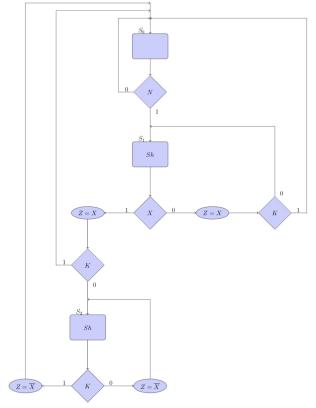
Points to Remember

Aditya Arora

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- 1. For Asynchronous circuits: The outputs are only to be written for the stable state condition while the other input conditions are all outputting don't cares i.e. X or —
- 2. **Fundamental mode:** The state diagram assuming fundamental mode operation (output is shown as a Moore output but it only assumes that value if the state is stable)
- 3. State Reduction Table: All states except first vertically down, all states except last horizontally right
- 4. **POS** and **SOP**: SOP \rightarrow 1 and POS \rightarrow 0 (to remember when writing equation from K-Map)
- 5. Asynchronous circuit analysis: Question 13 from Assignment 10 is so smart, so many little tricks combined
- 6. Writing DFF equation: The DFF equations can be written directly since the property Q(t+1) = D is valid
- 7. Mealy and Moore: Mealy output on arrows, Moore output in state

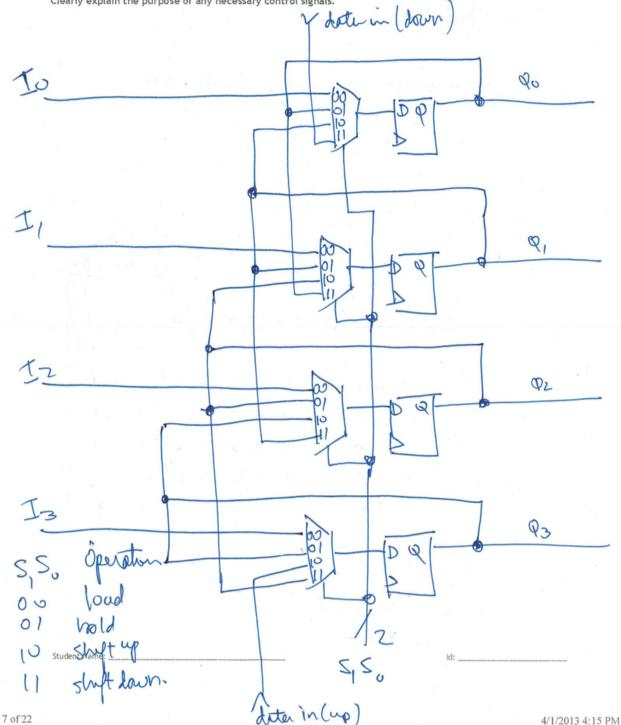


See the "Sh" shift signal for state dependent outputs

8. **ASM**:

9. 4 Bit Bi-Directional shift register using D Flip Flops: Part D) [4 MAKKS]

Design and draw the circuit diagram for a 4-bit bi-directional shift register with parallel load and hold using D-type flip-flops. Use can use any other necessary circuit blocks (e.g., multiplexers, logic gates, etc.) required. Clearly explain the purpose of any necessary control signals.



10. ASM: ASM State changes are clocked by the edge

11. **f:**
$$T_{clock} + T_{setup} + T_{data} = T \Rightarrow f_{max} = \frac{1}{T}$$

12. State Machine Diagram to Timing Diagram: Output follows in Mealy diagram

13. **DFF Equations:**

One hot encoding implies A is 0001, B is 0010, C is 0100 and D is 1000. This leads to the state table given by

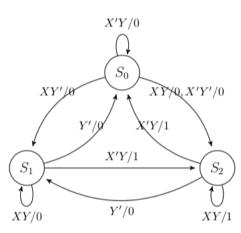
Current state	Next state		Outputs	
	x = 0	x = 1	x = 0	x = 1
$q_3q_2q_1q_0$	$q_3q_2q_1q_0$	$q_3q_2q_1q_0$	z	z
0001	0100	1000	0	0
0010	0010	0001	0	0
0100	1000	0001	0	0
1000	0100	0010	1	1

The DFF equations can be written down directly.

$$\begin{array}{rcl} d_3 & = & \overline{x}q_2 + xq_0 \\ d_2 & = & \overline{x}q_3 + \overline{x}q_0 \\ d_1 & = & \overline{x}q_1 + xq_3 \\ d_0 & = & xq_2 + xq_1 \end{array}$$

The circuit output is given as

$$z = q_3$$



Solution:

Simply look at incoming edges for each state to get the flip flop input equations:

$$\begin{array}{rcl} d_2 & = & XYS_2 + X'YS_1 + X'Y'S_0 \\ d_1 & = & XYS_1 + Y'S_2 + XY'S_0 \\ d_0 & = & X'YS_0 + Y'S_1 + X'YS_2 \end{array}$$

The circuit output is a Mealy output given by

$$z = XYS_2 + X'YS_2 + X'YS_1$$

Note that I've written the flip flop inputs in terms of the symbolic state. You'd get the same thing if you did a state assignment; e.g., S_0 is 001, S_1 is 010, and S_2 is 100 and then called the flip flop outputs $q_2q_1q_0$ — the S_i would simply get replaced by q_i .